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ANALYSIS OF TOTAL HARMONIC DISTORTION PERFORMANCE IN GRID-TIED SINGLE-PHASE VOLTAGE SOURCE INVERTERS THROUGH CLOSED-LOOP MODELING

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Tese submetida ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina como requisito parcial para a obtenção do título de Doutor em Engenharia Elétrica.

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O presente trabalho em nível de doutorado foi avaliado e aprovado, em 02 de fevereiro de 2024, pela banca examinadora composta pelos seguintes membros:

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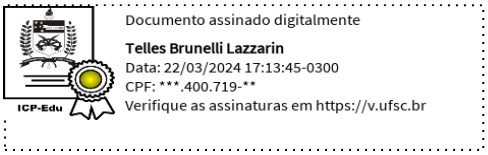

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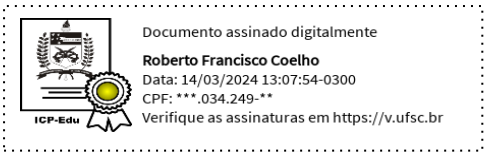

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À minha família.

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“Quem tem medo tem coragem.”

(Roberto, o Grande)

ABSTRACT

This thesis presents a methodology to estimate, in the design stage, the total harmonic distortion of the current injected into the power grid by two-stage voltage source inverters (VSI). As such inverters operate in a closed loop, the quality of the grid current is highly dependent on the dynamics of the control loops. Thus, it is necessary to focus on an approach to model the behavior of the grid current considering the closed-loop disturbances. The proposed approach allows the derivation of an equation to predict the behavior of the current injected into the grid and estimate its harmonic distortion, becoming an important tool for optimal design of grid-connected inverters. To validate the accuracy of the developed methodology, experimental results are presented in different operating scenarios.

Keywords: Closed-Loop Modeling, Grid-Connected Inverters, Power Quality, Single-Phase Inverters, Total Harmonic Distortion.

RESUMO

Esta tese apresenta uma metodologia para estimar, na etapa de projeto, a distorção harmônica total da corrente injetada na rede elétrica por inversores fonte de tensão de dois estágios. Como tais inversores operam em malha fechada, a qualidade da correte injetada na rede elétrica é altamente dependente da dinâmica das malhas de controle. Assim, é necessário focar em uma abordagem que modele o comportamento da corrente injetada na rede considerando as perturbações em malha fechada. A abordagem proposta possibilita a derivação de uma equação para prever o comportamento da corrente injetada na rede e estimar sua distorção harmônica, tornando-se uma importante ferramenta para otimizar o projeto de inversores conectados à rede. Para validar a acurácia da metodologia desenvolvida, são apresentados resultados experimentais em diferentes cenários de operação.

Palavras-chave: Distorção Harmônica Total, Inversores Conectados à Rede, Inversores Monofásicos, Modelagem em Malha Fechada, Qualidade de Energia.

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LIST OF ABBREVIATIONS

RES	Renewable Energy Sources
DGS	Distributed Generation Systems
VSI	Voltage Source Inverters
THD	Total Harmonic Distortion
IEEE	Institute of Electrical and Electronics Engineers
ABNT	*Associação Brasileira de Normas Técnicas*
IEC	International Electrotechnical Commiission
VDE	*Verband der Elektrotechnik*
RMS	Root Mean Square
PRODIST	*Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional*
INEP	*Instituto de Eletronica de Potência*
HERIC	Highly Efficient and Reliable Inverter Concept
NPC	Neutral Point Clamping
PI	Proportional Integral
PR	Proportional Resonant
IEEE	Institute of Electrical and Electronics Engineers
NBR	Norma Brasileira
DC	Direct Current
AC	Alternate Current
PLL	Phase Locked Loop
PV	Photovoltaic
MPPT	Maximum Power Point Tracker
SOGI	Second Order Generalized Integrator

SRF	Synchronous Reference Frame
DSC	Digital Signal Controller
PWM	Pulse Width Modulation

LIST OF SYMBOLS

v	Voltage
i	Current
V_n	N harmonic voltage peak value
I_n	N harmonic current peak value
THD_i	Current total harmonic distortion
V_{dc}	Volts direct current
S_n	Switches
D_n	Diodes
L	Inductor
C	Capacitor
R	Resistance
L_o	Output inductor
v_g	Grid voltage
i_g	Grid current
L_1	Converter's side inductor
L_2	Grid side inductor
C_f	LCL+RC filter capacitor
C_d	Damping capacitor
R_d	Damping resistance
C_{trap}	Trap capacitance
f_g	Grid frequency in Hz
f_s	Switching frequency in Hz
v_{bus}	Bus voltage
V_{bus}	Bus voltage mean value

k_v	Bus voltage measurement gain
k_i	Grid current measurement gain
k_g	Grid voltage measurement gain
V_{ref}	Voltage reference mean value
I_{ref}	Current reference mean value
i_{ref}	Current reference
C_v	Voltage loop compensator
C_i	Current loop compensator
H_{pll}	PLL transfer function
H_{ff}	Feedforward transfer function
d	Duty cycle
k_{amp}	Output from voltage loop compensator
e_v	Voltage error
e_i	Current error
i_{cont}	Output from current loop compensator
s	Laplace operator
H_{bpf}	Band pass filter transfer function
ω_g	Grid frequency in rad/s
k	A general gain
k_{pll}	PLL gain
k_{ff}	Feedforward gain
f_{vbus}	Bus voltage frequency in Hz
C_{bus}	Bus capacitance
V_Δ	Peak voltage of the triangular waveform

k_{ii}	Current compensator integral gain
k_{pi}	Current compensator proportional gain
k_{iv}	Voltage compensator integral gain
k_{pv}	Voltage compensator proportional gain
G_{aa}	Anti-aliasing transfer function
C_{aa}	Anti-aliasing capacitor
R_{aa}	Anti-aliasing resistance
v_{ac}	Alternate parcel from v_{bus}
v_{ab}	Quasi-instantaneous average value of the bus voltage

CONTENTS

1 INTRODUCTION

1.1 BACKGROUND

The global demand for electricity is constantly growing and the recent concern with the environment has driven the spread of the so-called renewable energy sources (RES) [1], in which fuel cells, photovoltaic, wind turbines, biogas and hydraulics has been established as alternatives for distributed generation systems (DGS) [2]. In these systems, voltage source inverters (VSI) are widely used for integrating RES with the grid due to their superior features, such as full controllability, sustainability, and improved efficiency [3]-[4].

DGS connected to the electricity distribution network must meet the recommendations and requirements defined in technical standards to avoid the degradation of the quality of the energy delivered and guarantee the safety of operation of the electric power system. A common method for assessing power quality is to compute the THD (Total Harmonic Distortion), which measures the deviation of the waveform from a pure sinusoid. The harmonic distortion can be defined as follows:

> Harmonic distortion – the change of the voltage or current waveform relative to that of a pure sine wave by the addition of other waveforms, usually at multiples of the fundamental frequency (p-11, [5])

The harmonic distortion concern begins in 1916 when Steinmetz proposes the Delta connection in transformers in order to confine the third order harmonic currents in alternate power systems. These harmonic currents were caused by the magnetic saturation of iron in transformer and machines [6]

The sinusoidal waveform is perfect conditions in the power systems, once machines, transformers and electric equipment are designed based on it. However, in practice, this sinusoidal waveform is rarely seen. Any periodic waveform, whether a distorted sine, a square or triangular forms, or even regular peaks, is the result of the superposition of sine waveforms that have a fundamental component and a series of waves called harmonics, responsible for the distortion.

Recently, due to increased use of electronics equipment/systems, the presence of harmonic contents in the grid has grown [7]. Some examples of distorted waveforms and its respective harmonic spectrums are shown in Figure 1.

Figure 1 – Examples of distorted waveforms and their respective harmonic spectrum.

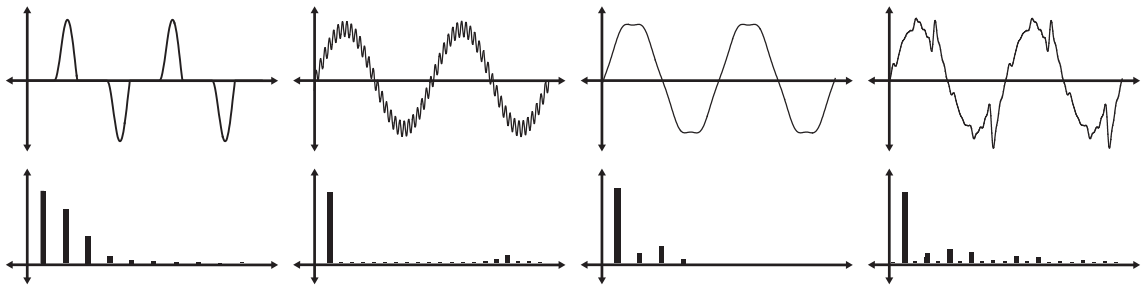

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Figure 1 (a) shows the behavior of the input current of classic rectifiers, while (b) shows the current waveform distortions from the high frequency switching effect. The waveform in Figure 1 (c) shows the typical voltage of the main grid, emphasizing the sags at the peak consumption, which comes from many non-linear loads connected at the same substation transformers. Finally, Figure 1 (d) represents a switching effect in the output current of a photovoltaic inverter with a poorly designed control loop, in which the output current cannot follow the reference.

In the literature, it is possible to find several methods for harmonic analysis. Among them, the following stand out:

1) Fourier series
2) Fourier transform
3) Wavelet transform

In summary, harmonic distortion is related to events associated with currents and voltages waveforms deformations in relation to the sinusoidal waveform at the fundamental frequency [8].

Distorted voltage and currents can be described as:

$$v(t) = V_o + V_1 \sin(\omega t + \varphi_1) + V_2 \sin(2\omega t + \varphi_2) \ldots \quad (1)$$

$$i(t) = I_o + I_1 \sin(\omega t + \varphi_1) + I_2 \sin(2\omega t + \varphi_2) \ldots \quad (2)$$

The current total harmonic distortion (THD_i), focus of this work, is defined as follow:

$$THD_i = \frac{\sqrt{\sum_{n\neq 1} I_n^2}}{I_1}, \quad (3)$$

in which I_1 represents the amplitude of the fundamental component and I_n the amplitude of the *n-order* harmonic components. It is worth mentioning that the THD measurement is carried out on steady state and current values can be both, peak or Root Mean Square (RMS).

The THD of the output current in grid-connected inverters, for example, should be kept under 5% during normal operational conditions according to the IEEE1547:2003 (North America) [9], IEC61727:2004 (International Safety) [10], NBR16149:2013 (Brazil) [5] and VDE0126-1-1:2013 (Germany) standards. Table 4, in the appendix, provides a comparative analysis of the main power quality criteria for grid-connection according to each of the standards mentioned.

These harmonic distortions can cause unnecessary overheating of transformers and rotating equipment, nuisance tripping of circuit breakers and blowing of fuses, overloading of neutral conductors, in addition to overstressing of power factor correction capacitors [11], [12]. Moreover, such current harmonics also lead to voltage harmonics in weak grids, characterized by large and variable impedances. This results in low power quality of the grid, resonances, and finally, stability issues in the power system [11], [13].

One of the biggest contributors to the appearance of grid-current harmonics is the grid voltage itself. It is important to highlight that the regulatory agencies also set harmonic limits for grid voltage. Table 5 - in the attachment section at the end of this document - shows the limits for Brazilian concessionaires, determined by the PRODIST module 8 [8].

1.2 RELATED WORKS AND RESEARCH GAP

The THD is a metric used to quantify the extent of harmonic distortion in a signal. It is calculated as the sum of the magnitude of all harmonic components to the magnitude of the fundamental frequency. To achieve the THD requirement defined in

standards, various types of control methods have been introduced in the literature [14], so that the most traditional current controllers for grid-connected inverters have been based on the usage of proportional-integral (PI) [15], [16] and proportional-resonant (PR) controllers [17], [18]. Nevertheless, the value of the THD output current in grid-connected systems interfaced by power electronic devices varies significantly [19]. Typically, at lower power levels, the current THD is increased, becoming the object of study by many researchers, in order to find the causes of such a phenomenon. A common explanation is that the closed-loop current controls, which are intended to minimize the harmonic components, are less effective as the power is reduced [19]. The quantization and resolution effects of measurement and control devices are also pointed out as possible causes [20], meanwhile some researchers have suggested that DC-link voltage regulation is highly related to the reference current resolution [21].

Basically, the current THD of grid-connected inverter may be affected by harmonics produced from the reference signal, external grid voltage, and DC-link voltage ripple [22]. The reference signal may be distorted by the signal supplier or grid harmonics passing through the phase locked loop (PLL) [23], [24]. Therefore, a high performance PLL is mandatory for grid-tie inverters, and normally enough to not degrade the quality of the output current waveform.

Regarding the grid-voltage harmonic, distinct mitigation methods can be found in the literature [22], but a simple voltage feedforward loop is typically effective to suppress the harmonics in the output current [25].

The effect of the DC-link ripple on harmonic generation, on the other hand, is more difficult to mitigate, so many methods have been proposed to solve this problem [26]-[33]. Although many studies assume the DC-link voltage as constant for the modeling, in single-phase grid-connected inverters, the instantaneous output power exhibits a pulsation at the double-line frequency, whereas the input power generated by the RES is considered constant at normal operation. This incompatibility makes necessary the inclusion of a decoupling capacitor at the DC-link to store or delivery the excess of energy [26], which results in double-line frequency voltage ripple at the DC-link. One issue caused by this double-line voltage ripple is the harmonic distortion in the output current. To reduce the ripple, electrolytic capacitors with large capacitances can be used, but they have been avoided due to their limited lifetime [27]. Active decoupling methods using additional circuitry have also been proposed [28], [29], however, they can increase cost, complexity, and power losses of the system.

Moreover, control solutions range from the simple usage of a stop-band filter [30] tunned at the double-line frequency during the DC-link voltage measurement for feedback control, to the implementation of advanced strategies based on active coupling [31], [32].

Even though the aforementioned methods have been proposed to solve this problem, comprehensive and systematic analysis of the harmonic generation process due to DC-link voltage ripple are not common in the literature. A generalized approach that analytically determines the harmonic spectrum of the DC-link for any VSI is proposed in [33], but this study only focus on high-frequency switching ripples, while lower order DC-link voltage harmonics are ignored; in addition the effect of these harmonics on the output grid current is not evaluated. By contrast, Du *et al.* [34] develops a closed-form solution for the grid-current harmonics caused by the double-line frequency ripple voltage on the DC-link. However, double-line frequency is not the only harmonic ripple component that generates distortion in grid current waveform. When the ripple-caused harmonics are reflected back to the DC-link voltage, it generates an endless iterative process, so that a complex harmonic spectrum is found in the DC-link voltage ripple [33].

Thus, a more complete method describing the relation between the grid-current harmonics and DC-link voltage ripple is still missing in literature. This method is necessary to accurately estimate the THD of the grid current produced by grid-connected inverters.

1.3 CONTRIBUITIONS

In view of the above, this thesis proposes a novel method to estimate the THD of the output current generated by grid-connected single-phase inverters with feedback control. The method is based on the modeling of the closed-loop control system and takes into account the effects of all low-order harmonic perturbations generated by both DC-link and grid voltage.

The obtained closed-form equation that quantifies the THD of the grid current can be an important tool for analyzing harmonic requirements imposed by standards and evaluating the effectiveness of existing THD improvement approaches. Furthermore, it may also be useful in the designing of feedback controllers, output

filters, and decoupling capacitor of grid-connected systems without penalizing their power quality performance.

1.4 STRUCTURE OF THE THESIS

The remainder of this study is organized as follows: initially, section 2 introduces grid-connected single-phase system considered in the modeling and also presents a brief analysis of each part of the control loop that interferes in the grid current. Afterward, in section 3, it is presented the proposed closed-loop analysis considering the disturbances on the grid and on the DC-bus voltage in order to identify the harmonic content and THD of the grid current. Lastly, section 4 reveals the outcomes from simulations and experimental tests, exploring five different scenarios for validation. Following that, Section 5 offers the conclusions, providing a clear summary of the insights gained.

2 GRID-CONNECTED *VSI* SYSTEM DESCRIPTION

Initially, the idea and conception of this thesis arose from a project carried out by the company LUG Power Electronics in partnership with INEP - Institute of Power Electronics for the development of a Photovoltaic (PV) microinverter.

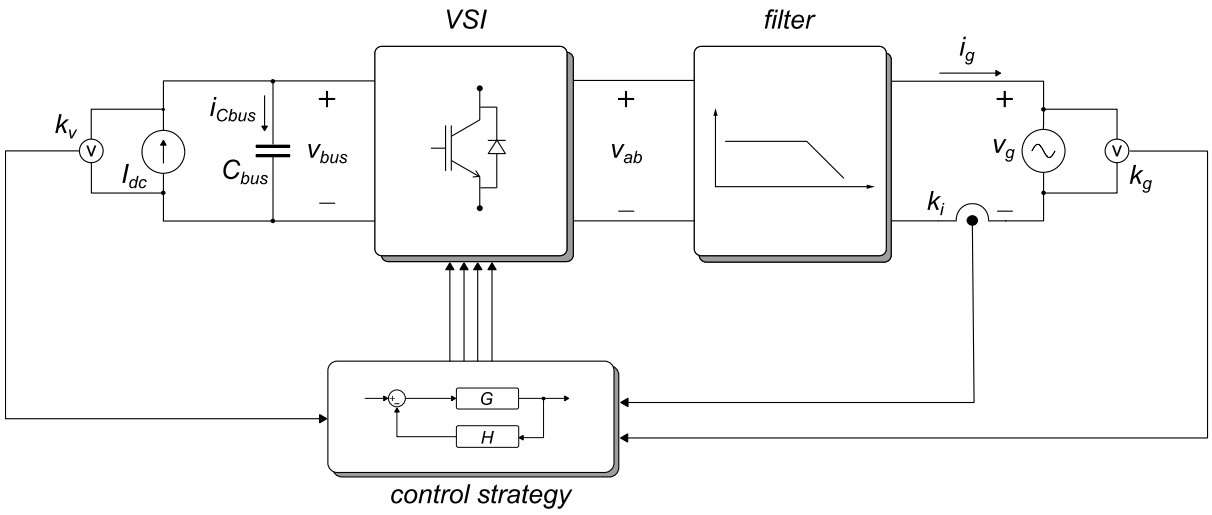
During the practical converter tests, significant efforts were expended in numerous attempts to improve the quality of the current injected into the electrical grid. A substantial portion of these efforts was focused on exploring different compensator's configurations, which, in some cases, eventually led to instability in the converter. This issue highlighted the need for a detailed understanding of the effects of controllers on the behavior of the output current in closed-loop operation.

The primary objective is to anticipate the THD (Total Harmonic Distortion) of the output current according to the parameters defined by the designer, thereby avoiding rework on the test bench and enhancing the converter's stability. Consequently, it is possible to pre-evaluate different solutions and seek the optimization of components, especially passive elements, thereby reducing the overall solution cost and always ensuring compliance with standards.

The generic grid-connected single-phase system considered in this study is depicted in Figure 2. The RES is modeled by a DC current source and the grid voltage is represented by an AC voltage source. Since each RES has specific characteristics, in this study, the chosen source is selected to be a photovoltaic array, aligned with the mentioned project. This simplifies the process of defining the topology, filter, and control strategy, as they are tailored to a particular application.

It is commonly known that there are numerous topologies, filter types, and control strategies for connecting a single-phase PV inverter to the electrical grid. This section aims to provide a brief review of traditional options, highlight their advantages and disadvantages, and define the one to be used in this work. It is worth noting that the methodology applied in this study can be replicated for any type of topology, filter, or control strategy.

Figure 2 – Generic Grid-converter system.



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2.1 VSI TOPOLOGY

The research goals on converters that make up the DC-AC stage are defined to provide high performance interface to PV generation. The first point to be considered is that the DC-AC converter must have high efficiency, with low conduction losses, minimizing the number of switches at the current path.

Other point that must be analyzed is the safety, since the PV module construction process and its installation make appear a capacitance to earth, generating a path for leakage current [38]. Allied to this, and respecting NBR16149:2013 standards, the inverter needs to guarantee low dc current injection into the main grid.

In the literature, it is found two inverters' options: isolated and transformerless [39]. Although isolated topologies reduce common-mode problems and DC current injection, galvanic isolation compromises the systems efficiency by approximately 1 or 2 % [38], in addition to decreasing the system's power density.

Since photovoltaic systems have low efficiency in relation to the energy provided by the sun, the losses in the energy-processing converters must be as small as possible, thus, transformerless topologies are preferred. A survey of commercial PV microinverters topologies [40] shows the benefits of non-isolated topologies in terms of volume, weight, and efficiency, becoming a cheaper solution in relation to the isolated topologies.

Transformerless topologies pose significant challenges, particularly with respect to common-mode current and DC injection, compared to isolated topologies. In recent years, a range of converters have been proposed in the literature to overcome these hurdles. Many of these solutions involve adaptations of traditional topologies, as depicted in Figure 3.

The main alternatives for transformerless dc-ac converters for grid connection are:

1) H-bridge
2) H5, H6 and variations
3) NPC-based topologies
4) HERIC
5) Two paralleled buck converters

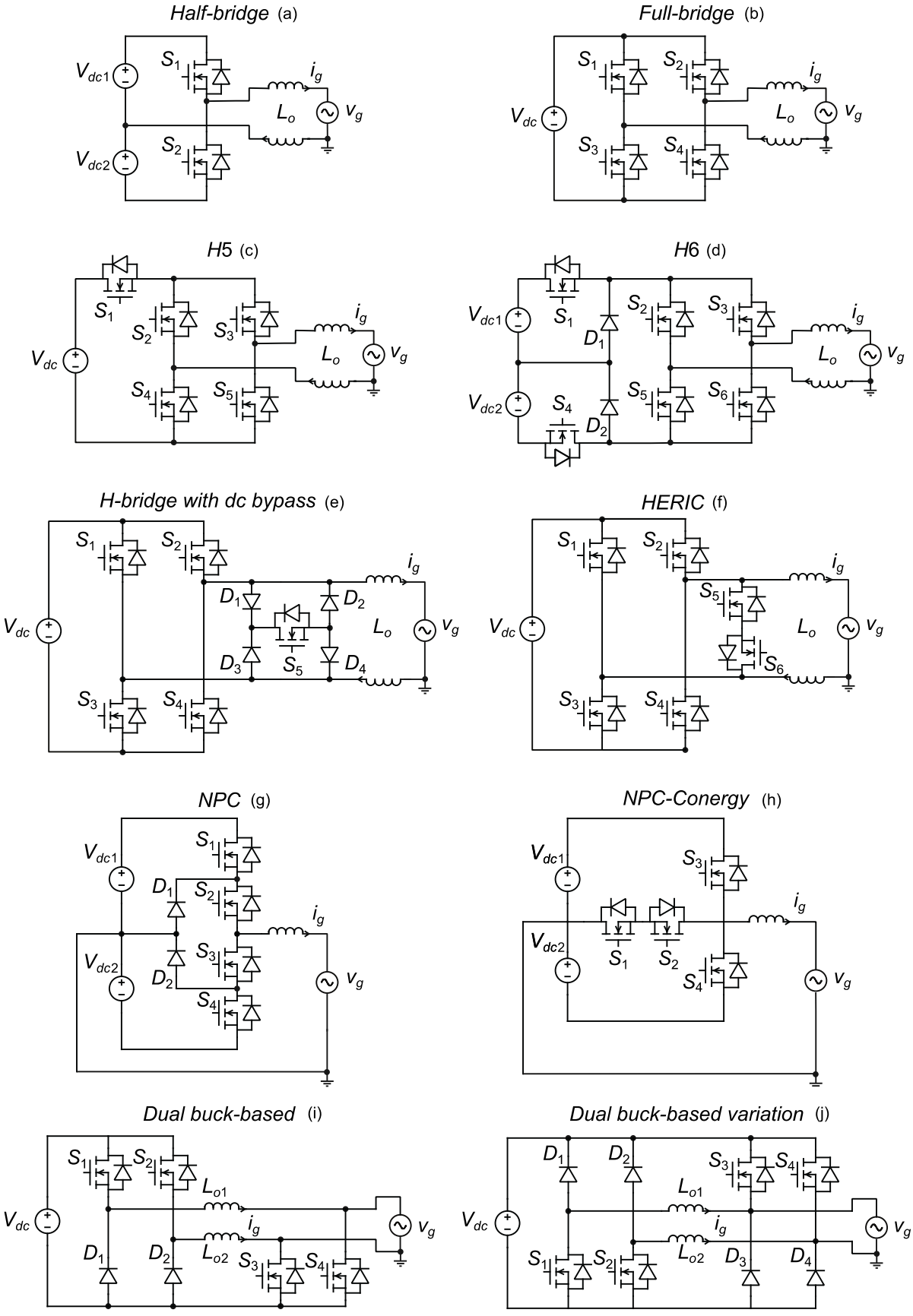
Despite having few semiconductors in the current path, conventional Half-Bridge inverters as shown in Figure 3 (a), has capacitors associated to generate a midpoint, reducing its leakage current, but requiring some care with their voltage balance. Furthermore, the voltage gain is reduced by half the bus voltage, and it is only able to synthesize two-level voltages. Full-bridge inverters [Figure 3 (b)], on the other hand, employ more semiconductors, but a voltage gain more suitable for grid-connected applications than the half-bridge inverters [39], [42].

The unipolar modulation is the most popular for Full-bridge inverters, ensuring the three-level voltages and improving the output current THD, however, when the zero level is synthesized, a high leakage current surges because of the low impedance of the parasitic PV module capacitor that creates a path for the common mode current circulation when both, grid and PV module are grounded.

Thereby, this topology usually requires large common-mode filters [38], [43]. A way to overcome this effect is applying unipolar modulation, in which the level zero is not synthesized, however, compromising the injected current quality and the volume of the grid-side filter [41].

The H5-inverter, H6-inverter, and H-bridge with dc bypass shown in Figure 3 (c), (d) and (e) respectively, try to remedy these problems by inserting a high-frequency switch between the ac and dc sides. Its main function is performing electrical decoupling between PV and grid, avoiding high-frequency components circulation through them. The disadvantage is that these inverters will always have at least three semiconductors in the current path, increasing conduction losses [44]-[47].

Figure 3 – Single-phase PV inverters topologies.



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The Highly Efficient and Reliable Inverter Concept (HERIC) shown in Figure 3 (f), presents a viable solution with only two semiconductors in the current path at all stages of operation, similarly to the classical Full-bridge inverter. This converter also reduces the leakage current influence by decoupling input from the output when the zero-voltage level is synthetized on the output. The main drawback is that such converter is patented [50].

In the NPC-inverter topologies illustrated in Figure 3 (g) [48] and Figure 3 (h) [49], the neutral is connected to the bus midpoint avoiding leakage current, since the voltage on terminal of the PV modules are constant with respect to the earth point. Such inverters still have the advantage of synthesizing 3 voltage levels, but they end up being harmed because a high input voltage dependence, usually 2 times bigger than the others mentioned before, being a solution with greater potential for higher voltage applications [43].

Considering the exposed, one of the main solutions still remain in the paralleled buck converters, each one performing a half-cycle [51]. The benefits of this type of topology, called dual-buck based inverters, are:

1) Shoot through free at least in their DC-side
2) Low impedance between the DC-bus and the AC-port
3) Employment of low-frequency switches, reducing switching losses
4) Maximum of two semiconductors in the current path
5) Simplicity
6) No patents

Due to the advantages mentioned, the DC-AC converter chosen in this work is the classic dual-buck inverter shown in Figure 3 (i). Reference [40**Error! Reference source not found.**] discussed about a comparison between DC-AC stages from commercial microinverters that point to the dual-buck as one of the best solutions, mainly in relation to efficiency, which is a mandatory project requirement in this thesis, aiming at the optimization of a PV 500 W system. The two-inductor dependence is the main drawback of this structure, but with techniques that increase the magnetic utilization according to [52], this negative aspect may be overcame.

2.2 GRID-CONNECTED FILTER

One of the biggest challenges of grid-connected power converters today is to reduce cost and increase the power density [53]. It implies that their output passive filters must present low size and volume besides complying with the harmonic limitations set by the aforementioned standard [54]. Some of the most traditional filter's topologies used in grid-connected applications are shown in shown in Figure 4.

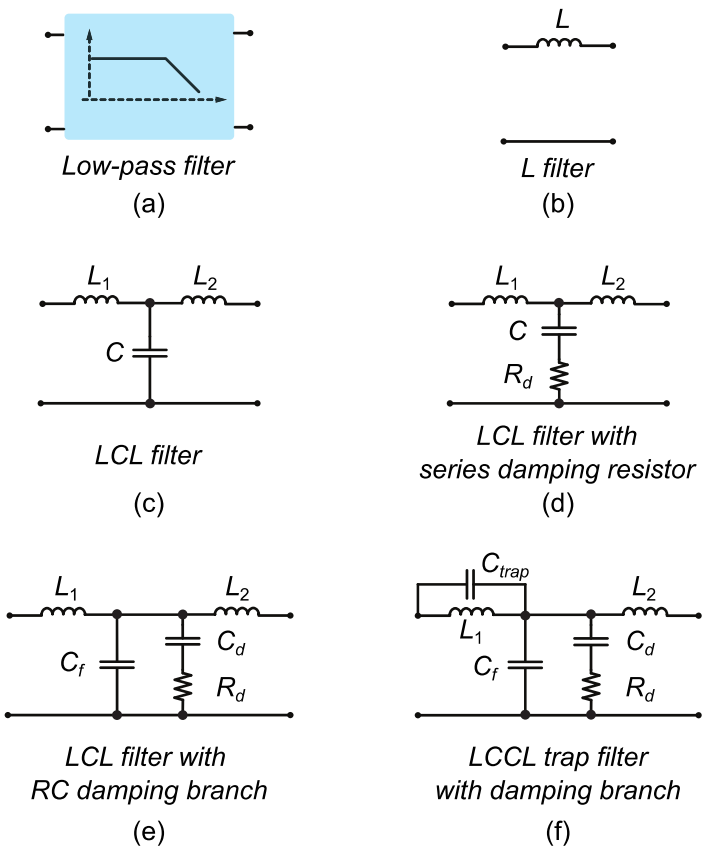
In order to attenuate the high-frequency harmonic components caused by the switching [55], in general, the output filter consists of a low-pass filter (Figure 4(a)) whose attenuation factor is directly associated with the complexity of implementation [56] - [58]. Although *L* filters (Figure 4 (b)) are an option and have already been employed in several previous works [59], [60], high-order *LCL*, *LCL+RC*, *LCL-trap* filters, are becoming a trend in grid-connected applications, since they can meet the harmonic limitations established by grid-connection standards with smaller size and cost [62], [63]. Furthermore, *LCL* filters (Figure 4 (c)) can reduce losses and provide an attenuation of 60 dB/decade after the resonance frequency compared to the 20 dB/decade from *L* filters [61], [64], [65].

Conversely, high-order filters require more complex designing methodology and the resonance caused by the exchange of energy between the inductors and the capacitor may imply oscillations and instabilities; thus, damping techniques must be employed [66]. Several topologies of low-pass filters with passive and active damping are extensively addressed in the literature [65] - [71].

The objective of the *LCL* filter with damping is to minimize the magnitude value of the output current or voltage around the resonance frequency, avoiding oscillations and instabilities. This attenuation would be easy to be reached only by inserting a resistor in parallel with the capacitor C_f of Figure 4 (d). However, this solution results in high losses since the resistor is in the patch of the current in the fundamental frequency.

Alternatively, the damping resistor R_d may be connected in series with a second capacitor C_d, resulting in the damping branch shown in Figure 4 (e). When correctly calculated, the capacitor C_d provides high impedance at low frequencies and prevents power dissipation over the resistor. Conversely, near the resonance frequency, which typically appears in kilohertz, the mentioned impedance is reduced, and the damping effect becomes more significant.

Figure 4 – Passive filters structure with low-pass characteristic.



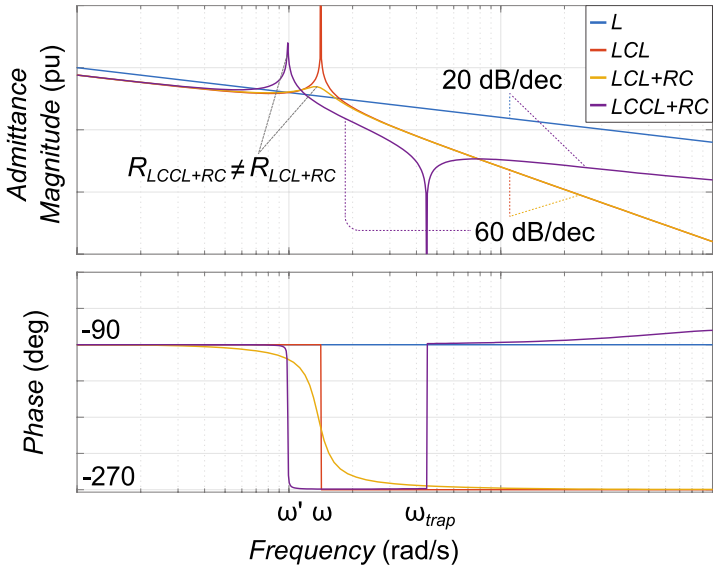
Source: prepared by the authors.

In summary, the output filter purpose is the mitigation of switching harmonics that appears in electronic processing. A suitable filter for this application must have the following characteristics:

1) Low attenuation of the signal to be transmitted (f_g)
2) High attenuation of the signal to be filtered (f_s)
3) Low resonance amplitude (high damping)
4) Low losses (high efficiency)
5) Low price, volume and weight

In Appendix 1 of this document, a more comprehensive study relating the filters under discussion can be found. This section unfolds detailed mathematical analyses of each filter, leading to the derivation of their transfer functions. From these transfer functions, a generalized Bode diagrams for the respective filters can be plotted (Figure 5), highlighting the filters characteristics.

Figure 5 - Generalized bode plot of the passive filters.



Source: prepared by the authors.

The *LCL+RC* filter was selected for implementation in this work due to the superior performance and numerous advantages, which include a smaller volume compared to lower order filters, damping simplicity, reduced losses, and high attenuation factor. These benefits make the *LCL+RC* filter an optimal choice for grid connection in this context. [69].

A design suggestion of the elements that make up the filter is presented in detail in Appendix 2 of this document.

2.3 CONTROL STRATEGY

The growth of distributed generation, driven by photovoltaic energy, brings with it some problems such as security, instability, outages, and energy quality. To overcome these issues, a suitable PV inverter must be designed along with its control structure. The literature presents a wide range of control techniques for single-phase inverters [72]. [73] classifies them according to feedback, control parameters, output filter, and modulation.

This section aims to present a classic and usual control strategy that contains the main characteristics for grid-connected inverters that process power from a PV source.

The control strategy for photovoltaic inverters also encompasses routines for checking the proper functioning of the inverter, as maximum power point tracker (MPPT) and anti-islanding methods. Usually, a state machine is running during the converter's operation, checking the measurements to keep the operation within the standards. The supervisory system also performs the converter's initialization procedures foreseen in the standards, such as measuring the impedance of the positive and negative PV terminals to the earth point and checking the relays responsible for disconnecting the converter from the grid.

However, it's important to emphasize that the development of the thesis proposal is not affected by the supervisory system, as it does not interfere on all cycles of the current injected into the electrical grid. The minor disturbances from active anti-islanding methods can be disregarded from the analysis since their frequency is much smaller than that related to the current injected into the electrical grid [74].

2.3.1 DC-AC control loop

The DC-AC control loop consists of maintaining bus-voltage regulation, and also overseeing the power distribution to the electrical grid, thereby ensuring a high quality of the current injected into the grid.

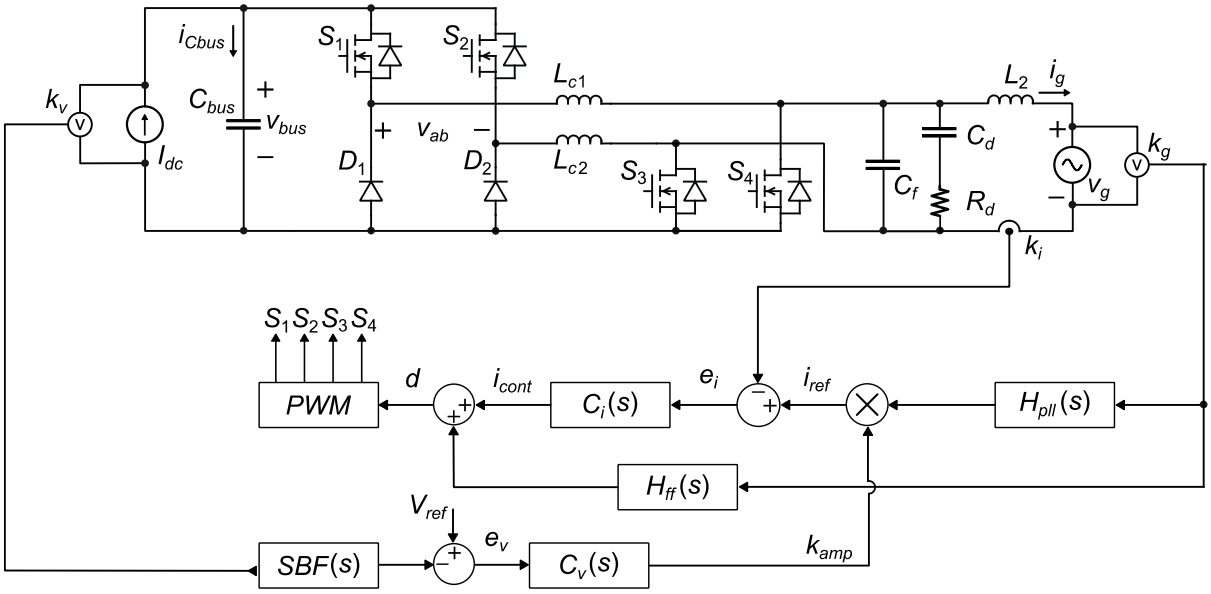
As highlighted in the introduction, a multitude of structure types have been suggested, and a diverse array of controllers have been put forward over recent years [15] – [18].

In this work, the feedback control is formed by an inner and an outer controls loop. In the outer loop, the DC-link voltage is measured by a transducer with gain k_v. The measured signal passes through a stop-band filter with transfer function $SBF(s)$ and it is compared with the DC-link voltage reference V_{ref}. The error resulting from the comparison is compensated by a voltage controller with transfer function $C_v(s)$. The output of the voltage controller determines the amplitude of the grid-current reference i_{ref} to be used in the inner loop. The shape of the grid-current reference is generated by a phase-locked loop ($H_{pll}(s)$) whose input comes from the measurement of the grid voltage by a transductor with gain k_g. In the inner loop, the grid current is measured by a transducer with gain k_i and is compared with the reference current i_{ref}. Similarly, the error resulting from the comparison is compensated by a current controller $C_i(s)$. To minimize the controller efforts, a grid voltage feedforward loop $H_{ff}(s)$ is added to the

current controller output, ensuring it compensates only the variations around the steady-state operating point. Finally, the signal enters a pulse-width modulator (PWM) to generate the control signals of the VSI switches.

The structure selected for implementing the control strategy in this thesis is conventional, employing straightforward compensators to simplify the mathematical validations. This methodology is flexible and can be expanded to fit various control strategies and compensators. Now, it is possible to substitute the blocks in Figure 2 and fully reproduces the structure under analysis (Figure 6).

Figure 6 – Dual-buck converter with an LCL+RC, integrated with a control structure.



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Proceeding further, an individual analysis will be conducted on each block of the control structure. This will pave the way for defining the equations and gains employed in the derivation of the closed-loop model.

2.3.1.1 The block H_{pll}

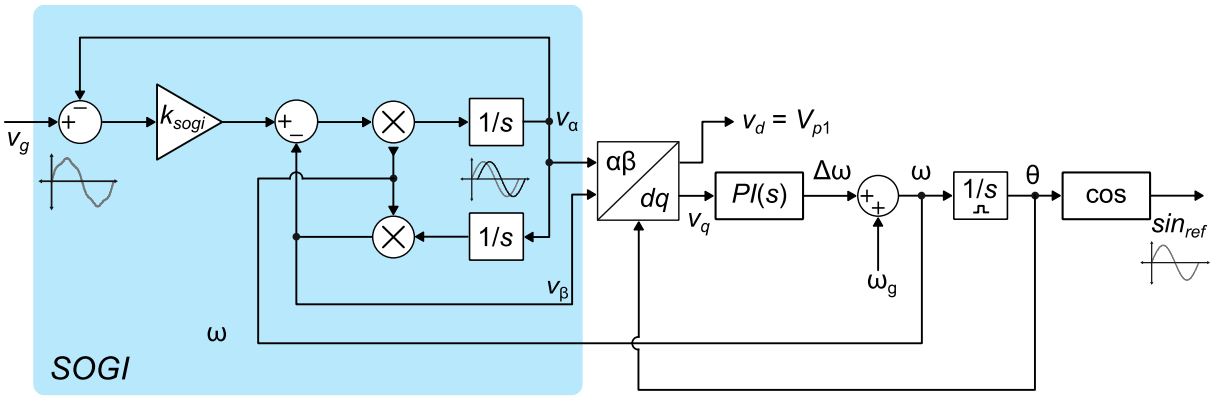
There are several synchronization techniques with the power grid in the literature, such as zero-crossing-detection-base methods [75], Fourier transform [76], neural networks [77], among others. In the power electronics scenario, a technique that is prominent nowadays is the Phase-Locked Loops (PLL's) due to its robustness, simplicity, and effectiveness [78].

The PLL's output is normally a sine wave in phase with the fundamental component of the grid voltage, allowing the inverter operation with high power factor. To meet these requirements, plenty of single-phase PLL has been proposed in recent years [79]-[85]. In a simple way, all PLLs have three basic parts, the phase detector, the loop filter, and the voltage controller oscillator [79].

Reference [86] makes a comprehensive review about the most usual PLL topologies and it points to the Second Order-Generalized Integrator (SOGI) as one of the most popular structures applied in the phase detector part. The Synchronous Reference Frame (SRF) SOGI-PLL proposed by [84] has excellent dynamic response, noise rejection, harmonic filtering and for these benefits will be used in this work for practical validations.

As the goal is to make the reference signal as immune as possible from grid disturbances, the SOGI harmonic filtering can be enhanced using second-order SOGI-QSG [87], pre-filter DSOGI-FFL-WPF [88], among others. Further analysis of SOGI-SRF-PLL dynamics, its modeling, and the loop filter controller design can be found in Appendix C.

Figure 7 – SOGI-SRF-PLL.



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For mathematical validations, this section presents a simplified model to describe the PLL dynamics at low frequencies in steady state, since the PLL is a non-linear structure due to sine and cosine operations.

Ideally, for phase-locked loops, it is expected unitary gain at the signal's fundamental frequency and null gain at all other frequencies. Such a characteristic leads to a second-order band-pass filter (4). This type of filter, which is also employed

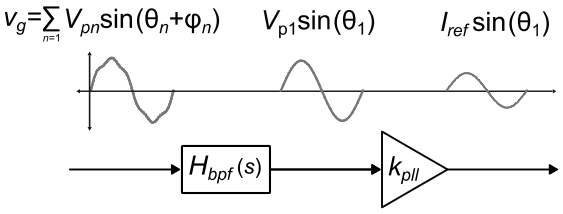
in the SOGI's technique, is commonly used in measurement circuits that need to select a specific frequency range and have a high sensitivity to signal variations. Therefore, with these considerations, it can be stated that the PLL, at low frequencies and steady state, can be modeled as a band-pass filter:

$$H_{bpf}(s) = \frac{k\omega_g s}{s^2 + k\omega_g s + \omega_g^2} \tag{4}$$

In the mathematical validation presented in this thesis, the PLL is assumed to have a unitary gain (k = 1) at the fundamental frequency and a null gain at all other frequencies. Additionally, a gain parameter k_{pll} , predefined in the project specifications, is used to adjust the amplitude of grid voltage to the amplitude of the grid-current reference, as show in Figure 8.

This consideration implies that the PLL will prevent the current reference waveform from containing direct disturbances from the power grid in steady state.

Figure 8 – Simplified PLL representation.



Source: prepared by the authors.

Under the adopted assumption, considering that the PLL is properly designed, and that the system is operating in a steady state (condition under which the Total Harmonic Distortion of the grid current is measured) the band-pass filter will no longer affect the mathematical analysis of grid current. Therefore, it can be disregarded from the block diagram, leaving only the gain k_{pll} as a significant factor to consider.

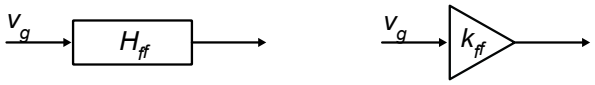
2.3.1.2 The block H_{ff}

Feedforward compensators are used to improve the performance in closed-loop converters by anticipating the effects of disturbances or changes in the input

voltage or the output load [89]. This way, the feedforward compensator can reduce the error and improve the stability and bandwidth of the system.

In general, this method employs an additional compensator in parallel to the main feedback current control loop, which reads the input voltage (in this case, the grid voltage) and adjusts the output signal accordingly. Usually, a proportional gain is applied to the read voltage to achieve this compensation, as represented in Figure 9. Due to its simplicity and effectiveness, this strategy will be applied in this work.

Figure 9 - Feedforward controller schematic model.



Source: prepared by the authors.

In this configuration, the feedforward minimizes control efforts by making the current compensator act only on the small perturbations around the steady-state operating point. Without the feedforward loop, the compensator of the closed loop has to bear all the efforts to ensure a sinusoidal shape for the grid current, requiring more sophisticated structures (usually proportional resonant controllers) tuned to provide high gains at the grid frequency and its multiples, increasing the complexity of the control strategy.

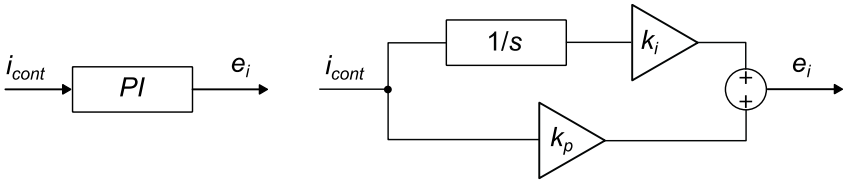
The feedforward compensator control technique assists the controller in this problem and uses the grid voltage acquisition to generate a control signal, which try (in open loop) to cancel the disturbance effect. This strategy is subjected to parametric variations, since it is not a feedback loop, but it helps in coarse adjustments, easing transients and control efforts. In this context, the feedforward loop takes the system to the operating point, whereas the fine adjustment of i_g is accomplished by the main controller, which is implemented into a feedback loop and guarantees precision with simplest format.

The feedforward compensator gain design in this work is based on the analysis of the system transfer function. The mathematical model that describes the system behavior will be derived in Chapter 3 of this document, and from there, the feedforward controller gain can be easily determined. Moreover, a brief description of its impact on the system is also provided.

2.3.1.3 The blocks C_v(s) and C_i(s)

To develop the closed-loop modeling for determining i_g, a PI type controller will be incorporated in both control loops (current and voltage). The configuration of the PI controller applied in this work is presented in Figure 10.

Figure 10 – Proportional Integral schematic model.



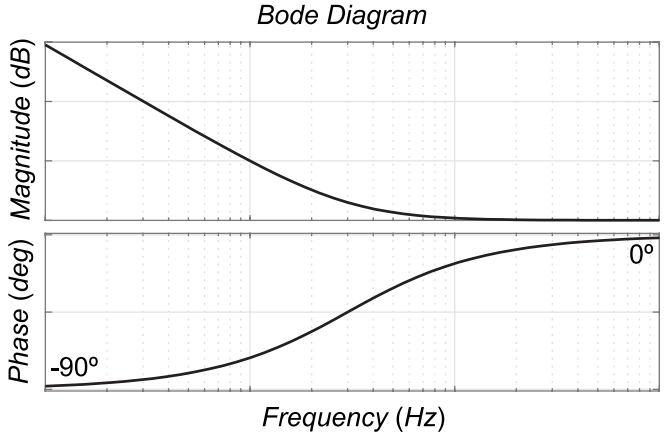
Source: prepared by the authors.

Rearranging the equation to have a better understanding in terms of the gain and frequency of the left-plan zero, it is obtained:

$$PI(s) = k_p \frac{s + \frac{k_i}{k_p}}{s} \tag{5}$$

The frequency response of the PI controller, expressed by its Bode diagram, is shown Figure 11, where k_i/k_p is the zero frequency.

Figure 11 – Generic Bode plot of a Proportional-Integral controller.



Source: prepared by the authors.

It is known that for given a sinusoidal reference, the PI compensator presents a non-zero tracking error in steady state. Nonetheless, the choice of the PI compensator in this work is intentional, aiming to understand and clarify the ability of the feedforward compensator to bring the PI controller to its operating point and presenting a proper dynamic response even with a sinusoidal reference.

In addition, it is worth mentioning that the modeling proposed in this thesis does not restrict the topology of the controller, so even if there is a choice for a proportional-resonant compensator, tuned at the fundamental frequency for reference tracking with zero error in steady state, and others, tuned at the harmonic components for disturbance rejection, the methodology remains valid.

2.3.1.4 The block SBF(s)

In a grid-connected inverter, the bus voltage's primary harmonic component is typically twice the grid fundamental frequency ($f_{vbus} = 2f_g$). This bus voltage is commonly subjected on filtering during its acquisition. These filtering play a pivotal role in providing a current reference free of disturbances, thereby facilitating the use of capacitive bus bars with reduced capacitance values. However, it is mandatory to keep a check on the maximum ripple value to prevent the saturation of the modulation index.

One of the most applied filters, as the one chosen for this application, is the stop-band filter. This filter was selected because it focuses on suppressing only the DC-bus voltage component tuned at 120 Hz, unlike a low-pass filters, that would also attenuate higher-order harmonics. Thus, through mathematical analysis, the stop-band filter allows examining the propagation of other harmonics throughout the circuit.

The filter's Bode plot is illustrated in Figure 12 and the transfer function is defined as follows:

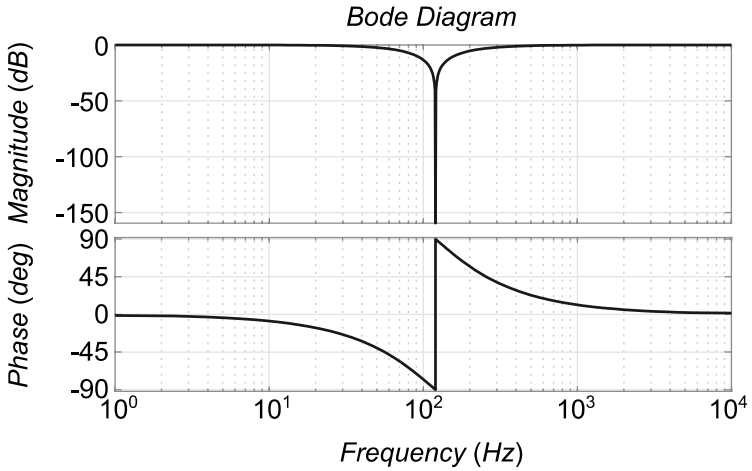
$$SBF(s) = \frac{s^2 + \omega^2}{s^2 + Bs + \omega^2} \tag{6}$$

Herein, ω symbolizes the undesirable frequency in radians per second, while B corresponds to the stopping band frequency width f_b, in Hz ($f_b = B / (2\pi)$).

It is important to note that the oscillation frequency of the bus is twice the fundamental frequency, assuming a perfectly sinusoidal grid voltage. In practice, this is not the case, as frequencies greater than $2f_g$ will manifest in the bus voltage.

However, higher frequencies, while exhibiting smaller amplitudes than that at $2f_g$, are also more extensively filtered due to the passive high-frequency filtering of C_{bus}. Consequently, there is no need to incorporate additional stop-band filters tuned to frequencies exceeding $2f_g$ to improve the quality of the grid current.

Figure 12 – Stop-band filter Bode Diagram.



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2.3.1.5 The block PWM

The PWM block is responsible for modulating the DC-AC converter. Carrier-Based Pulse Width Modulation use comparators between a reference signal and triangular carriers. Such a comparison results in a high or low logic level for switch activation. This logical level is the Digital Signal Controller (DSC) output, which is applied to the driver circuit, responsible for adapting the voltage signal to the level required by the switch, maintaining insulation when necessary.

The PWM schematic model is shown in Figure 13 and the comparator input waveforms are presented in Figure 14.

Figure 13 – PWM schematic model.

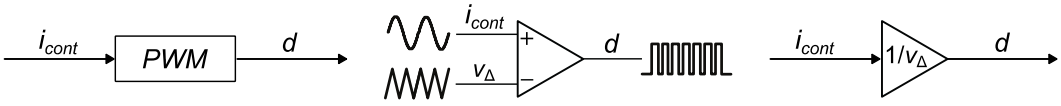

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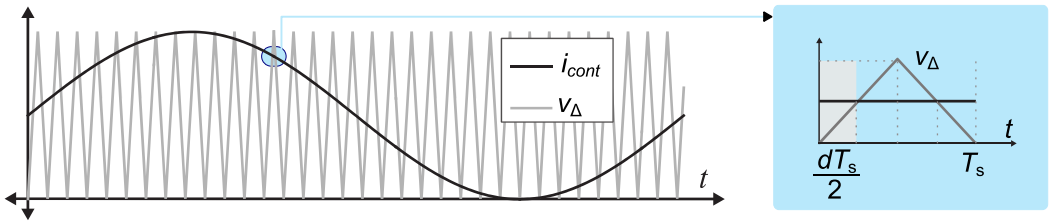
Figure 14 – Bipolar Sinusoidal Pulse Width Modulation.



Source: prepared by the authors.

Considering that the switching frequency is significantly higher than the grid frequency, it can be assumed that the modulator signal, i_{cont}, maintains a DC value within a switching period, thereby rendering the negligible inclination. Upon examination of Figure 14, an equation can be derived to determine the gain of the PWM modulator:

$$\frac{d}{i_{cont}} = k_{pwm} = \frac{1}{V_\Delta} \tag{7}$$

Thereby, in the proposed modeling the PWM will assumed as a gain dependent on the peak voltage of the triangular carrier.

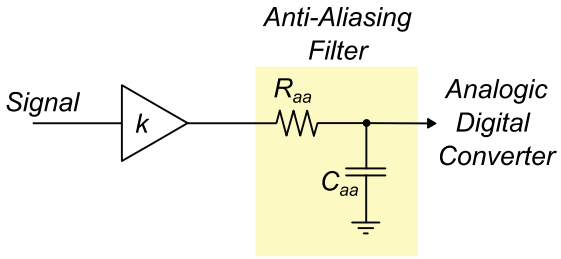
2.3.1.6 The blocks k_v, k_g and k_i

The signals circuit measurement is carried out by means of specific sensors, each one with its particularities. Because of this, signal-conditioning circuits are necessary to adjust the voltage or current levels of the sensor acquisitions to the voltage levels allowed by the DSC.

In cases where the sampling frequency of the DSC is not high enough, the spectrum overlaps (aliasing effect), making it impossible to recover the original signal. In order to prevent this effect, and aiming to maintain the signal acquisition integrity, an anti-aliasing filter is necessary.

Such a filter must have a low-pass characteristic and be positioned at the signal acquisition path (see highlighted area in Figure 15). Its objective is to limit the maximum frequency of the signal at least to half of the sampling frequency, and still guarantee attenuation of the high-frequency components generated by the converter switching.

Figure 15 – Measurement circuit.



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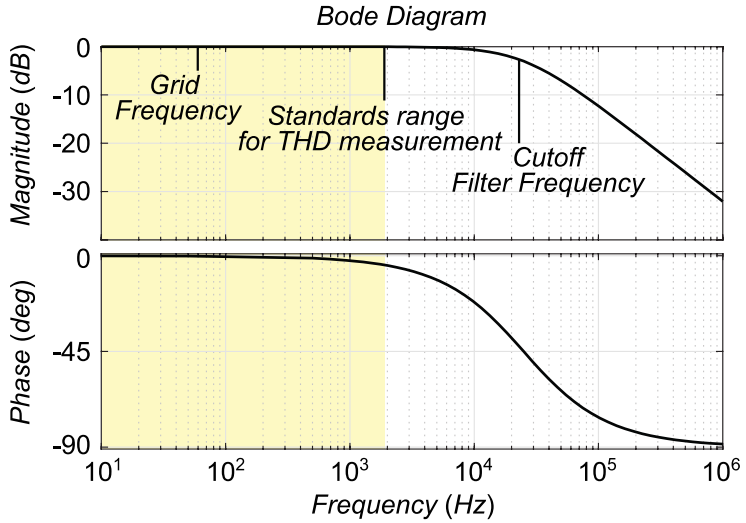
Applying the Laplace transform on the anti-aliasing circuit and adding the conditioning circuit gain, the relation between input and output voltage of the measurement circuit is obtained:

$$G_{aa}(s) = \frac{k}{sC_{aa}R_{aa} + 1} \tag{8}$$

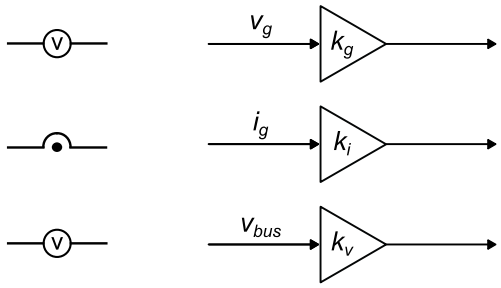
Figure 16 shows the Bode diagram of the measurement circuit. It can be noted that the anti-island filter, if properly designed to attenuated high-frequency content from switching, has its cut-off frequency after the standard limit where THD is measured. Given its flat behavior within this specific range, it can be omitted from the analysis without affecting the overall accuracy of the results. This simplification allows us to reduce the complexity of the measurement circuit to a simple gain, as clearly depicted in Figure 17.

Figure 16 – Bode plot from the measurement circuit.



Source: prepared by the authors.

Figure 17 – Measurement schematic model.



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2.3.1.7 Control system transfer functions

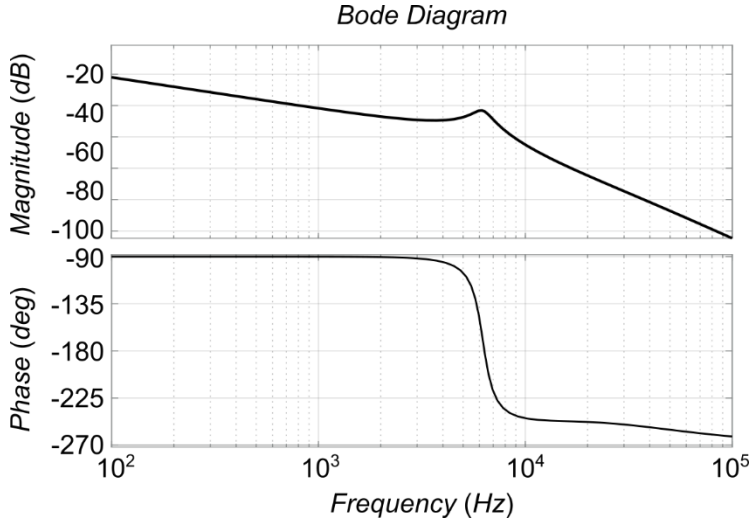
The circuit's transfer functions are designed to provide a mathematical representation of a system's response to an input or disturbance. In this specific context, the two primary variables that should be monitored are the current injected into the grid (which is used in the THD measurement) and the bus voltage, the latter dependent on the grid current itself and on the level of energy processing by the inverter.

From the analysis of the filter (Appendix A) used in this work, it is possible to obtain the equation that determines the behavior of the current injected into the grid i_g in relation to the control variable *d*:

$$\frac{ig(s)}{d(s)} = \frac{v_{bus}(sC_dR_d + 1)}{s^4L_1L_2C_fC_dR_d + s^3L_1L_2(C_f + C_d) + s^2(L_1 + L_2)C_dR_d + s(L_1 + L_2)} \quad (9)$$

The bode diagram of equation (9) it is shown in Figure 18.

Figure 18 - Bode diagram that relates grid current by the control variable *d*.



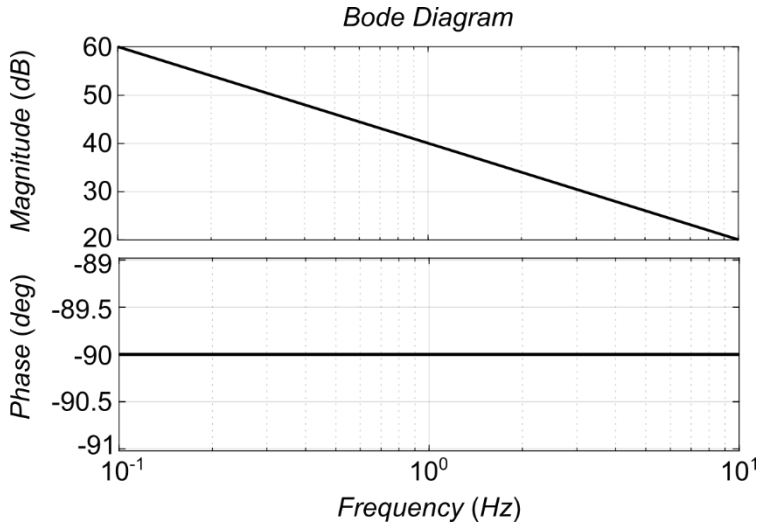
Source: prepared by the authors.

Similarly, the behavior of the bus voltage in relation to the grid current can be represented as:

$$\frac{v_{bus}(s)}{i_g(s)} = \frac{V_p}{2V_{dc}C_{bus}s} \tag{10}$$

The bode diagram of equation (10) it is shown in Figure 19.

Figure 19 – Bode diagram that relates the bus voltage by the grid current.



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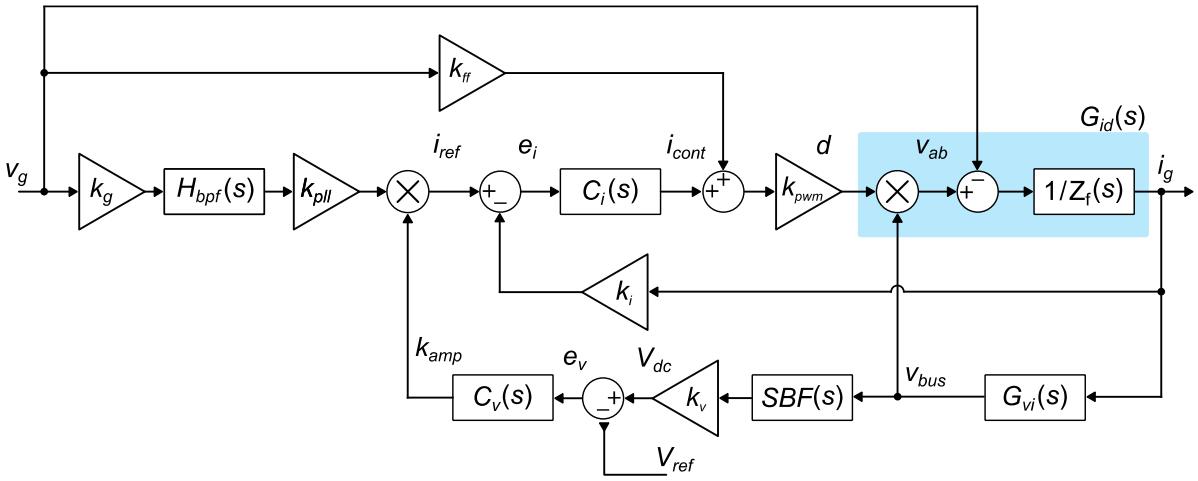
2.3.2 System Analysis through Block Diagram Representation.

Upon evaluating the influence of each block of the proposed system (Figure 2), a block diagram that governs the whole system's operation can be derived, as depicted in Figure 20.

Expanding the block of the transfer function, which is highlighted in blue and correlates the output current with the control variable *d*, the impact of the bus voltage on the grid current becomes evident. This implies that any disturbances in the bus voltage are directly mirrored to the grid current. These disturbances are only attenuated by the impedance of the inverter, which evidences the critical role of the output impedance in maintaining the stability of the grid current amidst voltage fluctuations. As the inverter output impedance is intrinsically linked to the output filter, in this case the LCL+RC, it can be derived from the circuit analysis:

$$Z_{LCL+RC}(s) = \frac{s^4 L_1 L_2 C_f C_d R_d + s^3 L_1 L_2 (C_f + C_d) + s^2 C_d R_d (L_1 + L_2)}{s^3 L_2 C_f C_d R_d + s^2 L_2 (C_f + C_d) + s C_d R_d + 1} \quad (11)$$

Figure 20 – System's general block diagram.



Source: prepared by the authors.

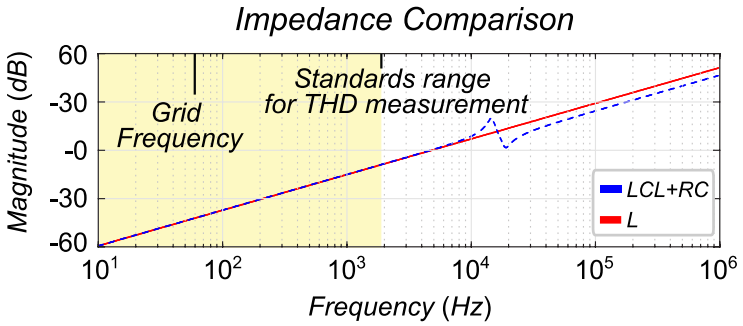
While it's important to note that the filter may be of a high order, its behavior at low frequencies, where Total Harmonic Distortion (THD) is measured, is primarily influenced by the inductances. This is attributed to the fact that capacitors, at these lower frequencies, exhibit the characteristics of an open circuit due to their inherent impedance.

Thus, the equation that describe the impedance of the LCL+RC filter in low frequencies can be simplified as follows:

$$Z_f(s) = s(L_1 + L_2) \quad (12)$$

From Figure 19, it can be observed that both mathematical models (equation (11) and (12)) maintain the same behavior and gain throughout the yellow area, which is the range for the THD measurement according to the standards, validating the previous assumption.

Figure 21 – Impedance gain comparison between Z_{LCL+RC} and Z_f.



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Now, in possession of all the gains and transfer functions of the blocks that describe the closed-loop operation of the circuit proposed in Figure 6, it is possible to proceed with the analysis.

3 CLOSED LOOP MODELING

As mentioned before, the system has two perturbations: the grid voltage and the bus voltage. The grid voltage perturbations are caused by its harmonic components, while the bus voltage disturbance comes from the power oscillations typical of single-phase inverters. When the inverter injects a pure sinusoidal current over a pure sinusoidal voltage with the same frequency, the product between these two quantities results in a grid power with an average value and an oscillating parcel at twice of the voltage frequency.

The same behavior is expected when the grid contains harmonic components, but in this case the product between currents and voltages at harmonic frequencies will result in power oscillation. This power oscillation appears on the dc bus and is partially decoupled by the bus capacitor, making v_{bus} also oscillatory. In this context, the bus capacitor C_{bus} is responsible for mitigating the oscillations of v_{bus}, that is, higher the capacitance, lower the bus voltage ripple. Without loss of generality, one can thus consider that the bus voltage is composed of a continuous (V_{dc}) and an alternating (v_{ac}) parcel. Thus:

$$v_{bus} = V_{dc} + v_{ac} \tag{13}$$

Based on this consideration and analyzing the signals of the outer control loop implemented in the system of Figure 6 (page 45), it is possible to write that:

$$k_{amp} = C_v(s)\left[V_{ref} - k_v SBF(s)(V_{dc} + v_{ac})\right]. \tag{14}$$

The inspection of (14) reveals it can be written as the sum of a constant and alternating parcels, as per:

$$K_{dc} = C_v(s)\left[V_{ref} - V_{dc} k_v SBF(s)\right] \tag{15}$$

$$k_{ac} = -k_v SBF(s) C_v(s) v_{ac} \tag{16}$$

In practical terms, k_{amp} is responsible for adjusting the amplitude of the current reference i_{ref}, which is described by:

$$i_{ref} = k_{amp}k_{pll}k_g v_g = (K_{dc} + k_{ac})k_{pll}k_g v_g \quad (17)$$

By contrast, the analysis of the inner control loop (Figure 6), results in:

$$d = k_{pwm}\left[k_{ff}k_g v_g + \left(i_{ref} - k_i i_g\right)C_i(s)\right] \quad (18)$$

Considering a buck-type dc-ac converter, the quasi-instantaneous average value of the voltage v_{ab} is given by:

$$v_{ab} = d v_{bus} \quad (19)$$

Thus, substituting (13) and (18) into (19), makes possible to write that:

$$v_{ab} = k_{pwm}\left[k_{ff}k_g v_g + \left(i_{ref} - k_i i_g\right)C_i(s)\right](V_{dc} + v_{ac}), \quad (20)$$

In addition, by the circuit analysis, the grid current i_g can be obtained as follow:

$$i_g = \frac{v_{ab} - v_g}{sL_f}. \quad (21)$$

where $L_f = (L_1+L_2)$

Although (21) was obtained by considering that the output filter is of type L, this result is also valid for higher-order filters, such as LCL or LCL+RC, since they are predominantly inductive (type L) at the low frequency range in which harmonic continent is relevant for the THD calculation.

Substituting (20) in (21) yields to:

$$i_g = \frac{\left[k_{ff}k_g v_g + \left(i_{ref} - k_i i_g\right)C_i(s)\right]k_{pwm}v_{bus} - v_g}{sL_f} \quad (22)$$

Organizing (22):

$$i_g = \frac{C_i(s)k_{pwm}v_{bus}i_{ref} + k_{ff}k_g v_g k_{pwm}v_{bus} - v_g}{sL_f + k_i C_i(s)k_{pwm}v_{bus}}. \quad (23)$$

Through (23), one can observe how the feedforward loop (k_{ff}) operates in the system. Without a feedforward controller in the control loop (k_{ff} = 0), (23) will have terms dependent on v_g, meaning it will be influenced by the harmonic components of the grid voltage. Conversely, when a feedforward controller is inserted in the control loop, it can generate a control signal that attempts (in an open-loop manner) to cancel the disturbance caused by the grid voltage. As pointed out in chapter 2, this strategy is subject to parametric variations since it is not a feedback loop; however, it allows for smoothing transients and control efforts. To properly decouple v_g from equation (23), k_{ff} must be calculated by:

$$k_{ff} = \frac{1}{k_g k_{pwm} v_{bus}} \quad (24)$$

Therefore, substituting (24) in (23), it is possible to write:

$$i_g = \frac{C_i(s)k_{pwm}v_{bus}}{sL_f + k_i C_i(s)k_{pwm}v_{bus}} i_{ref}, \quad (25)$$

where i_g is directly dependent on i_{ref}.

$$i_g(s) = H(s)i_{ref}(s). \quad (26)$$

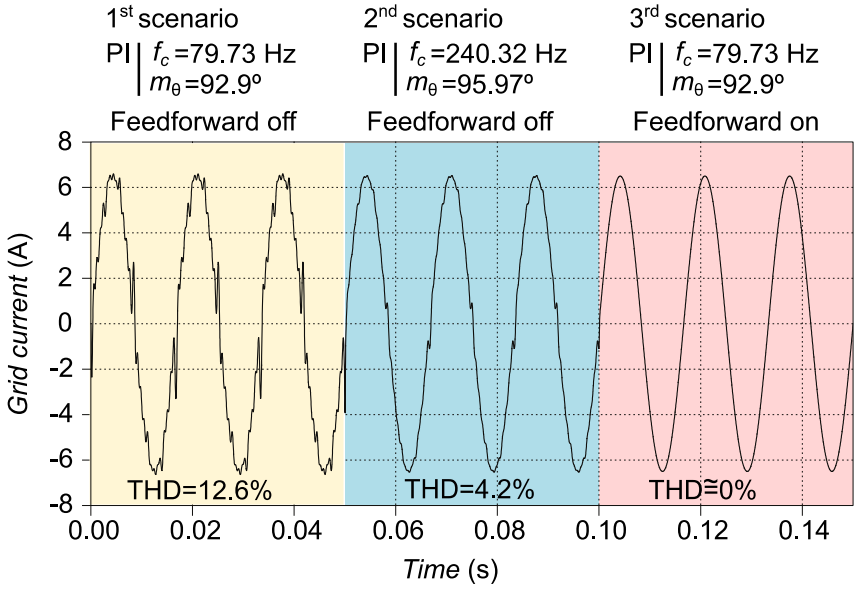
In scenarios where a feedforward controller is absent, the control effort is completely imposed by the PI controller, as previously discussed. This condition can even ensure the attenuation of the harmonic content of the grid current, however, it requires a PI controller with a large bandwidth. In simpler terms, the PI controller must guarantee that the periodic mean value of the voltage v_{ab} is an accurate reflection of the grid voltage. This approach allows producing a purely sinusoidal grid current, even without the use of a feedforward controller.

Conversely, the use of fast controllers in the current loop can lead to certain issues. These include the amplification of resonances, disturbances, and unwanted noises, which can potentially destabilize the system.

A simulation based on Figure 6, involving three distinct controllers, was conducted to demonstrate the behavior of a feedforward + PI controllers within the grid current control loop. These controllers are designed with varying phase margins and crossover frequencies, as depicted in Figure 22.

From the analysis of Figure 22, it is clear that the integration of the feedforward controller enables the PI controller to operate with a lower cut-off frequency. This setup provides the necessary bandwidth to amplify low-frequency components and ensures attenuation from the switching frequencies.

Figure 22 – Simulation results: THD from three types of control design.



Source: prepared by the authors.

It is worth mentioning that in both scenarios, with and without feedforward, i_{ref} still depends on the alternating components of v_{bus}. Therefore, to fully understand the behavior of the current i_g, it is necessary to obtain an equation to describe v_{ca}.

3.1 GRID VOLTAGE PERTURBATION

In the event of a DC bus oscillation, the first step is to determine its alternating parcel (v_{ca}). Therefore, it is considered in the mathematical analysis that the power

provided to the grid is the product between voltages and currents including the fundamental and harmonic components. In this initial analysis, only the third harmonic component will be accomplished to facilitate the identification of a pattern. After that, the equations will be extended to a generic model.

3.1.1 Grid power oscillation

The grid voltage, current and power considering only the third harmonic can be respectively represent as:

$$v_g = V_{p1}\sin(\omega t + \varphi_{v1}) + V_{p3}\sin(3\omega t + \varphi_{v3}), \tag{27}$$

$$i_g = I_{p1}\sin(\omega t + \varphi_{i1}) + I_{p3}\sin(3\omega t + \varphi_{i3}), \tag{28}$$

$$p_g = v_g i_g. \tag{29}$$

Expanding (29) from (27) and (28), leads to:

$$\begin{aligned} p_g = v_g i_g = {} & V_{p1}\, I_{p1}\sin(\omega t + \varphi_{v1})\sin(\omega t + \varphi_{i1}) + \\ & V_{p1}\, I_{p3}\sin(\omega t + \varphi_{v1})\sin(3\omega t + \varphi_{i3}) + \\ & V_{p3}\, I_{p1}\sin(3\omega t + \varphi_{v3})\sin(\omega t + \varphi_{i1}) + \\ & V_{p3}\, I_{p3}\sin(3\omega t + \varphi_{v3})\sin(3\omega t + \varphi_{i3}), \end{aligned} \tag{30}$$

in which V_{p1} and V_{p3} are the voltage amplitudes, φ_{v1} and φ_{v3} are the voltage initial phases, I_{p1} and I_{p3} are the current amplitudes, and φ_{i1} and φ_{i3} are the current initial phase of the fundamental and third harmonic components, respectively.

Each power term of (30) can be expanded and grouped accordingly with the harmonic order, resulting in:

$$\begin{aligned} p_g = P_{avg} + p_{2a}\cos(2\omega t) + p_{2b}\sin(2\omega t) + p_{4a}\cos(4\omega t) + \\ p_{4b}\sin(4\omega t) + p_{6a}\cos(6\omega t) + p_{6b}\sin(6\omega t), \end{aligned} \tag{31}$$

in which:

$$P_{avg} = \frac{V_{p1}I_{p1}}{2}(\cos\varphi_{v1}\cos\varphi_{i1} + \sin\varphi_{v1}\sin\varphi_{i1}) + \frac{V_{p3}I_{p3}}{2}(\cos\varphi_{v3}\cos\varphi_{i3} + \sin\varphi_{v3}\sin\varphi_{i3}), \quad (32)$$

$$p_{2a} = \frac{V_{p1}I_{p1}}{2}(-\cos\varphi_{v1}\cos\varphi_{i1} + \sin\varphi_{v1}\sin\varphi_{i1}) + \frac{V_{p1}I_{p3}}{2}(\cos\varphi_{v1}\cos\varphi_{i3} + \sin\varphi_{v1}\sin\varphi_{i3}) + \frac{V_{p3}I_{p1}}{2}(\cos\varphi_{v1}\cos\varphi_{i1} + \sin\varphi_{v3}\sin\varphi_{i1}), \quad (33)$$

$$p_{2b} = \frac{V_{p1}I_{p1}}{2}(\cos\varphi_{v1}\cos\varphi_{i1} + \sin\varphi_{v1}\sin\varphi_{i1}) - \frac{V_{p1}I_{p3}}{2}(\cos\varphi_{v1}\sin\varphi_{i3} - \sin\varphi_{v1}\cos\varphi_{i3}) + \frac{V_{p3}I_{p1}}{2}(\cos\varphi_{v3}\sin\varphi_{i1} - \sin\varphi_{v3}\cos\varphi_{i1}), \quad (34)$$

$$p_{4a} = \frac{V_{p1}I_{p3}}{2}(\sin\varphi_{v1}\sin\varphi_{i3} - \cos\varphi_{v1}\cos\varphi_{i3}) + \frac{V_{p3}I_{p1}}{2}(\sin\varphi_{v3}\sin\varphi_{i1} - \cos\varphi_{v3}\cos\varphi_{i1}), \quad (35)$$

$$p_{4b} = \frac{V_{p1}I_{p3}}{2}(\cos\varphi_{v1}\sin\varphi_{i3} + \sin\varphi_{v1}\cos\varphi_{i3}) + \frac{V_{p3}I_{p1}}{2}(\cos\varphi_{v3}\sin\varphi_{i1} + \sin\varphi_{v3}\cos\varphi_{i1}), \quad (36)$$

$$p_{6a} = \frac{V_{p3}I_{p3}}{2}(\sin\varphi_{v3}\sin\varphi_{i3} - \cos\varphi_{v3}\cos\varphi_{i3}), \quad (37)$$

$$p_{6b} = \frac{V_{p1}I_{p1}}{2}(\cos\varphi_{v1}\sin\varphi_{i1} + \sin\varphi_{v1}\cos\varphi_{i1}). \quad (38)$$

By grouping the harmonic terms in (31)-(38), it becomes possible to write:

$$p_g = P_{avg} + p_2\sin(2\omega t + \varphi_2) + p_4\sin(4\omega t + \varphi_4) + p_6\sin(6\omega t + \varphi_6) \quad (39)$$

As can be observed, the frequencies of the power components are determined by the sum and subtraction of the frequencies of the voltage and current components that are multiplied. In other words, the product between voltage and current components of the same frequency generates an average power component, since

$\omega t - \omega t = 0$ and $3\omega t - 3\omega t = 0$, and an oscillatory component, considering that $\omega t + \omega t = 2\omega t$ and $3\omega t + 3\omega t = 6\omega t$. Additionally, the product of voltages and currents with different frequencies generates only oscillatory components, with a null average value, since $3\omega t - \omega t = 2\omega t$ and $3\omega t + \omega t = 4\omega t$.

Therefore, it is possible to generalize an equation to describe the output power to accomplish all harmonic content:

$$p_g = P_{avg} + \sum_{n=1}^{\infty} p_n \sin(n\omega t + \varphi_n), \tag{40}$$

in which p_n and φ_n represent the amplitude and phase of the n^{th} harmonic component of the grid power:

$$p_n = sign(p_{nb})\sqrt{p_{na}^2 + p_{nb}^2} \tag{41}$$

$$\varphi_n = \tan^{-1}\left(\frac{p_{na}}{p_{nb}}\right) \tag{42}$$

3.1.2 DC bus power oscillation

The inverter input power can be obtained by the analysis of the power processed by C_{bus}, which, according with Figure 6, is given by:

$$p_{bus} = \left(I_{dc} + C_{bus}\frac{dv_{bus}}{dt}\right)v_{bus} \tag{43}$$

Replacing (13) into (43), yields to:

$$p_{bus} = \left(I_{dc} + C_{bus}\frac{dv_{ac}}{dt}\right)(V_{dc} + v_{ac}) \tag{44}$$

For properly designed inverters, the DC-bus voltage ripple tends to be much less than its average value, i.e., $V_{dc} >> v_{ac}$. In this context, it is possible to assume that:

$$C_{bus}\frac{dv_{ac}}{dt}v_{ac} \approx 0 \tag{45}$$

and thus:

$$p_{bus} = V_{dc}I_{dc} + v_{ac}I_{dc} + V_{dc}C_{bus}\frac{dv_{ac}}{dt} \tag{46}$$

3.1.3 Conservation of Power

Assuming that the inverter is ideal, that is, it operates without losses, it is possible to write that:

$$p_{bus} = p_g \tag{47}$$

By separating equations (40) and (46) into their respective continuous and alternating parts, and promoting the equality between these equivalent parts, it is possible to write:

$$V_{dc}I_{dc} = P_{avg}, \tag{48}$$

$$v_{ac}I_{dc} + V_{dc}C_{bus}\frac{dv_{ac}}{dt} = \sum_{n=1}^{\infty} p_n \sin(n\omega t + \varphi_n). \tag{49}$$

Since equation (49) is linear, the superposition theorem can be applied:

$$\frac{d}{dt}v_{ac1} + \frac{I_{dc}}{V_{dc}C_{bus}}v_{ac1} = \frac{p_1}{V_{dc}C_{bus}}\sin(\omega t + \varphi_1), \tag{50}$$

$$\frac{d}{dt}v_{ac2} + \frac{I_{dc}}{V_{dc}C_{bus}}v_{ac2} = \frac{p_2}{V_{dc}C_{bus}}\sin(2\omega t + \varphi_2), \tag{51}$$

and so on.

As can be observed in (50) and (51), the ordinary differential equations (ODEs) resulting from the superposition assume a pattern that will even be extended to cases

that include other voltage and current harmonics. Thus, given the pattern, a generic ODE can be formulated:

$$\frac{d}{dt}v_{acn} + \frac{I_{dc}}{V_{dc}C_{bus}}v_{acn} = \frac{p_n}{V_{dc}C_{bus}}\sin(n\omega t + \varphi_n) \tag{52}$$

in which v_{acn} represents n^{th} harmonic component of v_{ac}.

Knowing that the THD is a quantity measured in steady state, only the part of (52) that describes its behavior also in steady state is relevant to the following analyses. Therefore, given the composition of the ODE, it is assumed that the particular response should assume the following format:

$$v_{can} = A_n \sin(n\omega t + \theta_n). \tag{53}$$

By deriving (53) with respect to time and substituting the found result, together with (53), into (52), it is obtained:

$$\frac{p_n}{V_{dc}C_{bus}}\sin(n\omega t + \varphi_n) = n\omega A_n \cos(n\omega t + \theta_n) + \frac{I_{cc}}{V_{dc}C_{bus}}A_n \sin(n\omega t + \theta_n)\,. \tag{54}$$

Using trigonometric relations and grouping the sine and cosine terms together, results in:

$$\begin{gathered}\frac{p_n \cos\varphi_n}{V_{dc}C_{bus}}\sin(n\omega t) + \frac{p_n \sin\varphi_n}{V_{dc}C_{bus}}\cos(n\omega t) = \\ \begin{bmatrix} \frac{I_{dc}A_n \cos\theta_n}{V_{dc}C_{bus}} \\ -n\omega A_n \sin\theta_n \end{bmatrix}\sin(n\omega t) + \begin{bmatrix} \frac{I_{dc}A_n \sin\theta_n}{V_{dc}C_{bus}} \\ +n\omega A_n \cos\theta_n \end{bmatrix}\cos(n\omega t)\end{gathered} \tag{55}$$

Separating (55) in two equations, described in terms of the sine and cosine parcels, given that:

$$\begin{cases} \frac{I_{dc}A_n \cos\theta_n}{V_{dc}C_{bus}} - n\omega A_n \sin\theta_n = \frac{p_n \cos\varphi_n}{V_{dc}C_{bus}} \\ \frac{I_{dc}A_n \sin\theta_n}{V_{dc}C_{bus}} + n\omega A_n \cos\theta_n = \frac{p_n \sin\varphi_n}{V_{dc}C_{bus}} \end{cases} \quad (56)$$

By defining:

$$A_{nx} = A_n \cos\theta_n \quad (57)$$

$$A_{ny} = A_n \sin\theta_n \quad (58)$$

the solution of equations in (56) may be written as:

$$A_{nx} = p_n \frac{I_{dc}\cos\varphi_n + V_{dc}n\omega C_{bus}\sin\varphi_n}{{I_{dc}}^2 + (V_{dc}n\omega C_{bus})^2}, \quad (59)$$

$$A_{ny} = p_n \frac{I_{dc}\sin\varphi_n + V_{dc}n\omega C_{bus}\cos\varphi_n}{{I_{dc}}^2 + (V_{dc}n\omega C_{bus})^2}. \quad (60)$$

Defining A_{nx} and A_{ny} as the real and imaginary parts of a complex number, respectively, it is possible to express it in polar coordinates, as an angle θ_n and a module A_n. *Firstly,* θ_n can be calculated as:

$$\theta_n = \tan^{-1}\left(\frac{A_{ny}}{A_{nx}}\right). \quad (61)$$

Replacing (59) and (60) into (61) yields to:

$$\theta_n = \tan^{-1}\left(\frac{I_{dc}\sin\varphi_n + V_{dc}n\omega C_{bus}\cos\varphi_n}{I_{dc}\cos\varphi_n + V_{dc}n\omega C_{bus}\sin\varphi_n}\right) \quad (62)$$

Similarly, the sum of (57) and (58) makes possible to isolate A_n:

$$A_n = \frac{A_{nx} + A_{ny}}{\sin\varphi_n + \cos\varphi_n} \quad (63)$$

Therefore, substituting (59) and (60) into (63) results in:

$$A_n = p_n \frac{\frac{\sin\varphi_n + \cos\varphi_n}{\sin\theta_n + \cos\theta_n} I_{dc} + \frac{\sin\varphi_n - \cos\varphi_n}{\sin\theta_n + \cos\theta_n} V_{dc} n\omega C_{bus}}{{I_{dc}}^2 + (V_{dc} n\omega C_{bus})^2} \tag{64}$$

With the terms A_n and θ_n, it is possible to accurately describe the bus voltage oscillation v_{ca} according to:

$$v_{ca} = \sum_{n=1}^{\infty} [A_n \sin(n\omega t + \theta_n)], \tag{65}$$

Replacing equations (62) and (64) into equation (65):

$$v_{ca} = \sum_{n=1}^{\infty} p_n \frac{\frac{\sin\varphi_n + \cos\varphi_n}{\sin\theta_n + \cos\theta_n} I_{dc} + \frac{\sin\varphi_n - \cos\varphi_n}{\sin\theta_n + \cos\theta_n} V_{dc} n\omega C_{bus}}{{I_{dc}}^2 + (V_{dc} n\omega C_{bus})^2} \times \sin\left(n\omega t + \tan^{-1}\left(\frac{I_{dc}\sin\varphi_n + V_{dc} n\omega C_{bus}\cos\varphi_n}{I_{dc}\cos\varphi_n + V_{dc} n\omega C_{bus}\sin\varphi_n}\right)\right) \tag{66}$$

It can be observed that equation (66) yields a considerably extensive equation. However, it is important to note that the term I_{dc} will always be much smaller than $V_{dc} n\omega C_{bus}$. This observation holds true as both C_{bus} and I_{dc} are proportional to grid power, implying that they increase or decrease as a function of P_o. In other words, if the converter is design to deal with higher power while maintaining the same bus voltage, the DC current I_{dc} will increase, but, concurrently, it will be necessary to adjust the C_{bus} capacitor to maintain the voltage ripple within acceptable limits. This adjustment is crucial to prevent potential issues such as overmodulation and reverse current flow.

Given these considerations, equation (66) can be reformulated as follow:

$$v_{ca} = \sum_{n=1}^{\infty} p_n \frac{\frac{\sin\varphi_n - \cos\varphi_n}{\sin\theta_n + \cos\theta_n}}{V_{dc} n\omega C_{bus}} \sin\left[n\omega t + \tan^{-1}\left(\frac{\cos\varphi_n}{\sin\varphi_n}\right)\right] \tag{67}$$

Replacing (67) into (13), the bus voltage is obtained:

$$v_{bus} = V_{dc} + \sum_{n=1}^{\infty} p_n \frac{\frac{\sin\varphi_n - \cos\varphi_n}{\sin\theta_n + \cos\theta_n}}{V_{dc} n\omega C_{bus}} \sin\left[n\omega t + \tan^{-1}\left(\frac{\cos\varphi_n}{\sin\varphi_n}\right)\right] \tag{68}$$

3.1.4 v_{bus} validations and discussions

To validate the equation for v_{bus}, a simulation is performed to determine the magnitude and angle of the grid current i_g via Fourier transform. This is done for a bus capacitance (C_{bus}) with values of 100 µF and 250 µF. Subsequently, the current data is used as an input parameter to derive the v_{bus} waveform through equation (67). This step is crucial as the oscillation patterns of v_{bus} are dependent on the harmonics of the grid current. The simulation parameters used to validate v_{ca} are presented in Table 1.

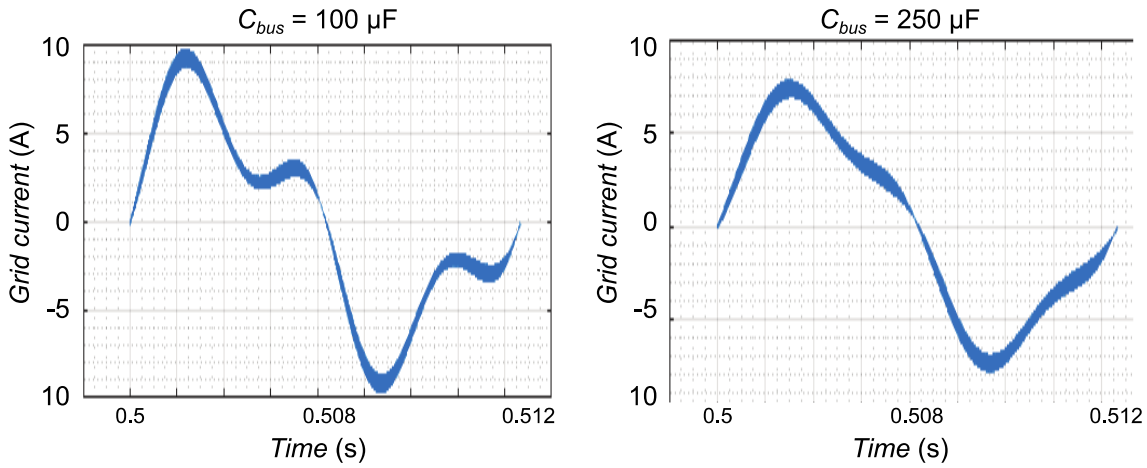
In this validation, the grid voltage is assumed to have the fundamental and a third harmonic components. The current shape considered in both scenarios (C_{bus} = 100µF and C_{bus} = 250 µF) is depicted in Figure 23. The harmonic spectrum values of the grid current for both scenarios, are presented in Table 2

Table 1 – Simulation parameters used for validation of v_{ca}.

Parameters	Variable	Values
Average ouput power	P_o	500 W
Grid voltage frequency	f_g	60 Hz
Bus capacitance	C_{bus}	250 µF / 100 µF
Bus voltage reference	V_{bus}	200 V
Grid current sensor gain	k_i	1
Grid voltage sensor gain	k_g	1
Bus voltage sensor gain	k_v	1/200
Current controller proportional gain	k_{pi}	0.034
Current controller integral gain	k_{ii}	123.63
Voltage controller proportional gain	k_{pv}	11.0
Voltage controller integral gain	k_{iv}	846.15
PWM triangular voltage peak	V_Δ	1 V
Feed-forward gain	k_{ff}	$1/v_g$
Stop-band filter	*SBF*	off
Inductors	L_f	2 mH
Fundamental grid voltage peak	V_{p1}	155 V
Fundamental grid voltage phase	φ_{v1}	0º
Third harmonic grid voltage peak	V_{p3}	25.45 V
Third harmonic grid voltage phase	φ_{v3}	30º

Source: prepared by the author.

Figure 23 – Current i_g (for C_{bus} = 100μF and C_{bus} = 250 μF) used for validation of v_{ca}.



Source: prepared by the author.

Table 2 – Specification of the grid voltage and current used for validation of v_{bus}.

Parameters	Variable	Values
Cbus = 100 μF		
Fundamental grid current peak	I_{p1}	6.59 A
Fundamental grid current phase	φ_{i1}	21.65º
Third harmonic grid current peak	I_{p3}	3.11 A
Third harmonic grid current phase	φ_{i3}	-23.98º
Cbus = 250 μF		
Fundamental grid current peak	I_{p1}	6.60 A
Fundamental grid current phase	φ_{i1}	14.40º
Third harmonic grid current peak	I_{p3}	1.79 A
Third harmonic grid current phase	φ_{i3}	-53.57º

Source: prepared by the authors.

In the simulation, a comparison was conducted between the waveform produced by the equation and simulations carried out with bus capacitances of 100μF and 250 μF, as illustrated in Figure 24. Under these conditions, it can be inferred that an increase in capacitance results in a decrease in voltage ripple on the C_{bus}, which is expected.

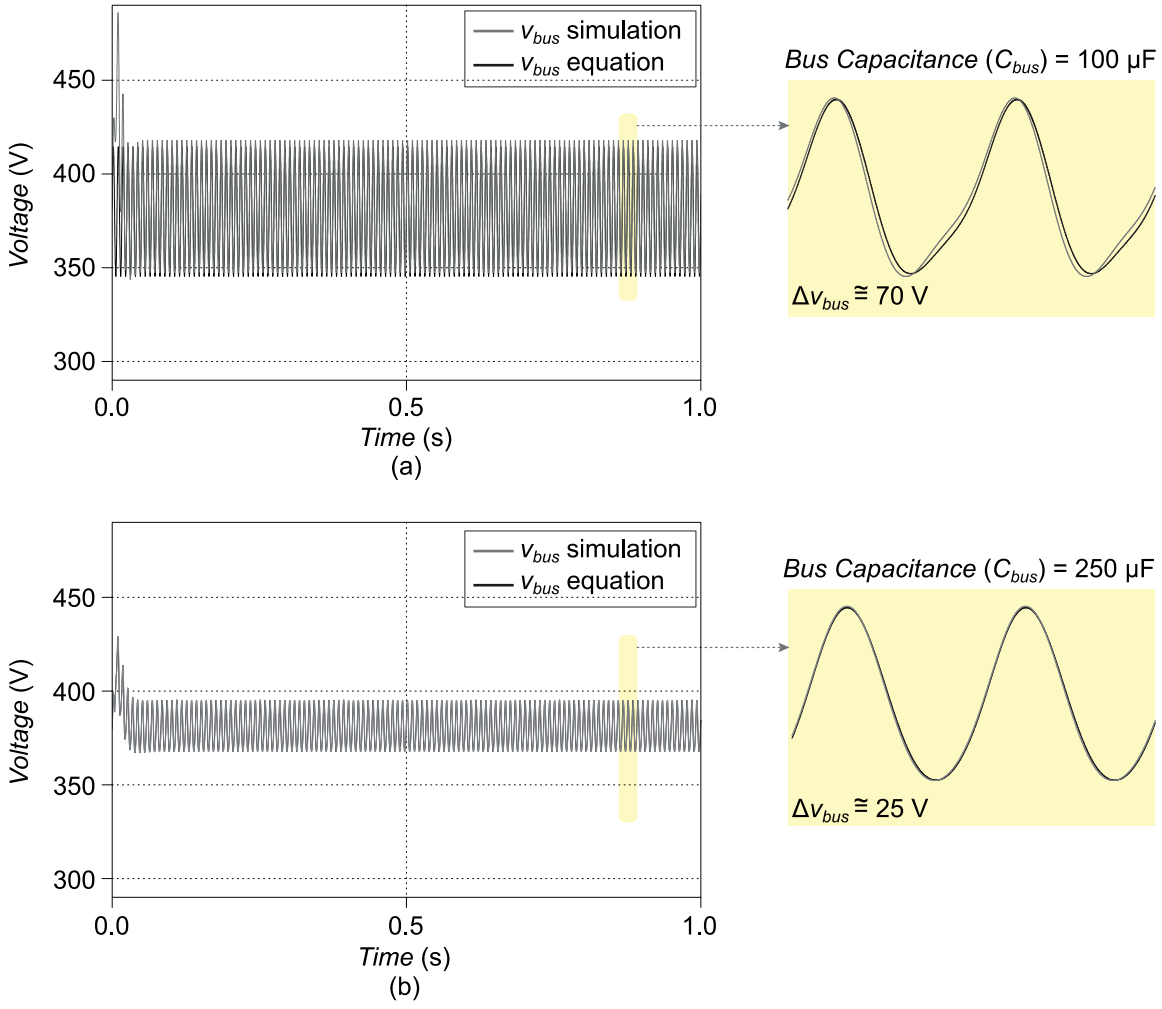
However, a small discrepancy can be observed between the simulated model and the calculated model in Figure 24 (a). This discrepancy arises because the

modeling was carried out considering that V_{cc}>>v_{ca}, nevertheless for C_{bus} = 100μF, the voltage ripple becomes slightly significant. The increase in voltage ripple imposes operational constraints on the model, as the only way to satisfy the condition V_{cc}>>v_{ca} is to reduce the voltage bus ripple Δv_{bus} by increasing C_{bus}. This behavior, which is not accounted for in the model, directly impacts the quality of the grid current.

Moreover, it can be inferred that the higher frequency components of v_{ca}, originating from grid power oscillation, are significantly filtered by the bus capacitor. As illustrated in Figure 25 (a), the most challenging frequencies to filter are those of lower frequency. The voltage ripple in the DC bus (Δv_{bus}) is depicted in Figure 25 (b).

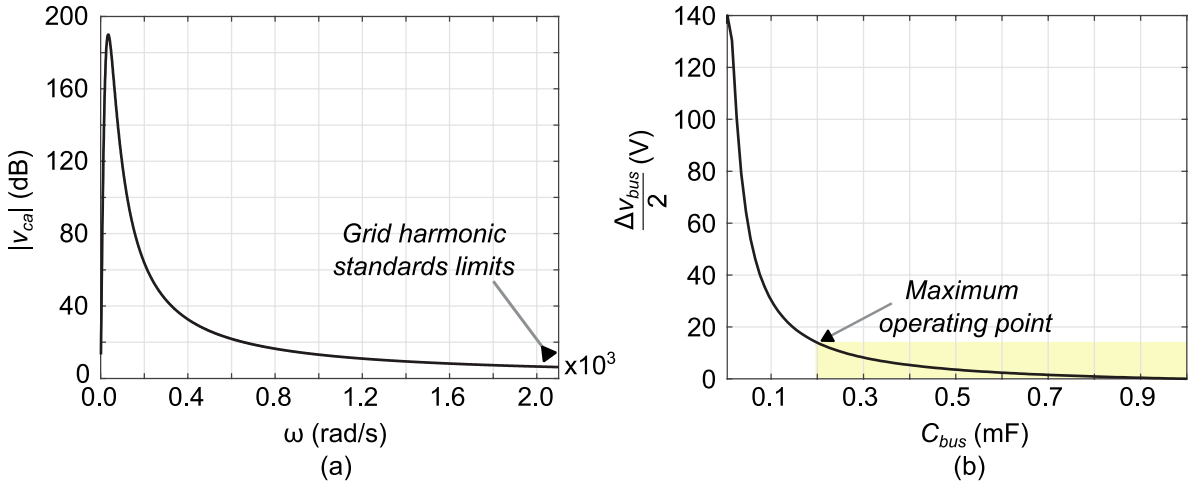
To meet the condition V_{cc}>>v_{ca}, the capacitance should be selected in the area highlighted in Figure 25 (b). Under this condition, equation (67) can be assumed to accurately represent the DC bus voltage.

Figure 24 – Validation of the equation for v_{ca}: comparison between the (67) and the simulation results.



Source: prepared by the authors.

Figure 25 - (a) Magnitude of v_{ca} by ω variation. (b) Voltage ripple amplitude by bus capacitance.



Source: prepared by the authors.

3.2 DISTURBANCE EFFECTS ON CURRENT REFERENCE (I_{REF})

Once the voltage v_{ac} is obtained, it is possible to verify its effects on the reference current i_{ref} which directly affects the grid current i_g.

Firstly, by substituting (67) into (16) and manipulating the result to express it in terms of magnitude and phase, the following equations are obtained:

$$k_{ac} = -v_{ac} k_v BSF(s) C_v(s) \tag{69}$$

$$k_{ac} = -k_v C_v(s) BSF(s) \sum_{n=1}^{\infty} [A_n \sin(n\omega t + \theta_n)] \tag{70}$$

$$k_{ac} = -k_v BSF(s) \sum_{n=1}^{\infty} |C_v(n\omega)| A_n \sin[n\omega t + \theta_n + \angle C_v(n\omega)], \tag{71}$$

$$k_{ac} = -k_v \sum_{n=1}^{\infty} |BSF(n\omega)||C_v(n\omega)| A_n \sin[n\omega t + \theta_n + \angle BSF(n\omega) + \angle C_v(n\omega)] \tag{72}$$

Now, substituting (72) into (17), where $k_{pll} v_g$ is equal to a perfect sine wave with amplitude and frequency corresponding to the fundamental frequency of the electrical grid ($V_{p1} \sin(\omega t)$), it is possible to obtain:

$$i_{ref} = \left(V_{ref} - V_{cc}k_v SBF(s)\right) C_v(s) k_g V_{p1} \sin(\omega t) - k_v k_g V_{p1} \sin(\omega t) \sum_{n=1}^{\infty} |BSF(n\omega) C_v(n\omega)| A_n \sin[n\omega t + \theta_n + \angle BSF(n\omega) + \angle C_v(n\omega)] \quad (73)$$

Considering that in steady state the voltage loop controller ensures zero error in tracking the voltage reference V_{ref}, such that the input power equals the output power, it becomes plausible to assume that the part of (49) at the fundamental frequency is rewritten as $\frac{2P_g}{V_{p1}}\sin(\omega t)$. Thus:

$$i_{ref} = \frac{2P_g}{V_{p1}} \sin(\omega t) - k_v \frac{2P_g}{V_{p1}} \sin(\omega t) \sum_{n=1}^{\infty} |BSF(n\omega) C_v(n\omega)| A_n \sin[n\omega t + \theta_n + \angle BSF(n\omega) + \angle C_v(n\omega)] \quad (74)$$

As can be seen in (74), the presence of an oscillation in the bus voltage imposes harmonic disturbances on the current reference, which can be literally described by:

$$i_{ref_{dist}} = k_v \frac{2P_g}{V_{p1}} \sin(\omega t) \sum_{n=1}^{\infty} Y_n \sin(n\omega t + \alpha_n) \quad (75)$$

where:

$$Y_n = A_n |SBF(n\omega) C_v(n\omega)| \quad (76)$$

$$\alpha_n = \theta_n + \angle SBF(n\omega) + \angle C_v(n\omega). \quad (77)$$

Applying trigonometric identities:

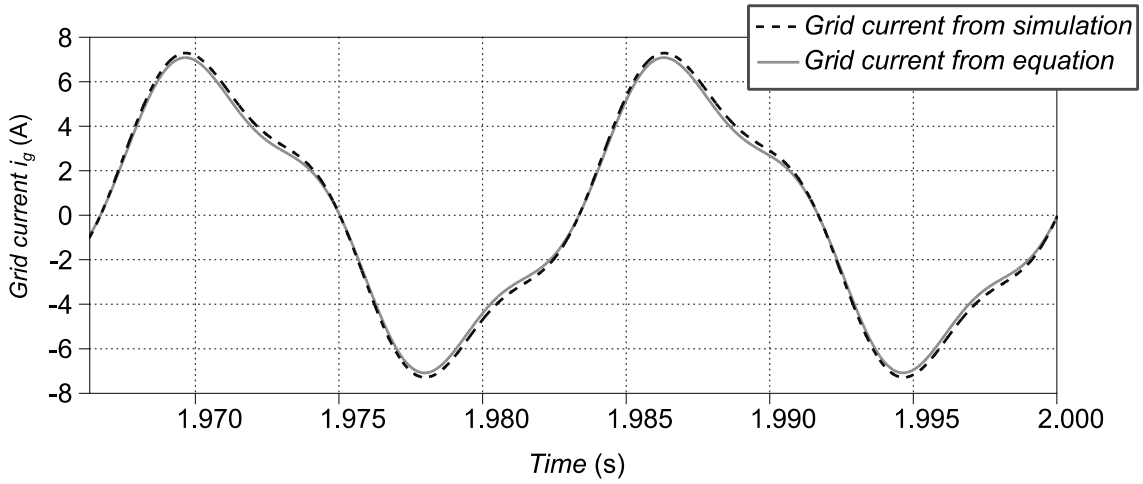
$$i_{ref_{dist}} = k_v \frac{2P_g}{V_{p1}} \sum_{n=1}^{\infty} \frac{Y_n}{2} \{\cos[(n-1)\omega t + \alpha_n] - \cos[(n+1)\omega t + \alpha_n]\} \quad (78)$$

Finally, it is possible to use an equation to describe grid current, in closed loop, considering the grid voltage and the DC-bus voltage as perturbations.

$$i_g = \frac{C_i(s)k_{pwm}v_{bus}}{sL_f + C_i(s)k_{pwm}v_{bus}}\left[\frac{2P_g}{V_p}\sin(\omega t) + k_v\frac{2P_g}{V_{p1}}\sum_{n=1}^{\infty}\frac{Y_n}{2}\begin{Bmatrix}cos[(n-1)\omega t + \alpha_n] \\ -cos[(n+1)\omega t + \alpha_n]\end{Bmatrix}\right] \quad (79)$$

Considering the same scenario proposed for the validation of v_{ca}, with C_{bus} = 250 µF, a simulation is conducted to compare the simulated current with that calculated by equation (79). The result is depicted in Figure 26

Figure 26 – Grid current (i_g) validation by simulation.



Source: prepared by the authors.

As illustrated in Figure 26, even when a small bus capacitance is employed, Equation (79) accurately mirrors the simulated waveform. This successful comparison highlights the equation as a new tool that can be applied in the design of converters aiming at the reduction of Total Harmonic Distortion (THD).

4 RESULTS

In this section, it is presented the experimental results. The tests were conducted in a manner that maximizes coherence with the theoretical approach and the comparison between these results and the described mathematical model is also presented, aiming to validate the developed models, in special the equation (79).

A VSI prototype based on the dual-buck topology, considering all the stages of closed-loop energy processing described in Section 2 was designed, built, and tested to validate the proposed mathematical models. The design parameters chosen for validations are switching frequency f_s = 20 kHz, DC-bus voltage reference V_{bus_ref} = 200 V, L_1 and L_2 =1 mH, C_1 and C_2 = 0.68 µF, R_d = 30 Ω. The controllers, both of the PI type, were adjusted as follows: voltage controller with a cut-off frequency of 6 Hz and a phase margin of 60º, leading to a proportional gain k_{pv} = 0.051 and an integral gain k_{iv} = 1.12; current controller with a cut-off frequency of 800 Hz and a phase margin of 89º, leading to a proportional gain k_{pi} = 9.88 and an integral gain k_{ii} = 63.89. The stop-band filter added in the DC-bus voltage measurement was tuned at 120 Hz, to mitigate the voltage ripple at this frequency.

The root mean square (RMS) value of the grid voltage at the fundamental frequency (60 Hz) was defined as 110V, and the phasors that represents the voltages for the 3rd and 5th harmonic contents were considered as $18\text{V}\angle 30°$ and $8\text{V}\angle 15°$, respectively.

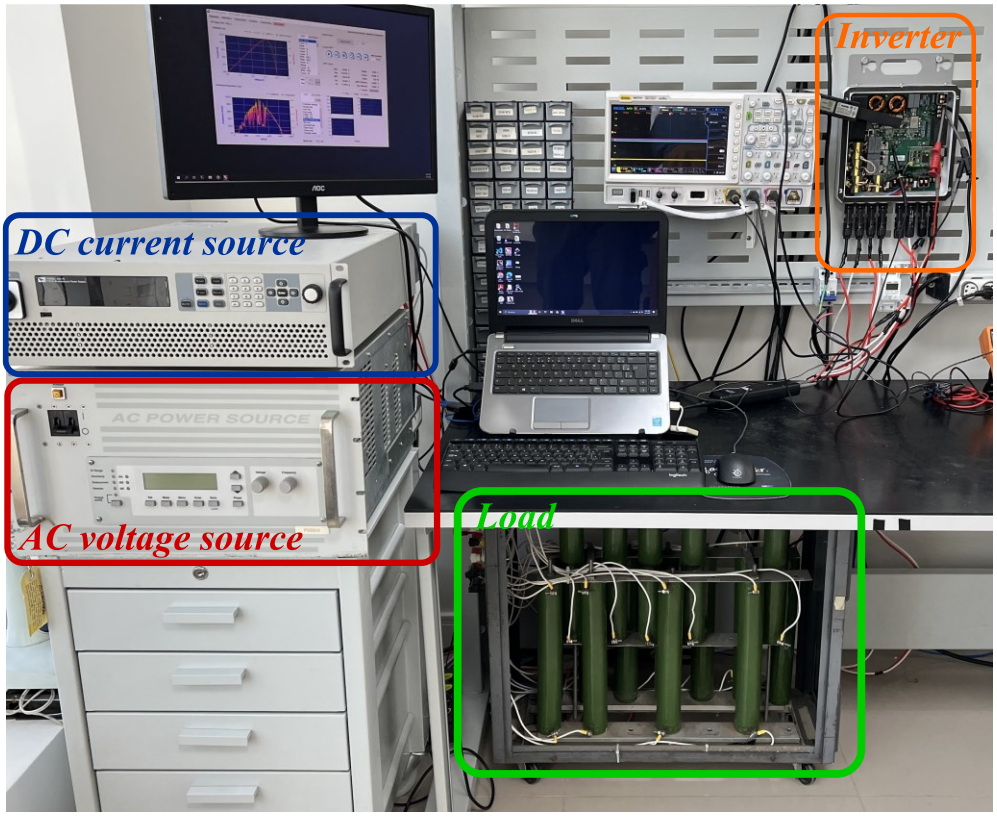
Among all the DC sources available for testing in the laboratory, the iTech IT6000C emerged as the one demonstrating the lowest output capacitance in the current mode. Consequently, in the subsequent validation scenarios, the capacitance will be confined to the value of the source's internal capacitance of 614 µF.

The prototype, with the aforementioned characteristics, used in the validation of this thesis, can be seen in Figure 27. Figure 28 illustrates the test setup used in the validation. The load is added to the test setup solely to enable bidirectionality, as the ac power supply employed in the tests operates exclusively within two quadrants. The probe used in the measurement of the grid current was the Tektronix TCP0030A.

Figure 27 – Prototype for validation of the concepts employed in this thesis.

Source: prepared by the authors.

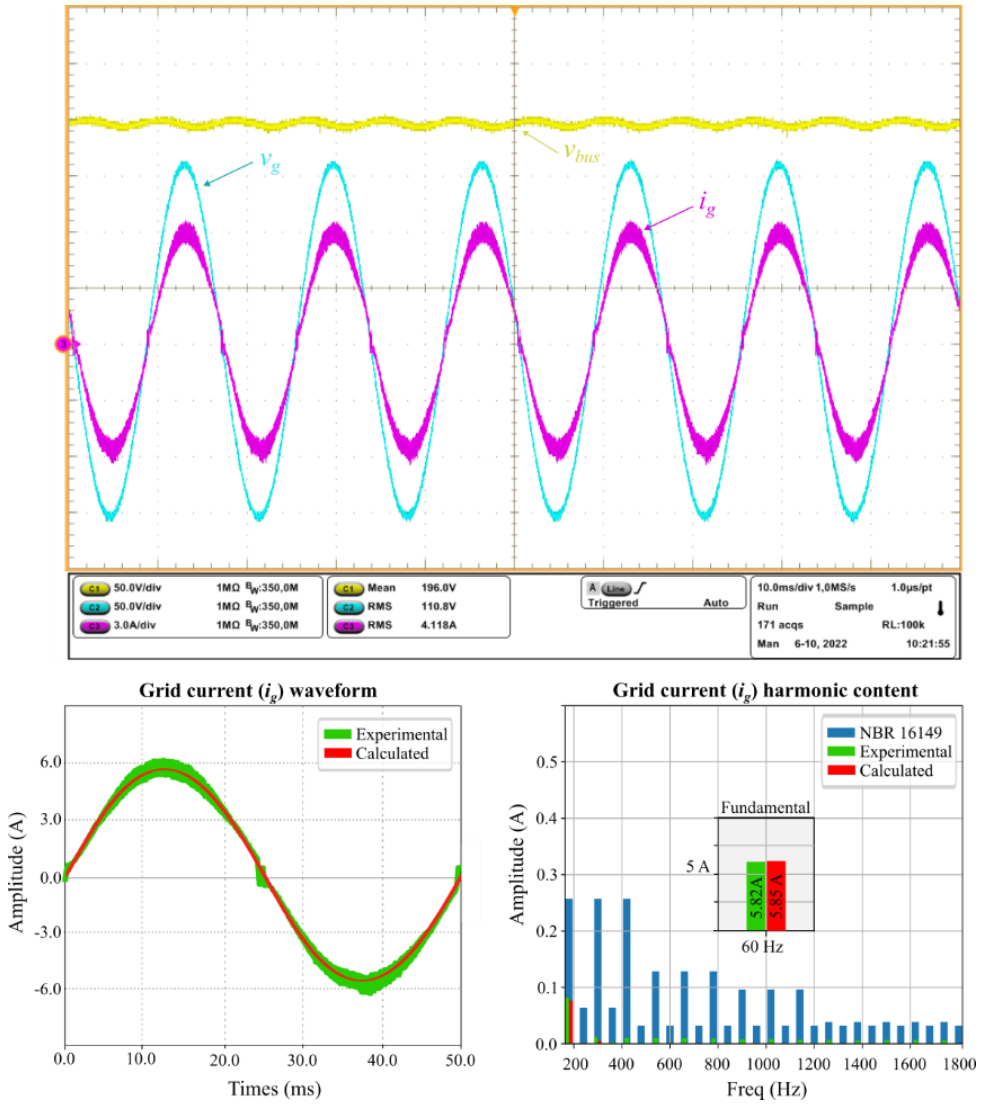
Figure 28 – Test setup for proposal validation.



Source: prepared by the authors.

To analyze the performance of the proposed method, the inverter output current is evaluated in five different scenarios. In the first scenario (Figure 29), the ac power source is adjusted to provide only the fundamental component of the grid voltage, representing the ideal scenario. The stop-band filter is tuned in 120 Hz and the feedforward gain is active. It's important to note that the validation of equation (79), in this work, will consider the analysis up to the 5th harmonic for achieving the THD_i. However, as we consider more harmonics, the equation becomes much more complex and extensive, complicating the analyses proposed in these validations.

Figure 29 – Results for the 500 W scenario with the grid voltage free of harmonics. Experimental waveforms (upper part); Grid current predicted by (79) in red against its experimental waveform (.csv) in green (lower left part); Harmonic content of the grid current (lower right part).



Source: prepared by the authors.

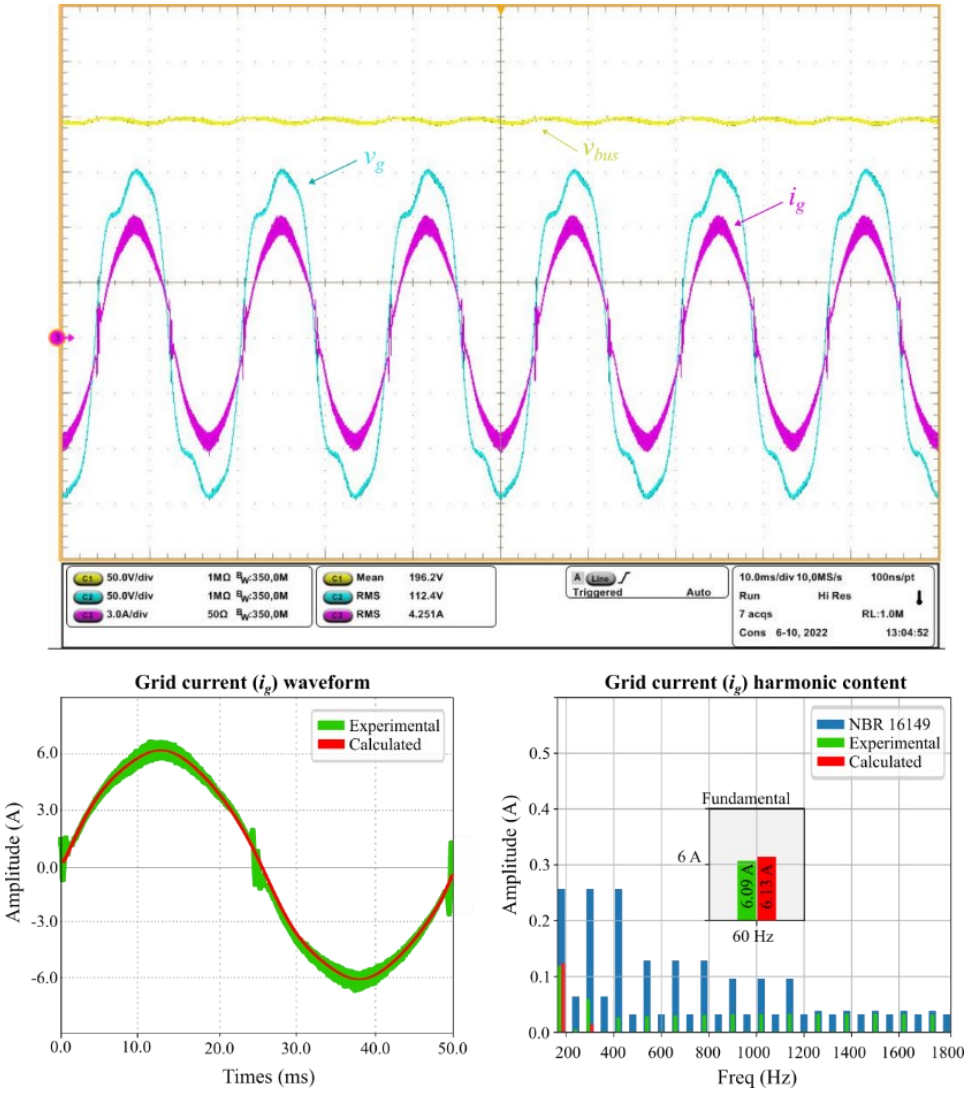
Figure 29 displays the DC-bus voltage in Channel 1 (C1), where the 120 Hz ripple can be observed. Channel 2 (C2) illustrates the grid voltage, and Channel 3 (C3) shows the grid current. At the bottom part of the figure, the overlap between the experimental waveform of the grid current (in .csv format) and its theoretical representation determined from equation (79) can be observed. Both have their harmonic content compared to the requirements of the Brazilian standard NBR16149.

In this first scenario, where the grid voltage is considered ideal, it is observed in the lower left frame that the low-frequency shape of the waveforms coincides. Similarly, in the lower right frame, the harmonic content calculated in the equation also matches the one measured in practice, pointing out the accuracy of the equation.

In the second scenario, the 3^{rd} and 5^{th} harmonics are added to the grid voltage. As expected, this grid voltage perturbation interferes within the closed-loop process, leading to an increase in the harmonic content of the grid current, as illustrated in Figure 30. This occurs because the system was designed to operate assuming an ideal grid, and since the controllers remain unchanged throughout the entire validation process, it is observed an increase in grid current harmonic content, since the initial design conditions were changed.

Even so, it is noticeable that the comparison of theoretical and practical waveforms coincides in the lower left frame, as well as the harmonic comparison in the lower right frame. This consistency validates the accuracy of the theoretical models when compared to practical measurements in this scenario.

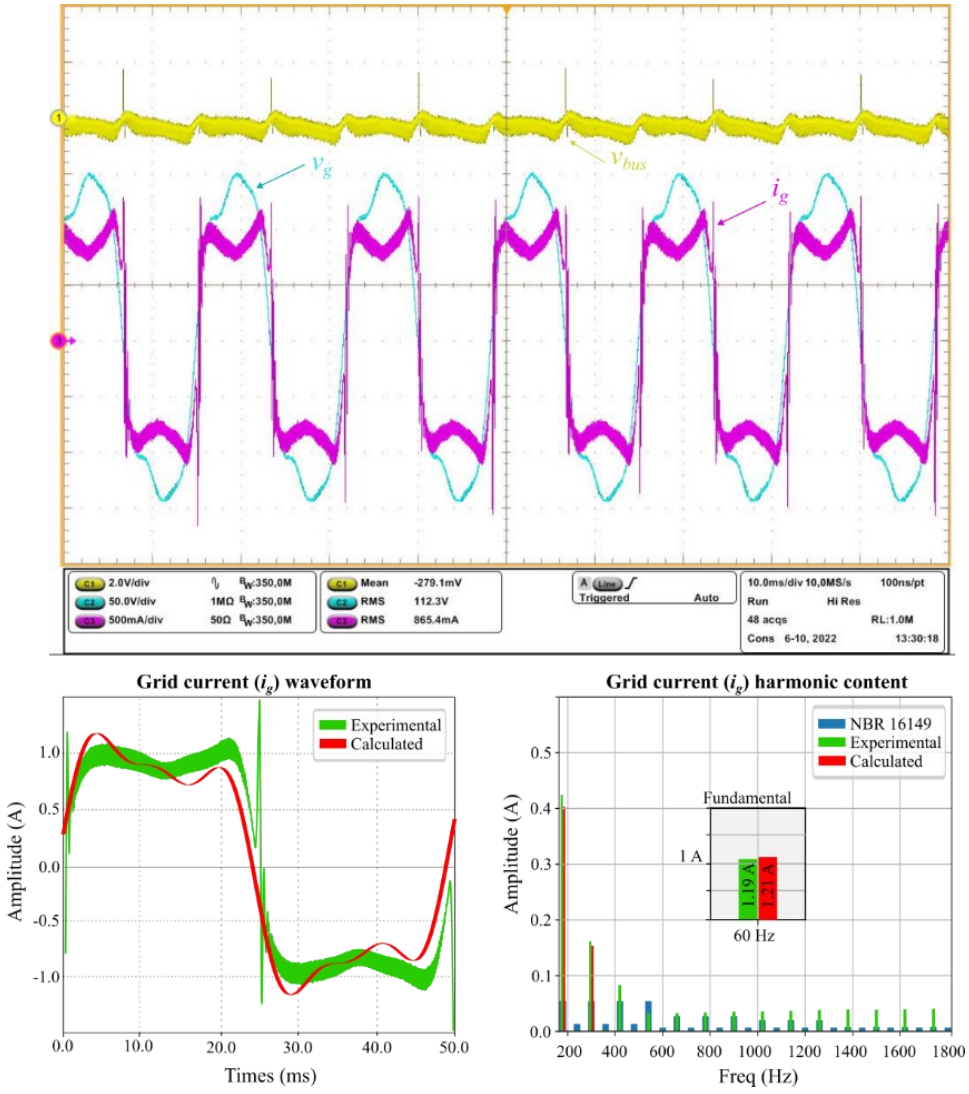
Figure 30 – Results for the 500 W scenario with 3rd and 5th harmonics in the grid voltage (upper part). Grid current predicted by (79) in red against its experimental waveform (.csv) in green (lower left part); Harmonic content of the grid current (lower right part).



Source: prepared by the authors.

In the third scenario, the level of power processed by the system was reduced to 20%, while maintaining the harmonics in the grid voltage. In light of Figure 31, a slight difference can be observed between the experimental and calculated waveforms. This deviation is caused because the waveform derived from the theoretical equation only considers the 3rd and 5th harmonic components, while the experimental waveform related to the grid current displays harmonic content at higher frequencies as well, resulting in a greater deformation for low power.

Figure 31 – Results for the 100 W scenario with 3rd and 5th harmonics in the grid voltage (upper part). Grid current predicted by (79) in red against its experimental waveform (.csv) in green (lower left part); Harmonic content of the grid current (lower right part).



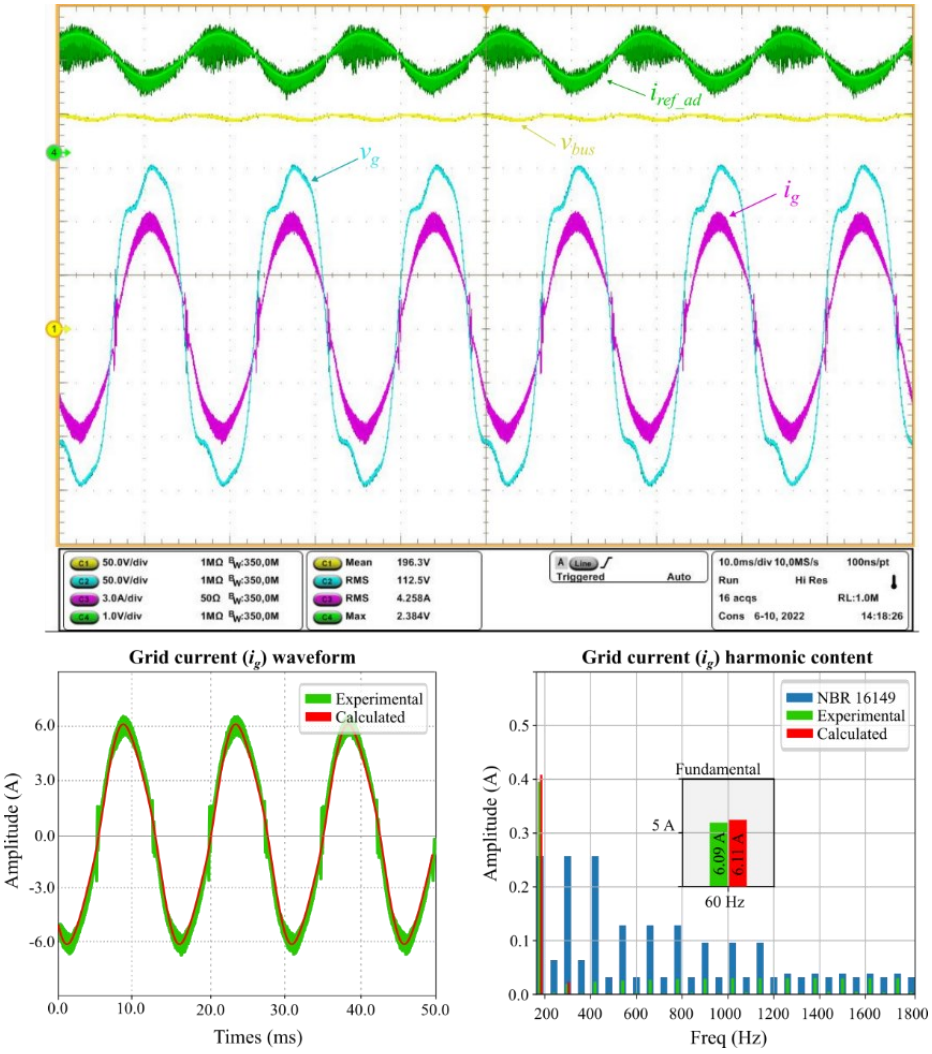
Source: prepared by the authors.

Thus, by increasing the number of harmonics considered in the equation, the result becomes more similar between the experimental and calculated waveforms. It should be emphasized again that by increasing the harmonic analysis, the equation becomes complex. Nevertheless, the equation has proven to be sufficiently adequate for estimating the THD, as indicated in Table 3

In Figure 32, the results of the fourth test scenario are observed. In this case, the harmonic contents of the grid voltage remain the same as in the previous test, while the power is restored to the initial value of 500 W, while the harmonic content in the grid voltage remain unaltered with the presence of the 3rd and 5th harmonic content.

Furthermore, a significant modification occurs in the control loop, as the stopband filter at 120 Hz has been removed.

Figure 32 – Results for the 500 W scenario with 3rd and 5th harmonics in the grid voltage without stop-band filter in the control loop (upper part). Grid current predicted by (79) in red against its experimental waveform (.csv) in green (lower left part); Harmonic content of the grid current (lower right part).



Source: prepared by the authors.

As can be seen in Figure 32, the waveform related to i_{ref} has been added in Channel 4 (C4). To achieve this, the variable was provided through a digital-to-analog converter on the microcontroller, allowing its capture with a voltage probe. The primary objective of displaying i_{ref} is to make the influence of the stop-band filter on the control loop visible. When the stop-band filter is removed, it can clearly be observed the presence of the 3rd harmonic content on i_{ref}. In this scenario, this phenomenon occurs

because the error of DC-bus voltage control loop exhibits significant oscillations at 120Hz, caused by the dc bus voltage ripple. Despite being designed to mitigate some of these oscillations, the voltage compensator is unable to completely eliminate them. As a result, the voltage controller's output still contains a 120Hz oscillation, which is further multiplied by the sinewave from the PLL. The product between these two signals not only generates components at 60Hz (120-60) but also produces components at 180Hz (120+60). The harmonic distortion in the reference signal is transferred to the grid current, which also starts to exhibit a non-negligible 180 Hz harmonic content.

Even in light of the above, the equation accurately represents the removal of the stop-band filter from the control loop.

In the last scenario, the harmonic conditions in the voltage grid and the processed power remain unchanged. However, the stop-band filter is reintroduced, while the feedforward compensator is removed from the circuit.

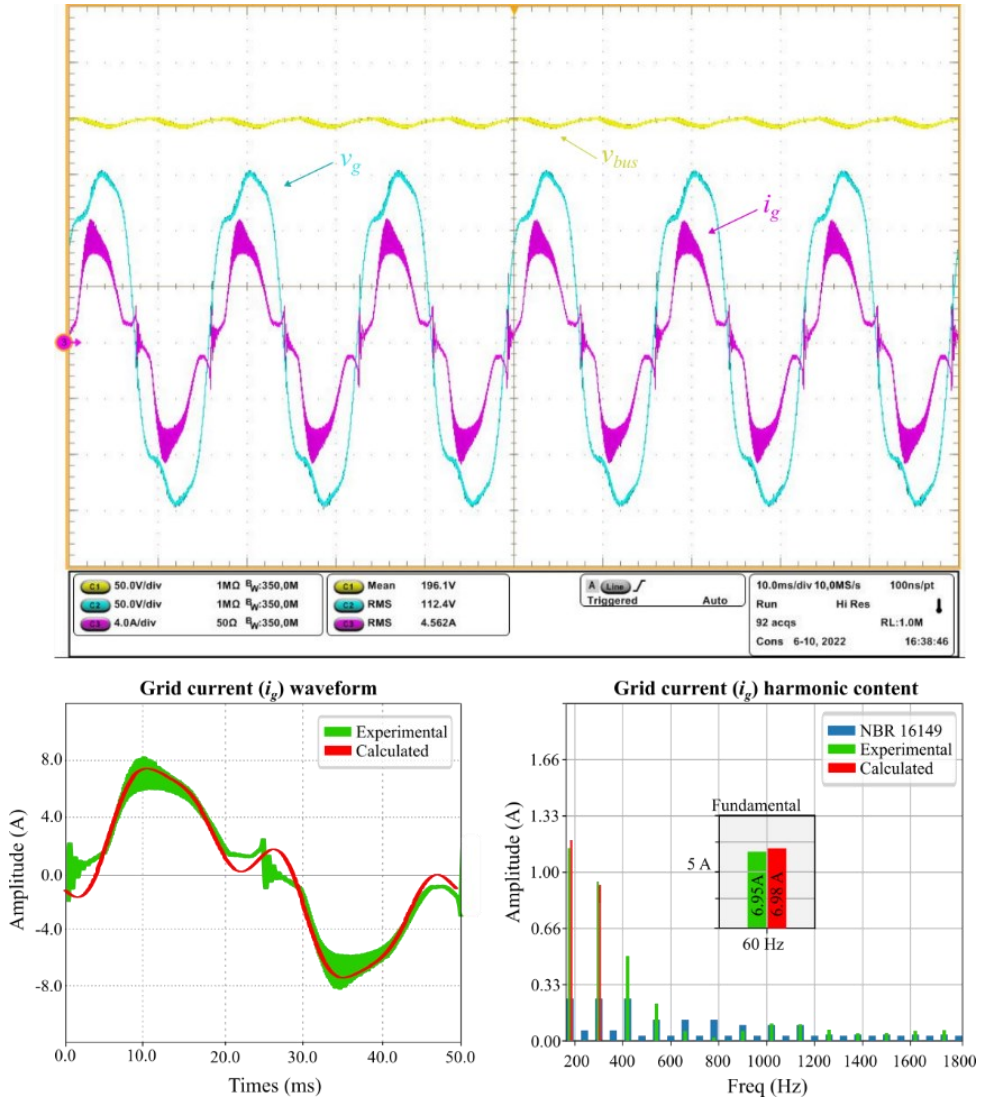
This change results in significant distortions in the grid current due to the direct influence of the grid voltage harmonic content. When canceling the feedforward gain, it is possible to rewrite i_g as follow:

$$i_g = \frac{C_i(s)k_{pwm}v_{bus}i_{ref}}{sL_f + k_iC_i(s)k_{pwm}v_{bus}} - \frac{v_g}{sL_f + k_iC_i(s)k_{pwm}v_{bus}}. \quad (80)$$

By incorporating the term dependent on the grid voltage in the equation that describes i_g, it becomes feasible to precisely reproduce the proposed harmonics, as demonstrated in Figure 33. This enhancement in the current equation allows for a more accurate representation of the harmonic content in this scenario, resulting in a closer alignment between the theoretical predictions and the experimental results.

It is always essential to emphasize that the emergence of harmonics in the current injected into the grid is not exclusively related to i_{ref} itself, which, in turn, remains free of harmonics in scenarios with the stop-band filter. The most significant impact is directly caused by the product between v_{bus} by i_{ref} in equation (80) and also in equation (79).

Figure 33 – Results for the 500 W scenario, 3rd and 5th harmonics in the grid voltage without the feedforward compensator in the control loop (upper part). Grid current predicted by (79) in red against its experimental waveform (.csv) in green (lower left part); Harmonic content of the grid current (lower right part).



Source: prepared by the authors.

To summarize the scenarios, comparing experimental and theoretical results, Table 3 is presented. This table provides a comprehensive overview of the system's performance under different conditions, allowing for a detailed analysis of the harmonic content and the effectiveness of the proposed equation. The THD calculation described in the Table 3 takes into account harmonics up to a frequency of 300 Hz, since the proposed equation, for validation, considers its formulation up to this frequency.

Table 3 - Grid current overall comparison between experimental and calculated results.

Scenario	**Fund. (A)**		**3rd Harmonic (A)**		**5th Harmonic (A)**		**THD (%)**		**Error in THD (%)**
	Exp.	*Calc.*	*Exp.*	*Calc.*	*Exp.*	*Calc.*	*Exp.*	*Calc.*	
P_o:500 W v_g: *Fund*.	5.83	5.85	0.08	0.07	$7.2e^{-3}$	$6.7e^{-4}$	1.41	1.30	7.91
P_o: 500 W v_g: *Fund*+3rd+5th	6.09	6.13	0.11	0.12	0.06	$7.1e^{-3}$	2.12	1.97	6.80
P_o: 100 W v_g: *Fund*+3rd+5th	1.19	1.21	0.43	0.40	0.16	0.15	38.3	35.5	7.01
P_o: 500 W v_g: *Fund*+3rd+5th *w/o SBF*(2π120)	6.09	6.11	0.39	0.41	0.03	0.02	6.52	6.76	3.64
P_o: 500W v_g: *Fund*+3rd+5th *w/o* k_{ff}	6.95	6.98	1.24	1.26	0.89	0.89	22.0	22.1	0.43

Source: prepared by the authors.

Upon analyzing Table I, it is observed that even the highest percentage errors are results of a slight difference between the absolute calculated and experimental values. In effective terms, the error in the estimation of THD remained below 8% in all evaluated scenarios, allowing for a satisfactory precision in converter projects based on the estimation of THD.

It is worth noting that the differences between theoretical and practical values arise due to the fact that the proposed model does not contemplate phenomena such as dead time of the switches, microcontroller sampling frequency, intrinsic parasitic elements to the components, and output filter voltage drop.

4.1 DISCUSSIONS

The experimental results presented in this chapter demonstrate that the proposed methodology, along with the equation, can effectively and satisfactorily reproduce the behavior of the grid. It is evident that disturbances in i_{ref} can be minimized with a well-designed PLL and the use of well-tuned filters to reduce the 120Hz ripple and its multiples. Furthermore, the use of large bus capacitors helps to minimize the direct impact of the bus voltage on the current injected into the electrical grid. Finally, disturbances in the grid voltage on the grid current can also be minimized using control methods parallel to the main loops, such as the feedforward compensator presented in this work. All these factors contribute to the quality of the grid current.

It should be noted that despite some percentage errors in Table 1 showing values of approximately 8%, this value is minimal when comparing the absolute value of the harmonics. In this scale, a minimal variation of approximately 0.1 between the absolute values of THD can result in elevated error percentages.

An Important point to be highlighted is that despite the recurrence of the proposed equation, it accurately represents the current injected into the grid. This fact points to the complexity of the study conducted and the validation of the equation in the proposed scenarios. Furthermore, the equation indicates to be a valuable tool when considering system optimization.

From an operating system, it is possible to apply the proposed methodology to predict scenarios where output filter optimization is possible. For example, controllers can be adjusted in advance, without the need for significant effort on the bench. With this in mind, an interesting application is to use the equation to apply optimization routines focused on various factors. In this thesis, we chose to focus on describing THD, but the methodology could be extended to reduce the bus capacitor, or to apply other types of controllers aiming to reduce CPU processing time.

Furthermore, by improving the proposed equation with dead time, parasites, and output filter voltage drop, it is even possible to create scenarios where the equation can be used to increase the converter’s efficiency. The great challenge lies in applying optimization methods capable of maximizing or minimizing the cost function, which would be the proposed equation, and stipulating the boundaries according to the designer’s needs.

5 CONCLUSIONS

This thesis has presented a methodology applied to the analysis of grid-connected inverters, which considers closed-loop modeling to determine an equation able of describing the current injected into the electrical grid, along with its harmonic content and associated THD. To achieve a precise equation, disturbances such as the harmonic components of the grid voltage and the dc bus voltage ripple were included in the analysis.

From the conduction of experiments, considering the operation of a dual-buck inverter in different scenarios, it was possible to verify that the obtained equation is suitable for predicting the THD of the current injected into the electrical grid, as evidenced by the results summarized in Table I. Furthermore, this equation can still be improved, including in the model the factors mentioned earlier (parasitic elements, dead time, sampling, and voltage drops). However, this would increase the degree of complexity of the equation.

The agreement between theoretical and experimental highlights the method’s efficacy and its practical applicability to optimize power quality. Nevertheless, the recurrence observed in the equation underscores the importance of pursuing advanced optimization techniques to enhance the controller's and passive filters effectiveness leading to best THD performances with high power density converters. The proper characterization and understanding of this harmonic distortion mechanism are crucial for effectively designing new control strategies. It is also important to note that the methodology proposed in this thesis can be extended to other systems, however, each with its peculiarities due to the control strategies adopted.

The insights gained from this study shed light on the trade-offs between complexity and accuracy when determining the current harmonic content from grid-tie inverters, enabling researchers and engineers to make informed decisions for optimizing converter performance and ensuring grid compliance as the demand for cleaner and more efficient energy solutions intensifies.

The methodology presented serves as an important starting point for the development of a powerful tool that allows for the optimization of such inverters, with the THD having a predefined design specification.

5.1 CONCLUSION SUMARY

To achieve these objectives, the thesis was structured into five parts. The first part consists of an introduction to the topic, highlighting the importance of energy quality. Subsequently, a literature review on the subject revealed the absence of studies proposing a methodology centered on energy quality.

Chapter 2 provides an overview of the main power structures and their respective control loops. Based on what was presented, the structure to be analyzed in the work is defined. Chapter 3 delves into mathematical analyses, proposing the use of a model to analyze the current injected in a closed loop. This chapter presents detailed analyses of the loop operation, as well as partial validations of the equations found through simulations.

With the aim of validating the proposed methodology in a real scenario, Chapter 4 presents experimental tests carried out on a prototype. These tests addressed five different scenarios, demonstrating the efficacy of the equation, regardless of the control strategy or parameters adopted. Finally, the conclusions report the findings of the work.

5.2 ACADEMIC CONTRIBUITION DURING THE DOCTORATE

5.2.1 Publications

Thesis subject:

- **V. F. Gruner**, C. F. Gonçalves, L. Schmitz, D. C. Martins, R. F. Coelho, “Metodologia para Estimação da Distorção Harmônica Total em Inversores Monofásicos Conectados à Rede Elétrica”, Revista Eletrônica de Potência, early access.
- Paper in the final stages of preparation for submission to IEEE Transactions on Circuit Theory

Other subjects:

- **V. F. Gruner**, J. W. Zanotti, W. M. Santos, T. A. Pereira, L. Schmitz, D. C. Martins, R. F. Coelho, “Modified Current Sensorless Incremental Conductance Algorithm for Photovoltaic Systems”, Energies, vol. 16, no. 2, pp. 1-10, 2023

- D. B. S. Oliveira, L. L. Glória, R. A. S. Kraemer, A. C. Silva, D. P. Dias, A. C. Oliveira, M. A. I. Martins, M. A. Ludwig, **V. F. Gruner**, L. Schmitz, R. F. Coelho, “Mixed-Integer Linear Programming Model to Assess Lithium-Ion Battery Degradation Cost”, Energies, vol. 15, no. 9, pp. 1-10, 2022.
- **V. F. Gruner**, T. P. Horn, L. Schmitz, D. Martins, R. F. Coelho, “Forward-Based High Step-Up DC–DC Converter with Input Current Sharing and Output Filter Reduction: Design, Modeling, and Control”, Journal of Control, Automation and Electrical Systems, vol. 31, no. 9, pp. 21-30, 2020.
- L. Munaretto, V. S. Zeni, H. Chaves, N. C. dal Pont, **V. F. Gruner** and R. A. S. Kraemer, "Smart Hybrid Inverter: A Practical Guide," 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Dubrovnik, Croatia, pp. 35-40, 2020
- V. S. Zeni, L. Munaretto, H. Chaves, N. C. Dal Pont, **V. F. Gruner** and G. Finamor, "Hardware-In-the-Loop Simulation of Smart Hybrid Inverter: A comparison of online simulation and practical results," 2020 47th IEEE Photovoltaic Specialists *Conference (PVSC), Calgary, AB, Canada, pp.* 2005-2009, 2020.
- **V. F. Gruner**, T. P. Horn, L. Schmitz, D. Martins, R. F. Coelho, ‘High Step-Up DC-DC Converter with Input Current Sharing Based on the Forward Converter’, 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), pp. 1-10, 2019.
- **V. F. Gruner**, L. Schmitz, D. C. Martins, R. F. Coelho, “Conversor CC-CC de alto ganho com compartilhamento da corrente de entrada, modulação phase-shift e compactação do filtro de saída”, Revista Eletrônica de Potência, vol. 23, não. 2, pp. 141-150, junho 2018.

5.2.2 Co-advising and Teaching

- Undergraduated thesis - Eduardo Eller Behr – *Filtros Passivos Aplicados A Inversores Monofásicos.*
- Teaching: Semester: 2021-1 Course: EEL7550 *Eletrônica Aplicada* 05220 Period: 05 Credits: 4
- Teaching: Semester: 2020-2 Course: EEL7550 *Eletrônica Aplicada* 05220 Period: 05 Credits: 4

5.2.3 Reasearch projects between industry and academy

- Development of a hybrid inverter – *ANEEL R&D Project in partnership with ENEL, Reivax, Certi and INEP*.
- Energy dispatch strategy development from battery banks of a hybrid microgrid, based on technical-economic criteria – *Project between Certi and INEP for the company AES Tietê.*
- Development of photovoltaic microinverter – *Project between LUG power electronics and INEP.*
    - 3 patents
        - **BR1020230080553** – Método de controle para comutação suave de inversores flyback em microinversores solares fotovoltaicos
        - **BR1020220109028** - Método híbrido para rastreamento da máxima potência de geradores de energia solar fotovoltaica.
        - **BR512023001701-9 -** Código fonte utilizado no microinversor LUGmi.
- Smart and modular lithium-ion battery packs for energy storage systems – *Project between LUG power electronics and IFSC.*

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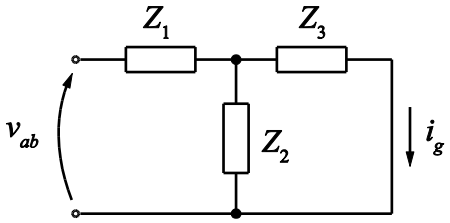
APPENDIX A
GRID-CONNECTED FILTER MODELING

A practical way to study the grid-connected filter behavior is to analyze the dynamic response (magnitude and phase) of the output to an input transfer function at some frequency. Transfer functions are mathematical representations of these dynamic responses for different excitation frequencies. As the main objective of this work is to analyze the grid current by the systems perturbations, the preferred filters transfer function will relate the output current to the input voltage disturbance.

The inverters output filters can be generically represented by the T connection shown in Figure A.1. The under analysis *LCL+RC* filter transfer function ($H_{LCL+RC}(s)$) that relates the grid current (i_g) with the quasi-instantaneous average voltage (v_{ab}) represented in Figure A.2Source: prepared by the authors.

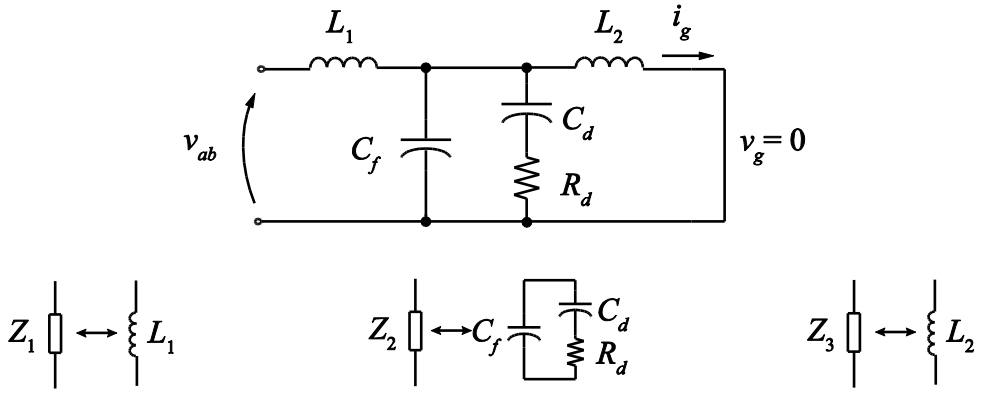
Figure is given by equation (A.0). It is worth mentioning that the representation shown in Figure A.2 is a small signals model of the inverter, in which a short circuit replaces the main grid.

Figure A.1– Generic T connection.



Source: prepared by the authors.

Figure A.2 – *LCL+RC* filter under analysis.



Source: prepared by the authors.

$$H_{LCL+RC}(s)=\frac{sC_dR_d+1}{s^4L_1L_2C_fC_dR_d+s^3L_1L_2\left(C_f+C_d\right)+s^2\left(L_1+L_2\right)C_dR_d+s\left(L_1+L_2\right)} \quad \text{(A.1)}$$

Extending the modeling analysis to those filters shown in Figure 4 (b), (c) and (f) the respective transfer functions can be obtained (see Eq. (A.1), (A.2) and (A.3)). In order to demonstrate the preliminary analysis of the filters, a Bode plot of each one is illustrated in Figure A.3, assuming the same ratings for the passive components. Figure 4 (d) was not plotted, because as previously mentioned, it has the same characteristic as the *LCL+RC* filter but with greater losses.

$$H_L(s)=\frac{1}{sL} \quad \text{(A.2)}$$

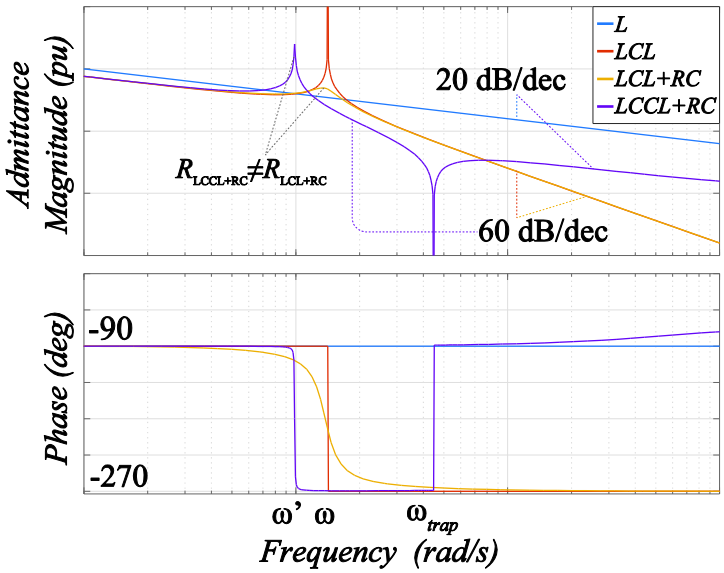
$$H_{LCL}(s)=\frac{1}{s^3L_1L_2C_f+s\left(L_1+L_2\right)} \quad \text{(A.3)}$$

$$H_{trap}(s)=\frac{\frac{C_t}{L_2C_{eq}}s^3+\frac{C_t}{L_2C_dR_dC_{eq}}s^2+\frac{1}{L_1L_2C_{eq}}s+\frac{1}{L_1L_2C_dR_dC_{eq}}}{s^4+\frac{C_d+C_{eq}}{C_dR_dC_{eq}}s^3+\frac{L_1+L_2}{L_1L_2C_{eq}}s^2+\frac{L_1+L_2}{L_1L_2C_dR_dC_{eq}}s}, \quad \text{(A.4)}$$

where: $C_{eq}=C_t+C_f$.

The Bode diagram analysis shows how the pulsed voltage (v_{ab}) applied at the filter input affects the injected grid current (i_g). Note that for low frequency the capacitive reactance tends to infinity value avoiding the current circulation along this path. In other way, the capacitor presents low impedance for high frequency current components. In the graphic, the lowest and highest positive resonance frequency are denoted by ω' and ω respectively. The trap frequency of the *LCCL+RC* filter is presented as ω_{trap}. In the *LCCL+RC* plot, the resonance is not correctly damped just to show different graphic dynamics. Obviously, the *LCCL+RC* filter, with an adequate resistance value, allows the necessary attenuation of the filter resonance.

Figure A.3 - Generalized bode plot of the passive filters from Figure 4 (b), (c), (e) and (f).



Source: prepared by the authors.

The *L* filter is the simplest but has a constant attenuation of 20 dB/decade, making its filtering not as efficient in some cases. *LCL* filter has only three passive elements, however, in practice, it is not applicable, since the high gain of the filter's resonance frequency can amplify undesirable noises leading to destructive events. The main drawbacks in the *LCCL+RC* filter are its complexity due to a high number of passive elements, and, after the trap frequency, the filter has only 20 dB/decade attenuation, making high-frequency noise to be poorly attenuated.

Reasons for choosing the *LCL+RC* filter are also justified by the graphical analysis, which show high attenuation at high frequencies and a damped behavior around the resonance frequency.

APPENDIX B
LCL+RC FILTER DESIGN

There are many criteria for sizing the differential mode filter aiming its optimization. The methodology presented below has the objective of adapting the filter in a practical way to meet the grid connections standards requirements. The main points for the filter project are:

1. Dynamics / Stability
2. Efficiency / Losses
3. Size / Cost

L_1 INDUCTANCE

The design of the L_1 inductance of the *LCL+RC* filter follows the same maximum ripple criteria as shown for the *L* filter. In this way, the figures and equations will be repeated for convenience.

The equation that allows inductance value calculation in the filter first stage is shown:

$$L_1 = \frac{MV_{bus}sen\left(\omega_{grid}t\right)\left[1-Msen\left(\omega_{grid}t\right)\right]}{f_s\Delta i_{Lmax}} \tag{B.1}$$

Normalizing (B.1), (B.2) it is obtained. Disregarding the parametric values, a normalized inductance graphic (bi and three dimensional) can be plotted by the ωt variation with distinct index modulation *M* as illustrated in Figure B.1.

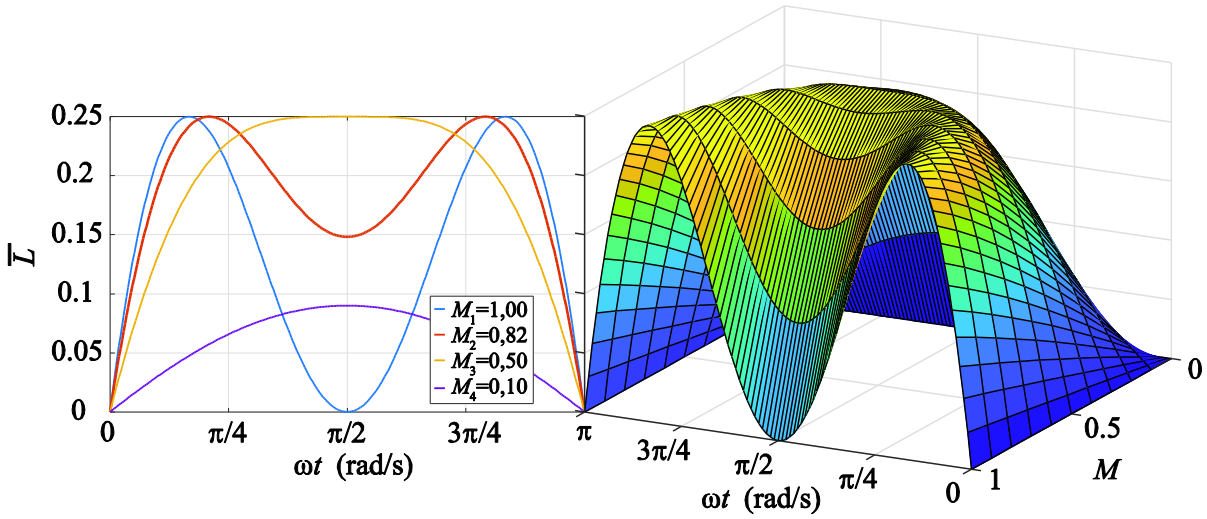
$$\overline{L_1} = \frac{Lf_s\Delta i_{Lmax}}{V_{bus}} = Msin(\omega t)[1-Msin(\omega t)] \tag{B.2}$$

As observed in Figure B.1, the minimum inductance to ensure the maximum current ripple limit changes on each instant of the grid half-cycle. Therefore, a maximum inductance value must be used to meet the ripple requirements all time.

The inductance maximum value can be obtained mathematically by deriving and equaling equation (B.2) to zero, resulting in:

$$L_{max} = \begin{cases} \dfrac{M(1-M)V_{bus}}{2f_s\Delta i_{Lmax}}, to\ \ 0 < M < 0.5 \\ \\ \dfrac{V_{bus}}{8f_s\Delta i_{Lmax}}, to\ \ 0.5 < M < 1 \end{cases} \tag{B.3}$$

Figure B.1 – Normalized inductance for ω*t* with distinct index modulation.



Source: prepared by the authors.

C_{eq} CAPACITANCE

The design of the equivalent capacitance value of the *LCL+RC* filter is perform by the filter resonance frequency. The resonance effect can cause instability in the output if some harmonic voltage/current occurs near the resonance frequency. Many works in the literature propose optimal resonance frequency calculation [58].

This methodology aims to design the resonance for the worst case, this, when the resonance is allocated at low frequencies, since lower the frequency, more difficult to attenuate it. In this case, the resonance frequency is assumed one decade below the converter switching frequency, since the cutoff frequency of the converter current control loop is projected at least more than one decade below the switching frequency. With this, the resonance will be attenuated in the system closed-loop response.

The worst attenuation case happens when L_{grid} tends to an infinite value leading to the *LCL* and *LCL+RC* resonance frequency closer to the low frequencies. Such frequency has the same value of the *LC* filter resonance frequency as shown the Bode diagram in Figure 6.

The equations that define *LC* and *LCL* filters resonance frequencies respectively are:

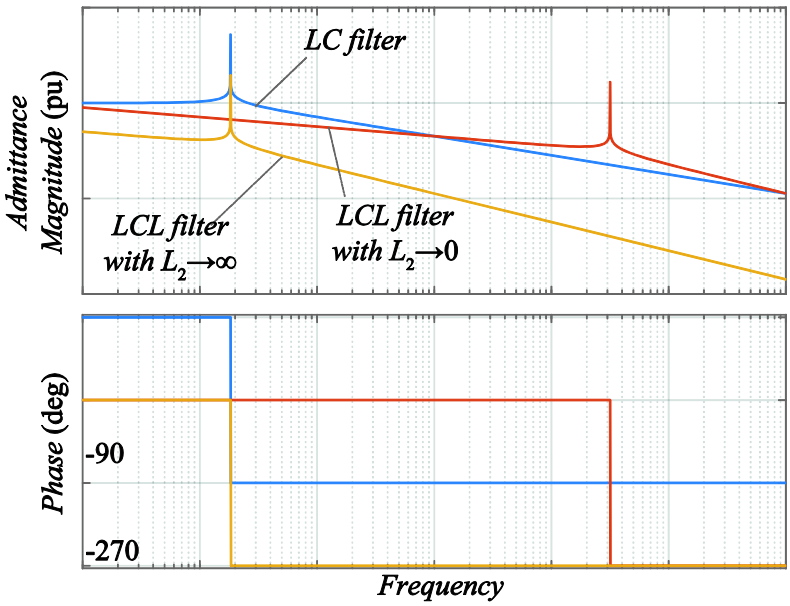
$$\omega_{r\_LC} = \sqrt{\frac{1}{LC}}; \qquad \omega_{r\_LCL} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{B.4}$$

As previously mentioned, in the worst case ($f_{r\_LCL} = f_{r\_LC}$) the resonance frequency project is set a decade below from the converter switching frequency. The equivalent capacitance value from *LCL+RC* filter is given by:

$$C_{eq} = \frac{1}{\left(2\pi \frac{f_s}{10}\right)^2 L_c} \tag{B.5}$$

where $C_{eq} = C_f + C_d$.

Figure B.2 – *LCL's* and LC filter resonance frequency.



Source: prepared by the authors.

Looking a for a good power factor, the fundamental reactive power processed by the filter capacitor should be less than 5\% of the total rated power [64]. The total reactive power in the capacitor is calculated by:

$$Q_{Ceq} = V_g{}^2 C_{eq} \omega_g, \tag{B.6}$$

and the current advance in relation to the voltage is calculated by:

$$\lambda_{\%} = \frac{Q_{Ceq}}{P_o}. \tag{B.7}$$

L_2 INDUCTANCE

The ratio between the inductances L_1 and L_2 are widely discussed by [64], which conclude that L_2 must be smaller than L_1 for stability reasons. Basically, this is due to the fact that the appearance of noise at lower frequencies are more constant and more difficult to attenuate than the high frequencies noises. Thus, the higher L_2, the resonance frequency shifts to a lower frequency and may coincide with some of these noises amplifying it.

Then, considering the system's stability L_2 is designed to define the maximum resonance frequency of the filter. The inductance L_2 is obtained by (B.8), where the maximum resonance frequency is set at least 2 times less than the switching frequency avoiding that even when the grid inductance was null, the resonance frequency will not coincide or will be after the switching frequency ensure the 60 dB attenuation.

$$L_2 = \frac{L_1}{\left(\frac{2\pi f_s}{2}\right)^2 L_1 C_{eq} - 1} \tag{B.8}$$

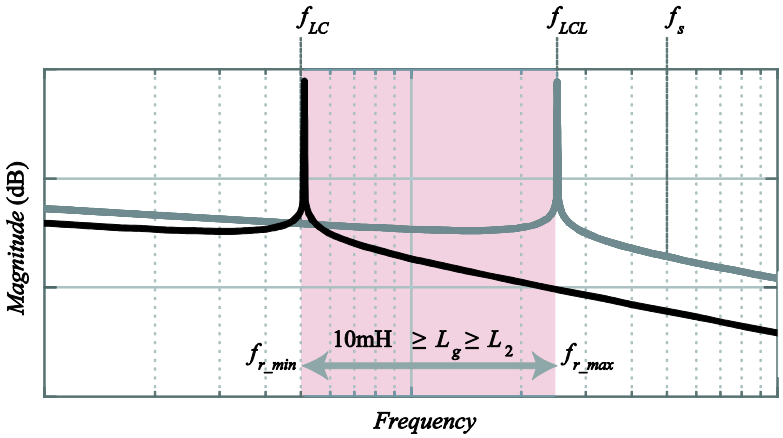
The maximum resonance frequency of the system is:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_{eq}}} \tag{B.9}$$

Considering that L_{grid} can vary from 0 to 10 mH, a magnitude graphic of the filter's Bode diagram is shown in Figure B.3. This shows the resonance frequency

range according to the grid inductance L_{grid}, thus defining a minimum and maximum resonance value.

Figure B.3 – Projected *LCL* filter by the grid inductance range.



Source: prepared by the authors.

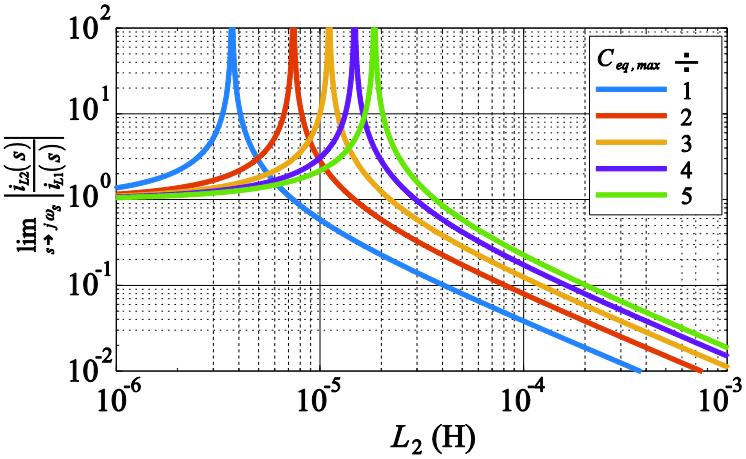
It is noteworthy that as the L_2 becomes higher (L_2 tending to infinite), the resonance frequency reaches the minimum f_{r_min} (B.10) which is determined by the *LC* resonance frequency as previously said. The difference between *LC* and *LCL* with L_2 equal to infinite lies directly in the system dB gain and not in the resonance.

$$f_{r\_min} = \frac{1}{2\pi}\sqrt{\frac{1}{L_1 C_{eq}}} \tag{B.10}$$

It is interesting to obtain an estimate of the total current ripple attenuation for different values of C_{eq} by L_2 rate. The current ripple attenuation of the *LCL* filter can be described by (B.11) and it is shown in Figure B.4. It is worth mentioning that this equation does not consider the grid inductance and the damping resistor.

$$\frac{i_{L_2}}{i_{L_1}}(s) = \frac{1}{s^2 C_{eq} L_2 + 1} \tag{B.11}$$

Figure B.3 – Ripple current attenuation to diverse C_{eq} values as function of L_2 range with $C_{eq,max} = 2.74$ µF.



Source: prepared by the authors.

It follow from Figure B.3 that lower the L_2 inductance, the greater is the grid current ripple. The same is also true for the C_{eq} capacitance value.

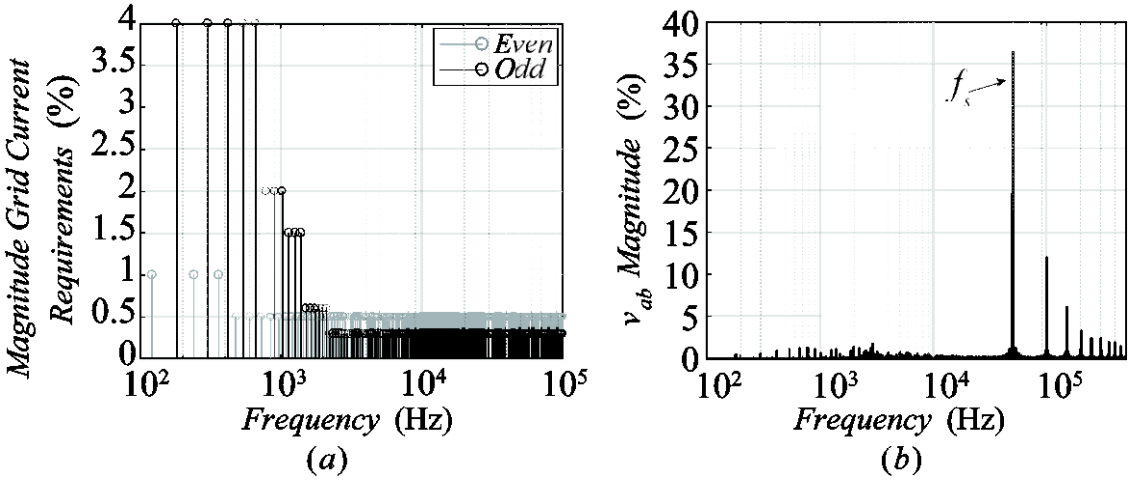
As a case study, inductance and capacitance values were determined following the proposed methodology for graphical examples. It is worth mentioning that the input values for the project were stipulated arbitrarily:

- $L_1 = 3.3$ mH
- $C_{eq} = 300$ nF
- $L_2 = 137$ µH

In order to analyze the filter performance was plotted in Figure B.4(a) a graphic that represents the magnitude of the grid current in per cent according to the standards by frequency. Figure B.4(b) shows the v_{ab} harmonic spectrum in per cent by the frequency of the chosen inverter with $f_s = 50$ kHz.

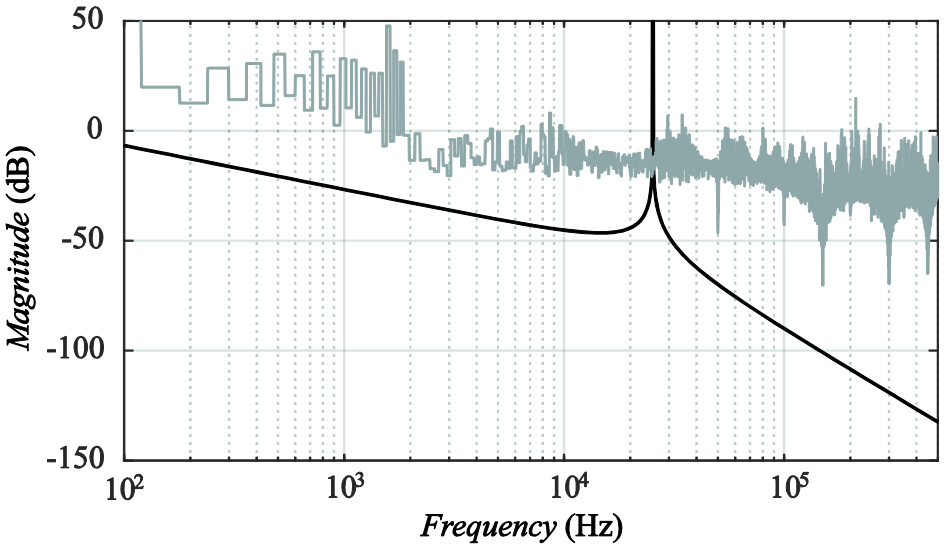
By dividing the injected grid current standards (Figure B.4a) by the rate of the input voltage filter [v_{ab} (Figure B.4b)], can be plotted the maximum limit allowed by the grid requirements. In the same figure it is also plotted a magnitude of the *LCL* filter transfer function (i_g/v_{ab}).

Figure B.4 – (a) Magnitude of the IEEE519 grid current requirements in %. (b) Converter v_{ab} magnitude in %.



Source: prepared by the authors.

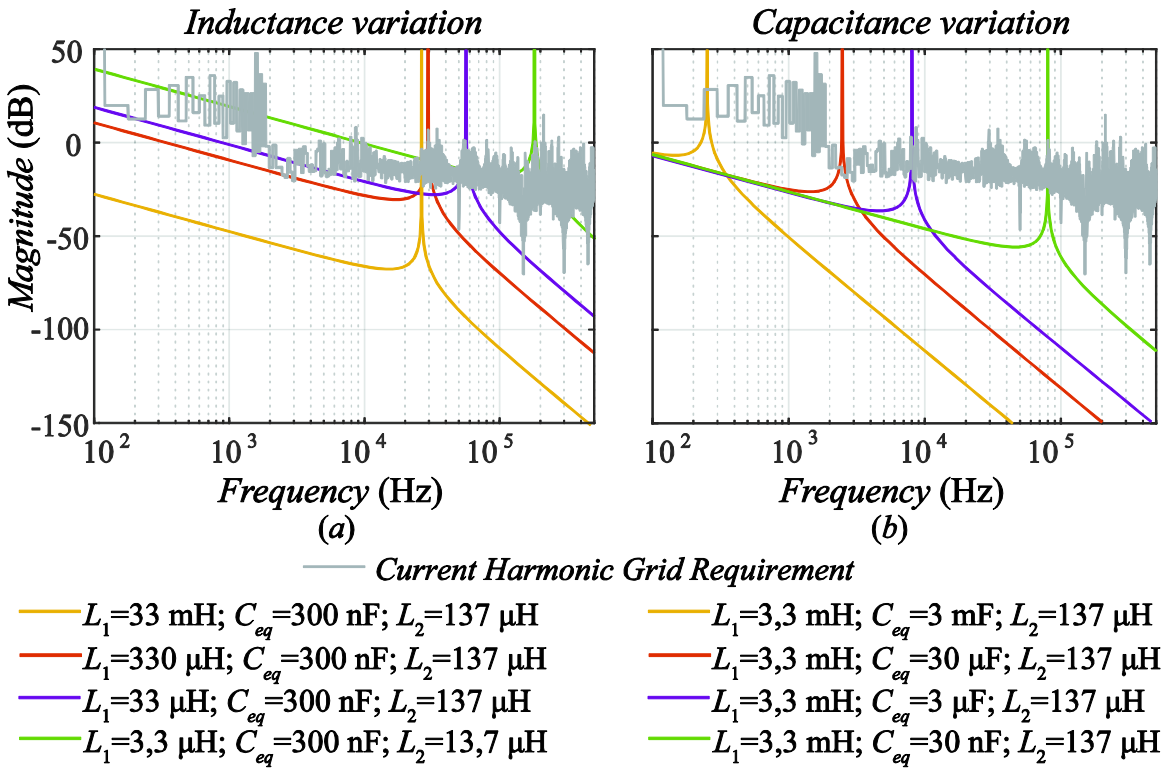
Figure B.5 – Project *LCL* filter magnitude and current harmonics grid requirement.



Source: prepared by the authors.

It can be easily seen that the *LCL* filter resonance directly interferes in the grid current, causing undesired frequencies to be amplified or poorly attenuated. Before dealing directly with the resonance, different magnitudes were plotted by the variation of the *LCL* filter inductance and capacitance as show in the Figure B.6 (a) and (b), respectively.

Figure B.6 – (a) *LCL's* magnitude with total inductance variation and fixed capacitance. (b) total capacitance variation with fixed inductance.



Source: prepared by the authors.

By changing the equivalent inductance, the gain and the resonance frequency also change, making the filter inadequate in some situations. When changing just the equivalent capacitance, only the resonance frequency varies. With this, it is concluded that the adequacy to the harmonic grid current standard depends directly on the value of the equivalent inductance, that is, the larger, easier to meet the requirements.

CAPACITANCE RATIO (C_{rate})

The ratio between the capacitances C_f and C_d of the *LCL+RC* filter is performed aiming the optimization of damping branch losses and filter attenuation.

To define C_{rate}, is necessary to determine the power dissipated in the damping resistor. Considering the fundamental frequency, neglecting the voltage drop on the inductor L_2, and knowing that the product of the voltage phasor by the conjugate of the current phasor gives the power apparent from this phase:

$$Q_{DB} = v_c I_{DB}^{*} \tag{B.12}$$

As the capacitor only consumes reactive power, it can be extracted the real part to know what it is the consumed power by the resistor.

$$P_{DB}\big|_{\omega=\omega_g} = real\left[v_c {I_{DB}}^*\right] \tag{B.13}$$

By applying the Laplace transform to solve (B.13) and then transforming to complex frequencies domain it is obtained the active power consumed in the damping branch by the influence of the fundamental frequency:

$$P_{DB}\big|_{\omega=\omega_g} = real\left[{v_c}^2 \frac{j\omega C_d\left(1-j\omega C_d R_d\right)}{1-\left(j\omega C_d R_d\right)^2}\right]$$

$$P_{DB}\big|_{\omega=\omega_g} = {v_c}^2 \frac{\omega^2 {v_c}^2 {C_d}^2 R_d}{1+\omega^2 {C_d}^2 {R_d}^2}, \tag{B.14}$$

where $v_c = v_g$.

The switching frequency losses are calculated assuming that at high frequencies, the grid voltage source is seen as a short circuit. Analyzing the capacitor voltage by the high frequency input voltage (v_{ab}) the following relation is presented:

$$v_c = \frac{v_{ab}\left(sL_2C_dR_d + L_2\right)}{s^3L_1L_2C_fC_dR_d + s^2L_1L_2\left(C_f + C_d\right) + s\left(L_1+L_2\right)C_dR_d + \left(L_1+L_2\right)} \tag{B.15}$$

Note that v_{ab}, in this case, is the maximum value of the switching frequency harmonic from the v_{ab} Fourier Fast Transform (FFT).

Applying a similar procedure performed for the fundamental frequency, it is obtained the damping branch current and losses for the switching frequency respectively:

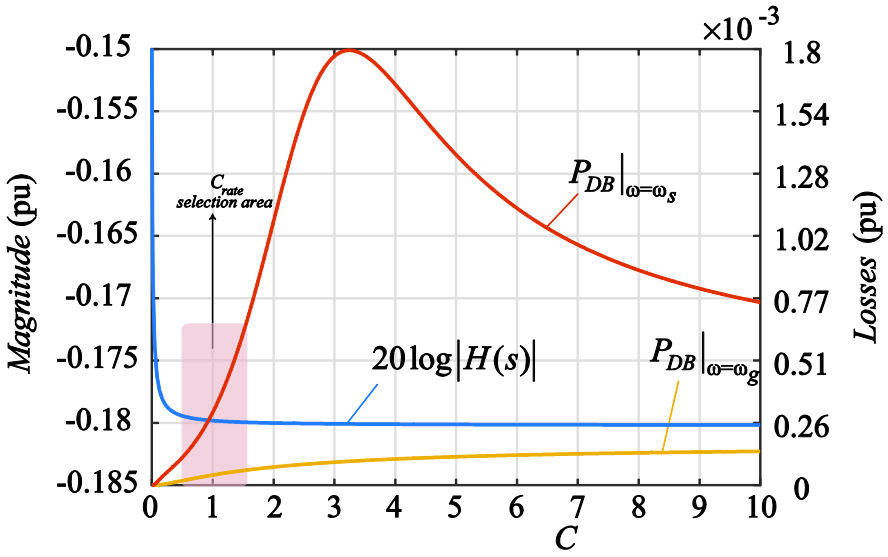
$$i_{DB} = \frac{v_c}{R + \dfrac{1}{j\omega_c C_d}}; \tag{B.16}$$

$$P_{DB}\big|_{\omega=\omega_s} = R_d\left(\frac{|i_{DB}|}{\sqrt{2}}\right)^2. \tag{B.17}$$

To analyze the relation between damping and losses is shown in Figure B.7 the magnitude of *H*(s) and the damping branch losses by the ratio of capacitors C_f and C_d.

If the relation between capacitors was very small (C_f >> C_d, C_{rate} tends to 0), the damping branch will be a very low impedance for the high frequency components, concentrating most of the current and thus, making it more difficult to attenuate. On the other hand (C_f << C_d, C_{rate} tends to ∞), the magnitude curve is already stabilized, but damping branch concentrate most of the current, increasing losses.

Figure B.7 – (a) *H*(s) filter transfer function magnitude and damping branch losses by capacitance ratio.



Source: prepared by the authors.

The C_{rate} selection area of the Figure B.7 ensures the compromise between attenuation and losses. The equations that determine the capacitances C_d and C_f are shown, respectively:

$$C_d = \frac{C_{eq}C_{rate}}{C_{rate}+1} \tag{B.18}$$

$$C_d = \frac{C_{eq}C_{rate}}{C_{rate}+1} \tag{B.19}$$

R_d DAMPING RESISTANCE

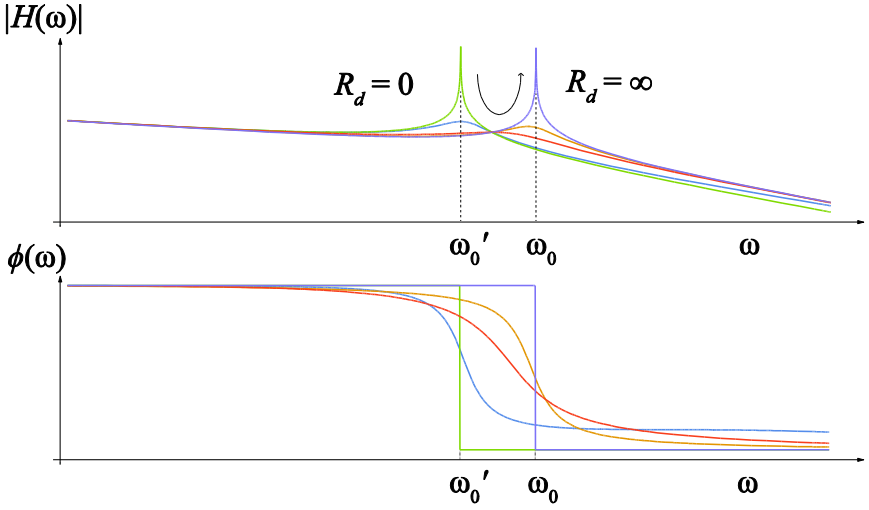
The damping resistor design methodology it is aiming for greater attenuation independent of the arrangement of inductors and capacitors of the *LCL+RC* filter.

As one can verify, changes on the damping resistance R_d strongly affect the poles of $H(s)$ and, thus, its dynamic behavior. Figure B.7 shows the Bode diagram of $H(\omega)$ for different values of R_d. When R_d tends to infinity, the damping branch is open and no longer influences the circuit, resulting in an undamped filter which resonance frequency is ω_0.

When R_d tends to zero, C_d and C_f are placed in parallel and the resonance frequency is shifted to ω_0', however, the filter is also undamped. For intermediary values of R_d the filter becomes damped around the resonance frequency, as evidence the plot shown in Figure B.8 .

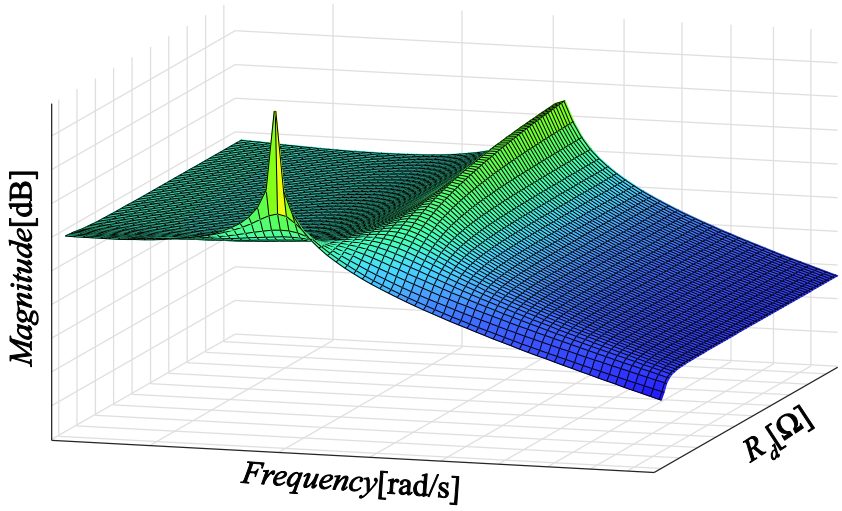
The diagrams of Figure B.8 and Figure B.9 shows that the magnitude of $H(s)$ changes according to the value set to R_d. In the following of this section will be presented a methodology to find the optimized damping resistance in order to minimize the magnitude of $H(s)$ at the resonance frequency.

Figure B.8 – $H(\omega)$ bode diagram for different values of R_d



Source: prepared by the authors.

Figure B.9 – $H(\omega)$ 3d bode diagram for different values of R_d



Source: prepared by the authors.

The first step to determine the optimized damping resistance is to analyze the poles of $H(s)$. As one of them is located at the origin, the remaining ones can be obtained by:

$$s^3 + as^2 + bs + c = 0 \tag{B.20}$$

where:

$$a = \frac{C_f + C_d}{R_d C_f C_d}, \qquad b = \frac{L_1 + L_2}{L_1 L_2 C_f} \qquad c = \frac{L_1 + L_2}{R_d L_1 L_2 C_f C_d} \tag{B.21}$$

The resonance of a third order system is associated to the existence of a pair of complex-conjugated poles. Therefore, (B.21) can be factored in accordance with:

$$\left(s - x_{real}\right)\left[s^2 + s\left(a + x_{real}\right) + \frac{c}{-x_{real}}\right] = 0, \tag{B.22}$$

where a and c were previously presented in (B.21) and x_{real} is a real pole of $H(s)$, here determined by the Cardano-Tartaglia method, derived in 1545 as a literal mathematical tool to find the roots of cubic polynomials.

$$x_{real} = S + T - \frac{a}{3} \tag{B.23}$$

where:

$$\begin{aligned} S &= \sqrt[3]{R + \sqrt{Q^3 + R^2}}, \\ T &= \sqrt[3]{R - \sqrt{Q^3 + R^2}}, \\ R &= \frac{ab}{6} - \frac{c}{2} - \frac{a^3}{27}, \\ Q &= \frac{b}{3} - \frac{a^2}{9}. \end{aligned} \tag{B.24}$$

The decomposition of the poles of *H*(s) allows rewriting it as:

$$H(s) = \frac{\frac{1}{L_1 L_2 C_1}\left(s + \frac{1}{C_2 R_d}\right)}{s\left(s - x_{real}\right)\left[s^2 + s\left(a + x_{real}\right) + \frac{c}{-x_{real}}\right]}, \tag{B.25}$$

which magnitude in decibels is calculated according to:

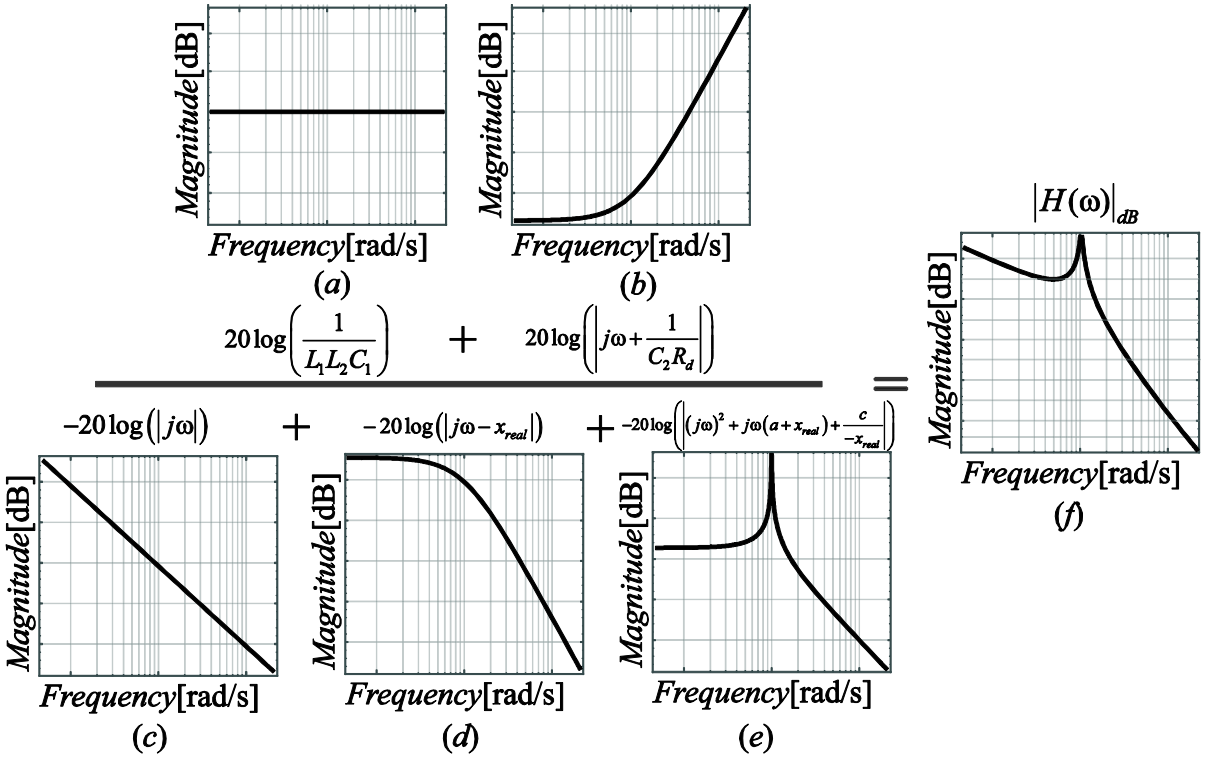
$$\begin{aligned} \left|H(\omega)\right|_{dB} = {} & 20log\left(\frac{1}{L_1 L_2 C_1}\right) + 20log\left(\left|j\omega + \frac{1}{C_2 R_d}\right|\right).. \\ & ..-20log\left(\left|j\omega\right|\right) - 20log\left(\left|j\omega - x_{real}\right|\right).. \\ & -20log\left(\left|\left(j\omega\right)^2 + j\omega\left(a + x_{real}\right) + \frac{c}{-x_{real}}\right|\right). \end{aligned} \tag{B.26}$$

By plotting each individual term of (B.26), as per Figure B.10 (a)-(f), one can verify that the resonance phenomenon is exclusively related to the second-order poles. Furthermore, as the magnitude plot of *H*(s) is obtained simply by the sum of these individual terms, Figure B.10 (f), it is intuitive to conclude the resonance frequency ω_r

of both *H*(s) and *G*(s) is the same, where G(s) is the transfer function associated to the second-order poles:

$$G(s) = \frac{1}{s^2 + s\left(a + x_{real}\right) + \dfrac{c}{-x_{real}}} \tag{B.27}$$

Figure B.10 – Magnitude plots



Source: author.

The resonance occurs when *G*(ω) reaches its maximum value, hence, the resonance frequency ω_r may be calculated by matching the derivative of |*G*(ω)| and equaling to zero:

$$\frac{d|G(\omega)|}{d\omega} = 0 \rightarrow \omega_R = \sqrt{\left(\frac{c}{-x_{real}}\right) - \frac{1}{2}\left(a + x_{real}\right)^2}. \tag{B.28}$$

Now, replacing (B.28) into (B.27), G(ω_r) is obtained:

$$|G(\omega_R)| = \frac{1}{\sqrt{\left(\dfrac{c}{x_{real}} + \omega^2\right)^2 + \omega^2\left(a + x_{real}\right)^2}}. \tag{B.29}$$

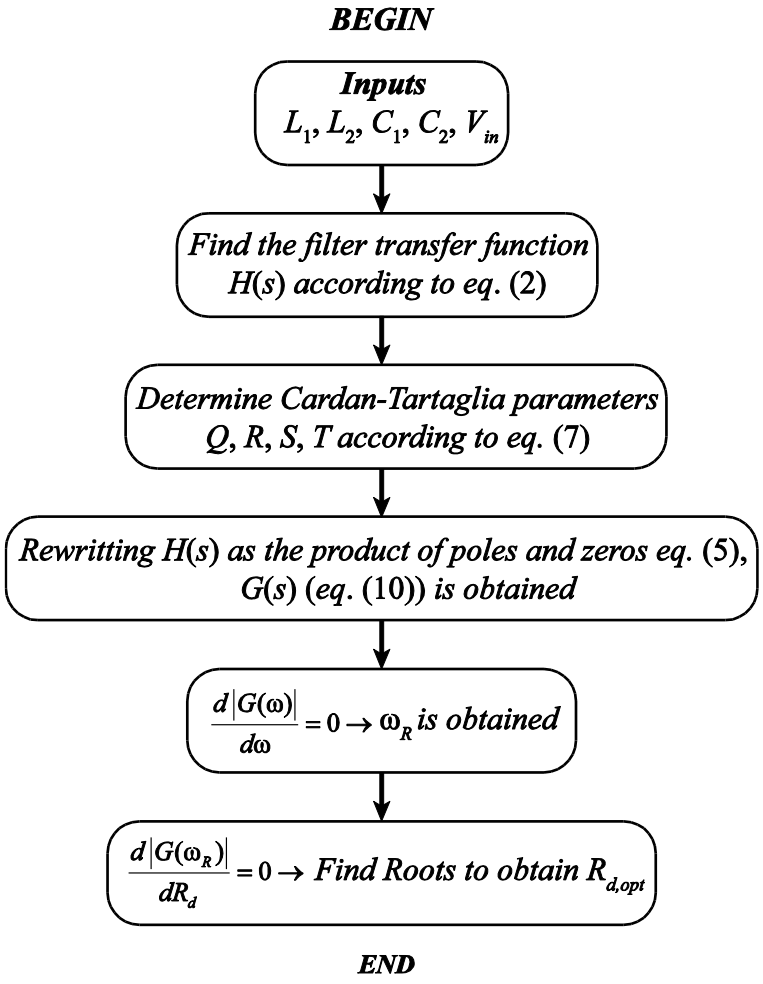
$$|G(\omega_R)| = \frac{1}{(a + x_{real})\sqrt{-\frac{1}{4}(a + x_{real})^2 - \frac{c}{x_{real}}}}. \tag{B.30}$$

Since the quantities *a*, *c* and x_{real} depends exclusively on R_d, $G(\omega_r)$ can be understood as $G(R_d)$. Thus, in order to define the value of R_d that minimizes this function, the derivate of $G(\omega_r)$ with respect to R_d need to be equaled to zero:

$$R_{d,opt} \rightarrow \frac{d}{dR_d}\left[\frac{1}{(a + x_{real})\sqrt{-\frac{1}{4}(a + x_{real})^2 - \frac{c}{x_{real}}}}\right] = 0. \tag{B.31}$$

This procedure will result in a large equation that can be easily solved by numerical methods. The flowchart depicted in Figure B.11 summarizes the steps of the proposed methodology.

Figure B.11 – Flowchart for the damping resistance optimization.



Source: prepared by the authors.

In order to validate the proposed methodology a *LCL+RC* filter was theoretical and experimentally evaluated. The inductors, capacitors and one of the resistors used in the setup test are illustrated in Figure B.12, while their values are listed below:

- $L_1 = 100\ \mu H$
- $C_f = 1\ \mu F$
- $C_f = 1\ \mu F$
- $L_2 = 100\ \mu H$
- $R_d = 0, 8.2, 15, 20, \infty\ \Omega$

Figure B.12 – Passive components employed during the experimental tests.

Source: prepared by the authors.

The theoretical value of $R_{d,opt}$ was obtained by applying the parameters value in the flowchart of Figure B.11, that returned:

$$R_{d,opt} = 14.9421\ \Omega\ for\ 0\Omega \leq R_d \leq \infty\Omega \tag{B.32}$$

To validate that $R_{d,opt}$ minimizes the magnitude of $H(s)$ at ω_r, $|H\omega)|$ was plotted, as per Figure B.13.

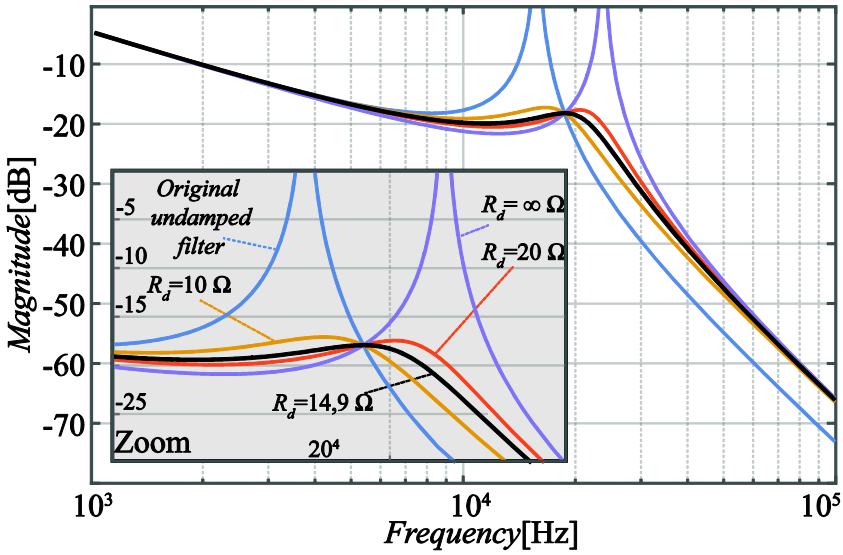
Additionally, from Figure B.14 it is possible to note that $R_{d,opt}$ really minimizes the magnitude of both $H(\omega)$ and $G(\omega)$. The understanding of this fact was crucial for the development of the methodology here presented.

The experimental tests were conducted by the employment of the scope DSO-X 4054A in ac sweep mode. In this configuration, the scope is able to generate an alternate voltage which frequency is varied in a previously specified range. This

voltage was applied to the filter input, while a probe was used to measure the filter output.

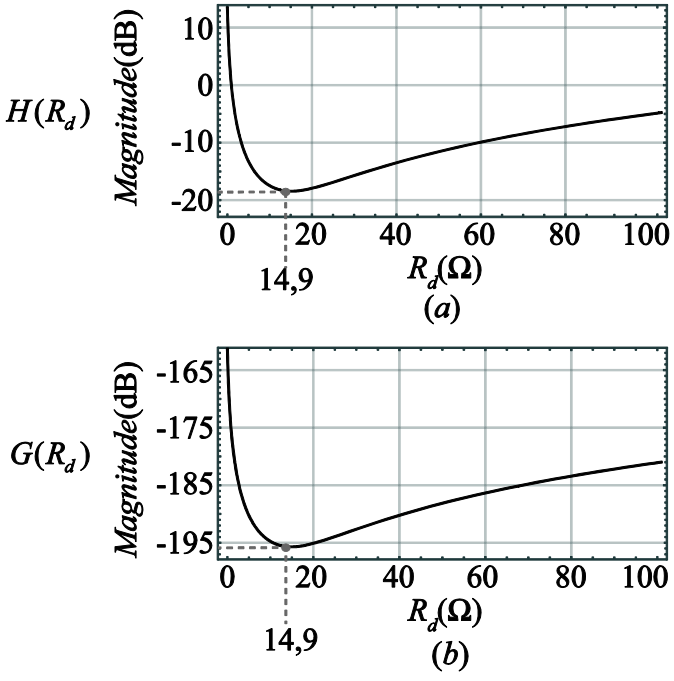
The tests were carried out under conditions similar to those considered to obtain theoretical results. A print of the scope image with the magnitude of $H(\omega)$ is presented in Figure B.15. The points in .csv format were also acquired and are shown in the miniature view inside Figure B.15.

Figure B.13 – Magnitude plot of $H(\omega)$ for different R_d values.



Source: prepared by the authors.

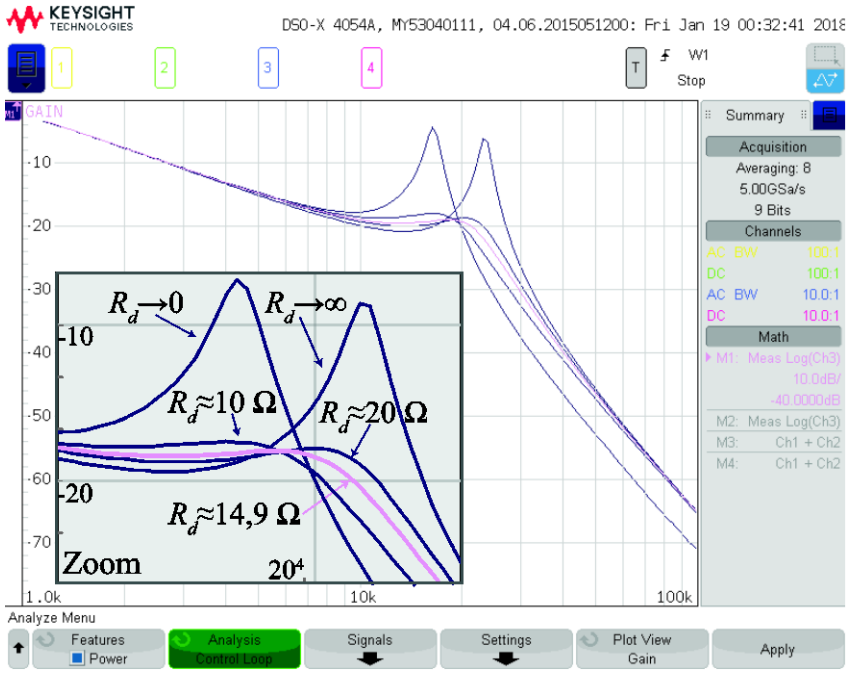
Figure B.14 – Same R_d for $H(R_d)$ and $G(R_d)$.



Source: prepared by the authors.

It is noteworthy that in the experimental tests, for R_d tending to zero (short circuit) and for R_d tending to ∞ (open circuit), the magnitude of $H(s)$ did not tend to infinite as it was predicted by the theoretical results, due to the presence of parasitic elements in the practical circuit. Still, it may be noted that $R_{d,opt}$ is the resistance that takes |H(ω)| to its minimum value. With that, it is concluded that the proposed methodology guarantees the highest gain attenuation of *LCL+RC* filters at the resonance frequency.

Figure B.15 – $R_{d,opt}$ practical results.

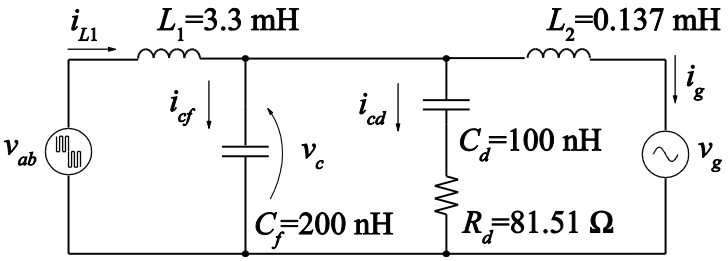


Source: author.

LCL+RC filter

Going back to the first case study, considering C_{rate} = 0.5 and applying the optimization method to the previous parameters, it is obtained the values of C_f, C_d and R_d as shown in Figure B.16.

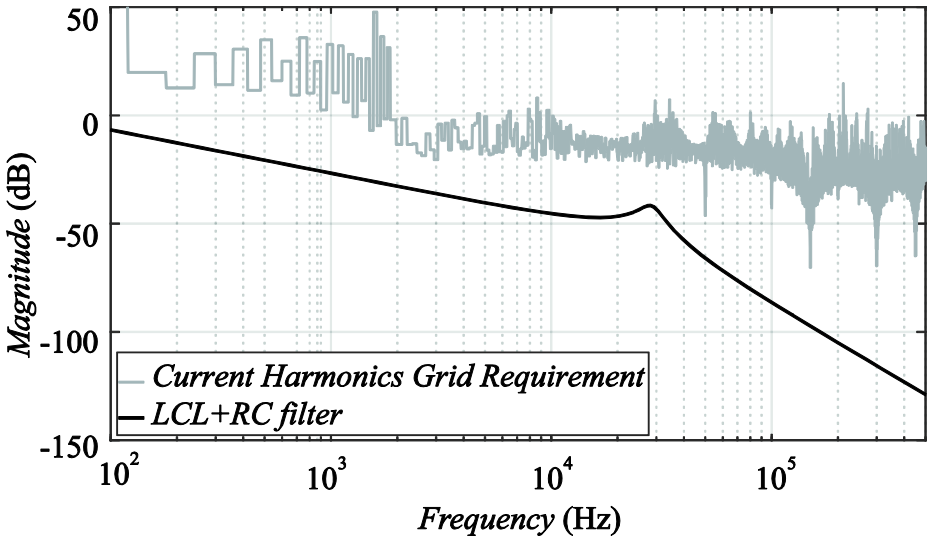
Figure B.16 – *LCL+RC* filter parameters calculated.



Source: prepared by the authors.

Figure B.17 shows the transfer function i_g / v_{ab} $ from *LCL* + *RC* filter in comparison to the current harmonics grid requirement in the frequency domain.

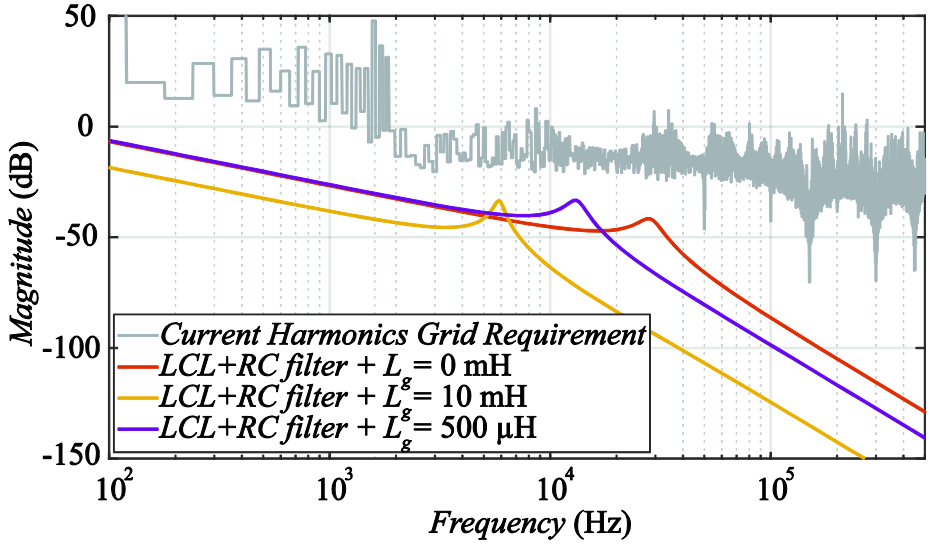
Figure B.17 – i_g / v_{ab} from *LCL* + *RC* filter in comparative analysis with current harmonics grid requirement.



Source: prepared by the authors.

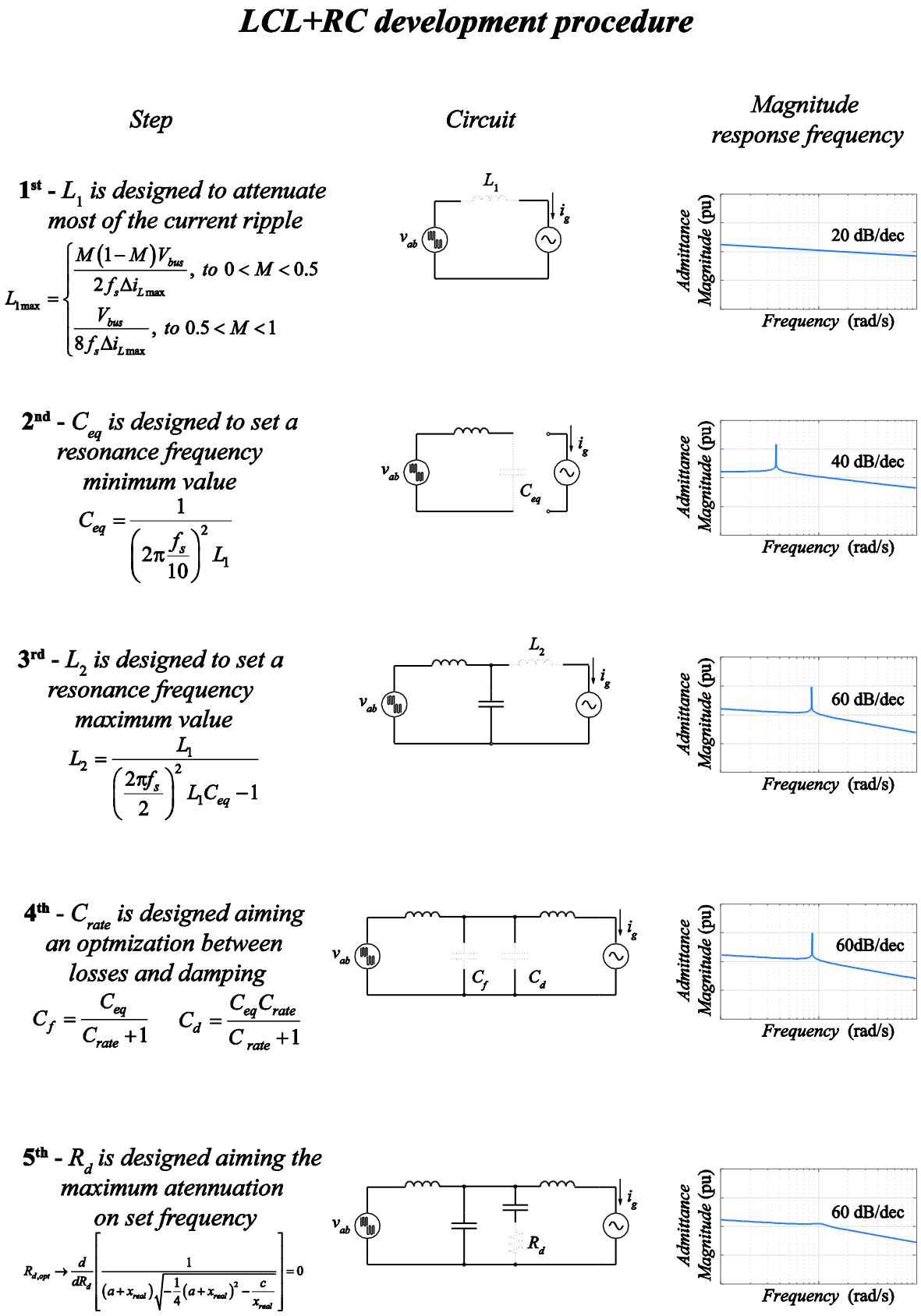
Even considering that the grid inductance can change from 0 to 10 mH, as shown in Figure B.18, the designed filter would meet the standards specifications. Due to the proposed methodology, the filter resonance frequency has its pre-determined maximum and minimum range values for an operation with greater stability and consequently a higher efficiency. The full simplified methodology is presented in Figure B.19.

Figure B.18 – Dynamic analysis of the designed filter with grid impedance variations.



Source: prepared by the authors.

Figure B.19 – Full methodology.



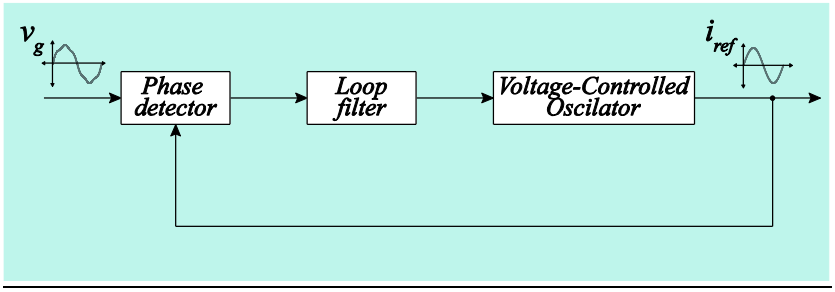
Source: prepared by the authors.

APPENDIX C
SOGI-SRF-PLL DESIGN

This appendix contains the detailed design and project of a single-phase Second-Order Generalized Integrator with Synchronous Reference Frame for Phase Locked Loops.

It is know that, commonly, three process steps compose single-phase PLLs as show Figure C.1:

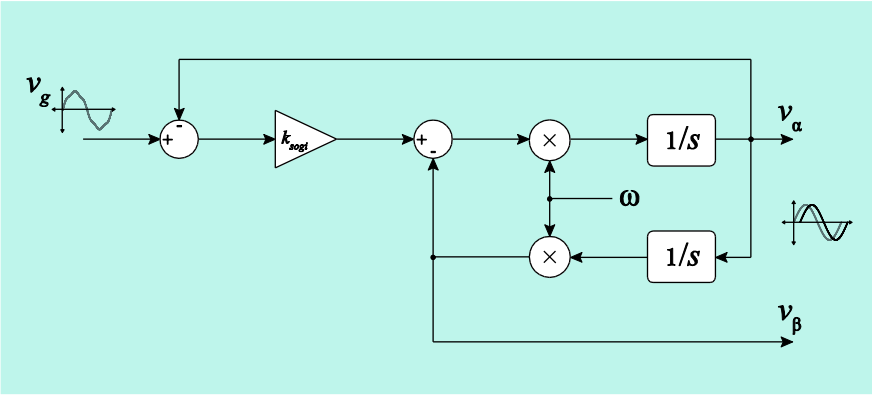
Figure C.1 – Single-phase PLL's.



Source: prepared by the authors.

In this case, the PLL phase-detector consists in generating an orthogonal signal from the distorted grid voltage using a second-order generalized integrator (SOGI - see Figure C.2) proposed by [84] and a Park transformation as show Figure C.3.

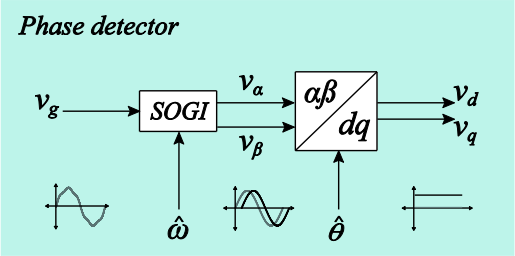
Figure C.2 – Second-Order Generalized Integrator.



Source: prepared by the authors.

Analyzing the block diagram of Figure C.2, its can be extracted the transfer function that describes the v_α and v_β behavior in relation to a input voltage (v_g). Their respective equations are presented in (C.1) and (C.2):

Figure C.3 – Phase detector block diagram.



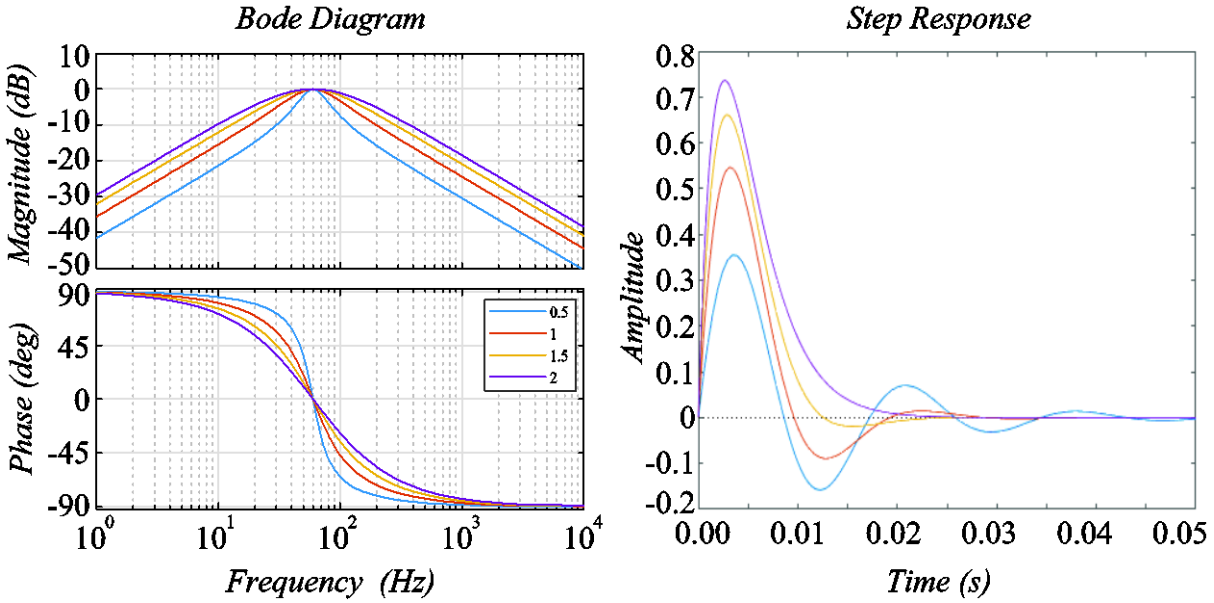
Source: prepared by the authors.

$$H\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k_{sogi}\omega_g s}{s^2 + k_{sogi}\omega_g s + \omega_g{}^2} \tag{C.1}$$

$$H\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k_{sogi}\omega_g{}^2}{s^2 + k_{sogi}\omega_g s + \omega_g{}^2} \tag{C.2}$$

The Bode diagram of equations (C.1) and (C.2) and their step response are illustrated in Figure C.4 and Figure C.5, respectively.

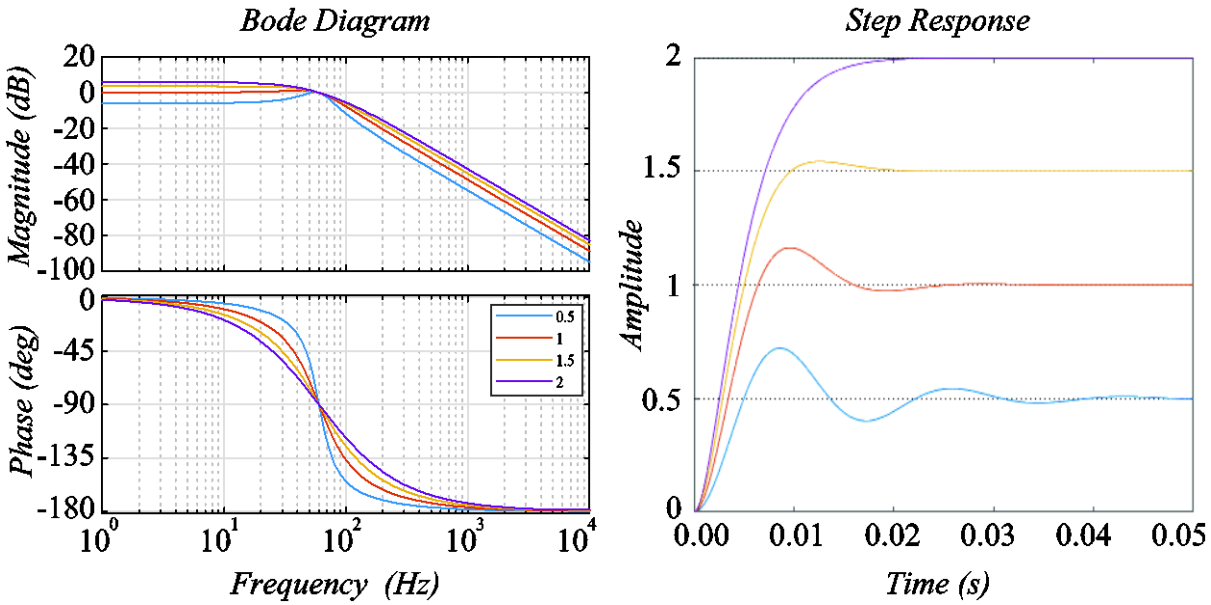
Figure C.4 – Bode diagram and step response from eq. (C.1).



Source: prepared by the authors.

The output v_α is a signal in phase with the input signal with 20 dB/decade attenuation after the PLL frequency. $H\alpha$ exhibits a band-pass filtering behavior and the bandwidth is determined by the damping factor k_{sogi}, in which the lower the gain, the smaller will be the bandwidth and greater side bands attenuation.

Figure C.5 – Bode diagram and step response from eq. (C.2).



Source: prepared by the authors.

v_β is a quadrature signal from input, with 40 dB/decade attenuation and the transfer function $H\beta$ exhibits a low-pass filtering characteristic where, in this case, the gain is directly linked to the filter's damping factor.

Small frequency variations in relation to SOGI frequency feedback ($\hat{\omega}_g$) cause disturbances in the amplitudes of the v_α and v_β sine waves, making the PLL frequency adaptable. Still part of the phase detector block, there is a park transformation (αβ to dq) defined as follow:

$$T = \begin{bmatrix} cos\,\hat{\theta} & sin\,\hat{\theta} \\ -sin\,\hat{\theta} & cos\,\hat{\theta} \end{bmatrix} \tag{C.3}$$

where $\hat{\theta} = \omega t + \hat{\phi}$ is the ouput PLL phase angle.

Thus, the phase detector block outputs is represented by the equation:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} . \begin{bmatrix} cos\,\hat{\theta} & sin\,\hat{\theta} \\ -sin\,\hat{\theta} & cos\,\hat{\theta} \end{bmatrix} = \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \tag{C.4}$$

Assuming $v_g = V_p sin(\omega t + \phi)$, a frequency-locked condition (i.e., $\omega = \hat{\omega}$) and after some algebraic manipulations, the transient behavior in time when input signal is suddenly applied can be described as:

$$v_\alpha(t) = V_p\, sin(\omega t + \phi) + A_\alpha\, sin\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\alpha\right) e^{-\frac{k_{sogi}\omega t}{2}} \tag{C.5}$$

$$v_\beta(t) = V_p\, cos(\omega t + \phi) + A_\beta\, cos\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\beta\right) e^{-\frac{k_{sogi}\omega t}{2}} \tag{C.6}$$

v_α and v_β in steady state are in phase and quadrature phase, respectively, with the input voltage signal. Applying the park transformation (C.3) in $v_\alpha(t)$ and $v_\alpha(t)$ it is obtained:

$$\begin{aligned} v_d(t) = {} & V_p\, cos(\theta - \hat{\theta}) + A_\alpha cos(\hat{\theta})\, sin\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\alpha\right) e^{-\frac{k_{sogi}\omega t}{2}} \\ & + A_\beta\, sin(\hat{\theta})\, cos\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\beta\right) e^{-\frac{k_{sogi}\omega t}{2}} \end{aligned} \tag{C.7}$$

$$\begin{aligned} v_q(t) = {} & V_p\, sin(\theta - \hat{\theta}) - A_\alpha sin(\hat{\theta})\, sin\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\alpha\right) e^{-\frac{k_{sogi}\omega t}{2}} \\ & + A_\beta\, cos(\hat{\theta})\, cos\left(\sqrt{1-\left(\frac{k_{sogi}}{2}\right)^2}\,\omega t + \phi_\beta\right) e^{-\frac{k_{sogi}\omega t}{2}} \end{aligned} \tag{C.8}$$

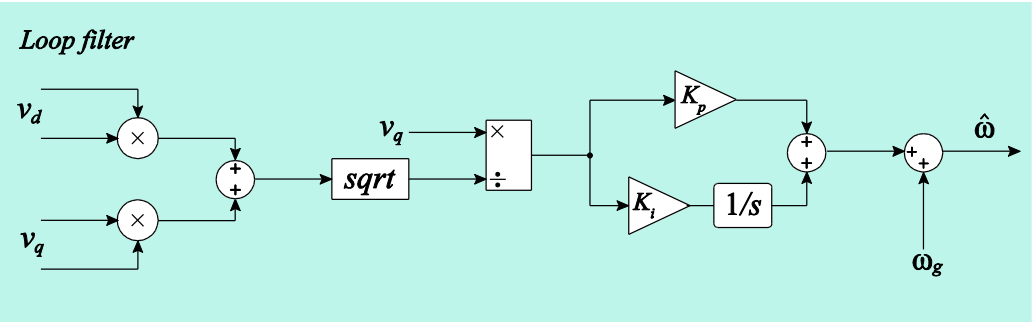
v_d represent the peak amplitude of the grid voltage and v_q gives the phase error information. Observing equations (C.7) and (C.8) and considering a small variation of θ in steady state, it is noticed the tendency of the terms with negative exponentials go to zero.

Following the analysis of the PLL general structure (Figure C.1) there is the loop filter. In turn, it is responsible for eliminating the phase error, also ensuring the high frequency noise attenuation. In this specific case, the PI type compensator was applied, which guarantees zero step error and high frequency noise attenuation. Series-connected to the PI, a feedforward tuned to the grid frequency is added to smooth the control efforts, mainly in the starting stage.

Also as part of the loop filter, before entering the compensator, a input voltage normalizer is positioned, making the PLL output reference unitary, regardless the voltage acquisition amplitude, so that it can be later multiplied by the current reference peak value. Figure C.6 illustrates in detail the loop filter block.

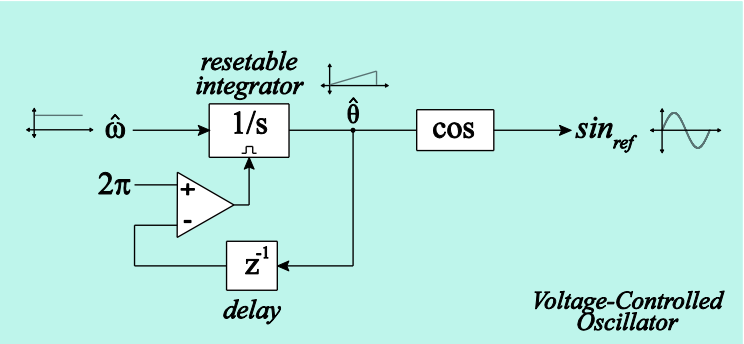
A resetable integrator set in 2π to generate the output angle composes the voltage-controlled oscillator block. Its output is multiplied by a cosine function to generate the sinusoidal unitary reference. Figure C.7 illustrates, in details, the voltage-controlled oscillator block.

Figure C.6 – Loop filter block diagram.



Source: prepared by the authors.

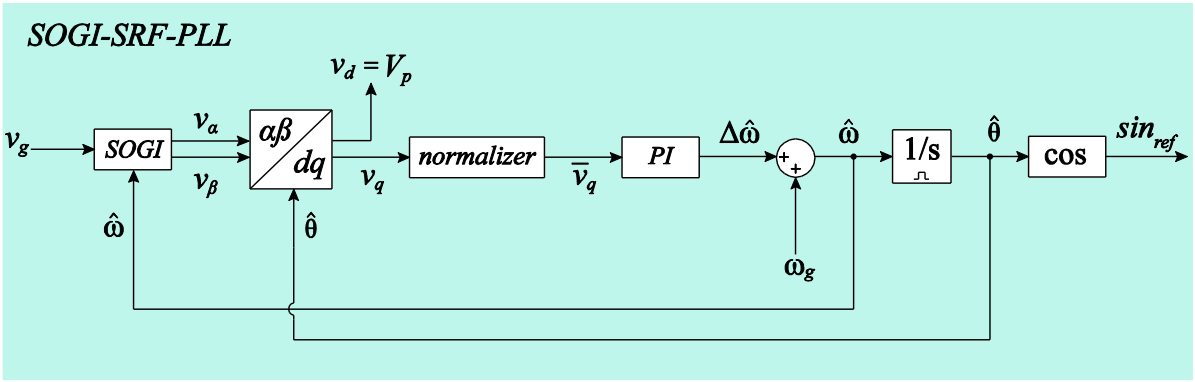
Figure C.7 – Voltage-controlled oscillator block diagram.



Source: prepared by the authors.

With all blocks together it is obtained the SOGI-SRF-PLL block diagram representation as illustrated in Figure C.8

Figure C.8 – SOGI-SRF-PLL.



Source: prepared by the authors.

SMALL SIGNALS LINEAR MODEL

To define the design guidelines, it is first necessary to obtain a linearized model for SOGI-PLL. For such model, conditions are established according to [84], where the estimated frequency is almost equal to the real one ($\omega \cong \hat{\omega}$) and is considered a small difference between the real and estimated phase angles $sin(\theta - \hat{\theta}) \cong (\theta - \hat{\theta})$ and $sin(\theta - \hat{\theta}) \cong 1$.

As observed, v_q has some of their terms decaying to zero in $2/k_{sogi}\omega$ time constant. With that, v_q tends to $sin(\phi - \hat{\phi})$, concluding that for a phase small step, v_q can be approximated in frequency domain to equation

$$v_q(s) \cong \frac{V_p}{\frac{2}{k_{sogi}\omega}s+1}(\theta-\hat{\theta}) \tag{C.9}$$

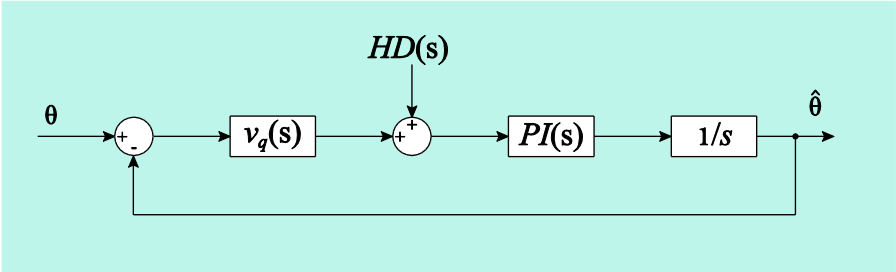
Now considering the input grid voltage harmonics, equation (A.9) can be rewritten, considering such disturbances, as follow:

$$v_q(s) \cong \frac{V_p}{\frac{2}{k_{sogi}\omega}s+1}(\theta-\hat{\theta}) + HD(s) \tag{C.10}$$

where HD is the harmonics disturbances.

Based on these considerations, a block diagram corresponding to small signal linear model for phase disturbances can be assembled.

Figure C.9 – Small signal linearized block diagram.



Source: prepared by the authors.

In order to design the compensator PI, it can easily obtained the open loop not compensated transfer function by analyzing Figure C.9.

$$OLTF_{nc\_\theta}(s) = \frac{V_p}{s(\frac{2}{k_{sogi}\omega}s+1)} \tag{C.11}$$

The specifications of the transitional period time response can be transcribed in the frequency domain in terms of phase margin, gain margin and bandwidth. These specifications can be easily read from the Bode diagram.

Through the behavior analysis of the system transfer function in open loop not compensated, it can be defined the zero frequency and the proportional gain of the PI compensator used in this application.

$$\omega_z = \frac{\omega_c}{tan\left[m_\phi - 90^\circ - \angle OLTF_{nc\_\theta}(j\omega_c) \right]} \tag{C.12}$$

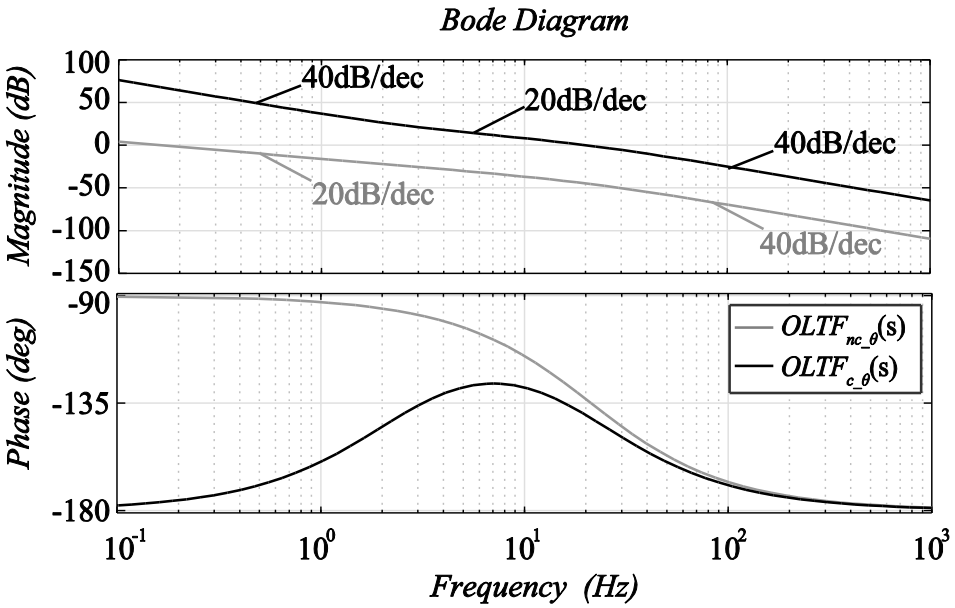
$$k_p = \frac{\omega_c}{\left| OLTF_{nc\_\theta}(j\omega_c) \right| \sqrt{\omega_c^2 + \omega_z^2}} \tag{C.13}$$

The PI cut-off frequency was designed in 20 Hz to eliminate high frequency noise. The cut-off frequency is an quantity related to the system's response speed, that is, the lower the cut-off frequency, slower is the system response until it reaches the steady state. The phase margin was designed in 40º to ensure the system stability, as it is an indirect measure of the system damping coefficient. Thus, it is possible to equate the compensated open loop transfer function as follow:

$$OLTF_{c\_\theta}(s) = \frac{V_p K_p \left(s + \frac{k_i}{k_p} \right)}{\frac{2}{k_{sogi}\omega} s^2 \left(s + \frac{k_{sogi}\omega}{2} \right)}, \tag{C.14}$$

and the Bode diagram of compensated and non-compensated functions is shown in Figure C.10.

Figure C.10 – Small signal linearized block diagram.

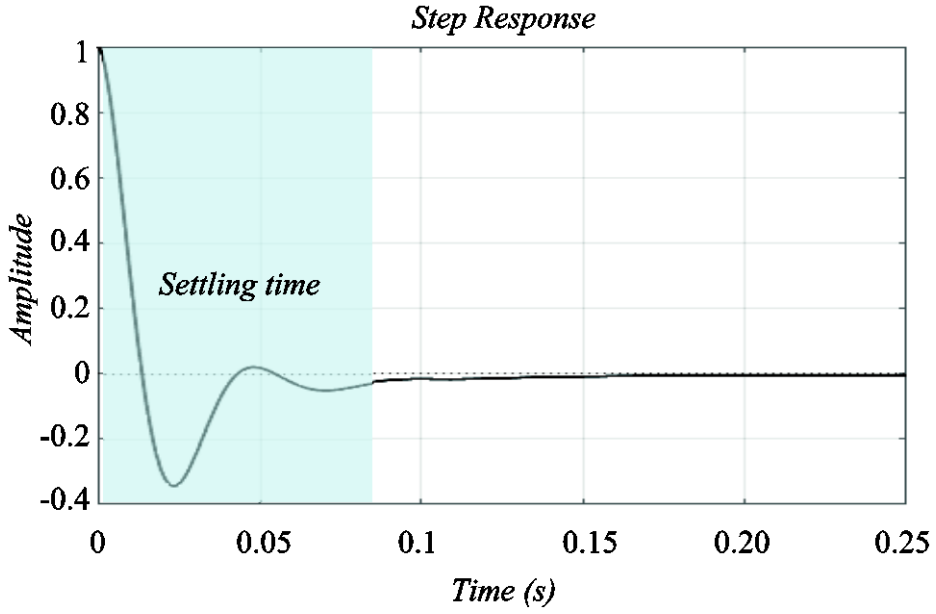


Source: prepared by the authors.

The closed loop transfer function compensated is described as equation (C.15) and its step response is shown in Figure C.11.

$$CLTF_{c\_\theta} = \frac{1}{1 + OLTF_{c\_\theta}(s)} \tag{C.15}$$

Figure C.11 – Small signal linearized block diagram.



Source: prepared by the authors.

To validate the PLL effectiveness, some simulations were performed. First scenario is considering v_g with harmonics of 3 and 5 order as presented in equation (C.16):

$$v_g = V_p\, sin(\omega t + \phi) + \sum_{h=3,5} V_h\, cos\big(h\omega t + \phi_h\big), \tag{C.16}$$

where V_h respect the worst case of grid voltage harmonic according to standards.

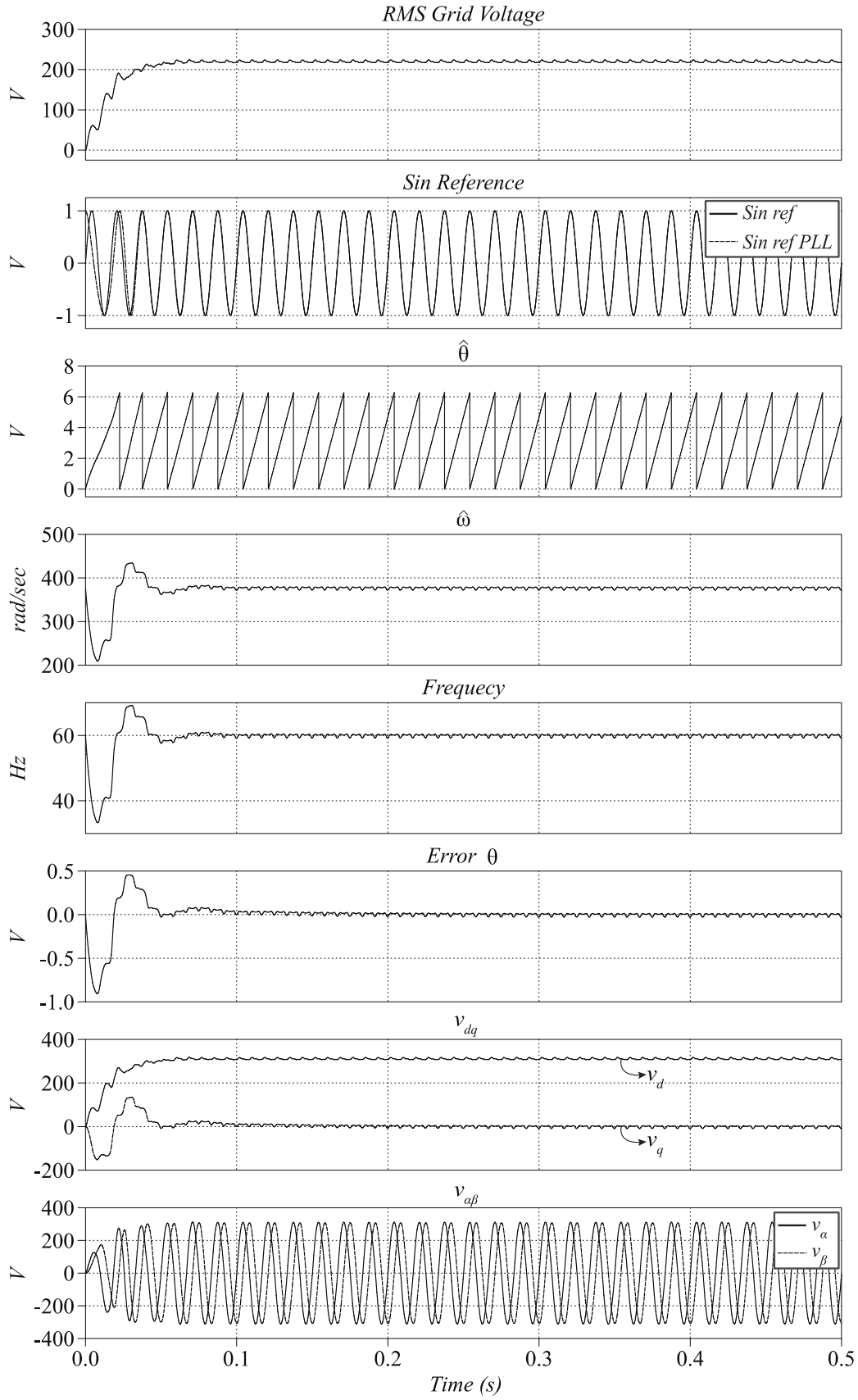
Figure C.12 presents the performance of the variables shown in Figure C.8, during the transient and steady-state intervals. Note that the PLL has a small frequency oscillation when v_g is submitted to harmonics disturbances. Such perturbations and high transients are easily transposed by enhanced SOGI harmonic filtering as previous mentioned.

The second scenario considers situations in which the PLL may be subjected, as: voltage sags; frequency variations; dc-bias. The PLL performance in such situations can be observed in Figure C.13.

In the first moment (t < 0.15 s), there is the nominal grid voltage with 311 peak voltage value and a 60Hz frequency, without DC bias. From 0.15 s < t < 0.3 s a small frequency perturbation is inserted, changing the grid frequency to a 58 Hz and returning to its nominal value in t = 0.3 s. In t=0.45 s occurs a voltage sag, dropping the voltage peak value to 200 V and returning to its nominal value in t=0.6 s. After, in t=0.75 s a 10 V DC bias is inserted to the grid voltage and removed after 0.15 s.

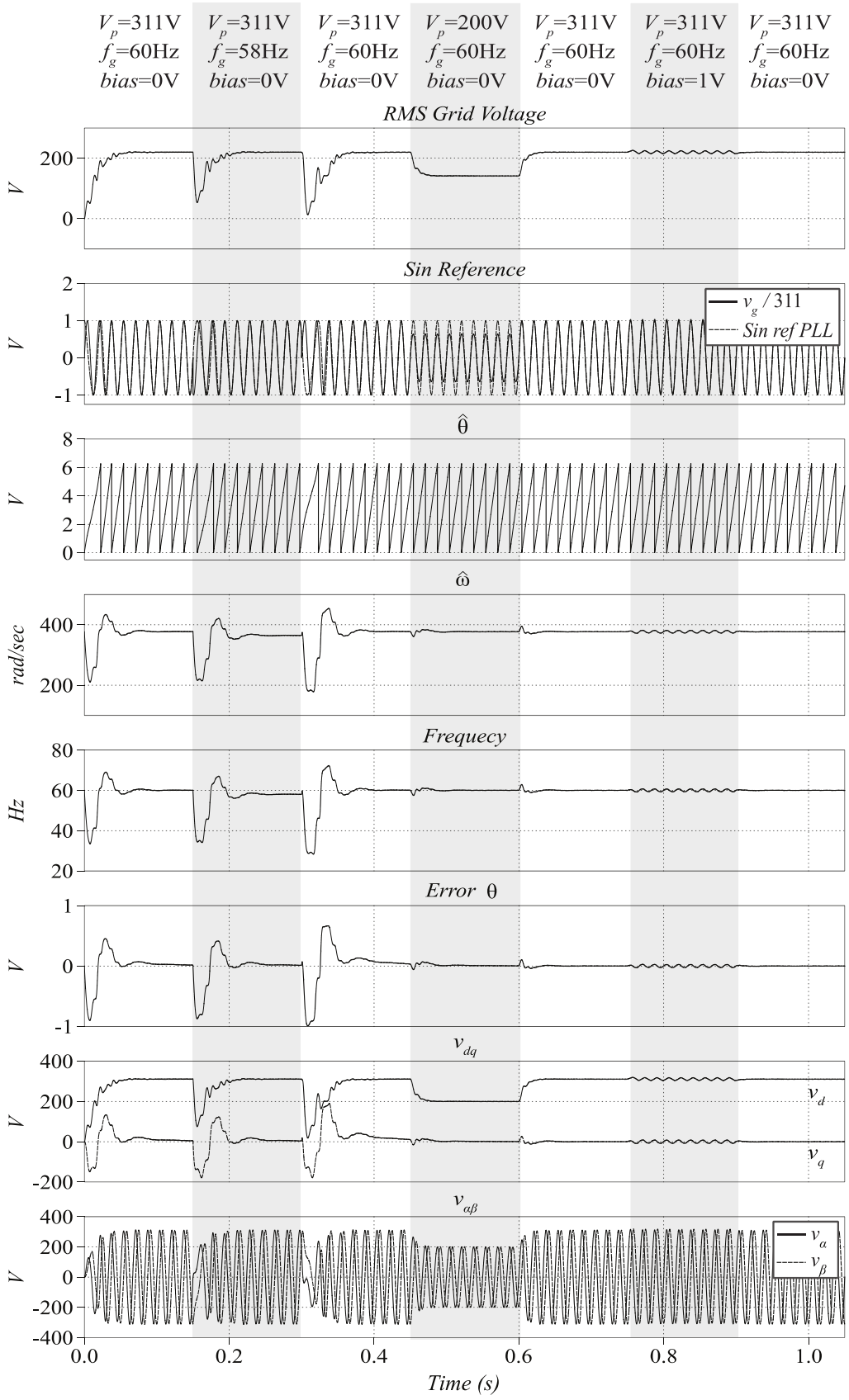
By analyzing Figure C.12 and C.12, which demonstrate the SOGI-SRF-PLL performance in a diverse environment of disturbance, it can be concluded that the PLL has great robustness despite its simple implementation. Note also the short period in which the PLL takes to reach the steady state, eliminating most of the disturbances arising from the grid voltage.

Figure 34 – SOGI-SRF-PLL performance when summited to vg with harmonics.



Source: prepared by the authors.

Figure C.13 – Some performance conditions of SOGI-SRF-PLL.



Source: prepared by the authors

APPENDIX D
CONTROLLERS DESIGN

CURRENT CONTROL

The specifications of the transient in time response can be transcribed in the frequency domain in terms of phase margin, gain margin, and bandwidth. These specifications can be easily read from the Bode diagram.

Through the analysis of the not compensated current Open-loop Transfer Function (OLTF), according to (D.1), it is possible to define the most suitable controller to be employed in the proposed application.

$$OLTF_{NC_i}(s) = k_{pwm} k_i G_{id}(s) \tag{D.1}$$

The choice for a PI controller comes from its good performance when working together with the feed-forward controller as previously explained. The PI transfer function had been previously presented.

Once the current controller has been defined, the current OLTF compensated is presented according to:

$$OLTF_{C_i}(s) = C_i(s) OLTF_{NC_i}(s) \tag{D.2}$$

By making *s*=jω and explaining (D.2) in terms of module and phase it is obtained:

$$\left|OLTF_{C_i}(j\omega)\right| = \left|OLTF_{NC_i}(j\omega)\right| k_{pi} \frac{\sqrt{\omega^2 + \omega_{zi}{}^2}}{\omega} \tag{D.3}$$

$$\angle OLTF_{C_i}(j\omega) = \angle OLTF_{NC_i}(j\omega) + atan\left(\frac{\omega}{\omega_{zi}}\right) - 90^\circ \tag{D.4}$$

The magnitude of transfer function, when it is at the cutoff frequency, presents a unitary gain according to equation (D.5). In contrast, the phase at the cutoff

frequency, corresponds to the phase margin required for the system output to undergo inversion. Thus, the phase margin is defined according to equation (D.6).

$$\left|OLTF_{C_i}(j\omega)\right|_{\omega=\omega_{ci}} = 1 \tag{D.5}$$

$$M_{\varphi_i} = 180 + \angle OLTF_{C_i}(j\omega)\Big|_{\omega=\omega_{ci}} \tag{D.6}$$

Replacing (D.3) and (D.4) in (D.5) and (D.6), respectively, it is obtained the equations set of (D.7).

$$\begin{cases} \left|OLTF_{NC_i}(j\omega_{ci})\right| k_{pi} \dfrac{\sqrt{\omega_{ci}{}^2 + \omega_{zi}{}^2}}{\omega_{ci}} = 1 \\ M_{\varphi_i} = 90^\circ + \angle OLTF_{NC_i}(j\omega_{ci}) + atan\left(\dfrac{\omega_{ci}}{\omega_{zi}}\right) \end{cases} \tag{D.7}$$

Performing the appropriate mathematical manipulations and isolating the necessary terms for the PI compensator design, the equations shown in (D.8), (D.9) are obtained:

$$k_{pi} = \frac{\omega_{ci}}{\left|OLTF_{i\_ncomp}(j\omega_{ci})\right| \sqrt{\omega_{ci}{}^2 + \omega_{zi}{}^2}} \tag{D.8}$$

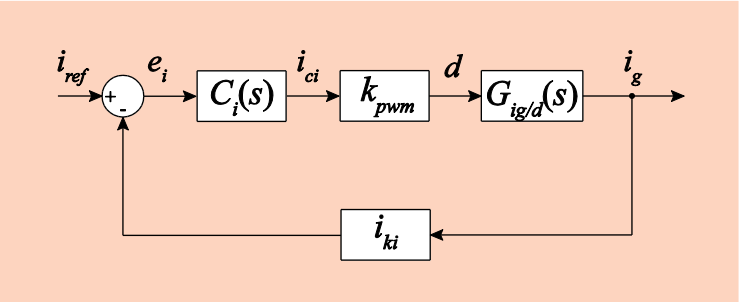
$$\omega_{zi} = \frac{\omega_{c_i}}{tan\left(M_\varphi - 90^\circ - \angle OLTF_{i\_ncomp}(j\omega_{ci})\right)} \tag{D.9}$$

VOLTAGE CONTROL

In order to simplify the voltage controller design and aiming to ensure that the voltage loop will not interfere in the current loop, the dynamic decoupling between both of them must be guaranteed, that is, the design of both must be at different cutoff frequencies, at least a decade away. As a result, the voltage loop (slow loop) sees the current loop (fast loop) only as a gain.

Such gain is determined by analyzing the current Closed-loop Transfer Function (CLTF). Analyzing the block diagram of Figure , the output current by the reference current transfer function can be obtained:

Figure A.1 – Simplified current closed-loop.



Source: prepared by the authors

$$\frac{i_g(s)}{i_{ref}(s)} = \frac{C_i k_{pwm} G_{ig/d}}{1 + C_i k_{pwm} G_{ig/d} i_{ki}} \tag{D.10}$$

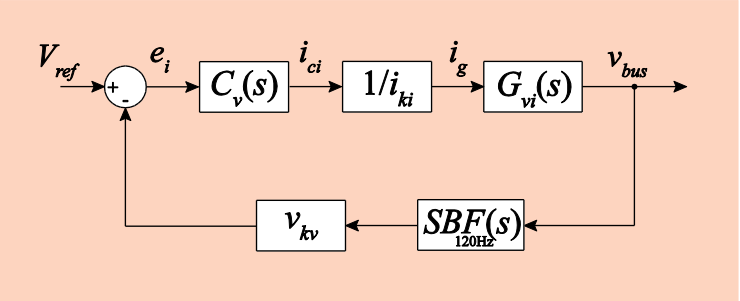
$$\frac{i_g(s)}{i_{ref}(s)} = \frac{k_{pi}\dfrac{(s+\omega_{zi})}{s}\dfrac{1}{V_{trip}}\dfrac{sC_dR_d+1}{s^4L_1L_2C_fC_dR_d + s^3L_1L_2(C_f+C_d) + s^2(L_1+L_2)C_dR_d + s(L_1+L_2)}}{1 + i_{ki}k_{pi}\dfrac{(s+\omega_{zi})}{s}\dfrac{1}{V_{trip}}\dfrac{sC_dR_d+1}{s^4L_1L_2C_fC_dR_d + s^3L_1L_2(C_f+C_d) + s^2(L_1+L_2)C_dR_d + s(L_1+L_2)}} \tag{D.11}$$

When $s \to 0$ (low frequencies), the result is the simplification of the internal current loop according to (D.12).

$$\frac{i_g(s)}{i_{ref}(s)} = \frac{Ek_{pi}\omega_{zi}}{k_i Ek_{pi}\omega_{zi}} = \frac{1}{i_{ki}} \tag{D.12}$$

Thus, the block diagram for the voltage loop is shown in Figure

Figure A.2 – Simplified voltage closed-loop.



Source: prepared by the authors

The voltage controller has similar design procedure, applying the same techniques in the frequency domain. The voltage OLTF not compensated (D.13) was obtained by the analysis of the simplified voltage loop block diagram (Figure).

$$OLTF_{NC_v}(s) = \frac{1}{i_{ki}} k_v G_v(s) \tag{D.13}$$

Using the same PI compensator duo its robustness and efficiency, the voltage OLTF compensated can be obtained according to:

$$OLTF_{C_v}(s) = C_v(s) OLTF_{NC_v}(s) \tag{D.14}$$

By the same analyzes applied in equations (D.3), (D.4), (D.5), and (D.6), the voltage controller set of equations is obtained:

$$\begin{cases} \left| OLTF_{NC_v}(j\omega_{cv}) \right| k_{pv} \dfrac{\sqrt{\omega_{cv}^2 + \omega_{zv}^2}}{\omega_{cv}} = 1 \\ M_{\varphi_v} = 90^\circ + \angle OLTF_{NC_v}(j\omega_{cv}) + atan\left(\dfrac{\omega_{cv}}{\omega_{zv}} \right) \end{cases} \tag{D.15}$$

The cutoff frequency for the voltage loop was designed to guarantee the dynamic decoupling between the loops and slow enough to attenuate low frequency harmonic oscillations. The phase margin, to guarantee the converter stability when operating in a closed-loop.

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ATTACHEMENT A

STANDARDS COMPARISON

Table 4 – Standards main items for grid-connected inverters.

	NBR16149:2013 BRA	IEEE1547:2003 USA	IEC61727:2004 Safety	VDE0126-1-1 GER
Odd Harmonics				
< 9º	< 4.0 %	≤ 4.0 %	< 4.0 %	3º – 3 A
11º to 15º	< 2.0 %	≤ 2.0 %	< 2.0 %	5º – 1.5 A
17ºto 21º	< 1.5 %	≤ 1.5 %	< 1.5 %	7º – 1.0 A
23º to 33º	< 0.6 %	≤ 0.6 %	< 0.6 %	9º – 0.7 A
> 35º	–	≤ 0.3 %	–	11º – 0.33 A 13º – 0.4 A
Even Harmonics				
2º to 8º	< 1.0 %	≤ 1.0 %	< 1.0 %	Even – 1.5 A
10º to 14º	< 0.5 %	≤ 0.5 %	< 0.5 %	> 40º – 4.5 A
16º to 20º	< 0.5 %	≤ 0.375 %	< 0.5 %	
22º to 34º	< 0.5 %	≤ 0.15 %	< 0.5 %	
> 36º	–	≤ 0.075 %	–	
Total Harmonics Distortion	< 5.0 %	≤ 5.0%	< 5.0 %	–
DC Current	0.5% – 1 s	0.5 %	1 %	< 0.22 A
Voltage Variation	V < 80 % - 0.4 s V > 110 % - 0.2 s	V<45% - 0.16s 45%< V <60% - 1s 60%< V <88% - 2s 110%>V>120% - 1s V > 120 % - 0.16s	V < 50 % - 0.1 s 50%<V<85% - 2 s 110%<V<150% -2s V > 150% - 0.05 s	V < 85% -0.2 s V >110% -0.2s
Frequency Variation	f < 57.5 Hz - 0.2 s f > 62 Hz - 0.2 s	f < 57 Hz - 0.16 s 57 < f < 59.3 - 0.2 s 60.5 < f < 62 - 2 s f > 62 Hz - 0.16 s	f < 57.5 Hz - 0.2 s f > 60.5 Hz - 0.2 s	f <47.5 Hz -0.2s f >50.2 Hz -0.2s

Source: prepared by the authors.

ATTACHEMENT B

STANDARDS COMPARISON

Table 5 – Individual voltage harmonic distortion (V ≤ 1 kV).

Odd not multiples of 3	**Harmonic Threshold**
5º	7.5 %
7º	6.5 %
11º	4.5 %
13º	4.0 %
17º	2.5 %
19º	2.0 %
23º	2.0 %
25º	2.0 %
> 25º	1.5 %
Odd multiples of 3	
3º	6.5 %
9º	2.0 %
15º	1.0 %
> 15º	1.0 %
Even	
2º	2.5 %
4º	1.5 %
6º	1.0 %
> 6	1.0 %

Source: [8].