Paulo Márcio Moreira e Silva

Contributions on the automatic tuning of *LC* networks using on-chip circuits

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Esta Tese foi julgada adequada para obtenção do Título de Doutor em Engenharia Elétrica e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina.

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RESUMO

Os sistemas de identificação por radiofrequência (RFID) têm sido usados em diversas aplicações incluindo localização de objetos, logística e localização. Além disso, eles têm sido considerados uma tecnologia facilitadora para a internet das coisas (IoT). Tanto o leitor quanto a tag de um sistema de RFID usam circuitos ressonantes que habilitam a comunicação entre eles. Entretanto, uma dessintonização entre esses circuitos ressonantes podem reduzir a distância de leitura ou até levar ao descarte da tag. Então, para resolver esse problema nós propomos novos sistemas de sintonia de redes LC que podem ser integradas em um chip RFID para sintonizar a tag automaticamente.

É possível sintonizar uma rede LC usando uma técnica de aumento do fator de qualidade como núcleo do sistema analógico de sintonia. Nesse sentido, um sintonizador de redes LC baseado em resistências negativas é descrito na tese. Um outro sintonizador basado em uma amostra da corrente de curto circuito do limitador de RF também é mostrado nessa tese. Pode-se dizer que os dois sintonizadores apresentados são complementares já que um sintoniza a rede LC baseado em tensão e o outro em corrente.

Também é possível sintonizar circuitos ressoantes quando sua resposta ao degrau é analisada. Dessa forma, nós propomos outro sistema que afere o Q do circuito ressonante e o quão sintonizado com o sinal de entrada esse circuito está.

Os sistemas propostos na tese são projetados usando processos CMOS com comprimento de canal de 130 nm e cada um deles ocupa uma área menor que 0.035 mm^2. Isso faz com que os protótipos apresentados sejam possíveis de serem integrados em um chip de RFID. Ao longo da tese são apresentados dois sintonizadores operando em 125 kHz e um extrator de parâmetros de redes LC operando em 900 MHz.

Palavras-chave: Sintonia LC. Sintonizador LC. Sintonizador LC com aumento do Q. Sintonizador LC integrado no chip. Circuitos LC. Circuitos de Sintonia. Extrator de parâmetros LC. Medida do Q. Medida da frequência de ressonância.

RESUMO EXPANDIDO

Introdução

Este estudo no ramo de testes envolvendo circuitos integrados, começou com uma interação com a CEITEC S.A., a qual é uma empresa brasileira que opera no ramo de semicondutores. Um dos principais interesses da CEITEC está no projeto de circuitos de RFID operando entre 134 kHz e 915 MHz.

Juntamente com a CEITEC foi possível simular e testar as etiquetas (*tags*) dessa empresa que operam em 134 kHz. Como conclusão desse estudo, foi visto que o sistema de RFID produzido pela CEITEC tem algumas particularidades que não permitem o uso de técnicas de sintonia automática previamente existentes. Dessa forma, foi concordado que seria interessante estudar e propor novas soluções que sintonizam automaticamente os circuitos ressonantes que estão presentes nas etiquetas de RFID.

Circuitos ressonantes são comumente usados em circuitos eletrônicos como osciladores, filtros, amplificadores, redes de adaptação e transmissores/receptores sem fio. Principalmente compostos por indutores (L) e capacitores (C), os circuitos ressonantes são usados por conta de seus efeitos observados na frequência de ressonância. Entretanto, um desvio no valor nominal de L e/ou C pode degradar o desempenho de circuitos que usam esse tipo de arranjo de circuito. As empresas que produzem circuitos RFID usam circuitos ressoantes com um fator de qualidade reduzido para contornar o problema de sintonia entre os componentes citados. Dessa forma, os efeitos da falta de sintonia do tanque LC é reduzido, mas a máxima distância de leitura também diminui.

São encontrados nesta tese dois sistemas de sintonia automática de circuitos ressonantes que resolvem o problema de sintonia de redes LC em circuitos de RFID. O primeiro sistema utiliza um núcleo de resistência negativa como parte principal do sistema analógico, pois é possível sintonizar uma rede LC utilizando esse tipo de circuito como é visto com mais detalhes no texto. Já o segundo sistema de sintonia proposto é baseado na corrente de curto-circuito do limitador de RF que é presente nas etiquetas de RFID. Baseado nessa corrente pode-se inferir quando a rede LC está sintonizada com o leitor de RFID.

Um extrator de parâmetros de redes LC também é proposto nesta tese. A motivação principal para esse trabalho é o seu uso em filtros LC ativos. Como normalmente resistências negativas são utilizadas para controlar a resposta em frequência desse tipo de filtro, faz-se necessário um sistema de controle que indique o valor equivalente do Q da rede e se ele deve ser aumentado/diminuído. Esse tipo de controle é necessário para manter o desempenho do filtro próximo ao projetado. Dessa forma, o extrator de parâmetros proposto detecta o Q de uma rede LC e se essa rede está sintonizada com o sinal de entrada.

Objetivos

Esta tese tem o principal objetivo de responder à seguinte hipótese: *é possível conceber novos circuitos de sintonia automática de redes LC, os quais minimizam a área integrada no chip, para serem integrados em um circuito RFID comercial.*

Metodologia

Para cumprir com o objetivo da tese, primeiramente os sistemas são concebidos a partir da necessidade de sintonia automática de redes LC. A partir daí, os projetos começam pela percepção física dos fenômenos que os permeiam. Após essa etapa, o sistema é simulado, validado e integrado em um *chip* para testes.

Com o intuito de aumentar a compreensão do tema pesquisado e a extensão desta tese, foi feito um estágio na forma de doutorado sanduíche na Universidade Carleton no Canadá.

Durante a fase de concepção e projeto dos sistemas descritos nesta tese, são consultados livros, artigos e patentes. Esse tipo de consulta permite melhor compreensão do tema abordado, como pode ser visto ao longo do texto.

Os resultados de toda tese são apresentados de forma quantitativa e contêm dados de simulação de circuitos e de testes com os *chips* projetados.

Resultados e Discussão

Podemos destacar e resumir as contribuições desta tese nos três projetos a seguir:

- Um sintonizador LC baseado em resistências negativas que tem o propósito de ser usado em aplicações de RFID operando em 125 kHz. Foi proposta uma nova aplicação para resistências negativas que reduz consideravelmente a complexidade do sistema de decisão de sintonia;
- Um sintonizador LC baseado na amostra da corrente de curto circuito do limitador de RF e uma diferente forma de escalar o circuito de comparação de corrente usada neste sintonizador;
- Um extrator de parâmetros de redes LC que reporta digitalmente o fator de qualidade e o valor de ressonância dessa rede. É proposto um novo método para medir o fator de qualidade da rede LC usando um capacitor adicional.

O sintonizador baseado em corrente foi concebido para suprir eventuais limitações impostas pelo sintonizador baseado em resistência negativa, o qual tem um limite de tensão de aproximadamente V_{DD} na rede LC.

O extrator de parâmetros apresenta o maior consumo entre os sistemas projetados (1.6 mA versus um consumo de corrente de $\cong 10\,\mu$A obtido nos outros projetos). Entretanto, ele trabalha em uma frequência mais elevada (900 MHz em contraste com a frequência de 125 kHz usada nos outros projetos) e tem a vantagem de reportar digitalmente o Q da rede LC e o quão próxima a frequência de ressonância da rede está do sinal de entrada. Essa característica faz esse sistema um bom candidato para implementação em sistemas de rádio definido por software.

Considerações Finais

A partir das motivações apresentadas neste breve resumo, foi possível conceber três novos sistemas para sintonia de redes LC. Dessa forma, o objetivo da tese foi cumprido. Assim, nota-se que a metodologia de pesquisa e as referências bibliográficas foram suficientes para realizar os procedimentos da tese. Como comentado anteriormente, várias contribuições para a comunidade científica foram feitas nesta tese, principalmente sobre sintonia de automática de redes LC de uma porta.

Palavras-chave: Sintonia LC. Sintonizador LC. Sintonizador LC com aumento do Q. Sintonizador LC integrado no chip. Circuitos LC. Circuitos de Sintonia. Extrator de parâmetros LC. Medida do Q. Medida da frequência de ressonância.

ABSTRACT

Radio-frequency identification (RFID) has been successfully used in many applications including object identification, logistics, localization and it has also been considered as an enabling technology for the Internet of things. Both the reader and the tag of the RFID system have a resonating network that enables data and energy communication. However, a mistuning of these resonating networks can either reduce reading range or lead to a disposal of the tag. Hence, to solve this problem we propose novel LC tuning systems that can be integrated on an RFID chip to automatically tune the tag.

It is possible to automatically tune LC networks using a Q-enhanced technique as the core of the analog tuning system. In this regard, one LC tuner based on negative resistances is described in the thesis. Moreover, it is possible to tune an LC network using a sample of the RF limiter current, that are present in RFID tags. It is possible to say that these tuners complement each other in the sense that the former system tunes its resonating network based on voltages, while the latter tunes its LC network based on currents.

It is also feasible to tune resonating circuits when their step response are analyzed. So we propose in this thesis another circuit that can measure the Q of its resonating network and also how close it is from the resonating frequency. This system digitally reports these parameters and it can also be used used in filters.

The systems are designed using a 130-nm CMOS process and they occupy an area smaller than $0.035\,\mathrm{mm}^2$, making the presented prototypes suitable for integration on an RFID chip. This thesis contains the two tuners that operate at 125 kHz and the LC parameter extractor operates at 900 MHz.

Keywords: LC tuning. RFID tunner. Q-enhanced LC tuner. On-chip LC tuner. LC circuits. Circuit tuning. LC parameter extractor. Q measurement. Resonance frequency measurement.

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ACRONYMS

C Capacitor. 17

I_{DS} Drain-to-source current [A]. 43

L Inductor. 17

M Mutual inductance. 19

Q Quality factor. 22

Q_r Detuned quality factor. 66

R_{DS} Drain-to-source resistance [Ω]. 43

R_{sh} Shunt resistance [Ω]. 43

ω Angular frequency [rad/s]. 20

f Frequency [Hz]. 20

g_m Transistor's transconductance [S]. 106

k Coupling factor. 20

I_D Drain to source current of the MOS transistor M [A]. 31

I_S Specific current of the MOS transistor M [A]. 31

I_T Tail current [A]. 30

U_T Thermal voltage [V]. 31

V_{TH} Threshold voltage of the transistor [V]. 31

δ_n Capacitance configuration. 28

ϕ Magnetic flux [Wb]. 19

n Slope factor of the transistor. 31

BiCMOS Bipolar complementary Metal-Oxide Semiconductor. 106

CCW Counter clockwise direction. 46, 47

CMOS Complementary Metal-Oxide Semiconductor. 18, 27, 34, 36, 42, 43, 50, 53, 59, 90, 95, 99

CW Clockwise direction. 46, 47

DUT Device Under Test. 67

MTPT Maximum power transfer point. 27

PDK Process Development Kit. 61, 103

RF Radio Frequency. 18, 41–44, 65, 84–86, 91

RFID Radio frequency identification. 17–20, 24, 25, 27, 32, 36, 39, 41–43, 97–100

RTD Resonant Tunneling Diode. 105

TD Tunneling Diode. 105

VGCA Variable-gain current amplifier. 41, 45, 48, 59

WTA Winner take all. 41, 50, 51, 56, 59

CONTENTS

1 INTRODUCTION

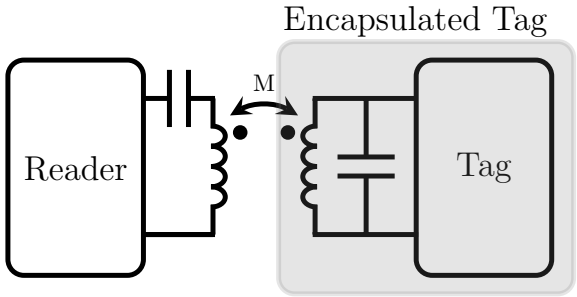
1.1 RESEARCH MOTIVATION

This study, in the field of integrated circuit testing, started with an interaction with CEITEC S.A., which is a Brazilian semiconductor company. One of Ceitec's main interest is the design of RFID circuits operating from 134 kHz to 915 MHz [1]. We had some meetings at CEITEC and we were able to simulate and test their RFID tag that operates at 134 kHz. We (the Ceitec's engineers and the author) found that their RFID systems have some particularities that do not allow the use of the existing automatic tuning techniques. Then, we agreed that it would be interesting to study and propose new solutions to automatically retune tuned circuits that are present on RFID tags.

The roots of radio-frequency identification (RFID) can be traced back to World War II. The Germans and the Allies were using radars to warn of approaching planes while they were miles away. The problem was to identify which planes belonged to the enemy. The Germans discovered that if the pilots rolled their planes as they returned to base, it would change the radio signal reflected back. Then, this action alerted the radar crew that these were German's planes [2].

Nowadays, RFID has been successfully used in many applications including object identification, logistics, localization and it has also been considered as an enabling technology for the Internet of things (IoT) [3]. A typical RFID system is composed of a reader device and semi-passive or passive tags (transponders), as seen in Fig. 3.1. Passive tags harvest energy from the electromagnetic field generated by the reader device to power a circuit that reads an identification code stored in read-only memory (ROM). The efficiency of the power harvesting is strongly dependent on the impedance matching between the electromagnetic transducer and the harvesting circuit. In near-field systems, the former is basically comprised of a high-quality factor LC network that enables the communication with the harvesting circuit.

Figure 1.1: Block diagram of an RFID system emphasizing the tag and its magnetic coupling with the reader.



Source: The author.

These resonating circuits are commonly used in electronic circuits such as oscillators, filters, amplifiers, matching networks, and wireless transmitters/receivers. Mainly composed of inductors (L) and capacitors (C), they are used because of their resonance effects. However, a deviation from the nominal value of L and/or C, can degrade the performance of the circuits that use these resonant circuits. To circumvent the problems of the aforementioned mistuning, the companies that produce the RFID tags use resonating circuits with a reduced quality factor. By doing this, the mistuning effects of an LC tank is reduced, but the maximum reading distance decreases.

Since tags usually contain a chip with a stored identification code, it is possible to formu-

late the hypothesis of this thesis as:

Hypothesis 1 (H1): *It is possible to conceive novel LC network tuning systems, that minimizes the required on-chip area, to be integrated on a commercial RFID chip.*

Thus, in this work we propose built-in self-repair (BISR) systems for tuning resonating networks.

The reader will see that we also worked with an LC parameter extractor. The presented system was conceived while I was in an internship at Carleton University, under the supervision of professor Calvin Plett. In the electronics group of that university, one PhD candidate was working with a single-ended on-chip multi-band bandpass filter operating at 900 MHz and 2.4 GHz. This filter was built in a CMOS process and it uses LC networks to implement its bandpass frequency response. With the physical insights that we obtained with the design of the LC tuners, it was possible to propose a system to measure the quality factor of this LC filter.

1.2 STRUCTURE OF THE THESIS

The remainder of this thesis is structured as follows:

- In chapter 2 it is presented a review of magnetic coupling between two coils, a circuit analysis of an RFID system, and some patents and papers on RFID tuning. The concepts and equations regarding LC circuits that are shown in this chapter are used throughout the thesis.
- An LC tuner based on negative resistances is presented in chapter 3. In this chapter we show the concepts of this tuner and we show how to the control the negative resistance value over a wide voltage range. The chapter finishes with the measurements results of a prototype that was built using a 130-nm CMOS process.
- Another LC tuner based on a sample of the short-circuit current that flows through the RF limiter is shown in chapter 4. Along the chapter, the circuits that compose the tuner and their simulated results are shown. The chapter finishes with the measurement results of a prototype built using a 130-nm CMOS process.
- We present, in chapter 5, an LC parameter extractor. This system can be used for tuning RFID circuits, but it was originally conceived for tuning Q-enhanced LC networks, as explained in the chapter. Throughout the chapter it is seen that the parameter extractor is conceived based on a transient analysis of the LC network. This chapter finishes with the LC parameter extractor designed using a 130-nm CMOS process and its measurement results.
- Lastly, in chapter 6, we finish the thesis comparing the designed tuners, we give the summary of contributions of the thesis, and we propose possible future works.

2 BASIC PROPERTIES OF *LC* NETWORKS AND AUTOMATIC TUNERS

As mentioned in chapter 1, *LC* networks are extensively used in electronic circuits and they are the main subject of the thesis. Hence, we review in this chapter some basic properties of these networks, that are used along this work. This chapter also presents some existing methods for tuning resonating circuits that are used in RFID applications.

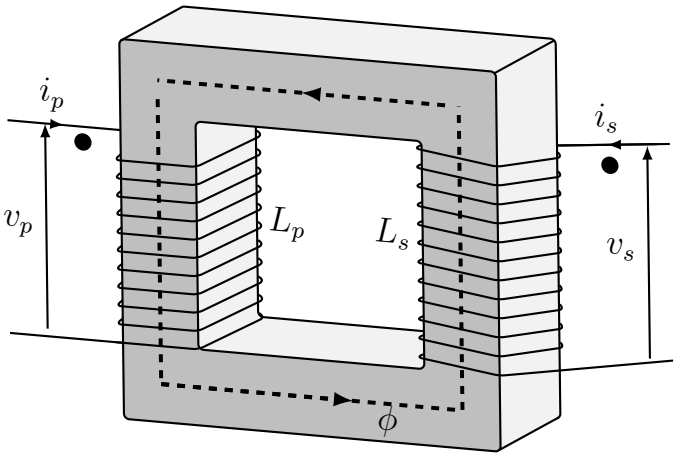
2.1 MAGNETICALLY COUPLED COILS

Ampère's law predicts that the flow of electric current creates a magnetic field. If this field is time-varying and if it links an electric circuit, Faraday's law predicts the creation of a voltage within the linked circuit. Then, using the circuit of Fig. 2.1, we consider that the magnetic field, represented by the magnetic flux ϕ, is produced by a current source with output current equal to i_p. We note that ϕ links the second coil, then v_s is induced. From Faraday's law and considering that L_s is not connected to a current source, v_s is calculated by:

$$v_s = M\frac{di_p}{dt}, \tag{2.1}$$

where M is defined as the mutual inductance.

Figure 2.1: Two magnetically coupled coils.



Source: The author.

If a second current source with output current equal to i_s is connected to the terminals of L_s, both currents i_s and i_p contribute to ϕ. For the shown configuration in Fig. 2.1, we have that [4]:

$$v_p = L_p\frac{di_p}{dt} + M\frac{di_s}{dt} \tag{2.2}$$

and

$$v_s = L_s\frac{di_s}{dt} + M\frac{di_p}{dt}. \tag{2.3}$$

Using Laplace transform:

$$V_p = sL_pI_p + sMI_s \tag{2.4}$$

and

$$V_s = sL_sI_s + sMI_p, \tag{2.5}$$

where $s = j\omega$. By its turn ω is known as the angular frequency and it is equal to $2\pi f$, where f is known as the frequency.

The mutual inductance can also be written as:

$$M = k\sqrt{L_p L_s}, \tag{2.6}$$

where k is known as either the coupling factor or coefficient of coupling. k lies between 0 and 1. If k is 0, there is no flux linkage between the coils and $M = 0$. When $k = 1$, all the flux that links L_p also links L_s and M is maximum. A $k \cong 1$ is usually seen in transformers and it is due to their cores that are made of magnetic materials. On RFID applications, k can easily be smaller than 0.1 and it depends on the distance between the tag and the reader, and on the geometry of the coupling coils.

The dots that are drawn in Fig. 2.1 are not required when the winding configuration is shown. However, to simplify the schematics, the dot convention is used and the symbol M should be drawn wherever there is a magnetic coupling. Using the dot convention, we can say that when a current enters the dotted terminal of a coil, it produces a voltage in the coupled coil which is positive at the dotted terminal.

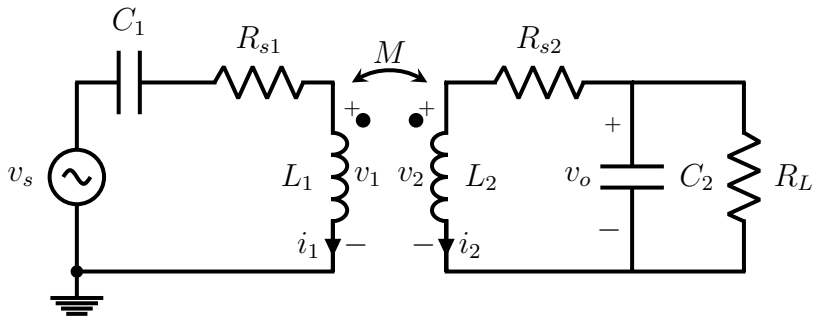
2.2 RESONATING *LC* NETWORKS

We start the analysis of resonating LC networks with the circuit of Fig. 2.2, which can be associated to a typical RFID system that uses magnetic coupling. In RFID, the RLC series circuit, shown in Fig. 2.2, is known as the reader. The circuit that is magnetically coupled with the reader is known as either the transponder or the tag. Analyzing the reader side, v_s can be calculated as:

$$v_s = i_1\left(R_{s1} + \frac{1}{j\omega C_1} + j\omega L_1\right) + j\omega M i_2. \tag{2.7}$$

This series resonant circuit operates at its resonating frequency, thus $j\omega L = -1/(j\omega C_1)$. By doing this, i_1 and the voltage induced on L_2 are maximized.

Figure 2.2: Example of resonating LC networks.



Source: The author.

By its turn, i_2 can be equated as:

$$i_2 = \frac{-v_2}{j\omega L_2 + R_{s2} + \frac{R_L}{1+j\omega R_L C_2}} = \frac{-j\omega M i_1}{j\omega L_2 + R_{s2} + \frac{R_L}{1+j\omega R_L C_2}}. \tag{2.8}$$

Then, using (2.7) and (2.8), the impedance seen from v_s can be found as:

$$Z_s = \frac{v_s}{i_1} = R_{s1} + \frac{\omega^2 M^2}{j\omega L_2 + R_{s2} + \frac{R_L}{1+j\omega R_L C_2}} = R_{s1} + \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + R_{s2} + \frac{R_L}{1+j\omega R_L C_2}}. \tag{2.9}$$

The parameters of the coupled circuit modify the impedance seen by v_s, as it is shown in (2.9). Thus, the tag's data can be passed to the reader by modifying one parameter of the second term of (2.9). We note that it is more common to modify the load resistance (R_L) by placing a switch, that closes and opens depending on the data, in parallel with it. This kind of data transmission is known as load modulation and it is a usual procedure for communication between the tag and the reader [5].

Now, taking the tag side of the presented LC network in Fig. 2.2 we have that the voltage on the load can be calculated as:

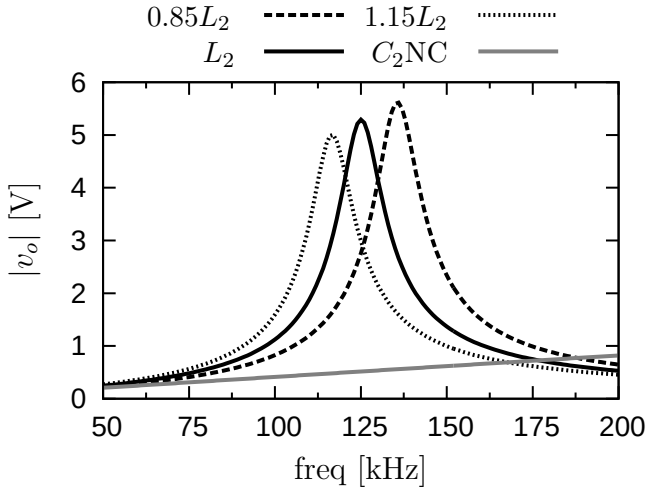
$$v_o = -i_2 \frac{R_L}{1 + j\omega R_L C_2}. \tag{2.10}$$

Using (2.8) we have that:

$$v_o = \frac{j\omega k\sqrt{L_1 L_2} i_1}{1 + \left(\frac{1}{R_L} + j\omega C_2\right)(j\omega L_2 + R_s)}. \tag{2.11}$$

$|v_o|$ reaches its maximum value when $\omega = \omega_0 = 1/\sqrt{L_2 C_2}$. Eq. (2.11) is plotted for different values of L_2 in Fig. 2.3. For this figure we used that: $L_1 = L_2 = 6.6\,\text{mH}$; $k = 0.01$; $i_1 = 10\,\text{mA}$; $C_2 = 1/\left[4\pi^2(125 \times 10^3)^2 L_2\right] = 245\,\text{pF}$; $R_s = 60\,\Omega$; and $R_L = 60\,\text{k}\Omega$.

Figure 2.3: Frequency response of $|v_o|$ for different values of L_2. It is also seen the frequency response of $|v_o|$ considering that C_2 is not connected (C_2NC).



Source: The author.

From Fig. 2.3, we note that L_2 resonates with C_2 at 125 kHz, because the obtained value of C_2 resonates with L_2 at this frequency. If the reader has a fixed current frequency of 125 kHz, we see that the LC networks with either $0.85L_2$ or $1.15L_2$ have a smaller $|v_o|$ at the reader frequency. Then, it is possible to conclude that as a result of variations around the nominal values of the passive devices, the mistuning of the LC networks may significantly degrade the circuit's required performance. For instance, in RFID applications, where both the reader and

the transponder have an LC network to enable data and energy communication, the network mistuning can reduce the reading range.

It is also plotted in Fig. 2.3, the frequency response of $|v_o|$ when C_2 is not connected (C_2NC). In this case $|v_o|$ is close to 0.5 V at 125 kHz, which is lower than the diode turn-on voltage.

It is possible to estimate the attenuation of k when the distance between the coils ($L1$ and $L2$) increases. For two parallel conductor loops the coupling coefficient can be approximated as [5]:

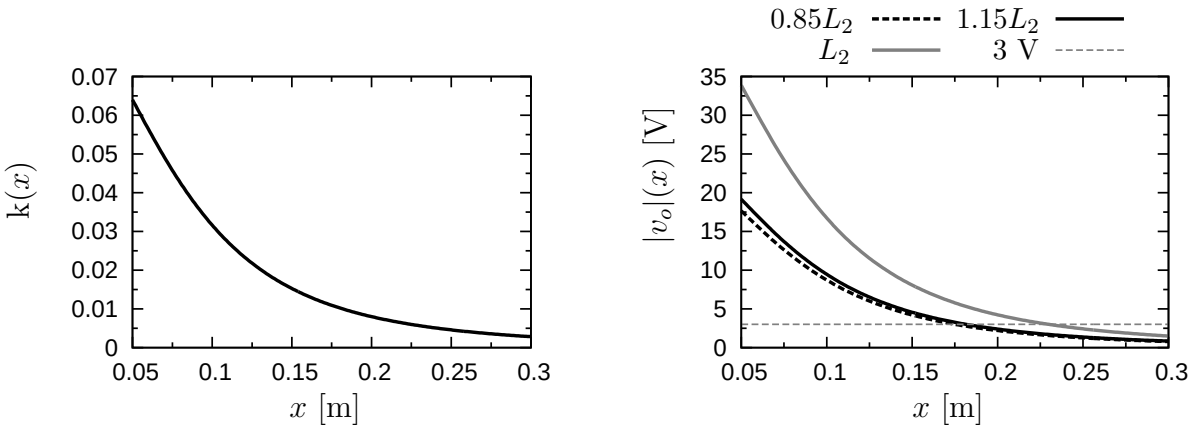
$$k(x) \cong \frac{r_{tag}^2 r_{reader}^2}{\sqrt{r_{tag} r_{reader}} \left(\sqrt{x^2 + r_{reader}^2}\right)^3}, \tag{2.12}$$

where x is the distance between the inductors whilst r_{tag} and r_{reader} are the radii of the tag and reader coils, respectively.

To illustrate the behavior of $k(x)$, (2.12) is plotted in Fig. 2.4(a) using $r_{tag} = 10$ cm and $r_{reader} = 2$ cm, which are generic values.

With the values used to plot Fig. 2.3, but using the obtained $k(x)$, we plot $|v_o|(x)$, at 125 kHz, in Fig. 2.4(b) for three values of L_2. Considering that the tag operates when $|v_o| > 3$ V and with the nominal L_2, a maximum reading distance equal to 23 cm is obtained. This distance decreases to $\cong$ 18 cm for the mistuned LC networks, as seen in Fig. 2.4(b). Hence, if a maximum reading distance higher than 20 cm is specified by the costumer/standard, these mistuned tags can not be sold. Then, it is the manufacturer decision to either discard the faulted tag or implement an automatic tuning system to compensate the observed mistuning effects on the tag that will be sold.

Figure 2.4: (a) $k(x)$ for two magnetically-coupled coils. (b) $|v_o|(x)$ considering different values of L_2.



(a) (b)

Source: The author.

2.3 QUALITY FACTOR (Q)

The quality factor Q of a passive circuit is generally defined as 2π times the ratio between the stored energy in the network and the energy dissipated per cycle by damping:

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy dissipated per cycle}}. \tag{2.13}$$

The Q can be measured by applying a step input and observing the decay of oscillations at the output, as it is well observed in [6]. The reader will note that we use this property in chapter 5

to extract the Q of an LC network.

Another useful way to estimate Q is to measure the impedance magnitude $|Z|$ of the resonating circuit in the frequency domain. The frequency response of $|Z|$ around ω_0 can be modeled as [7]:

$$|Z(\omega)| = \frac{Z_0}{\sqrt{1 + \left(\frac{2Q\Delta\omega}{\omega_0}\right)^2}}, \tag{2.14}$$

where Z_0 is the peak of $|Z(\omega)|$ and $\Delta\omega = \omega - \omega_0$. If $|Z|$ is replaced by $Z_0/\sqrt{2}$ in (2.14), Q can be written as:

$$Q = \frac{\omega_0}{2\Delta\omega_{-3\,dB}}, \tag{2.15}$$

where $\Delta\omega_{-3\,dB}$ is the frequency shift that sets $|Z| = Z_0/\sqrt{2}$. We note that (2.15) is a very useful and simple equation. It can be used to measure the Q of resonating circuits, as long as the -3-dB bandwidth have a symmetric behavior around ω_0. However, if the inductor of the LC network is removed, this definition can not be used.

In a third definition of Q, it can be shown that for an RLC network [8]:

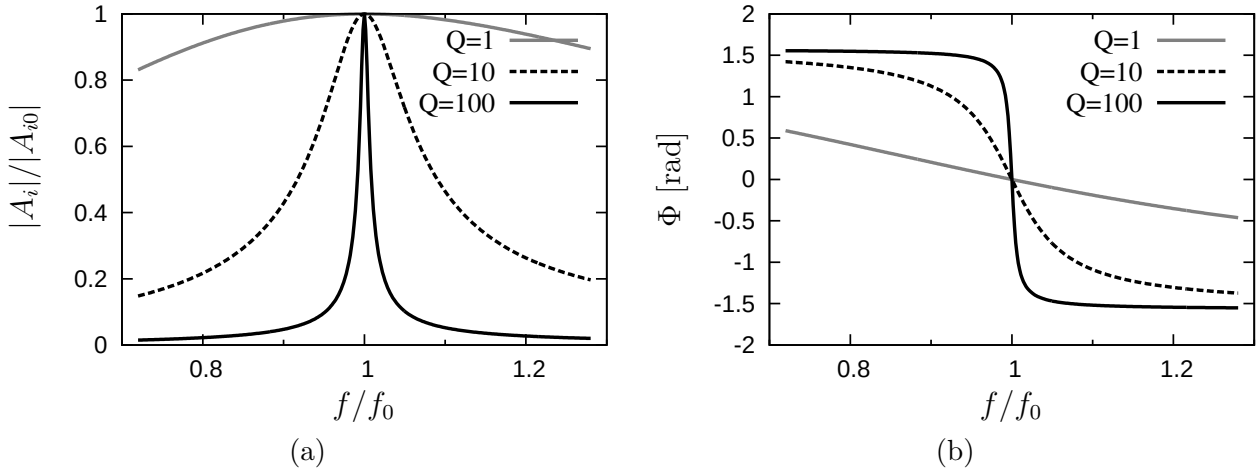
$$Q = \frac{\omega_0}{2}\frac{d\Phi}{d\omega}, \tag{2.16}$$

where $d\Phi/d\omega$ is the slope of the phase of the transfer function of the RLC network with respect to frequency.

Fig. 2.5 can be used to illustrate the two latter concepts of Q. In Fig. 2.5(a), we note that as Q increases, the bandwidth of the curve within 0.707 of gain decreases. It is possible to apply this concept on resonating filters, because their selectivity can be controlled by changing their Q. The reader will note that the tuner conceived in chapter 3 is based on this property.

It can be noticed in Fig. 2.5(b) that the slope of Φ increases with Q. If the frequency of an oscillator deviates from ω_0 when Q is high, there is a significant change in the phase shift. This shift violates the condition of oscillation and the frequency is forced to return to f_0. Hence, the Q can also be seen as how much a closed-loop system opposes to variations in the oscillation frequency [6].

Figure 2.5: (a) Frequency response of the current gain of a parallel RLC network normalized by its maximum amplitude and (b) phase of the current gain transfer function, for different values of Q.

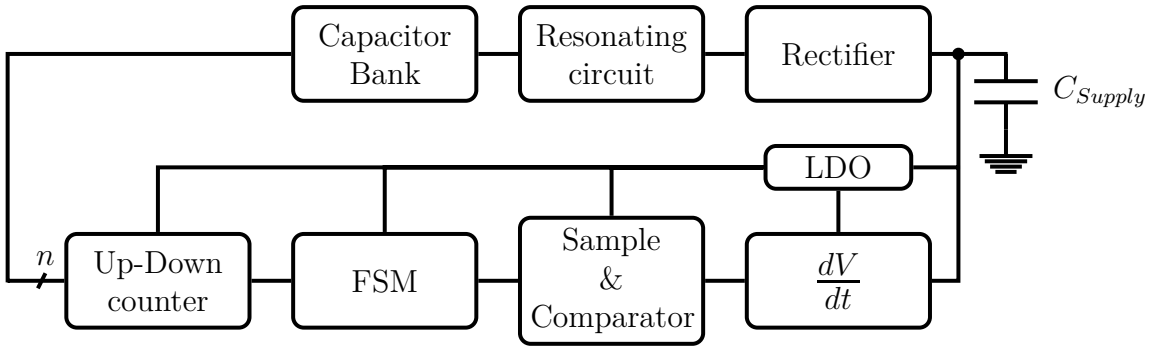


Source: The author.

2.4 AUTOMATIC RFID TUNERS

A control loop that tunes the resonating circuit is shown in [9]. This system uses a counter that enables/disables capacitances of a capacitor bank using n bits, as seen in Fig. 2.6. This tuning method requires that the AC voltage on the resonating circuit is rectified and stored using C_{supply}. The voltage slope of this capacitor is compared by the "sample & comparator" block with a previous sample. Then, this block determines if the voltage slope has increased or decreased. This information is passed to a finite state machine (FSM) that decides if the counter has to increase/decrease its output value.

Figure 2.6: A tuner based on the slope voltage of C_{supply}.



Source: From [9].

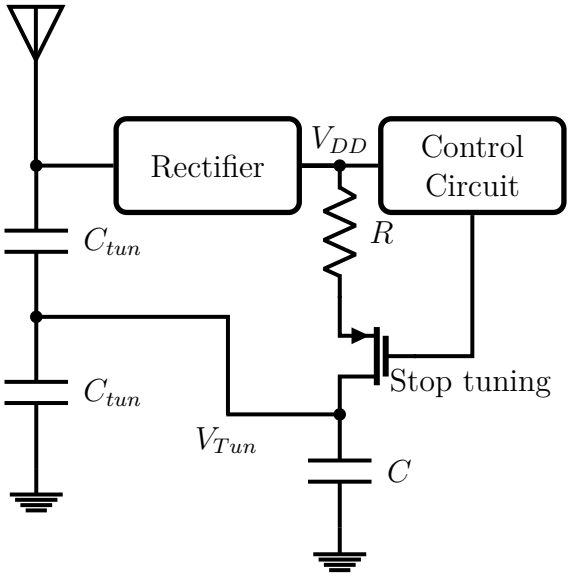
In [10] we can find a generic tuner. It is intended to tune its resonating circuit when a variable impedance is adjusted. In this patent the authors propose to detect either voltage or power of the resonating circuit. With this information they propose to control a variable impedance and retune the resonating circuit.

It is presented in [11] an automatic tuner for UHF RFID tags. This tuner uses a variable capacitor C_{tun} to tune the resonating circuit, as seen in Fig. 2.7. When the circuit is being powered up, V_{DD} rises. Then, if the RC constant is high enough, V_{Tun} can properly control the input impedance of the resonating circuit. The control circuit stops the tuning when V_{DD} is above a threshold level and the system is considered tuned. By doing this, the tuner does not look for the resonant frequency of the tag, but it searches for the capacitance configutation that turns on the tag.

If C_{tun} increases its capacitance with V_{Tun}, the resonant frequency of the tag has to be in a frequency that is higher than the incoming signal frequency. So, when the signal arrives, V_{Tun} increases and the resonant frequency decreases. The authors of [11] present some problems of their implemented controller, when the tuner either comes or goes away from the reader. Maybe due to these issues, these authors did not continue with this research of automatic tuners, as concluded from what is published by the authors.

In [12] we see a patent that claims to tune an RFID system in different UHF operating frequencies. The antenna is divided into segments and each segment represents one resonant frequency. Then, the tuning occurs when the length of the antenna is modified by severing it in one segment point. This method seems to be very expensive and not accurate enough. The authors claim that an example of operating frequency range would be from 868 MHz to 950 MHz. An antenna with equivalent inductance of 10 nH needs a varicap (or a capacitor bank) that is adjustable from 2.8 pF to 4 pF to resonate at that bandwidth. This capacitance range is relatively not significant and can be integrated on chip, so another non-evasive tuning method can be used.

Figure 2.7: Block diagram of the tuning system proposed in [11].



Source: From [11].

2.5 SUMMARY

In this chapter some basic properties of magnetically coupled coils and its application on RFID circuits are reviewed. We also calculated that a deviation on the value of the tag's inductor can decrease the induced voltage at the reader frequency. The main definitions of Q that are relevant for this thesis are seen in this chapter. We presented that the Q:

- can be measured by applying a step input and observing the decay of oscillations at the output;
- can be viewed as how selective a bandpass filter is;
- controls the slope of the phase of the transfer function of the RLC network;

There are other ways to view the Q, as the interested reader can see in [7].

We also presented some existing automatic RFID tuners. The reader noted that they are mainly based on a rectified voltage (or on the power) of the induced voltage on the RFID tag. This kind of solution may lead to high area circuits [1] and/or higher complexity searching algorithms.

[1]This is an assumption based on the diagrams shown by the authors. The implemented area is not mentioned in none of the RFID tuners.

3 LC TUNER BASED ON NEGATIVE RESISTANCES

It is possible to automatically tune LC networks using a Q-enhanced technique as the core of the analog tuning system. In this regard, we describe herein the design of an LC tuner based on negative resistances suitable for RFID applications. In this chapter we introduce the conceived LC tuning technique and show how the equivalent quality factor of the LC network is controlled over different voltage levels. We integrated the tuner prototype in a standard 130-nm CMOS process using an active area of $150\,\mu\text{m} \times 150\,\mu\text{m}$. Its performance was validated using off-the-shelf components that emulate the resonating circuits of an RFID system.

3.1 INTRODUCTION

A great challenge in the RFID industry is to produce very low cost tags and this demand has consequences in all production steps. For instance, mistuning of the input LC network may lead to the disposal of the tags. Even for highly tuned processes, with low rejection rates, the losses are not negligible, since millions of tags are produced and their price is at the level of cents.

Solutions for tuning the LC network of RFID circuits have been proposed in [9, 10] as seen in chapter 2. In both citations, an auxiliary circuit was used to find the maximum power transfer point (MTPT) at which the tank should be tuned. The MPTP searching circuit sweeps a bank of capacitors starting from an initial value and it stops after the received power starts to decrease. These tuning techniques require the use of an algorithm that searches for the MPTP and this adds area to the digital controller. A technique to keep the reader-tag system tuned is proposed in [13], in which the resonance frequency of the system is tuned with the aid of an electrically tunable inductance. This allows real-time tuning, but it has the drawback of requiring the retuning of the reader before interacting with a new tag.

LC tuning techniques have also been used for different applications, such as filters, in which tuning both the center frequency and the bandwidth are of importance. In [14] the authors use an auxiliary LC structure, which can be named as a master structure, to tune the filter center frequency and a negative resistance to adjust its bandwidth (Q). In [15], the authors presented an LC filter with automatic Q tuning, achieved by controlling the bandwidth with the aid of a negative resistance. These LC tuning techniques require an analysis of the input and output signals of the filter (or of the master structure) and both are not usually present in RFID tags.

To circumvent the aforementioned drawbacks of the LC tuners, we report in this chapter the design of an integrated circuit (IC) for tuning LC circuits, based on the technique presented in [16]. This technique, in contrast to [14] and [15], can be applied to one-port networks where the input and output are not simultaneously available. In this method, we artificially increase the quality factor of the LC network and analyze the voltage on its terminals to determine its resonating frequency. The circuit is implemented using a current-controlled negative resistance, a bank of capacitors and auxiliary circuits. The IC was laid out in a standard 130-nm CMOS process. Its performance was verified by connecting it to an off-the-shelf LC network that is magnetically coupled with a 125-kHz RFID antenna.

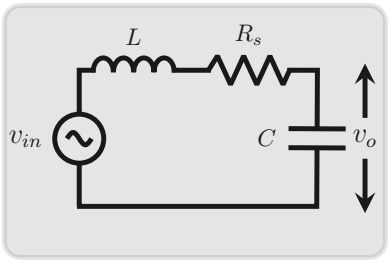
This chapter is structured as follows. In Section 3.2 we briefly review the tuning technique. The architecture of the tuning system is presented Section 3.3 with emphasis on the design and control of negative resistance, used to enhance the quality factor of the LC network, at different voltage levels. The simulation and measurement results are reported in Section 3.5. Lastly, the conclusions are given in Section 3.6.

3.2 PROPOSED TUNING METHOD

The induced voltage (v_{in}) on the tag can be represented as a voltage source connected in series with the RLC network, as seen in Fig. 3.1. The total losses of the system can be represented by R_s and the transfer function between the voltage on the capacitor (v_o) and v_{in} can be equated as:

$$H(s) = \frac{v_o}{v_{in}}(s) = \frac{1}{sC(sL + R_s) + 1}. \tag{3.1}$$

Figure 3.1: Equivalent RLC circuit of the tag seen by the induced voltage v_{in}.



Source: The author.

We consider that the nominal value of R_s is equal to R_{sn}, and that:

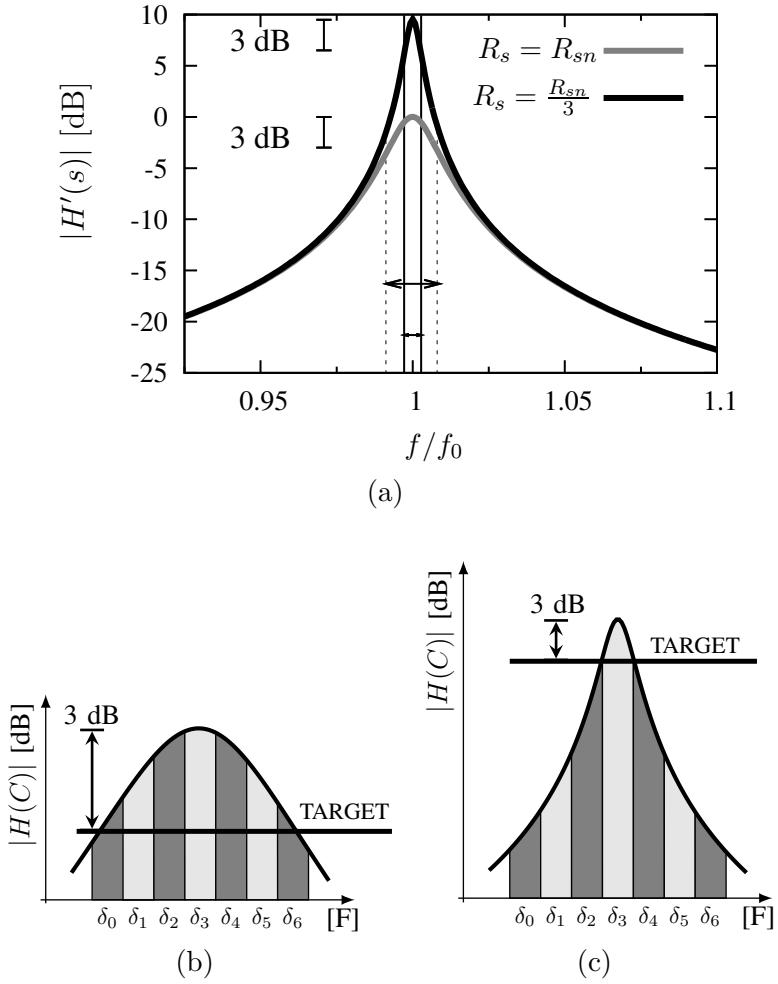
$$H'(s) = \frac{H(s, R_s)}{H\left(s, R_{sn}\right)\Big|_{s=j\omega_0}}, \tag{3.2}$$

where ω_0 is the resonance frequency of the LC network ($\omega_0 = 1/\sqrt{LC}$). Then, $|H'(s)|$ is plotted in Fig. 3.2(a) for two R_s values: one with R_{sn} and another with $R_{sn}/3$. On comparing the plotted curves, we note a significant increase in $|H'(s)|$ ($\cong 10\,\text{dB}$) when $R_s = R_{sn}/3$ at the resonance frequency ($f/f_0 = 1$). We also note, that when R_s decreases, the 3-dB bandwidth is decreased by the same amount.

Now, using the circuit of Fig. 3.1, we consider that: this circuit can be tuned when its equivalent capacitance C is changed; C belongs to a likely capacitance region represented by δ_n ($n = 0, 1, ..., 6$); and the frequency of v_{in} is fixed. Using these premises, we plot the response of $|H(C)|$ in Figs. 3.2(b) and 3.2(c) for a relatively low and high Q, respectively. If we draw a target line 3 dB below the peak of these curves, it can be noted that several capacitance regions are above this line in Fig. 3.2(b). However, if the procedure is repeated for the high Q network, only one capacitance region, named δ_3, is above the target line. Thus, with the aid of the target line, we can say that any capacitance value belonging to δ_3 tunes the LC network in the latter case.

Using the previous example, it can be concluded that we can tune an LC network when we increase its quality factor and determine whether or not the voltage on its terminals has reached a certain target voltage.

Figure 3.2: (a) $|H'(s)|$ considering two values of R_s. $|H(C)|$ for different capacitance regions (δ) with a relatively low and high Q in (b) and (c), respectively.



Source: The author.

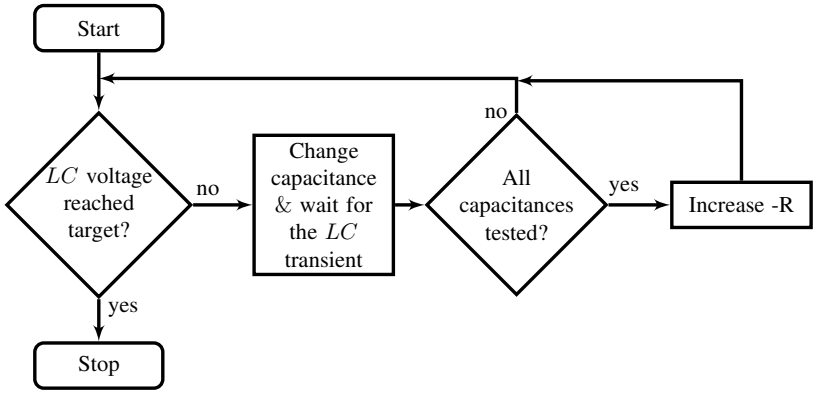
3.3 PROPOSED ARCHITECTURE

The proposed tuning method increases the quality factor of the LC network using a negative resistance, which is connected in parallel with the inductor. The tuning system enables the negative resistance, sweeps the equivalent capacitance of the LC network and determines if the resonant circuit is tuned based on a predetermined voltage target. If the target is not reached during the capacitance sweeping, the negative resistance is increased and the tuning process is repeated. This tuning procedure can be summarized with the flowchart shown in Fig. 3.3.

This solution is not based on large area circuits, since it requires one circuit to increase the input quality factor, a voltage detector, a controller, a reference signal source, and a counter, which is connected to the capacitor bank and to the negative resistance, as seen in Fig. 3.4(a).

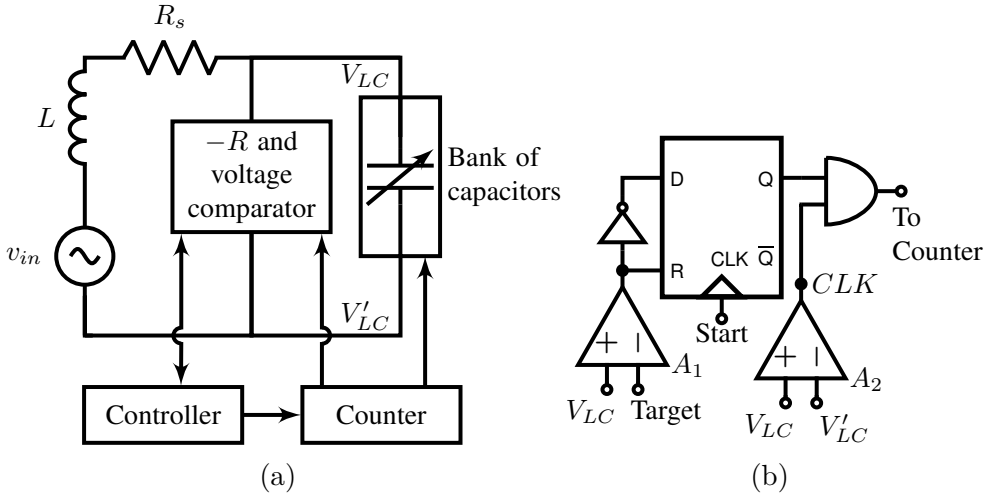
In Fig. 3.4(b) the implemented voltage comparator and the controller can be observed. We use this voltage comparator to define when the LC voltage (V_{LC}) is higher than the target voltage. The output of this comparator is connected to a digital controller that stops the tuning process if the voltage on the LC tank is higher than the target voltage. This controller is composed of a D flip-flop that receives, at its clock input, a 'start' signal that begins the tuning sequence. After a positive edge of the start signal, the flip-flop enables the counter and

Figure 3.3: Flowchart of the proposed tuning system.



Source: The author.

Figure 3.4: (a) Block diagram of the proposed tuner and (b) implemented voltage comparator and controller.



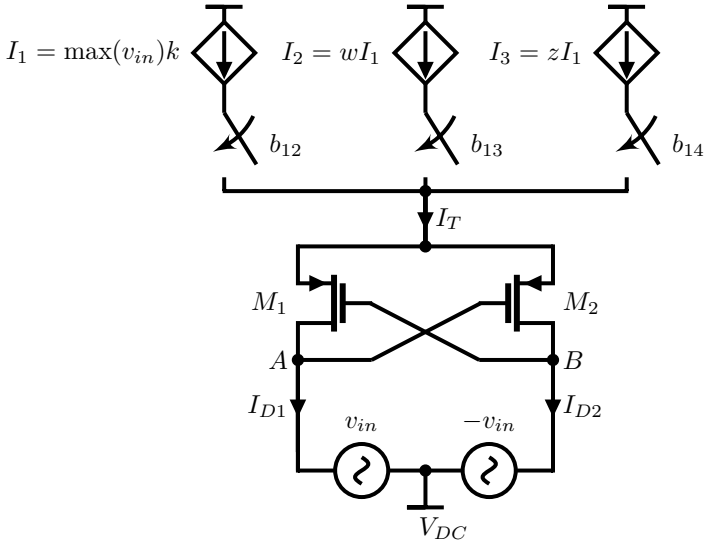
Source: The author.

the negative resistance if the voltage comparator output is off. However, when the voltage comparator output changes to on, the flip-flop resets and the counting process stops.

We implemented the negative resistance with a pMOS cross-coupled pair, as seen in Fig. 3.5. This circuit is connected in parallel with the LC network and its tail current (I_T) is given by the sum of the voltage-controlled current sources when the switches close. These current sources depend on the peak of v_{in} and on k, w, and z constants. In the next subsection, we focus on the design of the negative resistance and of the current source, because the tuning method requires that we use these circuits when the signal has high voltage levels ($v_{in} > 10\,\text{mV}$).

We also integrated a 14-bit synchronous binary counter that is enabled by the controller and receives the clock signal extracted from the LC network, as seen in Fig. 3.4(b). The less significant bits of the counter are used to divide the clock frequency. This allows us to better analyze the transient of the LC network between the different configurations of the capacitor bank. The 9^{th}, 10^{th} and 11^{th} bits of this counter control the bank of capacitors. The other 3 most significant bits (MSBs), named as b_{12}, b_{13}, and b_{14} in Fig. 3.5, modify the value of the negative resistance by connecting/disconnecting the controlled current sources. In the designed system, I_T is increased, and consequently the voltage gain effect on the LC network is enhanced, if the voltage comparator output does not change to the on state during the capacitance sweeping phase.

Figure 3.5: PMOS cross-coupled pair used as an adjustable negative resistance.



Source: The author.

3.3.1 Negative-resistance control

As mentioned above, we use a negative resistance cell as the analog core of the proposed *LC* tuning system. This resistance can be implemented with a pMOS cross-coupled pair, as seen in Fig. 3.5. Its resistance seen across terminals A and B can be calculated by [1] :

$$R_{in} = \frac{-2}{G_m}, \tag{3.3}$$

where G_m is the transistor transconductance. In general, when working with signals smaller than 10 mV, it can be assumed that G_m remains constant with variations in the voltage on its terminals. However, for higher voltage signals, G_m assumes a non-linear behavior that must be taken into account in order to implement the cross-coupled structure in this *LC* tuning system.

To understand the non-linear behavior of the cross-coupled pair with variation in the signal voltage, we first consider that the transistors of this cell are operating in the exponential regime, which is a trend in the design of low-power circuits. We can consider the following equation for the drain current of transistor M_y (I_D), based on [17]:

$$I_{Dy} = I_{Sy}\left(e^{\left(\frac{V_{TH}-V_{Gy}}{n}+V_S\right)\frac{1}{U_T}}\right), \tag{3.4}$$

where y is the transistor index, I_S is the specific current, V_{Gy} is the gate voltage, V_{Dy} is the drain voltage, n is the transistor slope factor, V_S is the source voltage of both transistors, U_T is the thermal voltage and V_{TH} represents the transistor threshold voltage. Considering that the transistors are physically matched we can write the differential current $I_D = I_{D2} - I_{D1}$, of the circuit presented in Fig. 3.5, normalized by the bias current I_T as:

$$\frac{I_D}{I_T} = -\tanh\left(\frac{v_{in}}{nU_T}\right). \tag{3.5}$$

If the input signal v_{in} is a sinusoidal of the form $v_{in} = V_{PK}\cos(\omega_o t)$, and the circuit operates in its steady-state condition, we can decompose (3.5) into a Fourier series whose coefficients are given by:

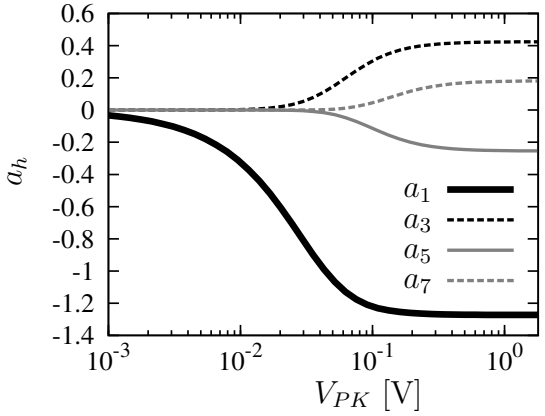
$$a_h = \frac{1}{\pi}\int_{-\pi}^{\pi} -\tanh\left(\frac{V_{PK}}{nU_T}\cos(\theta)\right)\cos(h\theta)d\theta, \tag{3.6}$$

[1] We recommend the interested reader to go to appendix B for more about negative resistances.

where h is the harmonic order, and $\theta = \omega_o t$.

Note that the Fourier coefficients are weakly dependent on the MOS technology. The coefficients of (B.12) can be numerically solved [18], and we present their solution in Fig. 3.6.

Figure 3.6: I_D/I_T Fourier coefficients of the MOS cross-coupled pair, as a function of V_{PK}.



Source: The author.

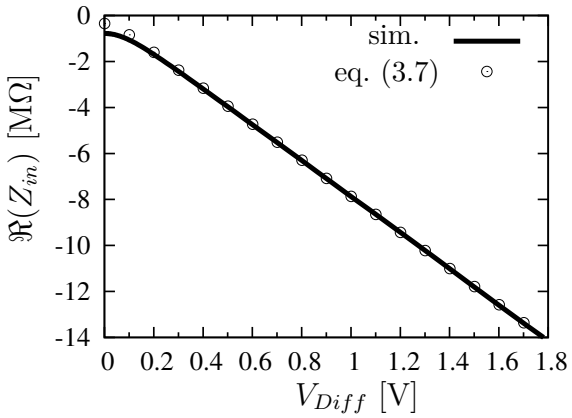
Now that a_1 can be estimated, we write the large signal input resistance as:

$$\Re(Z_{in}) = \frac{V_{Diff}}{a_1 I_T}, \tag{3.7}$$

where V_{Diff} is the peak value of $v_A - v_B$. In this case, we do not take into account the other odd coefficients in (3.7) due to the use of the LC network, which attenuates their effect.

We plot (3.7) versus V_{Diff} and the values obtained are compared with the results from a circuit simulation in Fig. 3.7. To obtain these values we used an input signal frequency of 125 kHz, $n = 1.2$, $U_T = 25\,\text{mV}$ and $I_T = 1\,\mu\text{A}$. From Fig. 3.7, we notice that the negative resistance is strongly degraded for voltage amplitudes higher than a few hundred of milivolts, which is much less than typical voltage values found in RFID tags.

Figure 3.7: Equivalent resistance of the cross-coupled pair at 125 kHz.

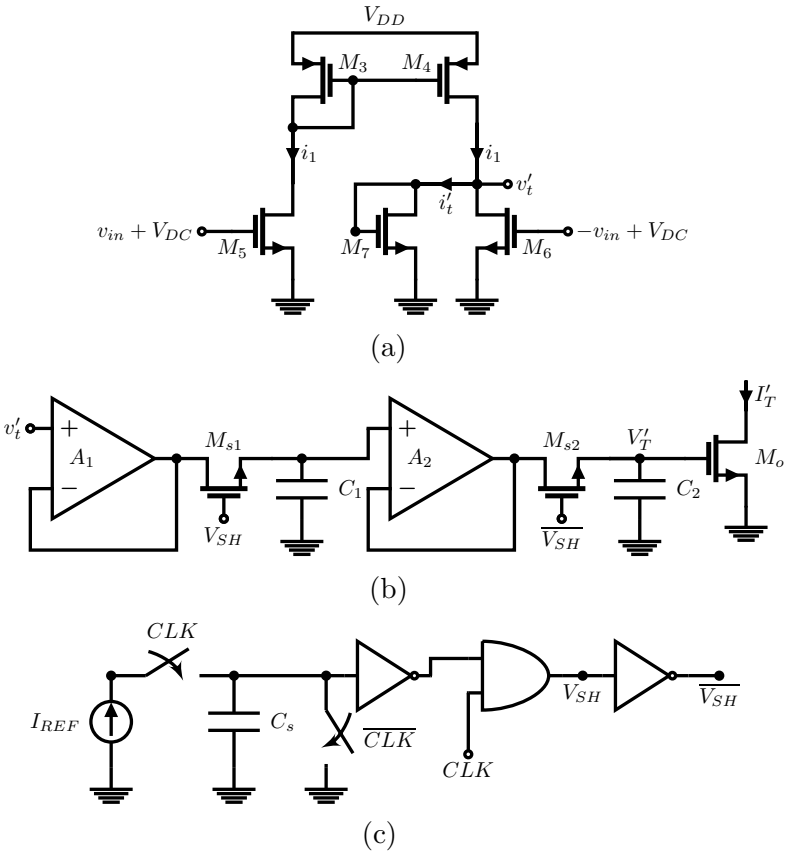


Source: The author.

It is possible to maintain a constant negative resistance over different input voltage levels by keeping I_T proportional to V_{PK} (for $V_{PK} > 100$ mV). Based on this assumption, we designed an I_T controller as seen in Fig. 3.8.

Fig. 3.8(a) shows a a half-wave-rectifier circuit, presented in [19]. If M_5 and M_6 are in strong inversion, we can prove that the output current i'_t is proportional to v_{in} and to the W/L ratio of these transistors when v_{in} is in its positive cycle.

Figure 3.8: Controlled current source blocks divided into: (a) proportional voltage to current converter, (b) v'_t peak sampler and I'_T current source, and (c) switching signal schematic.



Source: The author.

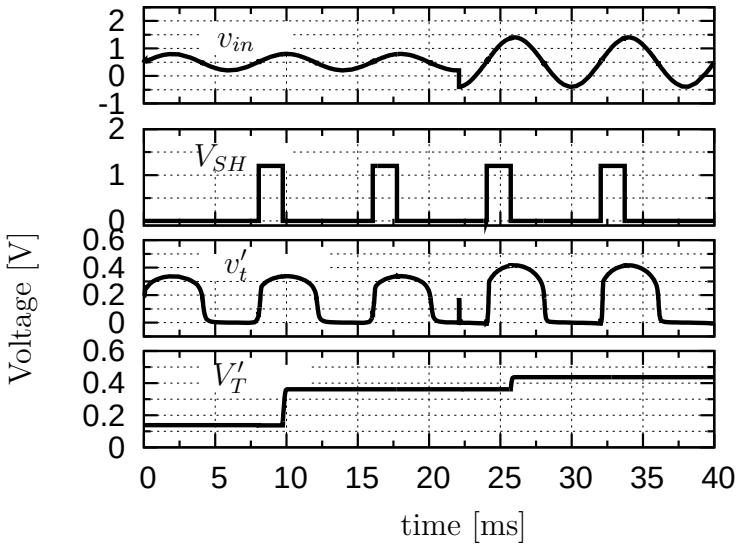
A voltage peak sampler is used to obtain I_T, which is a DC current, from v'_t. The voltage peak sampling is performed by the circuit of Fig. 3.8(b) when we properly switch transistors M_{s1} and M_{s2}. If the switching signal V_{SH} is high, v'_t is copied to C_1. V_{SH} becomes low when v'_t reaches its peak and the voltage value stored on C_1 is copied to C_2. The output transistor M_o implements a current source for an nMOS negative resistance, and with simple current mirroring it is possible to use the proposed circuit to control the tail current of a pMOS cross-coupled pair.

The switching signal V_{SH} is generated by charging C_s with a constant reference current, as seen in the simplified schematic of Fig. 3.8(c). The clock signal (CLK) is extracted from v_{in} and is in phase with it. The charging current (I_{REF}) and the value of C_s were chosen so that when v'_t is maximum, the voltage over C_s is equal to the inverter threshold voltage. With an AND operation with CLK we generate V_{SH}.

With these circuits I_T remains proportional to the peak of v_{in} and we properly control the value of the negative resistance for large voltage signals.

It is possible to see in Fig. 3.9, the simulated behavior of the v'_t peak sampler using two voltage levels of v_{in}. When the simulation starts, V'_T is equal to 0 V and the peak of v'_t is passed to V'_T when V_{SH} goes to 0 V. We also see that V'_T is changed when the amplitude of v_{in} increases.

Figure 3.9: Simulated behavior of the v_t' peak sampler that is shown in Fig. 3.8.



Source: The author.

3.4 COMPONENT SIZING

The reader will see that this "Component Sizing" section is presented in the following chapters as well. The main purpose of these sections is to facilitate the reproducibility of the presented designs. We note that the CMOS digital cells presented in the thesis are not included in these sections because they can be easily built. As a reminder, the "Component Sizing" sections contains the design of the circuits built using the IBM (GF) 0.13- μm standard CMOS process [2], unless stated otherwise.

The transistor sizes of the proportional voltage to current converter can be seen in table 3.1.

Table 3.1: Component sizes/values of the proportional voltage to current converter (Fig. 3.8(a)).

Component	**Value**	**Additional data**
M_5, M_6 [a]	W_{tot}/L=.68 μm/5 μm	fingers = 1, multiplicity = 1
M_3, M_4	W_{tot}/L=5 μm/.8 μm	fingers = 1, multiplicity = 1
M_7 [b]	W_{tot}/L=1 μm/1 μm	fingers = 1, multiplicity = 1

Source: The author.

[a] We placed 6 transistors in series. Each transistor is designed with the given dimensions and standard transistors were used.

[b] We placed 2 transistors in series. Each transistor is designed with the given dimensions.

The component sizes/values of the v_t' peak sampler can be seen in table 3.2.

The circuit used to implement the buffer of Fig. 3.8(b) can be seen in Fig. 3.10. The chosen topology is based on the circuit shown in [20]. This buffer was chosen because it uses negative feedback, implemented by transistors M_1, M_{10}, and M_{11}, that decreases the output impedance of the op.amp. .

The component sizes/values of the implemented buffer can be seen in table 3.3.

In Fig. 3.8(c) we have that I_{REF} = 100 nA and C_s=320 pF and the trip voltage of the first inverter is close to 0.6 V. The circuit used to charge/discharge C_s can be seen in Fig 5.19

[2] In our designs we used 3.3-V transistors. In the used process the minimum channel lenght of these transistors is 0.4 μm.

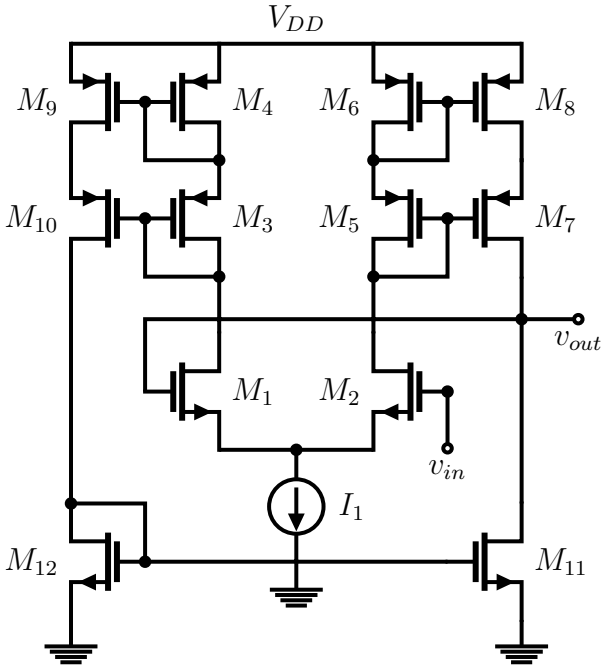
Table 3.2: Component sizes/values of the v_t' peak sampler (Fig. 3.8(b)).

Component	**Value**	**Additional data**
M_p [a]	W_{tot}/L=1 μm/1 μm	fingers = 1, multiplicity = 1
M_{s1}, M_{s2}	W_{tot}/L=.68 μm/.48 μm	fingers = 1, multiplicity = 1
C_1, C_2	680 fF	Dual MIM capacitor

Source: The author.

[a]We placed 2 transistors in series. Each transistor is designed with the given dimensions.

Figure 3.10: Implemented buffer of Fig. 3.8(b).



Source: Modified from [20].

Table 3.3: Component sizes for the buffer used in Fig. 3.8(b).

Component	**Value**	**Additional data**
M_1, M_2	W_{tot}/L=2.5 μm/.4 μm	fingers = 1, multiplicity = 2
M_3, ..., M_{10}	W_{tot}/L=5 μm/.4 μm	fingers = 1, multiplicity = 1
M_{11}, ..., M_{12}	W_{tot}/L=2.5 μm/1 μm	fingers = 1, multiplicity = 3
I_1	400 nA	

Source: The author.

of chapter 5.

In table 3.4 we report the size of the pmos cross-coupled pair seen in Fig. 3.5.

Table 3.4: Component sizes of the negative resistance circuit seen in Fig. 3.5.

Component	Value	Additional data
M_1, M_2	W_{tot}/L=5 μm/.4 μm	fingers = 2, multiplicity = 2
b_{12}, b_{13}, b_{14} [a]	W_{tot}/L=5 μm/.4 μm	fingers = 2, multiplicity = 1
M_{I1} *[b]	W_{tot}/L = 2.5 μm/.4 μm	fingers = 1, multiplicity = 1
M_{I2} *	W_{tot}/L = 7.5 μm/.4 μm	fingers = 3, multiplicity = 1
M_{I3} *	W_{tot}/L = 12.5 μm/.4 μm	fingers = 5, multiplicity = 1

Source: The author.

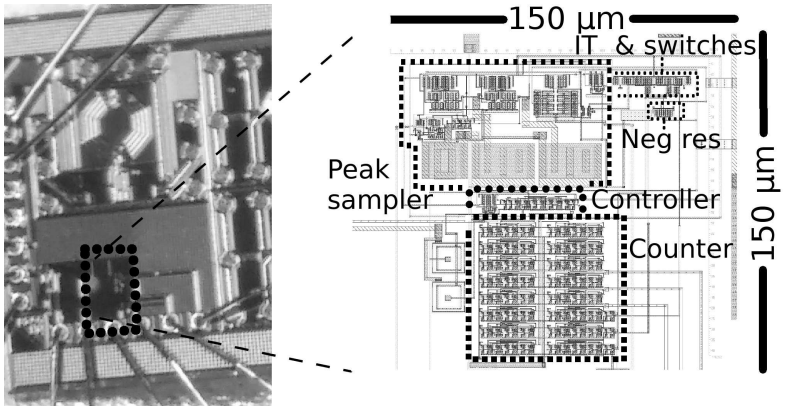
[a]Implemented by pMOS transistors.
[b]PMOS transistor used to implement the controlled current source

3.5 RESULTS

We implemented the LC tuner in a standard 130-nm CMOS process and the fabricated IC can be seen in Fig. 3.11. The tuner occupies an active area of 150 μm × 150 μm. It is located inside the dotted rectangle and its layout can be seen in the zoom.

The tuner was characterized using the configuration shown in Fig. 3.14. In this figure, L_0 and C_0 model an off-the-shelf RFID antenna that resonates at 125 kHz. L_1 and L_2 are unshielded inductors magnetically coupled with L_0 and they resonate with the bank of capacitors, which has an equivalent capacitance of C_1. The system comprised of these off-the-shelf components has an equivalent Q of 20 seen from the IC side. L_1 and L_2 have each an equivalent inductance of 3.3 mH and their equivalent parallel resistance, when they resonate with the capacitor bank is approximately 100 kΩ. The integrated tuner is connected to the parallel LC network and it controls the bank of capacitors with 3 bits. V_{DC} and V_{DD} are set to 0.8 V and 3.3 V, respectively.

Figure 3.11: Photograph of the designed integrated circuit and zoom of the tuning-system layout.



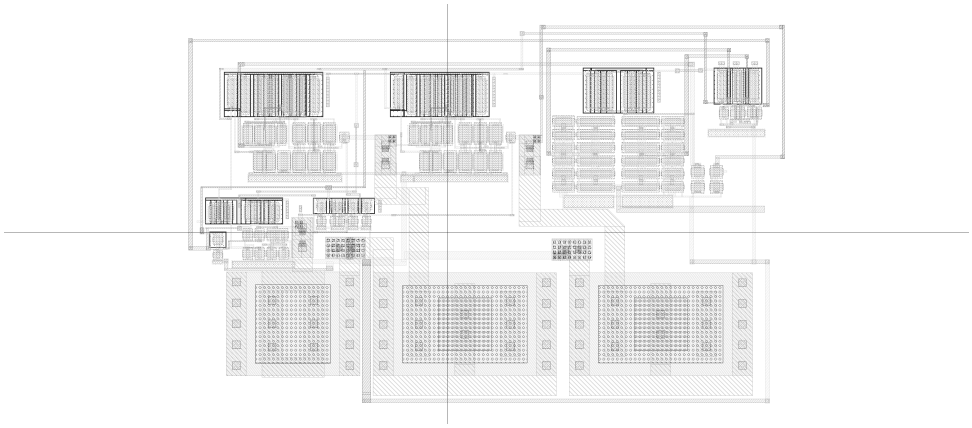
Source: The author.

We shown in Figs. 3.12 and 3.13 the layout zoom of the main designed blocks of the presented tuning system. It is possible to see the peak sampler, the controller, and the pMOS cross-coupled pair.

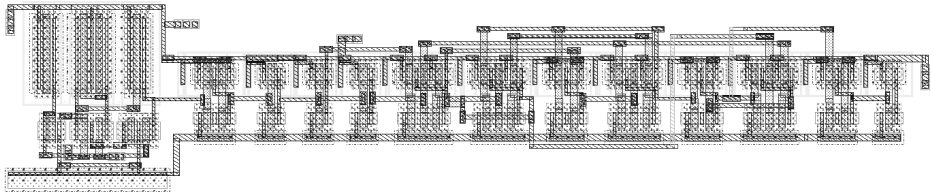
Using the configuration shown in Fig. 3.14, we measured the average current consumption of the tuner versus V_{Diff} as seen in Fig. 3.15(a). It can be noted that the measured and simulated average current consumption curves are close to each other and the current slope is approximately 12 μA/V.

The negative resistance obtained is seen in Fig. 3.15(b). The simulated negative resistance presents a nearly constant value for $V_{Diff} > 100$ mV and the measured resistance assumes a controlled behavior for a higher V_{Diff} compared to the simulated value. The resistance values of Fig. 3.15(b) are obtained by measuring the voltage increment of a tuned LC network when

Figure 3.12: Layout of the designed peak sampler and the controller in (a) and (b), respectively.



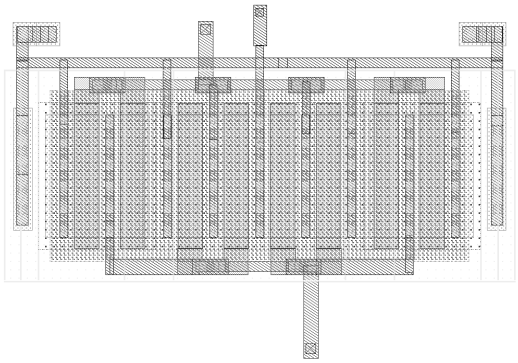
(a)



(b)

Source: The author.

Figure 3.13: Layout of the designed pMOS cross-coupled pair.



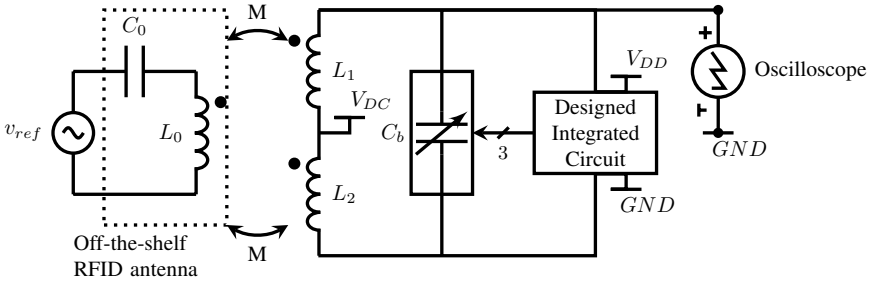
Source: The author.

the negative resistance and all the switches that control I_T are on.

When we use this negative resistance with $R_{in} \cong -250\,\text{k}\Omega$ to cancel the losses of the system, with an equivalent parallel resistance of $100\,\text{k}\Omega$, we have an equivalent resistance of $170\,\text{k}\Omega$. Then the voltage on the tuned LC network increases up to 70 % when this negative resistance is enabled.

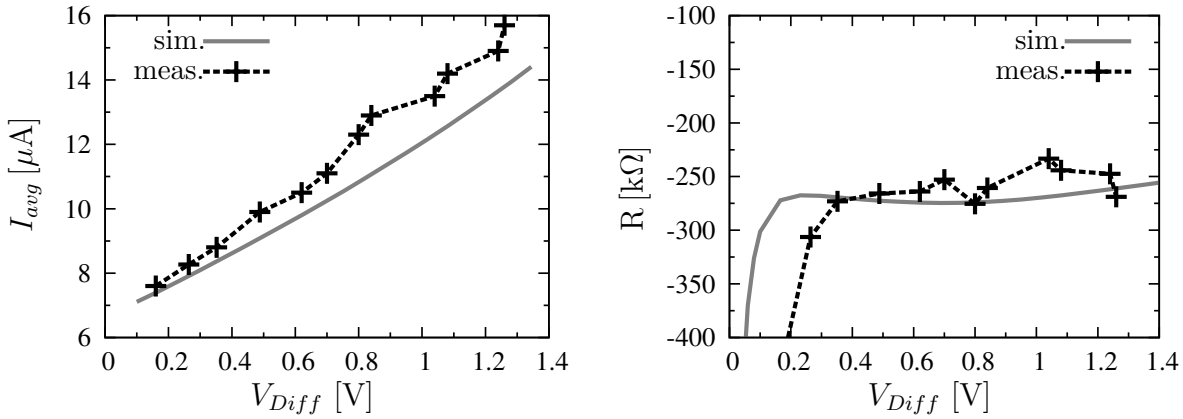
In Fig. 3.16 we present a complete tuning sequence of the schematic seen in Fig. 3.14. In the former figure, we show the measured voltage on one side of the LC network, the MSB that controls the capacitor bank (Cb_{MSB} which is shifted by +2 Volts and multiplied by 0.5),

Figure 3.14: Simplified schematic of the test bench used to validate the integrated tuner.



Source: The author.

Figure 3.15: (a) Average current consumption versus V_{Diff} and (b) equivalent parallel IC negative resistance.



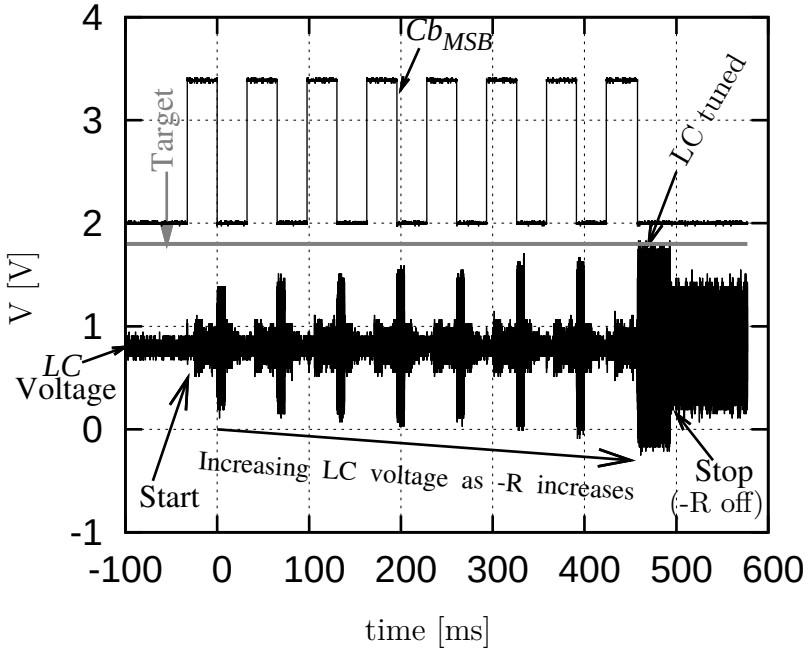
Source: The author.

and the target voltage, which is set to 1.8 V [3]. During the tuning process, the LC voltage changes due to the capacitance sweeping and there are eight voltage peaks between the start and stop points. On analyzing these voltage peaks, it can be noted that they increase when the negative resistance increases. Therefore, these peaks are at, or close to, the LC resonating frequency. It is important to mention that if a fixed negative resistance is used, the target voltage might not be reached due to process variations and mismatch. Then, it is required to use a variable negative resistance to compensate these variations. In the presented case, the negative resistance increases when C_{MSB} goes to 0 V.

In table 3.5 we report the lab. equipment used to make the presented measurement results.

[3]The voltage on both sides of the LC network, the target voltage, and the less significant bit of the capacitor bank are measured with a 4-channel oscilloscope. Each channel of this oscilloscope is connected to one of these signals by x10 passive probes, as it is demonstrated for one side of the LC network in Fig. 3.14.

Figure 3.16: Waveform of a complete tuning sequence of the integrated tuner.



Source: The author.

Table 3.5: Equipment used in the laboratory to obtain the presented measurement results.

Equipment	**Seller**	**Additional data**
Arbitraty waveform generator	Agilent	33220A, 20 MHz
Voltage Source	Agilent	E3634A
Source Measurement Unit (SMU)	Agilent	B2902A
Oscilloscope	Agilent	DSO-x-2014, 1 Gsample/s, 4 channel scope
Probe	Agilent	N2862B, 10:1, 150 MHz, passive, 10 MΩ//15 pF

Source: The author.

3.6 SUMMARY

RFID systems have been successfully applied in many applications. Their tags contain information acquired by the reader and they are generally comprised of a resonating and an integrated circuit. developed that is able to retune the resonating circuit of the tag back to its nominal specification. However, the tag performance can be degraded if there is a deviation in its LC network. Thus, we developed an integrated tuner able to retune the resonating circuit of the tag back its nominal specification. The right tuning decision is made when the target voltage is reached and it is not necessary to continue the sweeping procedure after that. The tuner is designed using a simple control logic and it occupies a small area due to its low analog and digital complexity.

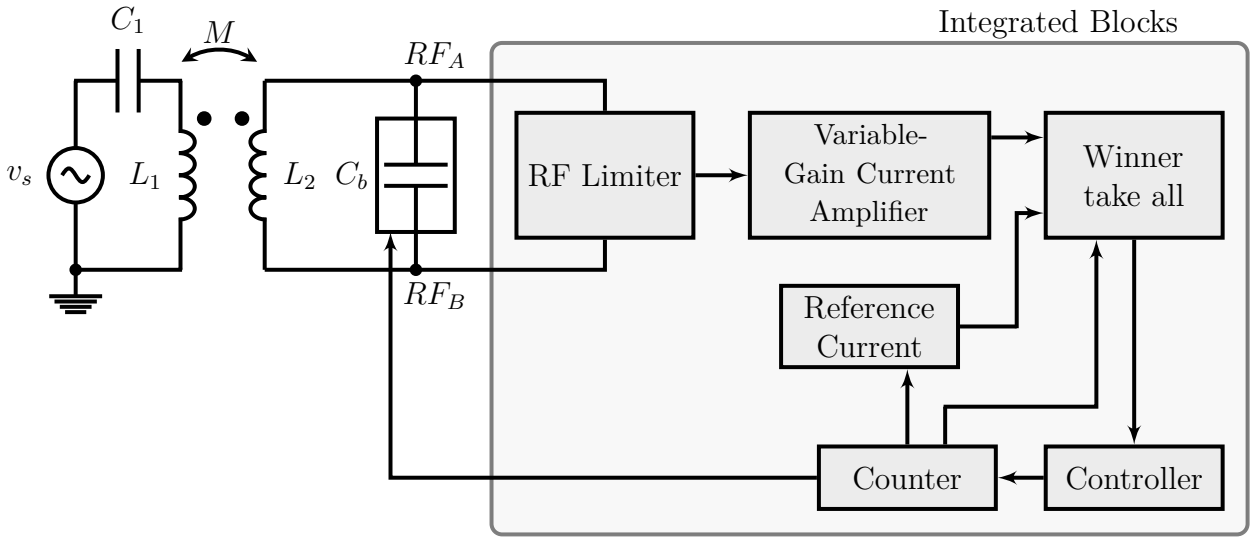
The use of a negative resistance to increase the LC network quality factor, in integrated circuits, is a classical technique and it is used in automatic filter tuners in [14, 15], as previously mentioned. However, in our case, we use the negative resistance to simplify the tuning decision and its required circuitry.

4 LC TUNER BASED ON THE RF LIMITER CURRENT

4.1 INTRODUCTION

The tuning method based on negative resistances depends on the induced voltage on the LC network. Thus, it is possible that, in some conditions, the voltage on the LC tank reaches the maximum or minimum allowed voltage for the operation of the negative resistance. Then, in a situation where we can not modify the voltage on the LC network the tuning method based on negative resistances should not be used. One way to circumvent this voltage swing limits is to use a complementary tuning method based on current. In this method, the limit is that the current is allowed to swing up to a specified power constraint. Hence, we show in Fig. 4.1, a block diagram of the tuning system used to tune LC networks based on current.

Figure 4.1: Block diagram of the LC tuning technique based on the current of the RF voltage limiter.



Source: The author.

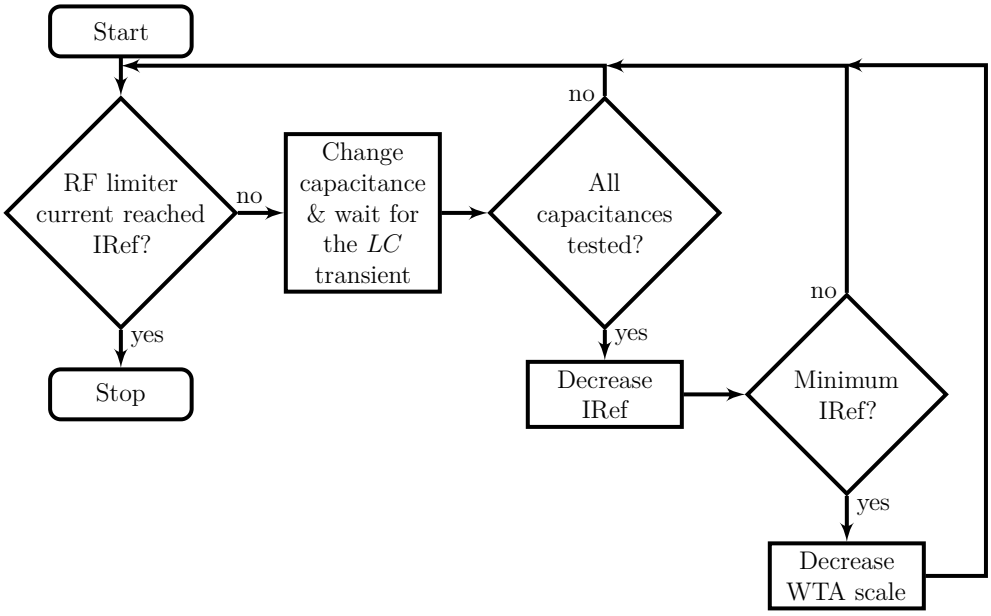
As we see in the next section, the use of an RF limiter is essential in RFID applications. Due to this, the designed tuning method of this chapter is based on a sample of the short-circuit current that flows through the RF limiter.

The Q of the LC network may be very small when the RF limiter turns on, as it is possible to see in the next subsection. With a low Q, the difference on the peak current of the RF limiter for different capacitance configurations, that are near the resonance frequency, is small and it may be difficult to distinguish among these capacitances. Hence, we use a variable-gain current amplifier (VGCA), that is designed to have a gain that increases with its input current signal, to increase the aforementioned current difference among different capacitance configurations. Thus, we can say that this VGCA makes an analogous operation that was seen with the negative resistance in chapter 3.

The equivalent capacitance of the capacitor bank (C_b) is swept until the winner-take-all (WTA) circuit detects that the output current of the VGCA is higher than the reference current. If the WTA circuit does not detect this difference, for all tested capacitance configurations, the value of the reference current, that is compared by the WTA, is decreased. The counter also modifies the scaling factor of the WTA cell. This can be useful to scale-up the reference current

and reduce power consumption. The flowchart shown in Fig. 4.2 summarizes the operation of this tuner.

Figure 4.2: Proposed flowchart of the tuner based on the RF limiter current.



Source: The author.

In this chapter we discuss in detail the presented blocks of this tuner based on the RF limiter current, we also present some simulation results of the design system, and we show the measurement results of a prototype designed using a 130-nm CMOS process.

4.2 RF VOLTAGE LIMITERS

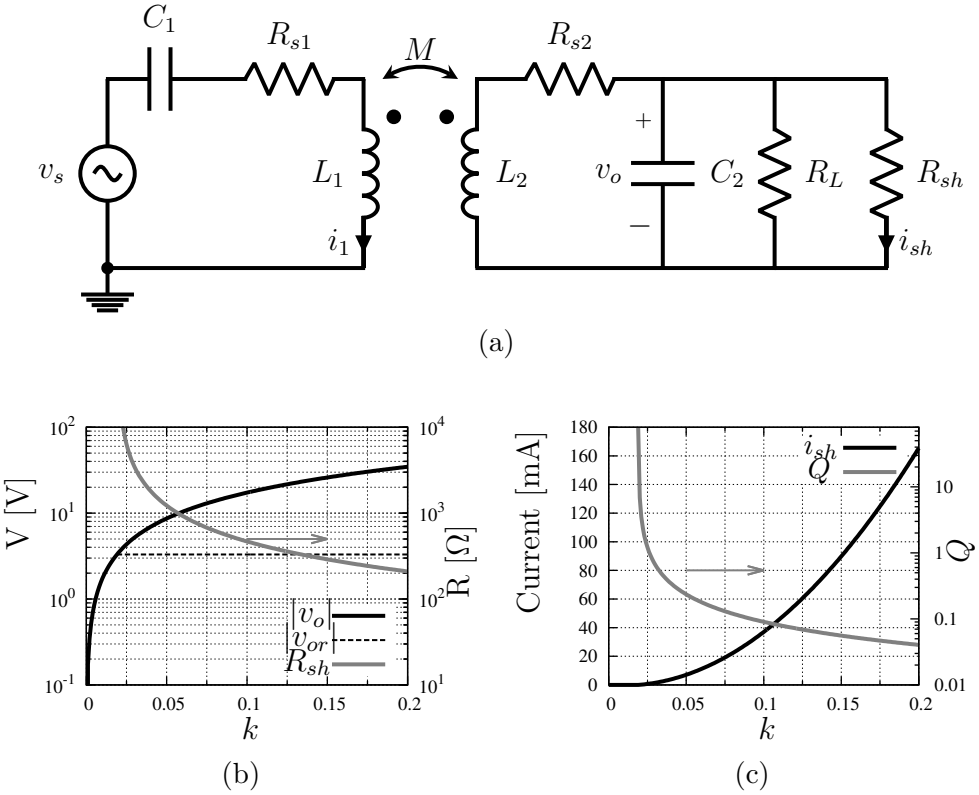
In RFID systems, the induced voltage across the resonant circuit, can quickly increase is the tag gets closer to the reader. Hence, the use of limiter circuits connected in parallel with the LC network is unavoidable. Otherwise, the active components of the tag might be damaged.

In Fig. 4.3(a) we show an example of an RFID circuit, that we illustrated in chapter 2, for the reader convenience. In Fig. 4.3(b), we plot the induced voltage on the tag ($|v_o|$) and the induced voltage using an ideal RF limiter ($|v_{or}|$) versus the coupling factor between the reader and the tag. Note that $|v_o|$ can easily reach dozens of Volts. Then, if $|v_o|$ must be up to 3.3 V the protection activates even when the resonating circuits have low k. We also plot the equivalent shunt resistance (R_{sh}) that is required to protect the tag. Note that R_{sh} is non-linear and it has a high slope when it starts the protection. These curves were obtained based on (2.11). In this equation R_{sh} is placed in parallel with R_L and the following values are used: $f = 125\,\text{kHz}$; $i_1 = 0.1\,\text{A}$; $L_1 = 5\,\text{mH}$; $L_2 = 6.6\,\text{mH}$; $C_2 = 1/(w^2 L_2)$; $R_s = 60\,\Omega$; and $R_L = 2\,\text{k}\Omega$.

It is possible to see in Fig. 4.3(b) the short-circuit current trough the ideal RF limiter (i_{sh}) and the equivalent Q of the LC network versus k. We note that i_{sh} can easily reach the milliampère scale and Q can go lower than 1.

We can see a simple and typical RF limiter that is composed by one nMOS transistor, in [21]. The antenna terminal is connected to the drain of the transistor and to its gate by a diode, as we can see in Fig. 4.4(a). The body diode limits the negative excursions of the RF signal to about 0.7 V. For positive RF excursions, the transistor act like a shunting device and limits the input voltage level. The gate to source voltage of this transistor is set by D_1 and by the parallel RC circuit on its gate. The authors comment that their RC time constant is chosen to be larger than the time of the low modulation pulse, so the circuit does not respond to the data modulation.

Figure 4.3: (a) Example of an RFID circuit. (b) Induced voltage on the tag's resonating circuit (v_o), limited voltage on the tag (v_{or}), and ideal shunt resistance used to control v_o (R_{sh}) versus k. (c) Equivalent short-circuit current trough the ideal RF limiter (i_{sh}) and the equivalent Q of the LC network versus k.



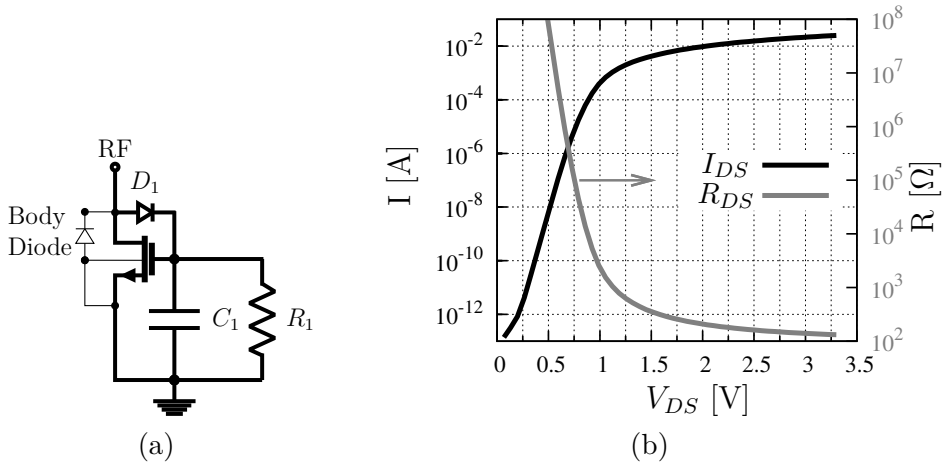
Source: The author.

We simulate and plot the drain-to-source current I_{DS} and resistance (R_{DS}) of an nMOS transistor with $W/L = 100/1$ in Fig. 4.4(c). In this simulation $V_{GS} = V_{DS} - 0.4$ V. Due to the exponential and quadratic characteristics of I_{DS} versus the gate-to-source voltage of the MOS transistor, R_{DS} and the ideal R_{sh} have a similar behavior. This characteristic makes the MOS transistors suitable to control the value of R_{sh}, as it is seen in the typical RF limiter shown in Fig. 4.4(a).

Since 1995, we have been able to see RF limiters based on MOS transistors. In [22] we see a novel passive tag using a 2-μm CMOS process. In this design, among other blocks, we can find an RF limiter that we depicted in Fig. 4.5(a). According to the authors, the diode connected transistors acts like a 'zener diode'. Basically, as soon as the voltage on the RF branch reaches a threshold, we have a voltage drop on R_1 that turns on transistor Mp_1. After that M_1, which is designed to carry most of the current, activates. Due to the design of their RFID system, the authors say that M_2 is added to reduce the drain voltage on M_1.

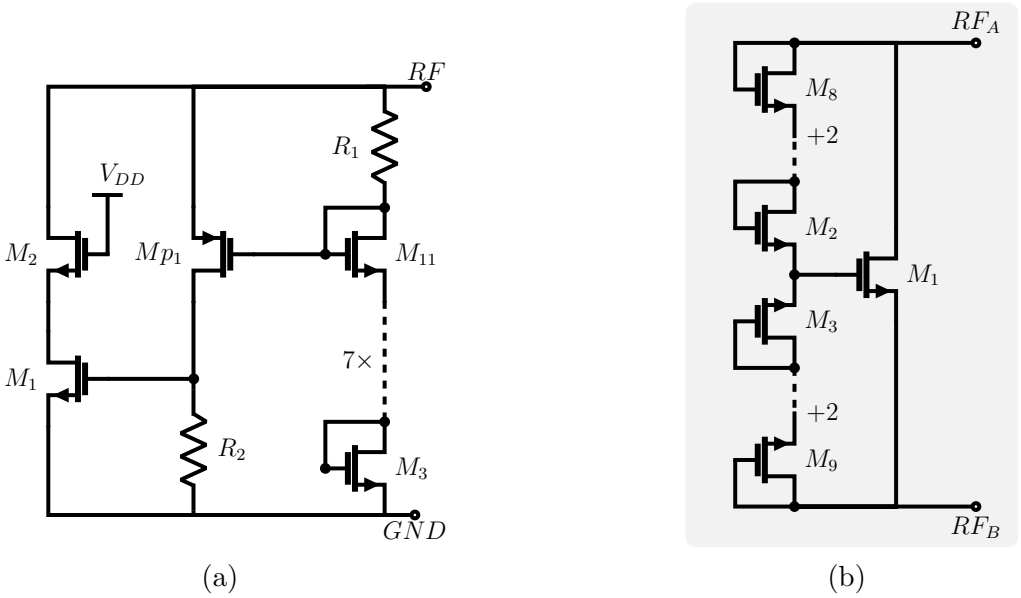
We can see a compact voltage limiter using transistors in [23] and an adapted version, using only nMOS transistors, in Fig. 4.5(b). In this circuit RF_A and RF_B are connected to the LC network and when RF_A is high, RF_B is low. Supposing that RF_A is high, the current that flows through the even-numbered diode connected transistors is small. This is due to M_3 that is off and sets the branch current equal to the reverse current of its reverse-biased drain-to-bulk junction diode. Then, the voltage drop between each drain and source of the even-numbered transistors connected in diode is approximately equal to V_{TH}. Hence, using this configuration, M_1 can provide a low path impedance between the RF nodes when the incoming signal should be clamped.

Figure 4.4: (a) Typical RF limiter and (b) simulated R_{DS} of this limiter.



Source: (a) Extracted from [21] and (b) the author.

Figure 4.5: (a) RF limiter and (b) implemented RF limiter using only nMOS transistors.

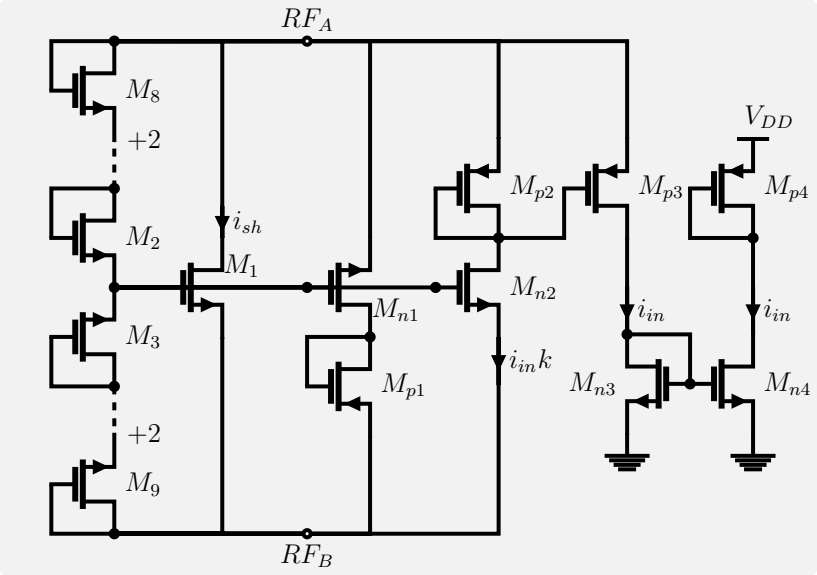


Source: (a) Extracted from [22] and (b) based on [23].

If we use a diode connected transistor on the drain of M_1 to mirror i_{sh}, we have only one direction for i_{sh}. Then, to copy a sample of the short-circuit current of the RF limiter, we keep the same structure shown in Fig. 4.5(b) and add the additional circuitry shown in Fig. 4.6 [1]. M_{n1} and M_{n2} have a lower aspect ratio compared to M_1, so that the current on these transistors is smaller than i_{sh}. Note that M_{n1} and M_{p1} are used to make the short-circuit current from RF_A to RF_B symmetric. The short-circuit current through M_{n2} is copied to M_{n3} by M_{p3}, that has a smaller aspect ratio compared to M_{p2}. M_{p3} is designed with a smaller aspect ratio to decrease the impact of the imbalance of the short-circuit current. But since we design that i_{sh} is at least two orders of magnitude higher than the other currents, this imbalance is not relevant during the tuning phase. Then, with the given circuit it is possible to scale down the value of i_{sh} and mirror i_{in} to the variable-gain current amplifier.

[1] We designed the pMOS transistors, in Fig. 4.6, with their bulk contact connected to V_{DD}. By doing this, the junction of the pMOS bulk with the chip's substrate is always reverse biased.

Figure 4.6: Implemented circuit used to scale down i_{sh}.



Source: The author.

4.2.1 Component Sizing

It is possible to view the used component sizes/values of the implemented RF limiter and the circuit used to scale down i_{sh} in table 4.1.

Table 4.1: Component sizes/values of the implemented envelope detector.

Component	**Value**	**Additional data**
M_1	$W_{tot}/L = 1.5\,\mu\text{m}/1.5\,\mu\text{m}$	fingers = 1, multiplicity = 1
M_2, ..., M_9	$W_{tot}/L = .7\,\mu\text{m}/.5\,\mu\text{m}$	fingers = 1, multiplicity = 1
M_{p1}, M_{p2} [a]	$W_{tot}/L = 4\,\mu\text{m}/2\,\mu\text{m}$	fingers = 1, multiplicity = 1
M_{p3} [b]	$W_{tot}/L = 1\,\mu\text{m}/2\,\mu\text{m}$	fingers = 1, multiplicity = 1
M_{n1}, M_{n2} [c]	$W_{tot}/L = 10\,\mu\text{m}/1.0\,\mu\text{m}$	fingers = 1, multiplicity = 1
M_{n3},M_{n4}	$W_{tot}/L = 4\,\mu\text{m}/2\,\mu\text{m}$	fingers = 1, multiplicity = 1

Source: The author.

[a] Implemented using 2 transistors connected in series. The second transistor is omitted in the schematic for simplification.

[b] Implemented using 2 transistors connected in series.

[c] Implemented using 4 transistors connected in series.

4.3 TRANSLINEAR LOOP USED AS A VARIABLE-GAIN CURRENT AMPLIFIER

The variable-gain current amplifier (VGCA), that is designed to have a gain that increases with its input current signal, is used to increase the current difference among different capacitance configurations, as it is explained in the introduction. One simple way to implement this amplifier is with translinear loops, as we see in this section. We will also see that these translinear loops have an independent temperature behavior, are easy to design, use few transistors to be implemented, and their output are easily controlled.

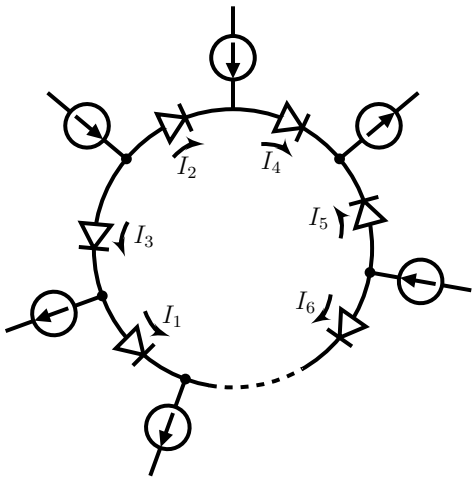
The translinear principle was formally defined by B. Gilbert in 1975 [24]. The author defines the translinear circuit as: 'a circuit that have inputs and outputs in the form of currents

and whose primary function arises from the exploitation of the proportionality of transconductance to collector current in bipolar transistors ...' . Hence, the translinear circuit can be used to receive the current sample of the RF limiter, modify it and send the modified current to the winner take all circuit.

We can see a circuit using the translinear principle in 1968, when Gilbert was working for Tektronix, in a high-bandwidth (DC-500 MHz) variable gain cell for oscilloscopes [25, 26]. However the term 'trans-linear' and its properties in a translinear loop were formalized almost ten years later. This term captures the exponential-current behavior of the BJT [26], i.e. it is based on the exponential relationship between the collector current and the base-emitter voltage of a BJT.

The translinear principle is the base of many useful nonlinear circuits such as wideband analog multipliers, translinear frequency multipliers, RMS-DC converters, operational current amplifiers and translinear current conveyors [27].

Figure 4.7: Generalized single-loop translinear circuit.



Source: Extracted from [24].

The voltage drop on a diode can be calculated by:

$$V_{Dr} = U_T \ln \frac{I_r}{I_S}, \tag{4.1}$$

where $U_T = kT/q$ is the thermal voltage, I_S is the diode reverse current, r is the diode index and I_r is the current on diode r. Continuing with Gilbert's translinear principle, we can identify a translinear loop when it uses an even number of forward biased p-n junctions arranged in one or more loops. Then, the closed loop voltage in Fig. 4.7 is equal to [24]:

$$\sum_{r=1}^{N/2} \left(U_{T2r} \ln \left(\frac{I_{2r}}{I_{S2r}} \right) - U_{T(2r-1)} \ln \left(\frac{I_{(2r-1)}}{I_{S(2r-1)}} \right) \right) = 0. \tag{4.2}$$

Note that the even diodes are in the clockwise direction (CW) and the odd diodes are in the counter-clockwise direction (CCW). If we consider that the diodes are at same temperature and have the same I_S we have that [24]:

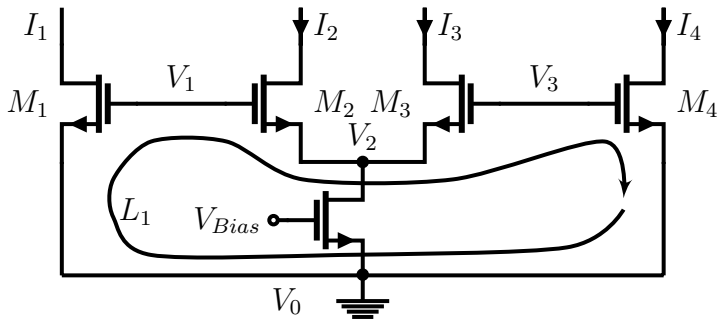
$$\sum_{r=1}^{N/2} \left(\ln I_{2r} - \ln I_{(2r-1)} \right) = 0, \tag{4.3}$$

which is equal to the translinear loop principle [24]:

$$\prod_{r=1}^{N/2} I_{2r} = \prod_{r=1}^{N/2} I_{(2r-1)}. \tag{4.4}$$

Now that we obtained the translinear principle in (4.4), we can understand the premises used by Gilbert in his paper in 1968 [25]. In these premises, he says that the transistors of his amplifier must have a good matching and we can easily see why his amplifier in [25] has a temperature-independent behavior.

Figure 4.8: Example of a translinear loop using MOS transistors



Source: Based on [27].

The MOS transistor can also be a translinear element only when it is working in its subthreshold region as we can see in [28]. To understand how the translinear loop is formed using MOS transistors, we can refer to [27, 29] and/or analyze the loop shown in Fig. 4.8. The current I_y of the CCW transistors (the ones that have the source-to-gate voltage in the loop direction, in the presented case: M_1 and M_3) can be calculated as:

$$I_{yCCW} = I_S e^{\frac{\frac{V_y - V_{TH}}{n} - V_{y-1}}{U_T}}, \tag{4.5}$$

where y is the index that either represents the nodes or currents. (4.5) can be rearranged to:

$$e^{\frac{V_y}{U_T}} = \left(\frac{I_{yCCW}}{I_S}\right)^n e^{\left(\frac{V_{TH}}{nU_T} + \frac{V_{y-1}}{U_T}\right)n}. \tag{4.6}$$

The current I_y of the CW transistors can be calculated as:

$$I_{yCW} = I_S e^{\frac{\frac{V_{y-1} - V_{TH}}{n} - V_y}{U_T}} \tag{4.7}$$

and can be rearranged to:

$$e^{\frac{V_y}{U_T}} = \frac{I_S}{I_{yCW}} e^{\frac{V_{y-1} - V_{TH}}{nU_t}}. \tag{4.8}$$

We can refer to the method used in [27] to build up the loop equation. In this method, the author uses the recurrence relationships of (4.6) and (4.8) and build the loop equation begining with one loop node and proceed sequentially around the loop. Using this method, we equate

the nodes of the translinear loop, presented in Fig. 4.8, starting with node V_0 as:

$$\underbrace{\left(\underbrace{\left(\underbrace{\left(\underbrace{\left(\frac{I_1}{I_S}\right)^n e^{\left(\frac{V_{TH}}{nU_T}+\frac{V_0}{U_T}\right)n}}_{e^{\frac{V_1}{U_T}}}\right)^{\frac{1}{n}} \frac{I_S}{I_2}e^{\frac{-V_{TH}}{nU_T}}}_{e^{\frac{V_2}{U_T}}}\right)^n \left(\frac{I_3}{I_S}\right)^n e^{\left(\frac{V_{TH}}{nU_T}\right)n}}_{e^{\frac{V_3}{U_T}}}\right)^{\frac{1}{n}} \frac{I_S}{I_4}e^{\frac{-V_{TH}}{nU_T}}}_{e^{\frac{V_0}{U_T}}} = e^{\frac{V_0}{U_T}}, \tag{4.9}$$

that can be simplified to:

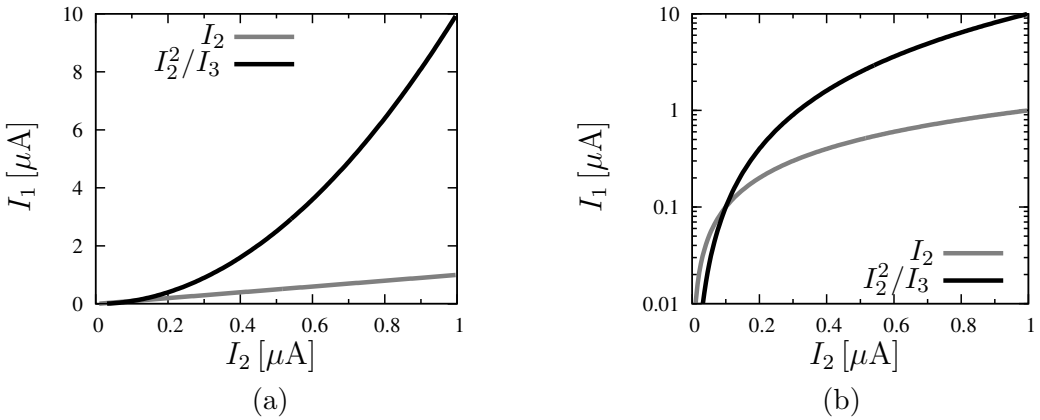
$$I_1 I_3 = I_2 I_4, \tag{4.10}$$

agreeing with the translinear loop principle. If I_1 is the output current, (4.10) simply turns to:

$$I_1 = \frac{I_2 I_4}{I_3}. \tag{4.11}$$

To have a VGCA we can consider that I_2 is the input current and that $I_2 = I_4$. With these considerations the output current of the VGCA can be I_1 that is equal to I_2^2/I_3. To aid with the understanding of the used VGCA quadratic behavior, two curves of I_1 versus I_2 are plotted in Figs. 4.9(a) and (b). For one curve $I_1 = I_2$ and for the other curve $I_1 = I_2^2/I_3$, where $I_3 = 100\,\text{nA}$. We note that the slope of the I_2^2/I_3 curve increases with I_2, as expected. This is the desired characteristic of a VGCA.

Figure 4.9: I_1 versus I_2 for $I_1 = I_2$ and $I_1 = I_2^2/I_3$ using a linear and log scale in (a) and (b), respectively.



Source: The author.

We designed some basic blocks using CEITEC's 0.6-μm CMOS process. Among these blocks, we integrated the translinear circuit that is seen in Fig. 4.10(a). The input current I_{IN}

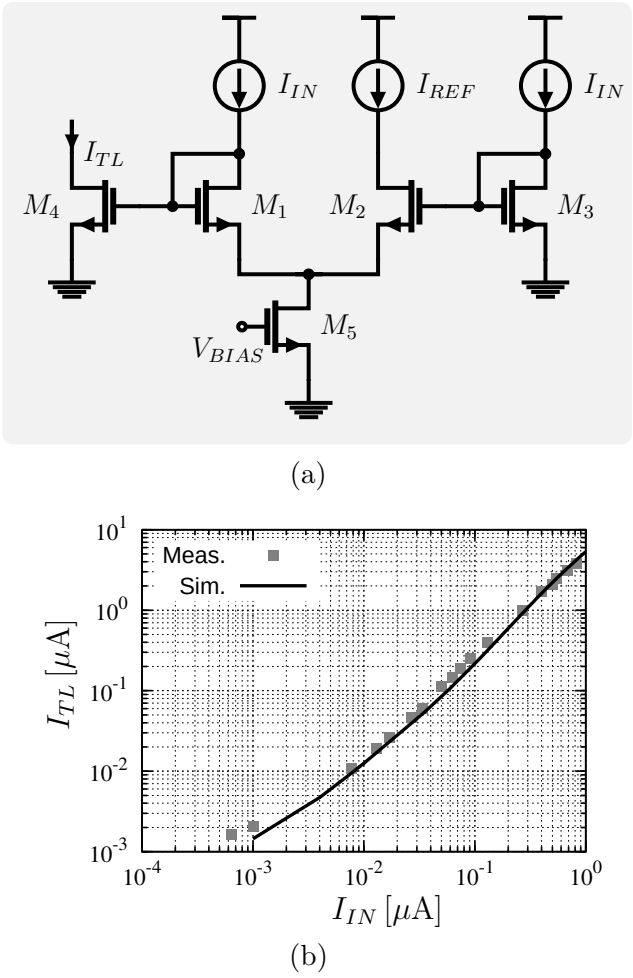
is mirrored to M_1 and M_3 and an on-chip reference current is copied to M_2. Using this circuit we have that:

$$I_{TL} = \frac{I_{IN}^2}{I_{REF}}, \tag{4.12}$$

as we have previously calculated.

We plot the simulated and measured results of this designed translinear loop in Fig. 4.10(b). Ideally, if $I_{IN} = 300\,\text{nA}$ and $I_{REF} = 100\,\text{nA}$, we have that $I_{TL} = 900\,\text{nA}$. If we set these input values in the circuit simulator we get that $I_{TL} = 960\,\text{nA}$, which is close to the desired value. We can see an interesting result when $I_{TL} > 1\,\mu\text{A}$. For instance, if $I_{IN} = 1\,\mu\text{A}$ and $I_{REF} = 100\,\text{nA}$, the output current is $\cong 5\,\mu\text{A}$ and not $10\,\mu\text{A}$, as we would expect. This happens because the aspect ratio of the transistors is equal to 2.5 and for currents higher than $1\,\mu\text{A}$, the transistors leave weak inversion and (4.10) is not valid anymore.

Figure 4.10: (a) Translinear loop using MOS transistors and (b) simulated and measured I_{TL} versus I_{IN} of this translinear loop.



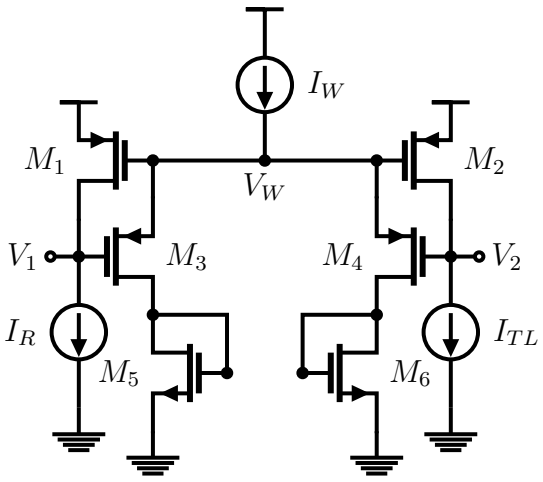
Source: The author.

Using the IBM 0.13 CMOS process we have implemented the translinear loop with M_1=M_2=M_3=M_4 with aspect ratio: $W_{tot}/L = 5\,\mu\text{m}/1.5\,\mu\text{m}$. M_5 by its turn has an aspect ratio equal to $W_{tot}/L = 5\,\mu\text{m}/2\,\mu\text{m}$.

4.4 WINNER TAKE ALL

The winner-take-all (WTA) block can be considered as a network of competing cells that reports the response of the most active cell. These circuits were implemented in CMOS in the 1980s, as we can see in [30]. In that work, it was used as a component in VLSI sensory systems that perform auditory localization [30]. We use the WTA circuit to compare the translinear loop output current (I_{TL}) with the reference current (I_R) and define when the LC network is tuned.

Figure 4.11: PMOS-based winner-take-all circuit.



Source: Based on [30].

We can view a WTA circuit in Fig. 4.11 and to understand this cell we first consider that: $I_{TL} = I_R = I_X$, where I_X is an arbitrary value for these currents; the transistors have the same dimensions and are operating in weak inversion. Then, I_X can be calculated as:

$$I_X = I_S e^{\frac{\frac{V_{TH}-V_W}{n}+V_{DD}}{U_t}}, \tag{4.13}$$

and I_W is equal to:

$$I_W = 2I_S e^{\frac{\frac{V_{TH}-V_\alpha}{n}+V_W}{U_t}}, \tag{4.14}$$

where $V_\alpha = V_1 = V_2$. Then, we can rearrange (4.14) to:

$$V_\alpha = V_{TH} + nV_W - nU_T \ln \frac{I_W}{2I_S}, \tag{4.15}$$

where

$$V_W = V_{TH} + nV_{DD} - nU_T \ln \frac{I_X}{I_S}, \tag{4.16}$$

using (4.13). Replacing V_W in (4.15) we have that:

$$V_\alpha = V_{TH}(n+1) + n^2 V_{DD} - n^2 U_T \ln \frac{I_X}{I_S} - n^2 U_T \ln \frac{I_W}{2I_S}. \tag{4.17}$$

Then, if $I_R \neq I_{TL}$ we have that:

$$V_1 - V_2 = n^2 U_T \left(-\ln \frac{I_R}{I_S} + \ln \frac{I_{TL}}{I_S} \right) = n^2 U_T \left(\ln \frac{I_{TL}}{I_R} \right). \tag{4.18}$$

Using (4.18) we note that if M_2 drives more current than M_1, $V_1 > V_2$. This happens because V_W decreases in this situation, as we can see in (4.16). And since M_1 and M_2 share the same gate voltage, when V_W decreases V_1 must increase to keep I_R constant.

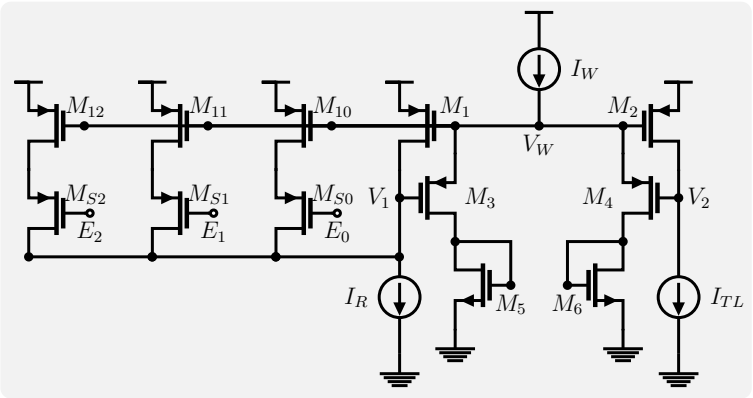
If M_1 has an aspect ratio A times M_2 we have that:

$$V_1 - V_2 = n^2 U_T \left(\ln \frac{I_{TL}}{A I_R} \right). \tag{4.19}$$

Hence, V_1 is equal to V_2 when I_{TL} is equal to AI_R.

Suppose that we implement a WTA circuit based on the results of (4.19) in Fig. 4.12. With this circuit we can scale the activeness of the left WTA cell when the M_{Sx} transistors, implemented as switches, are on/off. We can design M_1 with an aspect ratio 3 times smaller than M_2. So, when the switches are off we have $V_1 = V_2$ when $I_{TL} = 3I_R$. When all the switches are on, the transistors have an equivalent aspect ratio equal to M_2.

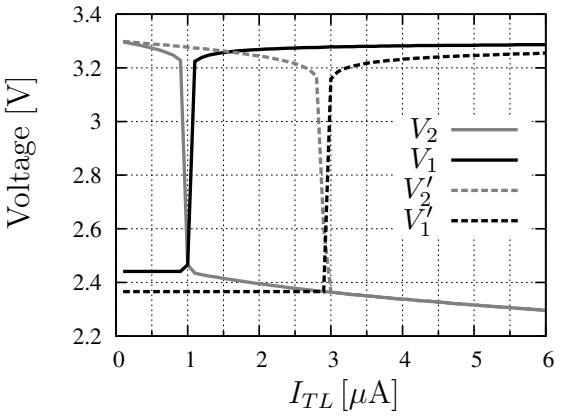
Figure 4.12: PMOS-based winner-take-all circuit that can scale I_R.



Source: The author.

The output voltages of the implemented WTA circuit versus I_{TL} can be seen in Fig. 4.13, for two values of A. If $I_R = 1\,\mu$A and $A = 1$ (switches are on), $V_1 = V_2$ when $I_{TL} = 1\,\mu$A. For $A = 1/3$ (switches are off), we have that $V_1' = V_2'$ when $I_{TL} \cong 3I_R$. Now it is clear that the aspect ratio of the WTA transistors can be used to artificially scale I_R and consequently reduce the power consumption required to compare higher currents.

Figure 4.13: WTA output voltages versus I_{TL}.

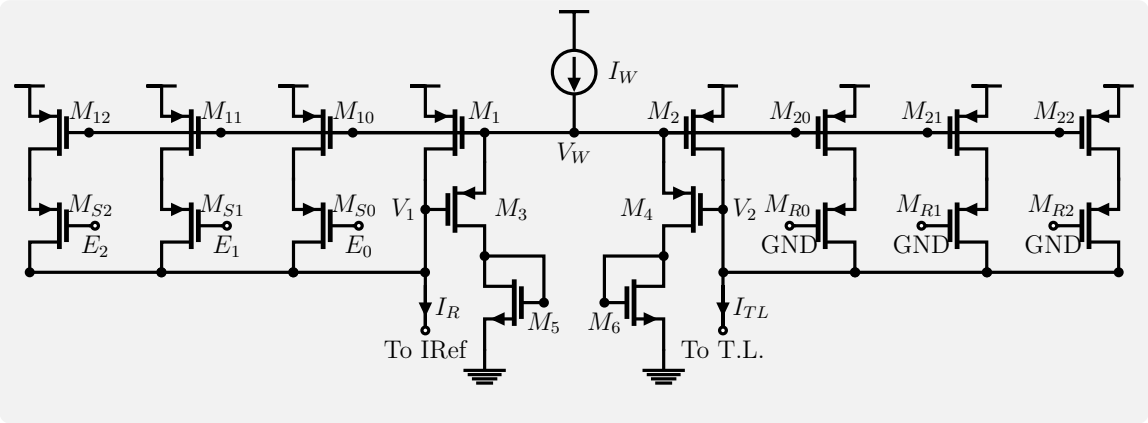


Source: The author.

For a good layout matching, we make this WTA circuit symmetric around V_W (in one direction), as it is seen in Fig. 4.14. We keep M_1 and M_2 with the same size, duplicate the

structure used to scale I_R and place it on the right WTA cell, as if it was going to scale I_{TL}. The difference is that the copied switches are always on.

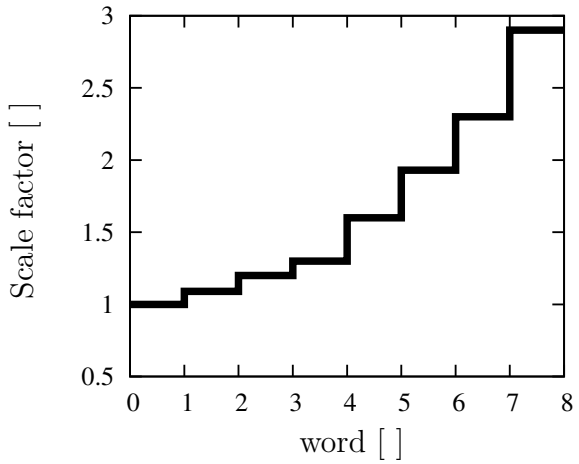
Figure 4.14: Implemented pMOS-based winner-take-all circuit.



Source: The author.

The aspect ratio (A) of the scaling transistors is implemented so that $A_{M_{12}} > A_{M_1} > A_{M_{11}} > A_{M_{10}}$ and $A_{M_{12}} + A_{M_1} + A_{M_{11}} + A_{M_{10}} = A_{M_{22}} + A_{M_2} + A_{M_{22}} + A_{M_{20}}$. The most significant bit that controls the WTA scale is E_2. We plot in Fig. 4.15 the scale factor of the implemented WTA versus its digital control word. We note that if high currents are compared (this is when the control words are between 7 and 4), the steps seen on the scale factor are bigger in contrast to the small steps seen when lower currents are compared (words between 3 and 0).

Figure 4.15: Scale factor of the implemented WTA versus its digital control word.



Source: The author.

4.4.1 Component Sizing

It is possible to view the used component sizes/values of the implemented pMOS-based winner-take-all circuit in table 4.2.

Table 4.2: Component sizes/values of the implemented pMOS-based winner-take-all circuit.

Component	**Value**	**Additional data**
I_1	300 nA	
M_1, M_2	$W_{tot}/L = 5\,\mu m/1.5\,\mu m$	fingers = 1, multiplicity = 1
M_3, M_4	$W_{tot}/L = 15\,\mu m/1.5\,\mu m$	fingers = 1, multiplicity = 1
M_5, M_6	$W_{tot}/L = 5\,\mu m/0.4\,\mu m$	fingers = 1, multiplicity = 1
M_{S0}, ..., M_{S2}, M_{R0}, ..., M_{R2}	$W_{tot}/L = 5\,\mu m/0.4\,\mu m$	fingers = 1, multiplicity = 1
M_{10}, M_{20}	$W_{tot}/L = 1.4\,\mu m/1.5\,\mu m$	fingers = 1, multiplicity = 1
M_{11}, M_{21}	$W_{tot}/L = 2.8\,\mu m/1.5\,\mu m$	fingers = 1, multiplicity = 1
M_{12}, M_{22}	$W_{tot}/L = 5.8\,\mu m/1.5\,\mu m$	fingers = 1, multiplicity = 1

Source: The author.

4.5 INDEPENDENT CURRENT REFERENCE

A standard CMOS current reference found in [31] and seen in Fig. 4.16 is implemented in this tuning system. This current reference is made up by the current mirror composed by M_3 and M_4, that fix the ratio of the branch currents and by M_1, M_2, and R_1 that are responsible to set the value of I_1 and I_2. I_2 can be written as:

$$I_2 = \frac{V_{GS1} - V_{GS2}}{R_1}. \tag{4.20}$$

If the transistors are saturated and in weak inversion:

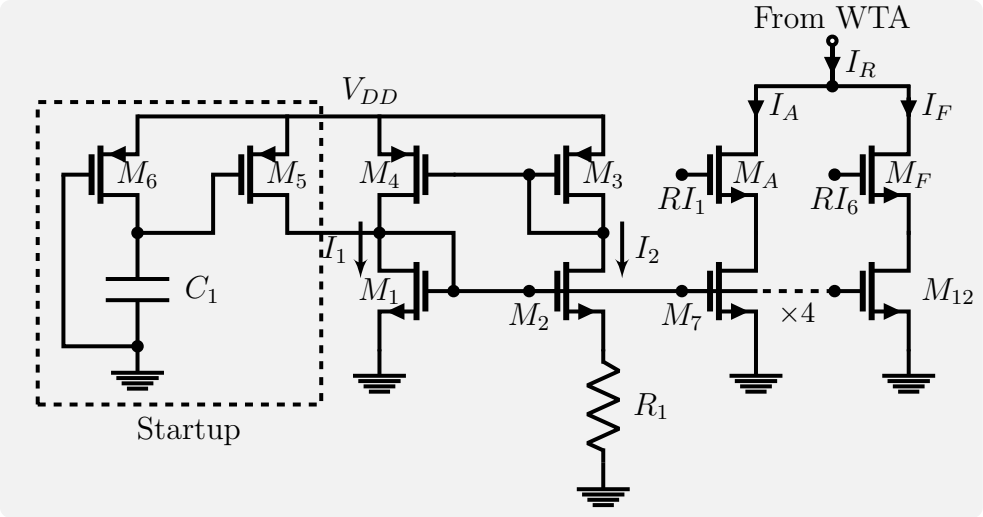
$$I_2 = \frac{1}{R_1}\left[V_{TH1} + n_1 U_T \ln\frac{I_1}{I_{S1}} - \left(V_{TH2} + n_2 R_1 I_2 + n_2 U_T \ln\frac{I_2}{I_{S2}} - R_1 I_2\right)\right]. \tag{4.21}$$

Solving the previous equation for I_2, considering that $V_{TH1} = V_{TH2}$ and $n_1 = n_2$, we get that:

$$I_2 = \frac{1}{R_1}\left[U_T \ln\left(\frac{I_1 I_{S2}}{I_2 I_{S1}}\right)\right]. \tag{4.22}$$

So I_2 can be increased by either reducing R_1 or by increasing the ratio between I_{S2} and I_{S1}.

Figure 4.16: Implemented current reference based on CMOS transistors.



Source: The author.

Usually, these current references have two operating points. One is at the nominal specification and another at the origin, where the branch currents I_1 and I_2 are zero. To avoid the

latter operating point, we use the circuit within the dashed rectangle in Fig. 4.16, that is known as a startup circuit. This circuit drives I_1 when V_{DD} is rising to its nominal value. Once V_{DD} is settled and C_1 is charged, M_5 turns off, and the branch currents have their designed values.

I_1 is used as a reference current and it is copied by transistors M_7 to M_{12}, that have an aspect ratio m_i times the aspect ratio of M_1. We designed the current mirrors so that M_7 is the transistor with the smaller aspect ratio $m_7 = 1/8$. m doubles every time the index i is increased by one, then M_{12} has $m_{12} = 4$.

4.5.1 Component Sizing

It is possible to view the used component sizes/values of the implemented independent current reference circuit in table 4.3.

Table 4.3: Component sizes/values of the implemented pMOS-based winner-take-all circuit.

Component	**Value**	**Additional data**
C_1	680 fF	
M_6	$W_{tot}/L = 1\,\mu$m$/4.5\,\mu$m	fingers = 1, multiplicity = 1
M_5	$W_{tot}/L = 5\,\mu$m$/0.4\,\mu$m	fingers = 1, multiplicity = 1
M_1,M_2	$W_{tot}/L = 10\,\mu$m$/5\,\mu$m	fingers = 1, multiplicity = 1
M_4,M_3	$W_{tot}/L = 10\,\mu$m$/5\,\mu$m	fingers = 1, multiplicity = 1
R_1	12 kΩ	
M_A, ..., M_F	$W_{tot}/L = 5\,\mu$m$/0.4\,\mu$m	fingers = 1, multiplicity = 1
M_7	$W_{tot}/L = 2.5\,\mu$m$/5\,\mu$m	fingers = 1, multiplicity = 1
M_8	$W_{tot}/L = 5\,\mu$m$/5\,\mu$m	fingers = 1, multiplicity = 1
M_9	$W_{tot}/L = 10\,\mu$m$/5\,\mu$m	fingers = 2, multiplicity = 1
M_{10}	$W_{tot}/L = 10\,\mu$m$/5\,\mu$m	fingers = 2, multiplicity = 2
M_{11}	$W_{tot}/L = 10\,\mu$m$/2.5\,\mu$m	fingers = 2, multiplicity = 2
M_{12}	$W_{tot}/L = 20\,\mu$m$/2.5\,\mu$m	fingers = 4, multiplicity = 2

Source: The author.

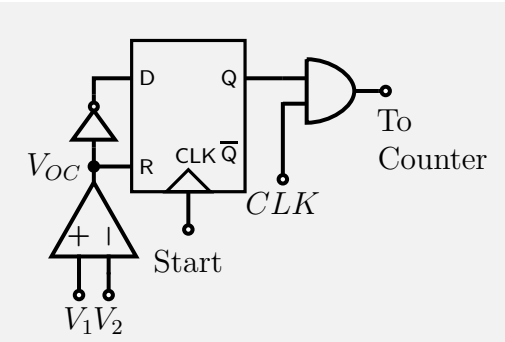
4.6 CONTROLLER AND COUNTER BLOCKS

We can see in Fig. 4.17 the implemented controller. We use the voltage comparator to define when the reference current (I_R) is lower than the translinear-loop output current (I_{TL}). The output of this comparator is connected to a digital controller that stops the tuning process if the system is considered tuned. The controller is composed by a D flip-flop that receives, on its clock input, an external start signal that starts the tuning sequence. After the positive edge of the start signal, the flip-flop enables the counter if the voltage comparator output, that is connected to its D input, is equal to 0 V. However, when the voltage comparator output goes to on, the flip-flop resets and the counting process stops.

We show in Fig. 4.18 the implemented 14-bit assynchronous binary counter that is used to sweep: the equivalent capacitance of the bank of capacitors; the reference current of the WTA (I_R); and its equivalent 'weight' on the WTA.

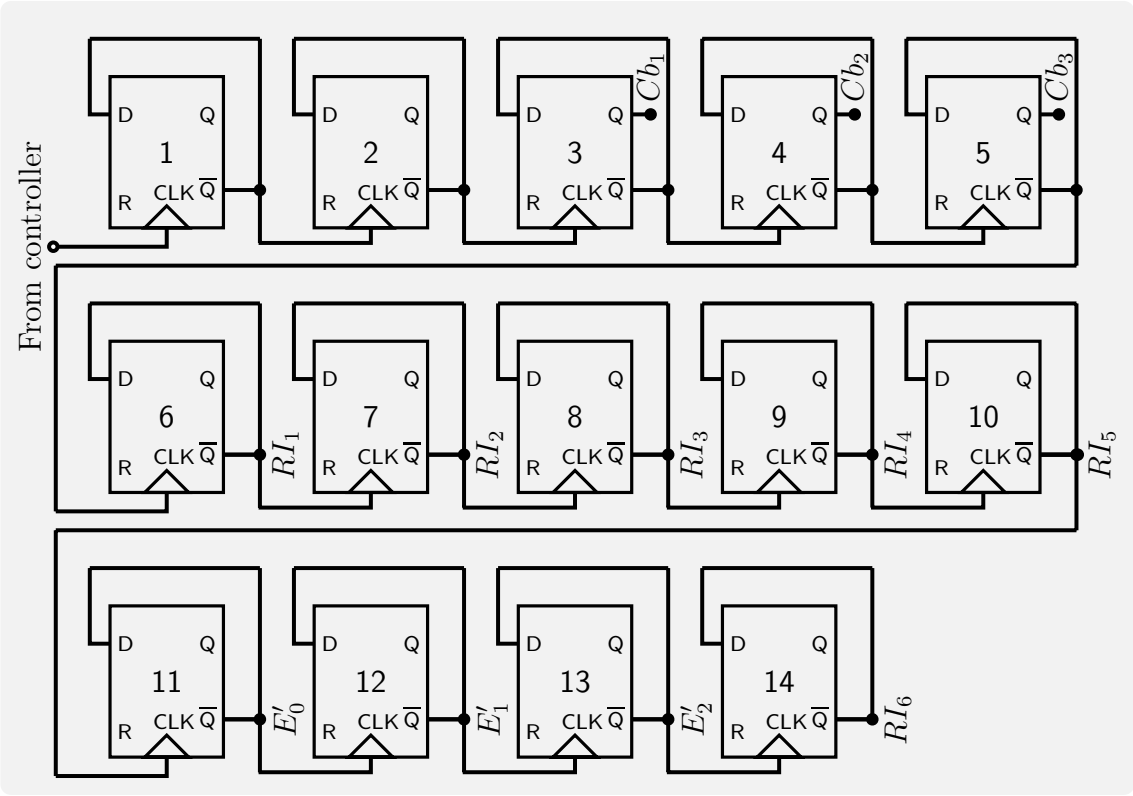
The two less significant bits of this counter are used to divide the clock frequency and wait for the transient response of the LC network. After this transient period Cb_1, Cb_2, and Cb_3 are used to sweep the capacitance of the capacitor bank. Next we take RI_1 to RI_5 to control the reference current value (I_R) of the WTA circuit. These signals decrease I_R if I_{TL} is not considered higher than I_R, when all capacitors are tested. If the LC network is still not

Figure 4.17: Implemented controller.



Source: The author.

Figure 4.18: 14-bit counter and its labeled connections to other circuits.

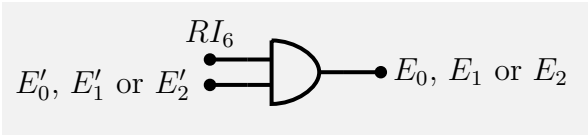


Source: The author.

considered tuned by the WTA, the scaling factor of I_R is decreased by E'_0 and the switching is repeated. All the reset pins of the flip-flops are connected together and they are externally reseted.

When all the scale factors of the WTA are decreased and the system is not tuned, we further decrease the reference current turning RI_6 off. This would be a situation where the tag is far away from the reader. When this happens we don't need to scale up I_R anymore. Then, we disable E'_0, E'_1 and E'_2 and the WTA compares I_{TL} and I_R with the same scale. We generate the WTA scale signals (E_0, E_1, E_2) with an AND operation with EI_6, as we see in Fig. 4.19.

Figure 4.19: AND operation with the counter signals that controls the WTA scale factor.

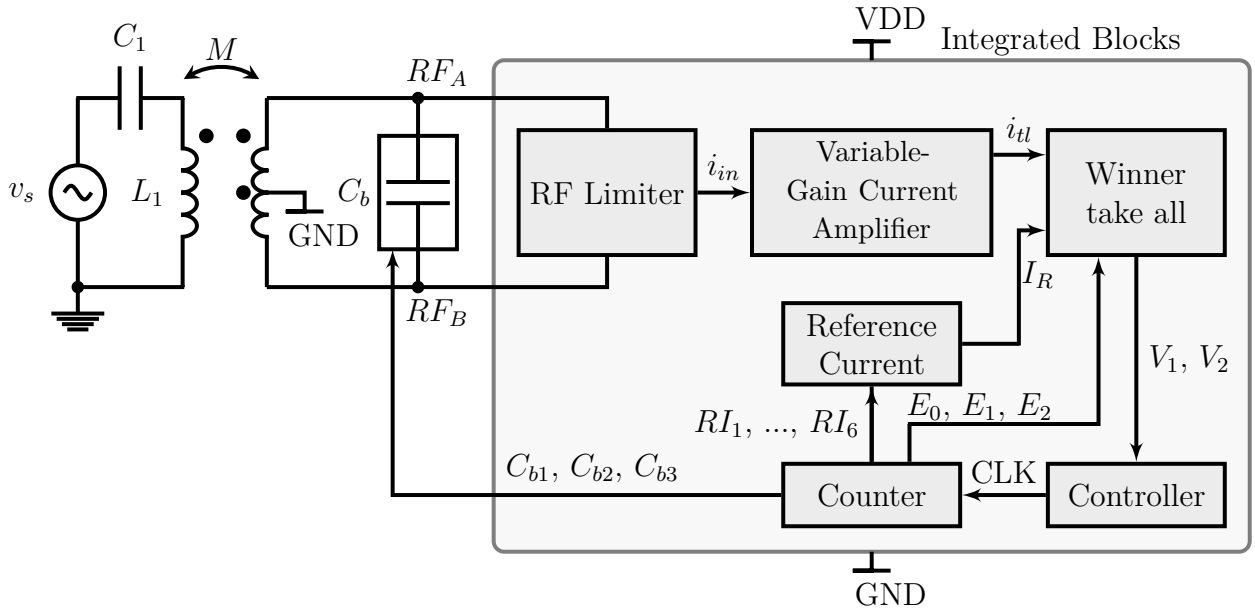


Source: The author.

4.7 SYSTEM BEHAVIOR

In this section we show the behavior of the implemented system based on the circuit seen in Fig. 4.20. Note in this figure that the main signals of the integrated system are written, for the reader convenience. The results shown in this section are obtained using transient simulations.

Figure 4.20: Circuit used to simulate the designed tuner and its main nets and current names.



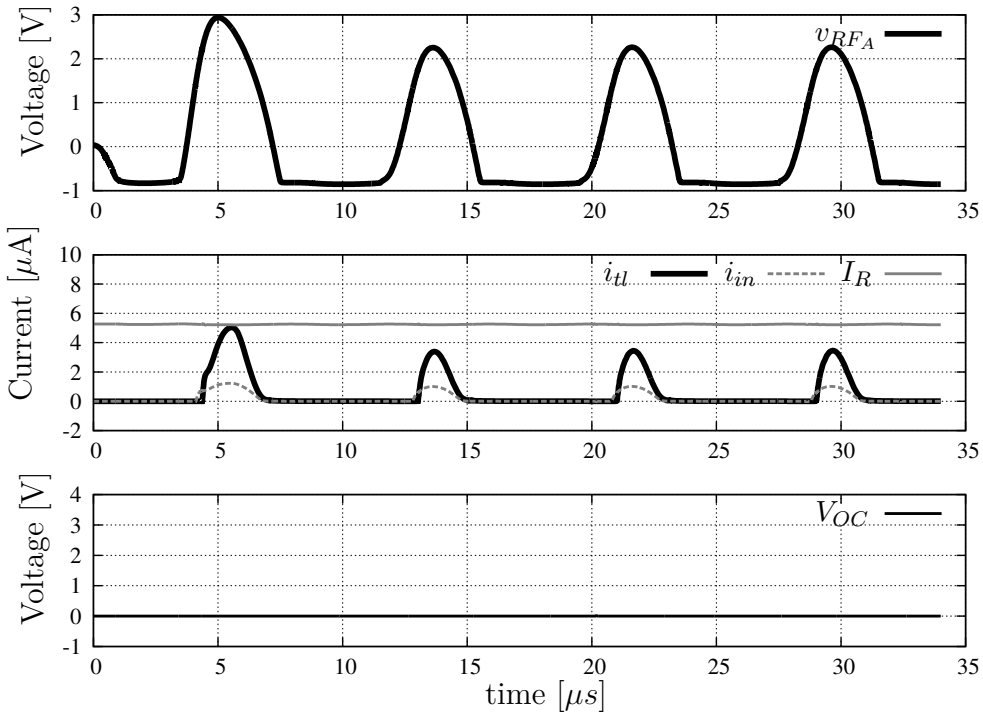
Source: The author.

For the first test we do not scale-up the reference current (I_R) and we keep the same equivalent capacitance of the LC network. It is possible to see the results of this test in Fig. 4.21. The input voltage in one side of the LC network (v_{RF_A}) is shown and it is in phase with the mirrored current from the RF limiter (i_{in}). I_R is always higher than the output current of the translinear loop i_{tl} and consequently the output of the voltage comparator (V_{OC}) is always off.

We show in Fig. 4.22 a case where I_R is lower than the peak of i_{tl} and consequently V_{OC} switches between the on and off states. We note that i_{tl} and I_R change their behavior when i_{tl} is higher than I_R. It seems that a glitch is observed. But, since both currents (i_{tl} and I_R) are connected to the WTA circuit and when i_{tl} is considered higher than I_R, the drain voltages V_1 and V_2 have a shift of approximately 0.8 V, as we see in Fig. 4.13. Since the drain-to-source current of the MOS transistors also depends on their drain-to-bulk voltage, we have the observed "glitch" behavior when $i_{tl} > I_R$.

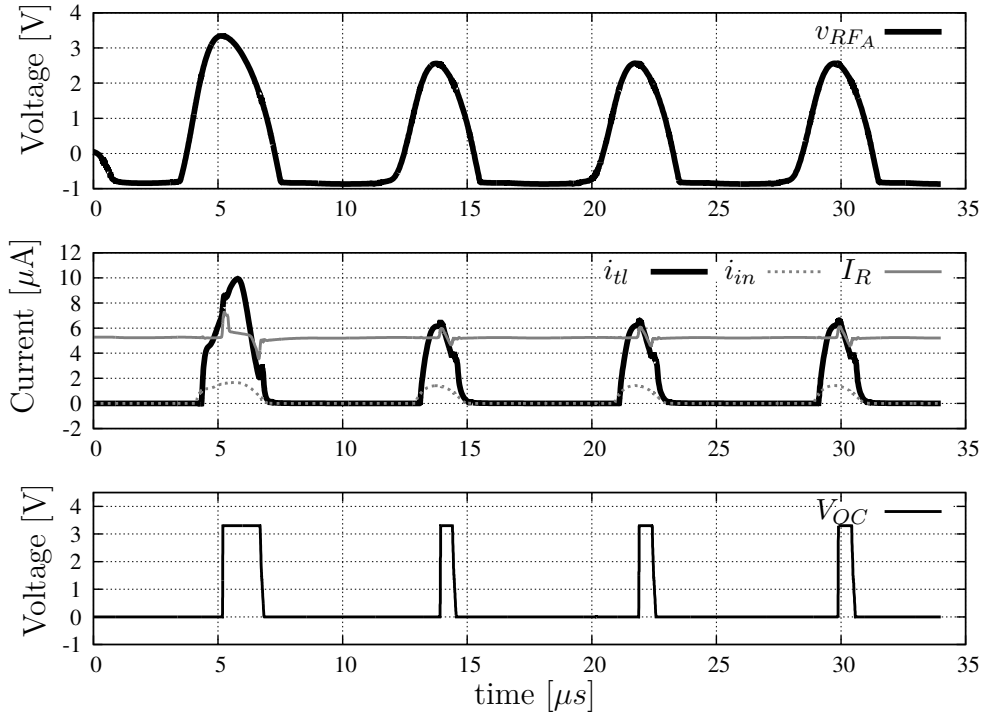
It is also important to see the behavior of i_{tl} when the equivalent capacitance of the bank of capacitors is changed. Then, we show in Fig. 4.23 a typical tuning sequence with the less

Figure 4.21: Main signals of the tuner when I_R is always higher than i_{tl} .



Source: The author.

Figure 4.22: Main signals of the tuner when I_R is lower than the peak of i_{tl}.

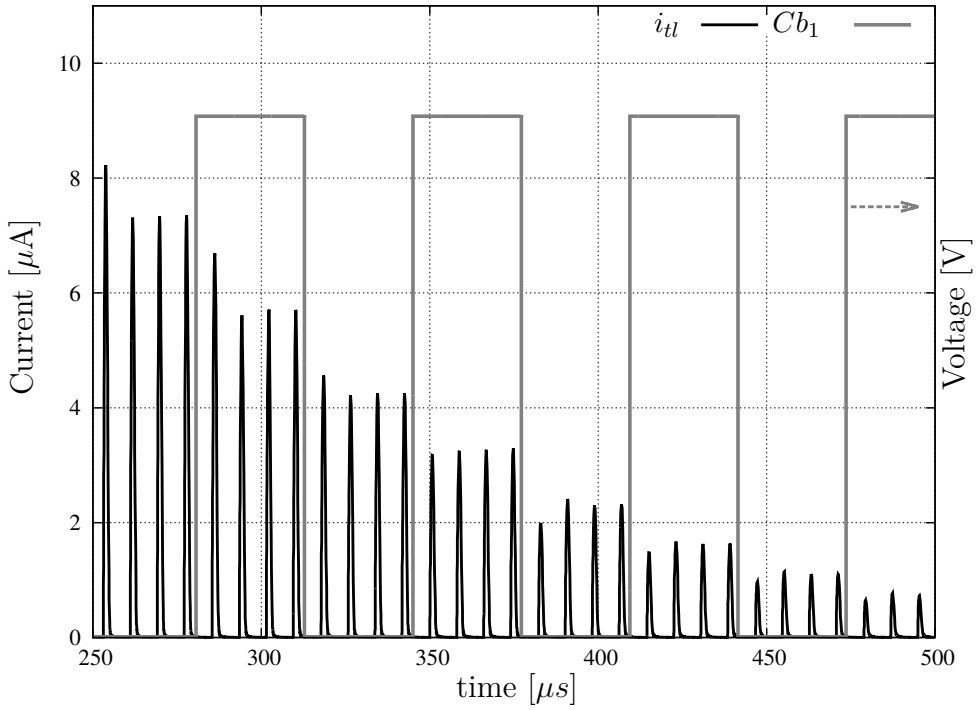


Source: The author.

significant bit that controls the bank of capacitor represented by Cb_1. In this simulation, eight different capacitances are tested and the system does not stop the tuning process during this sweeping.

We show the transient response of I_R, in Fig. 4.24. It is considered that the system is not tuned along the given time window. This current goes from 4.7 μA to 2.45 μA in 8.2 ms. If the

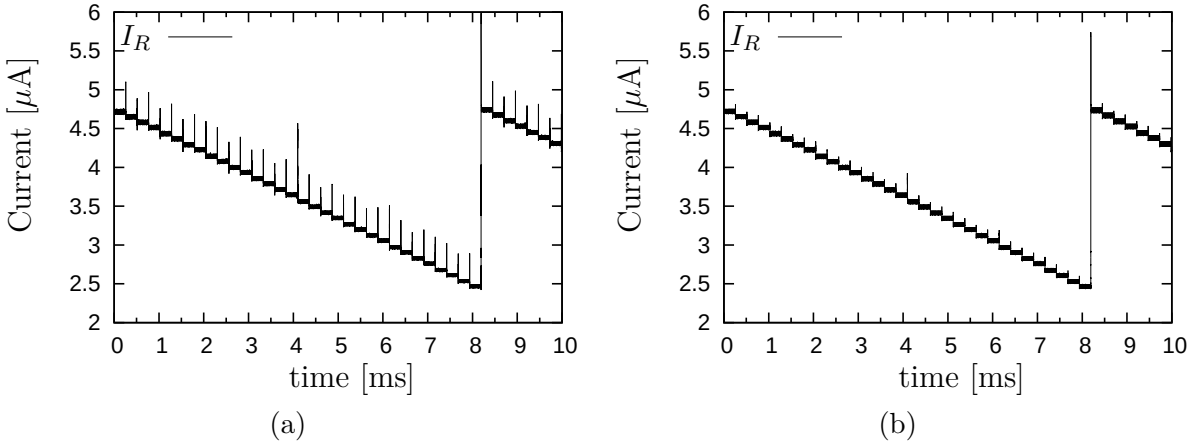
Figure 4.23: Transient response of i_{tl} when the capacitance of the LC network is changed.



Source: The author.

controller does not consider that the system is tuned during the first current sweep, I_R resets to its initial value and the tuning procedure is repeated with the WTA operating with a reduced scale factor for I_R.

Figure 4.24: I_R behavior along the tuning procedure with (a) Clock feedthrough noise and with a reduced noise in (b).



Source: The author.

It is possible to see a glitch every time that I_R decreases/increases. This glitch is due to the 'clock' feedthrough noise effect [32]. This effect happens when a high speed signal is used to open/close MOS switches. The sharper the rise/fall time the higher the frequency components presented in the signal. The higher the frequency the lower is the reactance of the capacitance between drain/source and gate. This means that a fast transient current/voltage can flow from drain/source to the gate of the transistor. This effect does not affect the tuning system, since it happens when $i_{tl} = 0\,\text{A}$. A 2-pF capacitor connected to ground and on the I_R node reduces

the clock feedthrough noise seen by the WTA, as seen in Fig. 4.24(b).

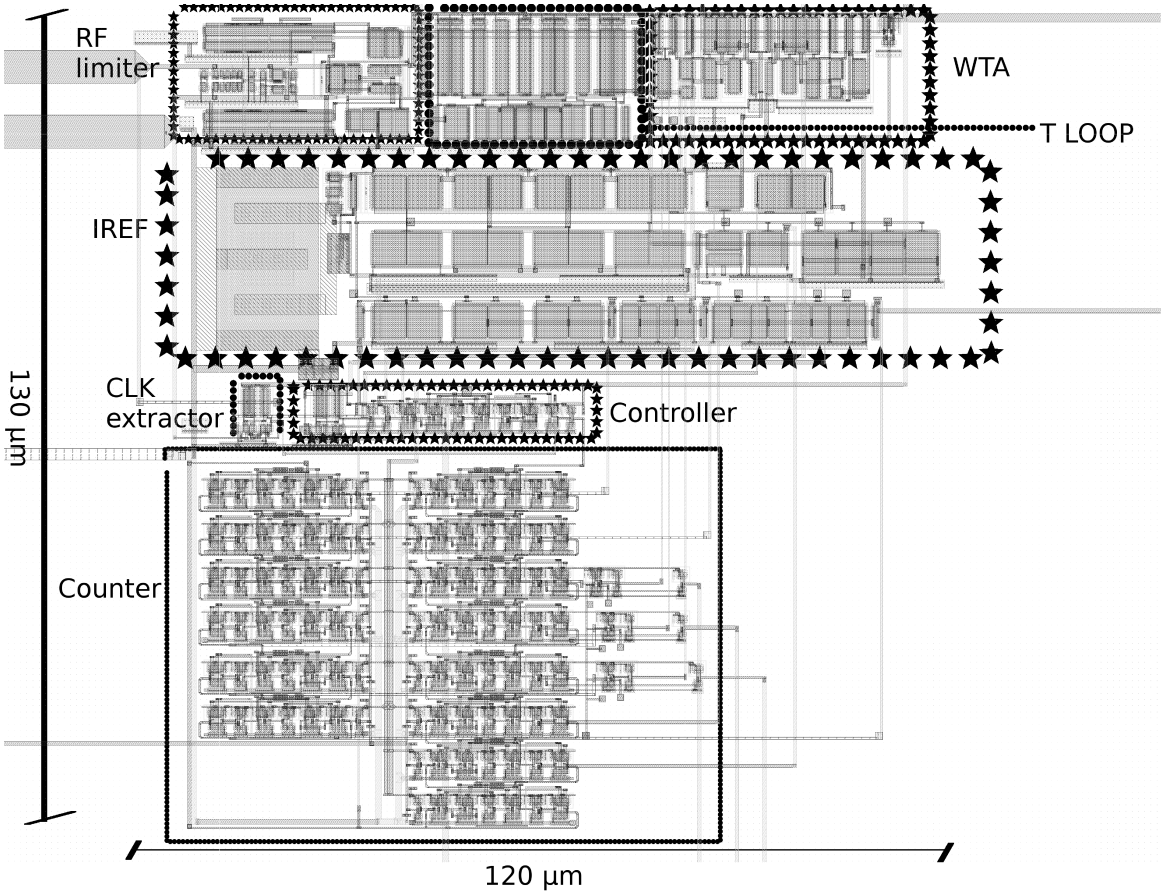
The prototype has an average current consumption of 10 μA with: VDD= 3.3 V; $i_{tl} = 5\,\mu$A of peak; and $I_R \cong 5\,\mu$A. Note that half of the current consumption is due to I_R. So, if one needs to decrease the power consumption I_R and i_{tl} can be reduced. We also spend 550 nA with I_1 and with I_2 of the current reference.

For the implemented system, and considering an input signal frequency of 125 kHz ($T = 1/f = 8\,\mu$s), we have a nominal tuning time approximately equal to 32 ms ($= 8\,\mu\text{s}(2^{12})$). This time is calculated considering that the circuit tunes when the 13th flip-flop toggles for the first time. The slowest tuning time, considering that the tag is far away from the reader takes approximately 139 ms ($= 8\,\mu\text{s}(2^{14} + 2^{10})$).

4.8 MEASUREMENT RESULTS

We implemented this *LC* tuner in a standard 130-nm CMOS process and the layout of this IC can be seen in Fig. 4.25. The designed blocks can be seen enclosed by the dots and by the stars. It is shown that this tuner occupies an area of 130 μm x 120 μm.

Figure 4.25: Layout of the implemented *LC* tuner.

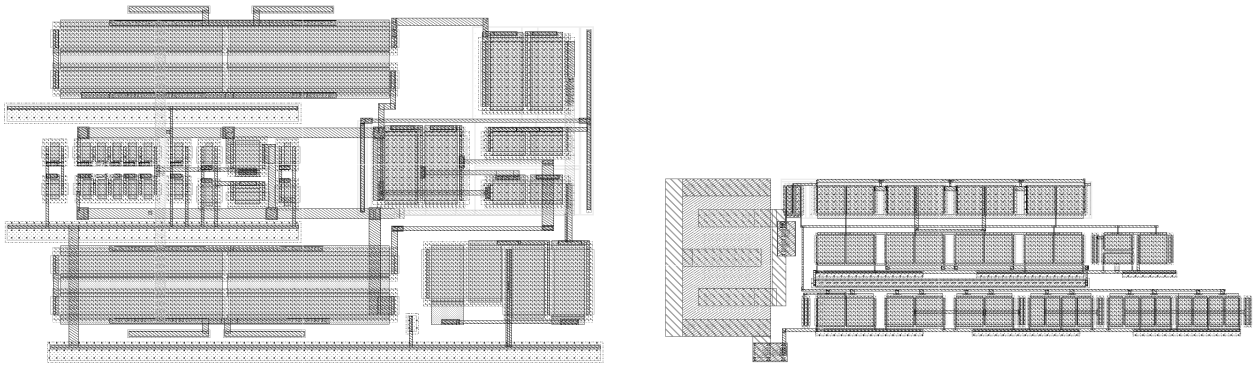


Source: The author.

In Figs. 4.26 and 4.27 the reader can see the layout zoom of the designed RF limiter, current source, WTA, and VGCA.

The prototype of the system presented in this chapter was fabricated using the MOSIS educational program. We also asked MOSIS to encapsulate this chip using a DIL-48 package. We can see a photo of this encapsulated chip in Fig. 4.28(a). In this figure we delimited with

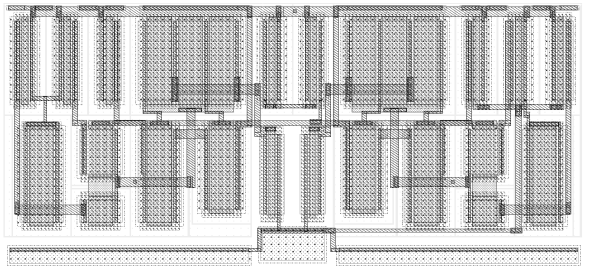
Figure 4.26: Layout of the designed RF limiter and the current source in (a) and (b), respectively.



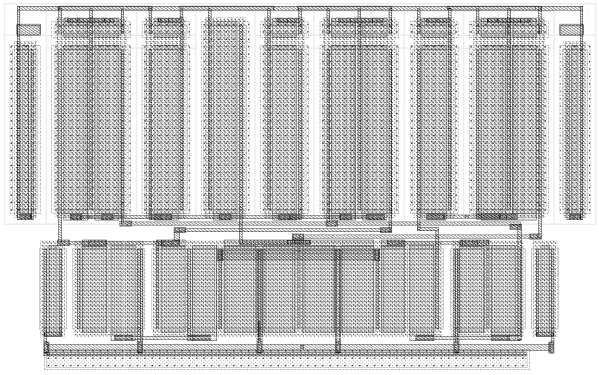
(a) (b)

Source: The author.

Figure 4.27: Layout of the designed WTA and the VGCA in (a) and (b), respectively.



(a)



(b)

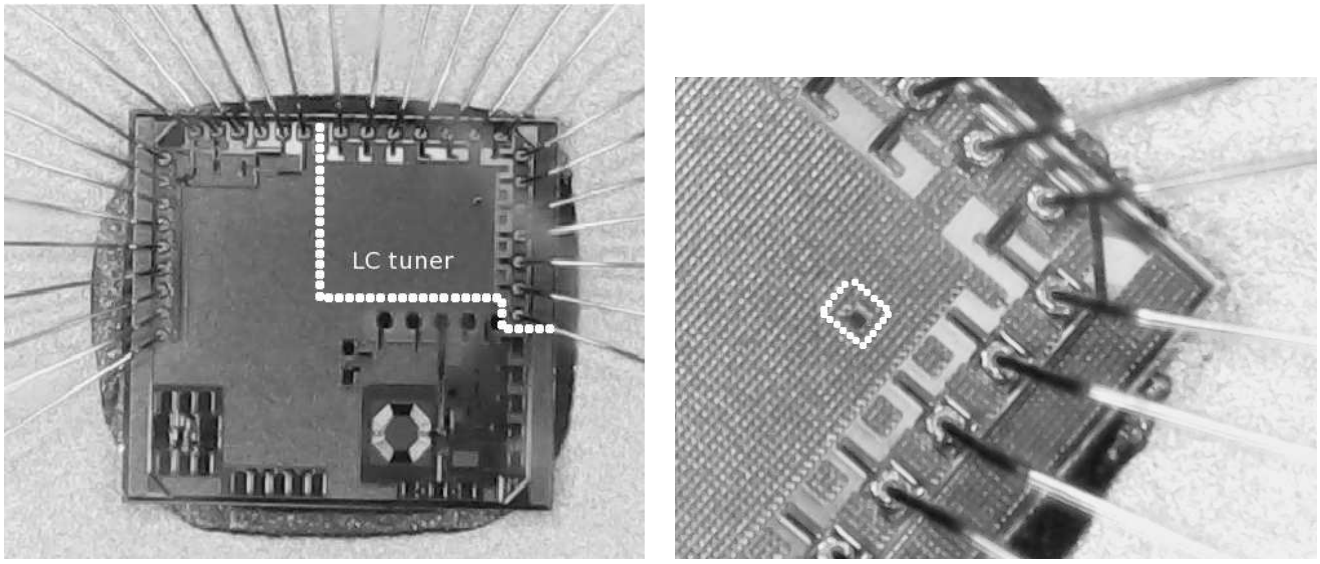
Source: The author.

white dots the pads used for this system. In Fig. 4.28(b) it is possible to see, enclosed by the white dots, the location where the LC tuner is placed. Note that the implemented system area is in the order of magnitude of a pad.

We show in Fig. 4.29 the main measured result from a prototype of the presented LC tuner. The voltage with respect to ground of one side of the LC network is shown (v_{in}) and it is also seen the current from the translinear loop (i_{tl}) and the current from the current reference (I_R).

It is possible to see that I_R is artificially multiplied by 3 by the WTA cell, from Fig. 4.29.

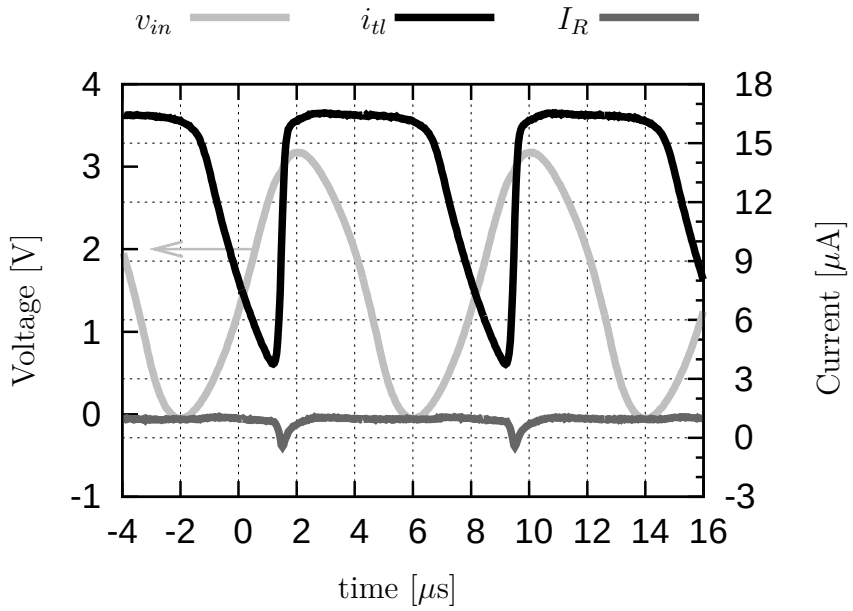
Figure 4.28: (a) Designed 2 mm x 2 mm chip and (b) chip zoom highlighting the area used by the proposed *LC* tuning system.



(a) (b)

Source: The author.

Figure 4.29: Main measured signals of the presented *LC* tuner.



Source: The author.

This can be inferred because the minimum peak of I_R happens when $i_{tl} \cong 3\,\mu$A.

We validated the current reference using a 200-run Monte Carlo simulation. In this run, I_1, which is used as the reference current for the other blocks, is between 430 nA and 750 nA with an average of 580 nA (I_R is between 3.3 μA and 7.2μA). Using corners simulation I_1 is between 540 nA and 620 nA for SSF (slow/slow functional) and FFF (fast/fast functional) corners, respectively. Unexpectedly, in the measurements results I_R is close to 1 μA while it should be around 5 μA according to the simulation. Hence, we concluded that I_1 reduced approximately by 4 to 5 times. This effect may be to a process variation that was not taken into account by

the model of the used PDK.

The translinear-loop output current (i_{tl}) is inversely proportional to the value of I_1. Hence if I_1 is extremely reduced, i_{tl} is amplified and goes above its designed limits that nominally should be around 7 μA.

The current reference presented a measured value below its expected value and due to this, no other measurements can be made.

In table 4.4 we report the lab. equipment used to make the presented measurement results.

Table 4.4: Equipment used in the laboratory to obtain the presented measurement results.

Equipment	**Seller**	**Additional data**
Arbitraty waveform generator	Agilent	33220A, 20 MHz
Voltage Source	Agilent	E3634A
Source Measurement Unit (SMU)	Agilent	B2902A
Oscilloscope	Agilent	DSO-x-2014, 1 Gsample/s, 4 channel scope
Probe	Agilent	N2862B, 10:1, 150 MHz, passive, 10 MΩ//15 pF

Source: The author.

4.9 SUMMARY

In this chapter an *LC* tuner based on the RF limiter current is presented. It is designed to complement the tuning method based on negative resistances, as explained.

During the chapter the basic blocks of the tuner are briefly explained and the implemented circuits are presented. It was also shown how to decrease the required power consumption of the system by scaling the aspect ratio of the transistors of the WTA.

We have measured a prototype that seems to be working well, except for the value of the reference current that is below the expectations. Due to that, another chip with a current source, that can be externally connected to the circuit, will be designed. By doing this, we will have a better control of the current source and if it deviates from the expected value, an external current can be used as a reference.

5 HIGH FREQUENCY LC PARAMETER EXTRACTOR

In this chapter we report the analysis and design of an LC parameter extractor. This system is intended to be used to obtain the quality factor of LC networks. In addition to this, it can be used to estimate if the LC network is detuned with the input signal.

Due to the relatively low Q of the designed integrated inductors (around 15), the PhD candidate at Carleton had to use negative resistances to compensate the losses of the system, and consequently have a low insertion loss in the desired filter bands. The implemented LC network with a quality factor approximately equal to 200 would result in an insertion loss $< 1\,\text{dB}$, as required by the filter.

Since negative resistances were used, it is necessary to have a control system that tells if the equivalent Q needs to be increased/decreased. This kind of control is necessary mainly because we want limit the current that increases the Q of the LC tank and there is also a concern on the stability of the system.

With this scenario, we proposed to study and conceive a new system that would be able to control the Q of LC networks. We were aiming in low-area solutions, so the new circuit would not have a significant impact on the filter area.

5.1 COMMONLY IMPLEMENTED SELF-TUNED LC FILTERS

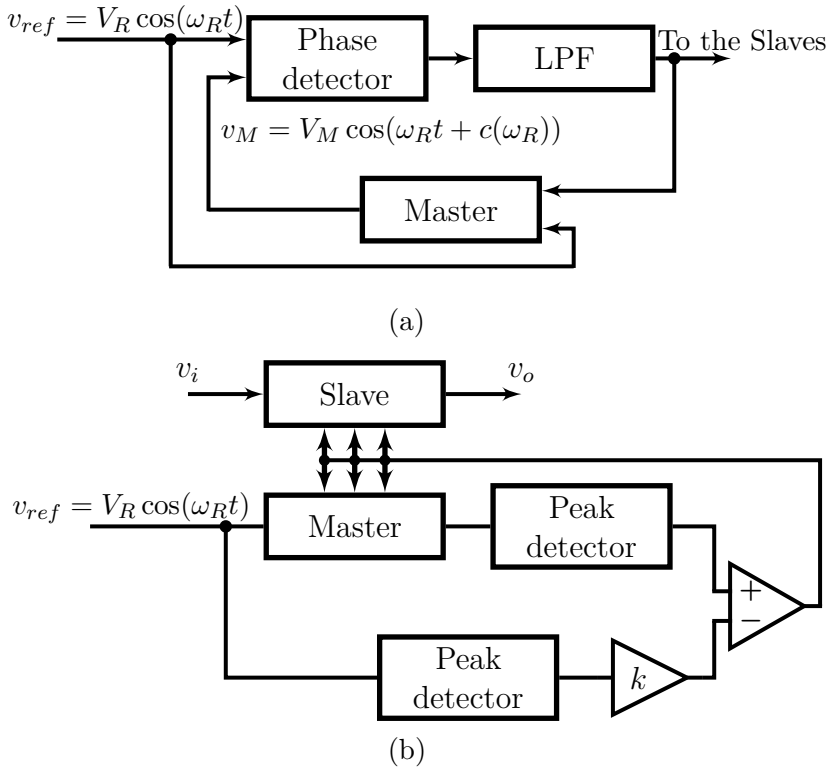
The high demand for low-cost wireless receivers motivated the LC bandpass (or notch) filters to be implemented on-chip as we can see in [33], [34], [35], and [36]. In these papers the authors use negative resistances to increase the quality factor of their resonating networks. When a negative resistance is used as a Q-enhancement device, an automatic tuning system is highly recommended to compensate the effects of divergences in the nominal frequency response due to process variation and aging.

One method that is commonly implemented for frequency and Q tuning is described in [37]. In this case a second filter named 'Master' is designed to model the behavior of the main filter called 'Slave'. The main idea of this tuning scheme is that a reference signal is applied to the input of the 'Master'. Then, the output of the master filter is processed and it controls the 'Slave' filter. We can see a block diagram of a Q and frequency tuning system, using the Master-slave method, in Fig. 5.1.

We note that a PLL is used to tune the frequency of the Slave filter in Fig. 5.1(a). In this case the error signal is applied to the master and to the slave to correct frequency errors. As we know, the phase of the transfer function of the filter is zero when the filter resonates with the input signal. Then, the scheme of Fig. 5.1(a) tunes the slave by minimizing the error signal that controls the master and the slave filter. We show in Fig. 5.1(b) a magnitude locked loop that controls the Q of the LC network. As we will see in the next section (or according to chapter 3), the voltage on the filter can be proportional to Q, when the resonance frequency of filter is equal to the incoming signal frequency. Then, the desired quality factor is set by the lower peak detector followed by an amplifier with fixed and relatively precise gain. The master's envelope voltage is compared with the desired envelope and the system acts to correct amplitude (Q) errors.

More papers exploiting the Master-Slave technique can be seen in [14] and [38]. We can also see this technique being used in notch filters as in [36], where basically the authors automatically tune the Q of an LC network to obtain a good notch response. When using this Master-Slave technique, the designer should make a well matched master structure. So, if the slave use inductors, the master should also use them and the on-chip area may significantly increase.

Figure 5.1: (a) Pll tuning scheme and (b) Magnitude locked loop to control Q.



Source: Exracted from [37].

5.2 TRANSIENT BEHAVIOR OF LC NETWORKS

To propose a new method to control the Q of a filter, we start considering a voltage source connected to an RLC series network through a switch as seen in Fig. 5.2. The behavior of the series RLC circuit, when the switch closes, is predicted by:

$$v_s(t) = v_c(t) + RC\frac{dv_c}{dt} + LC\frac{d^2v_c}{d_t}. \tag{5.1}$$

The solution to (5.1) leads to the following characteristic equation (considering that $v_s(t) = 0$, *i.e.*, if we consider that the source is a DC power supply):

$$0 = 1 + RCs + LCs^2 = 1 + (sT)2\zeta + (sT)^2, \tag{5.2}$$

where $T = 1/\omega_0$, $\zeta = 1/(2Q)$, $sT = -\zeta \pm \sqrt{\zeta^2 - 1}$. Hence we have 3 distinct cases for the damping factor (ζ) that solves s_1 and s_2. If $\zeta > 1$ the system has an overdamped response, if $\zeta = 1$ the system have a critical damped response and if $\zeta < 1$ the system has an underdamped response.

The solution of (5.1) can be written as:

$$v_c(t) = V_S + A_1 e^{s_1 t} + A_2 e^{s_2 t}. \tag{5.3}$$

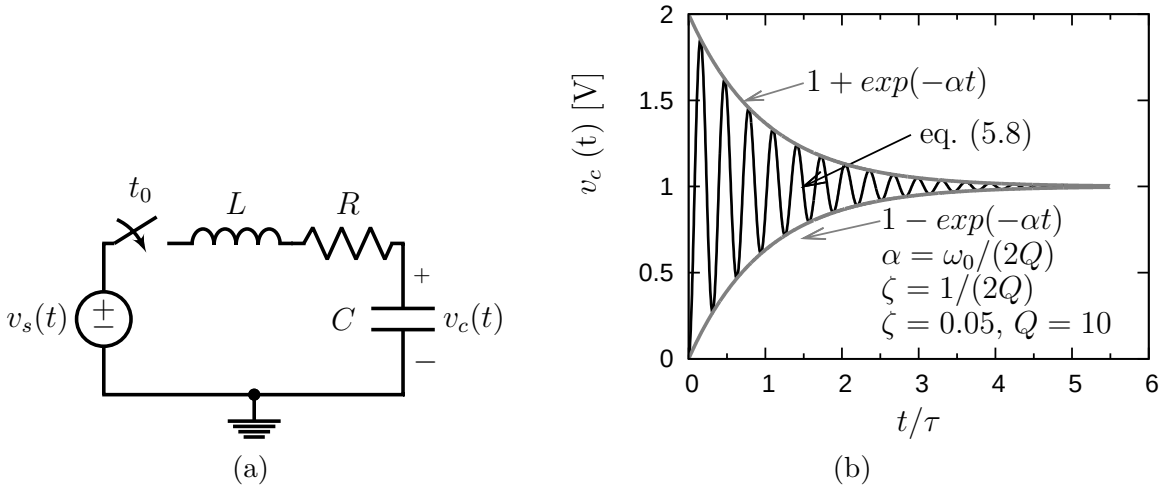
The boundary conditions are:

$$v_c(0) = V_S + A_1 + A_2 = 0 \tag{5.4}$$

and

$$i(0) = C\frac{dv_c(t)}{dt}|_{t=0} = 0. \tag{5.5}$$

Figure 5.2: (a) Voltage source connected to a series RLC network after $t = 0$. (b) Transient response of an underdamped RLC network when the switch closes at $t = 0$.



Source: The author.

Then we can write A_1 and A_2 as:

$$A_1 = -\frac{V_S}{1 - s_1/s_2} \tag{5.6}$$

and

$$A_2 = \frac{s_1/s_2 V_S}{1 - s_1/s_2} \tag{5.7}$$

Considering an underdamped response we can rewrite (5.3) as:

$$v_c(t) = V_S + e^{-\frac{t}{\tau}}(A_1 e^{j\omega_d} + A_2 e^{-j\omega_d}), \tag{5.8}$$

where $\omega_d = \sqrt{1 - \zeta^2}/T$. We plot an underdamped transient response of v_c, normalized by the circuit's time constant ($\tau = 1/\alpha = T/\zeta = 2Q/\omega_0 = 2L/R$), in Fig. 5.2(b). Note that it takes approximately 5τ to reach the steady response and that V_S is a DC voltage source equal to 1 V.

The oscillation frequency of $v_c(t)$ tends to ω_0 when $\zeta \to 0$ and the oscillation time around the steady state is proportional to Q. There is a work based on the latter property that estimates the Q using peak detectors and counters [39]. The authors claim that their technique can measure a quality factor up to 10^6 and they measure resonating devices at frequencies of hundreds of kilohertz. However, it is more common to test RF circuits with a signal tone always connected. Hence, we continue our analysis considering that $v_s(t) = sin(\omega t)$.

We can write the frequency response of (5.1) as:

$$\frac{v_c(s)}{v_s(s)} = \frac{1}{s^2 LC + sRC + 1}. \tag{5.9}$$

Considering that $v_s(t) = sin(\omega t)$ we have that:

$$v_c(s) = \frac{\omega}{(s^2 LC + sRC + 1)(s^2 + \omega^2)}. \tag{5.10}$$

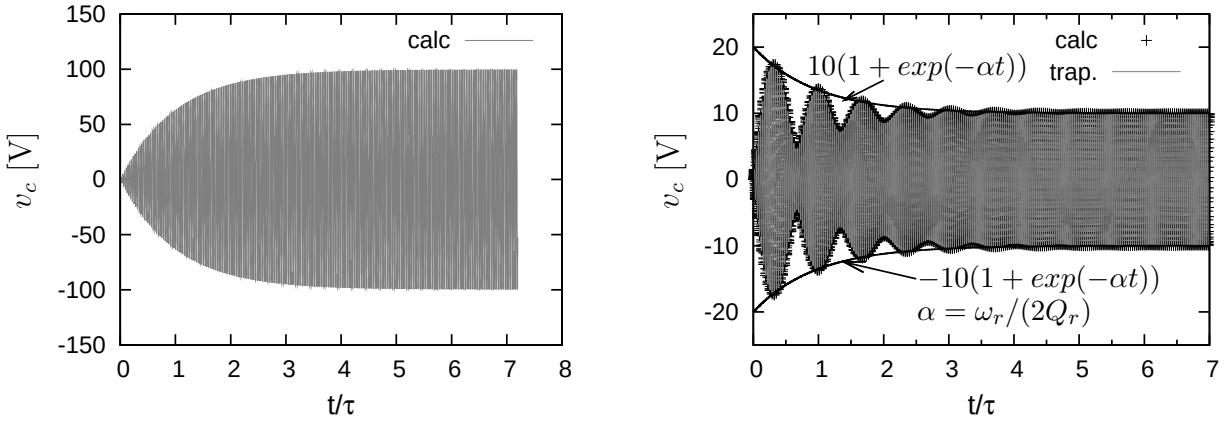
We can easily obtain the inverse Laplace transform of (5.10) and write it as:

$$\begin{aligned} v_c(t) = & \frac{-A\omega^2 \sin\omega t + \sin\omega t - B\omega\cos\omega t}{A^2\omega^4 + B^2\omega^2 - 2A\omega^2 + 1} + \\ & \frac{e^{-\frac{t}{\tau}}\omega\left[(2A^2\omega^2 + B^2 - 2A)\sinh(\theta t) + B\sqrt{B^2 - 4A}\cosh(\theta t)\right]}{(A^2\omega^4 + B^2\omega^2 - 2A\omega^2 + 1)\sqrt{B^2 - 4A}}, \end{aligned} \tag{5.11}$$

where $A = LC$, $B = RC$ and $\theta = \sqrt{B^2 - 4A}/2A$. The first term of (5.11) represents the final value of $v_c(t)$ while the second term represents the attenuation of $v_c(t)$ along time.

The time response of an LC network using (5.11) is shown in Fig. 5.3(a). We used $v_s = sin(\omega_0 t)$, $w_0 = 1/\sqrt{(L_0 C_0)}$ and $Q_0 = 100$ to plot this figure. We note that the envelope of v_c increases monotonically and that the final amplitude of $v_c(t)$ is equal to Q_0.

Figure 5.3: Transient response of a tuned and detuned RLC series circuit in (a) and (b), respectively.



Source: The author.

On the other hand, if the LC network is detuned with the source frequency, the envelope loses its monotonic behavior as seen in Fig. 5.3(b). The 'calc.' curve was obtained using (5.11) with: $v_s = sin(\omega_0 t)$; a detuned LC resonant frequency (f_r) equal to $1/\sqrt{L_0(C_0 + C_0/10)}$ resulting in a detuned quality factor (Q_r) $Q_r = 90.9$. The 'trap.' curve was obtained by simulating this LC network with the trapezoidal integration method and with a maximum time step of $1/(300 f_0)$. [1]

The amplitude response of the detuned LC network is approximately limited by:

$$V_{CMax} = V_F(1 + e^{-\alpha t}) \tag{5.12}$$

and

$$V_{CMin} = -V_F(1 + e^{-\alpha t}), \tag{5.13}$$

where V_F is the final voltage amplitude of the filter after its transient response, as seen seen in Fig. 5.3(b). So, we conclude that the maximum peak voltage of $v_c(t)$ is smaller than $2V_F$.

Since the envelope of $v_c(t)$ is limited by an exponential, it takes around $5\,\tau$ to reach its steady state. If the envelope of $v_c(t)$ is taken, we see that its frequency is given by $f_0 - f_r$, where f_r is the resonant frequency of the detuned LC network. Then, the number of peaks/valleys (N) can be estimated as:

$$N = 5\tau(f_0 - f_r) \cong 1.6\, Q_r \left(\frac{f_0}{f_r} - 1\right), \tag{5.14}$$

which is directly proportional to Q and depends on the ratio of f_r and f_0.

[1] There is a handful of integration methods that can be used in transient simulations. So, it is up to the designer to choose one of them very carefully. Methods such as Gear2 and Backwark Euler introduce an artificial damping factor to the LC network. Which means that when these methods are used, the resonating circuits apparently have a lower Q, compared to the Q obtained using the trapezoidal integration method [40].

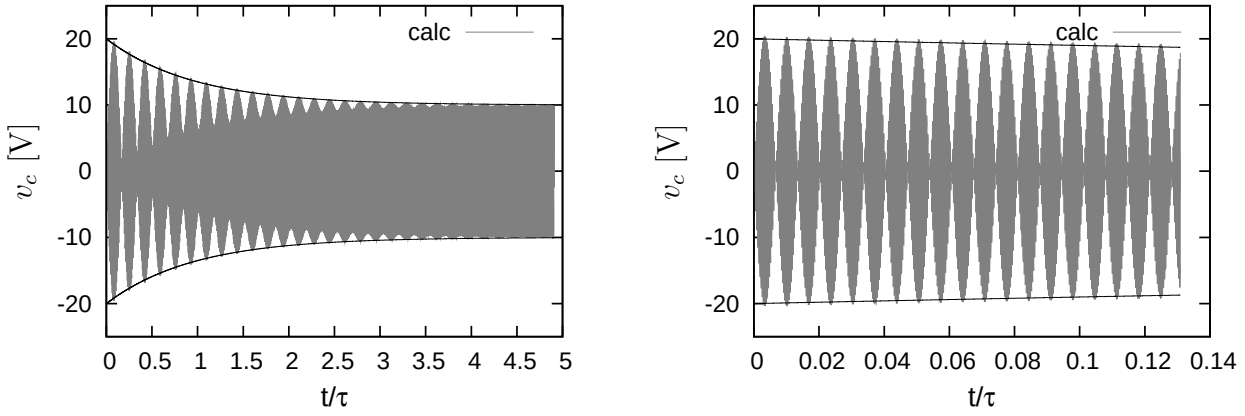
When $t = 5\tau$ the signal envelope is highly attenuated and its detection is difficult. Then, we can reduce the 1.6 ($\cong 5 \times 2/(2\pi)$) term to 0.6 ($\cong 2 \times 2/(2\pi)$) in equation (5.14). With this modification, the detectable number of peaks becomes:

$$N_d \cong 0.63\, Q_r \left(\frac{f_0}{f_r} - 1 \right). \tag{5.15}$$

Using the circuit used to plot Fig. 5.3(b), we have that $f_0/f_r = \sqrt{1.1}/1 = 1.05$ and $Q_r = 91$. So, $N = 7.2$ peaks or $N_d = 3$ detectable peaks.

We plot two transient responses of $v_c(t)$ when Q_0 is equal to 400 and when it tends to infinity in Fig. 5.4. This is done to gain a better insight on the behavior of the transient response of the detuned LC network that continues with $f_r/f_0 = 1.05$.

Figure 5.4: Transient response of a detuned RLC series circuit with $Q_0 = 400$ and $Q_0 \to \infty$ in (a) and (b), respectively.



(a) (b)

Source: The author.

5.3 IMPLEMENTED SYSTEM

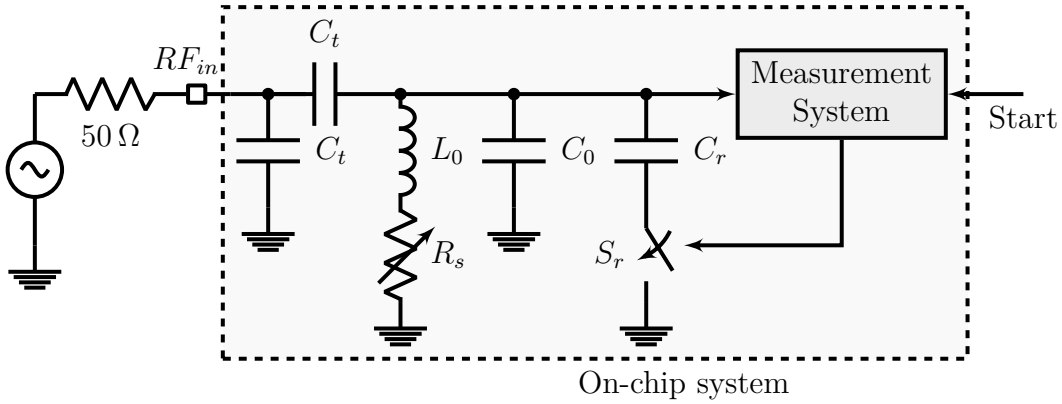
From the observed equations and results of the previous section, we conclude that the quality factor of an LC network can be estimated if it is excited by a sinusoidal and if there is a voltage step on its terminals. It is also possible to estimate how close the LC tank is tuned with the source frequency by the same means. Based on these conclusions we designed a prototype using the system of Fig. 5.5 to extract the parameters of the resonating network composed by L_0, C_0 and R_s. In other words, L_0, C_0, and R_s is the DUT.

Capacitors C_t in Fig. 5.5 are responsible for a voltage drop after the 50-Ω resistor of the power source and to increase the impedance magnitude seen from the filter. Usually these capacitors are implemented using a small capacitance in the order of units of picofarads. If the filter is part of a larger integrated system, such capacitive network may not be required.

The LC tank composed by L_0 and C_0 resonates approximately at 900 MHz and R_S can be viewed as the inductor's series resistance. We use an electrically modified R_s to be able to change and control the equivalent Q of the LC network. With this circuit we can measure different quality factors.

The step response of the LC network occurs when S_r opens and closes. When the 'Start' signal rises to a logic '1', S_r is closed. Then, the number of the envelope peaks on C_0 is stored

Figure 5.5: Simplified on-chip system implemented to extract the properties of L_0, C_0 and R_s.

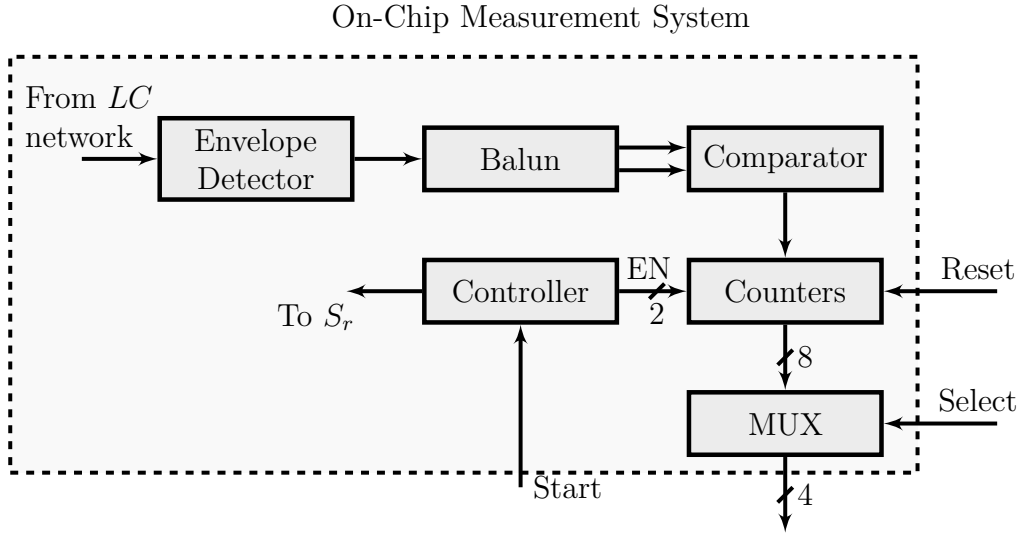


Source: The author.

by a 4-bit counter. The same happens when the S_r opens, but the number of the envelope peaks are stored by another 4-bit counter.

The measurement system contains the blocks that can be seen in Fig. 5.6. The group composed by the envelope detector, balun and comparator are responsible to detect the envelope peaks. The comparator output toggles every time its differential input change its polarity, what characterizes a peak occurrence. The envelope peaks when either S_r is closed or opened are passed to two distinct 4-bit counters. The controller block activates the measurement on the rising edge of the external 'Start' signal. This block is first responsible to close S_r and enable one counter that stores the output of the comparator for 1 μs. After this period, the controller opens S_r, disables the first counter and enables the second one for another 1 μs. The multiplexer (MUX) receives the output of the counters and its output displays either the Q or tuning values, if the external 'Select' signal is 0 or 1, respectively.

Figure 5.6: Block diagram of the designed LC-parameter-extractor system.



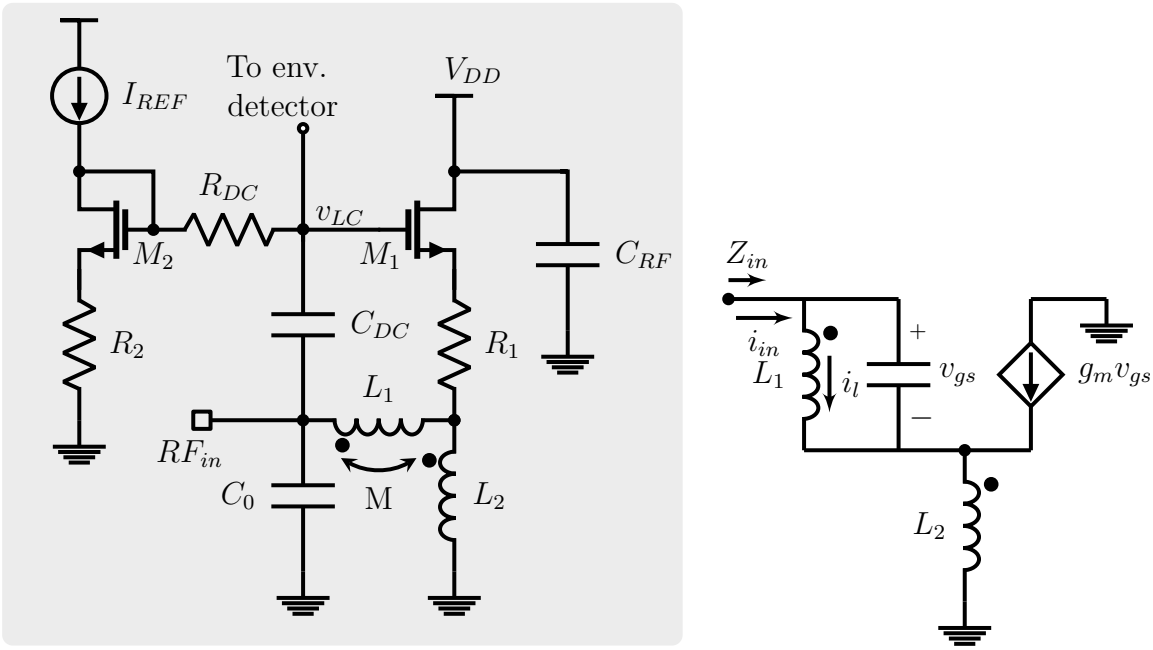
Source: The author.

In the following subsections we present the circuits that compose this LC parameter extractor.

5.3.1 Implemented LC network with adjustable Q

We present the implemented LC network in Fig. 5.7(a). In this schematic, the C_t network is omitted, C_{RF} is used as a decoupling capacitor, C_{DC} is used to block the DC voltage, and R_{DC} is a resistor used to increase the impedance seen by the signal on M_1's gate. R_1 is designed with a relatively small resistance $\cong 20\,\Omega$ and it is used to prevent that the signal on L_2 forward bias the bulk-to-source junction of M_1. M_2 is diode connected and has the same aspect ratio of M_1. Hence, the drain-to-source current of M_1 is approximately equal to I_{REF}, because $R_2 = R_1$. This cell works as a Q-enhanced LC network and its basic configuration is based on [41].

Figure 5.7: (a) Implemented LC network with adjustable Q and (b) simplified small-signal circuit of the Q-enhancing circuit.



(a) (b)

Source: The author.

Analytically, we can consider the simplified small-signal model presented in Fig. 5.7(b) to estimate the input impedance of the circuit in Fig. 5.7(a). The voltage on the inductors (v_{in}) is:

$$v_{in}(s) = i_{in} s X_{eq} + (i_{in} + g_m v_{gs}) sM + (i_{in} + g_m v_{gs}) sL_2 + i_l sM, \tag{5.16}$$

where

$$v_{gs}(s) = \frac{i_{in} s(L_1 + M)}{1 - s g_m M}, \tag{5.17}$$

$i_l = i_{in} - v_{gs} s C_{gs}$, and $X_{eq} = \omega L1 // -1/(\omega C_{gs})$. Then, Z_{in} can be decomposed as:

$$\Re(Z_{in}) = -\frac{\omega^2 g_m (X_{eq} + M)}{1 - g_m(\omega M)^2} \left[(M + L_2) + \omega^2 M^2 (X_{eq} + M) \right] \tag{5.18}$$

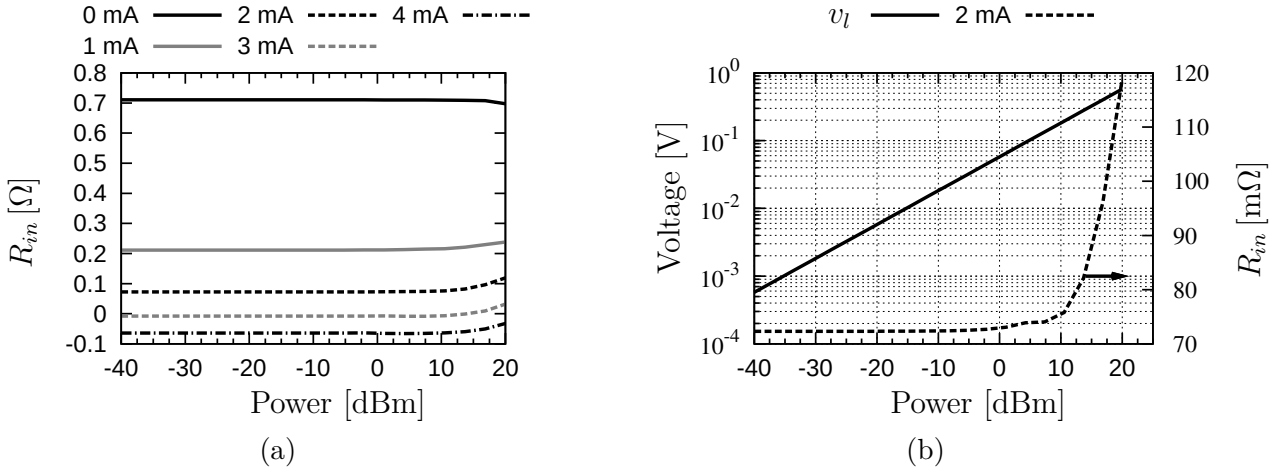
and

$$\Im(Z_{in}) = \omega(X_{eq}/\omega + L_2 + 2M) + \frac{\omega^3 M (X_{eq} + M)}{1 - g_m(\omega M)^2} \left(g_m^2 (M + L_2) + 1 \right). \tag{5.19}$$

The last term of (5.19) is usually smaller than the sum of the inductances and can be neglected. The same happens with the last term inside the brackets in (5.18) . The negative resistance seen in (5.18) mainly depends on g_m, M, and ω.

As seen in Fig. 5.7(a), the presented Q-enhancing circuit requires the use of a transistor to obtain the negative resistance effect. Due to this, its voltage response should be taken into account. Then, we show in Fig. 5.8(a) the input resistance of the Q-enhanced cell for different I_{REF} versus input power. These values are obtained using an input signal frequency equal to 900 MHz and considering that C_0 is not connected to the circuit. From this figure we see that the input resistance seems to be constant for a wide power range.

Figure 5.8: (a) Input resistance of the Q-enhanced cell for different I_{REF} versus input power and (b) zoom of the input resistance using $I_{REF} = 2\,\text{mA}$ and voltage on L_1 versus input power.



Source: The author.

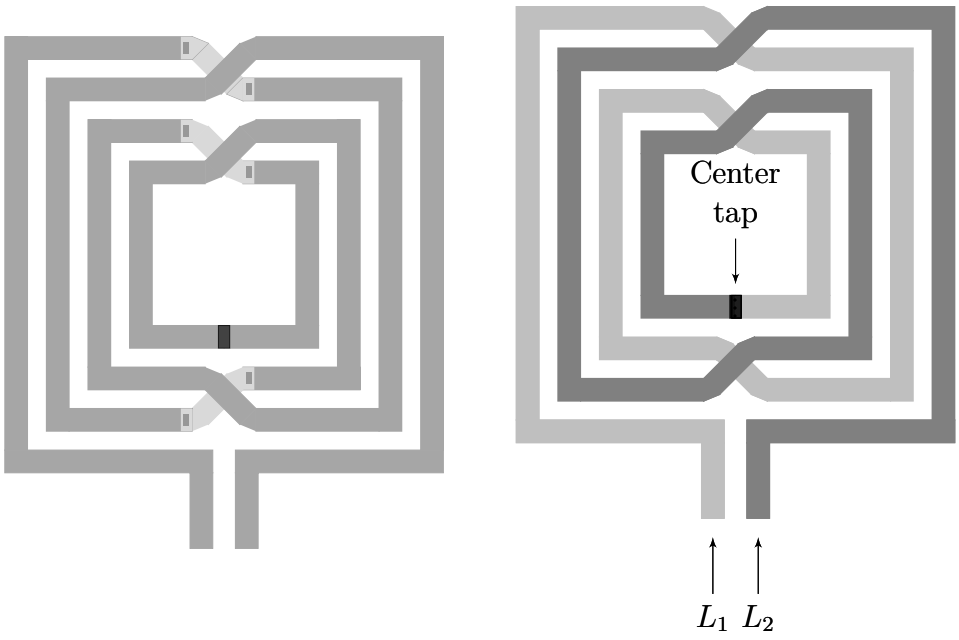
If now we resonate the Q-enhancing cell with C_0 and operate at its resonating frequency, we note that for an input power equal to $-30\,\text{dBm}$ and with an LC network with $Q = 300$, we have that the voltage on L_1 with respect to ground goes from 1.8 mV to 540 mV, as calculated using Fig. 5.7(b). With a signal with amplitude equal to 540 mV on L_1 and using $I_{REF} = 2\,\text{mA}$, we would have an equivalent input resistance equal to 115 mΩ on the Q-enhancing cell, which is 60 % higher than its small-signal resistance. So, even with low power input levels, such as $-30\,\text{dBm}$, the Q-enhancing cell already shows non-linear symptoms when the LC network resonates.

The devised method for estimating the Q is based on the number of the envelope peaks acquired when the LC network is detuned. In this case, the voltage amplitude on the resonating circuit decreases, so the Q of the detuned LC network is measured but not its Q when it is tuned. This may be a cause of error when the number of peaks are counted. One way to avoid this kind of error due to non-linearities is to have a look-up table that relates the input power with Q and the number of peaks. Another way to avoid these errors due to the amplitude change is to use a smaller detuning capacitor. In this case, the trade off is the reduced number of peaks.

Two series connected inductors used to implement L_1 and L_2 can lead to a weak coupling between them and to a large on-chip area. Hence, we use a symmetric center tapped inductor, which can be seen in Fig. 5.9(a). We have access to the center tap, which is located on the geometric center of this inductor and it is not drawn for simplification. This inductor is built in a way that there are two interwound inductors connected in series, as it is highlighted in Fig. 5.9(b). With this configuration, the inductors have a coupling factor $k \cong 0.7$.

We used an array of metal 1, that is located under the inductor and is provided by the design kit, to shield the inductor from substrate noise and to prevent induced currents in the substrate. One drawback of using this shield is the higher parasitic capacitance that reduces the self-resonant frequency of the inductor. But since we are operating at 900 MHz, this reduction

Figure 5.9: (a) A symmetric inductor layout that can be seen as two interwound inductors in (b).



(a) (b)

Source: Based on [42].

is not a problem because the implemented inductor has a self-resonant frequency close to 2 GHz. We also took some layout practices to ensure a good agreement with the model. Among them, we avoided closed current paths around the inductor and we kept the substrate contacts at least 100 μm away from the inductor.

5.3.1.1 Component Sizing

It is possible to view the used component sizes/values of the LC network with adjustable Q in table 5.1.

Table 5.1: Component sizes/values of the LC network with adjustable Q.

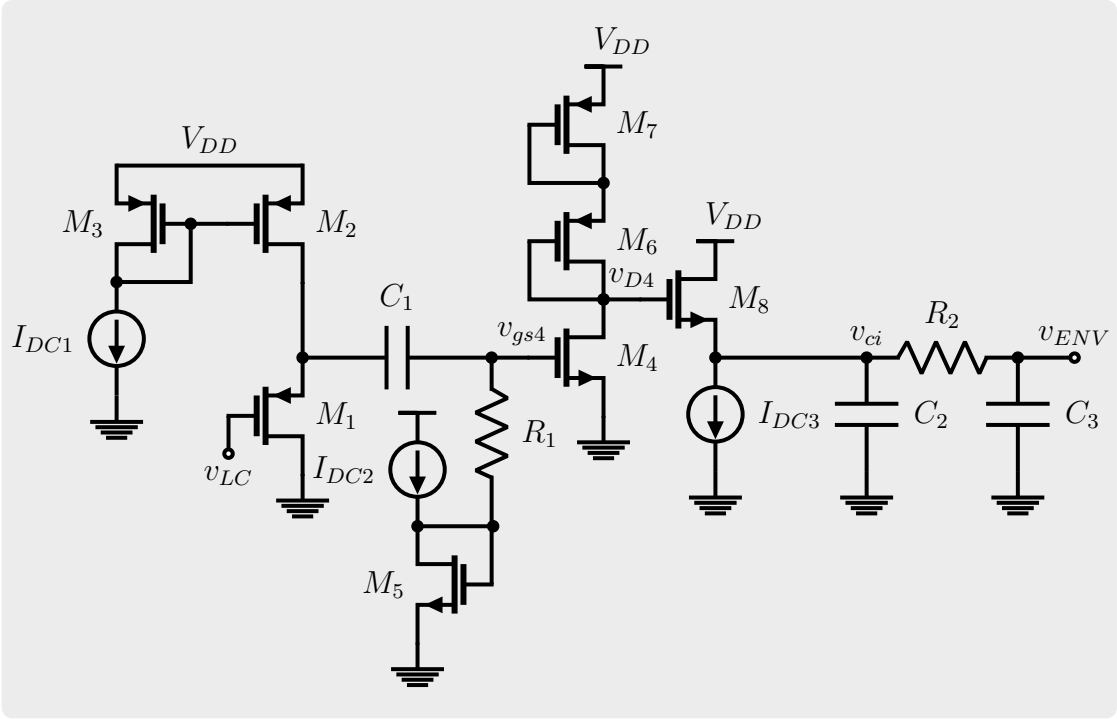
Component	**Value**	**Additional data**
R_{DC}	18 kΩ	
R_1, R_2	20 Ω	
M_1, M_2	W_{tot}/L=150 μm/.4 μm	fingers = 10, multiplicity = 4
L (L_1, L_2)	5.3 nH	outer dimension = 300 μm, turns=4, coil width = 10 μm, space = 5 μm
C_0	4.6 pF	Dual MIM capacitor
C_{RF}	40 pF	Dual MIM capacitor
C_{DC}	5.4 pF	Dual MIM capacitor
C_t	500 fF	MIM capacitor
C_r	500 fF	MIM capacitor

Source: The author.

5.3.2 Envelope detector

We present in Fig. 5.10 the circuit used to detect the envelope on the LC network. The voltage on the resonating circuit is acquired by the source follower implemented by M_1. In this case, a pMOS transistor is required because the average voltage on the gate of the Q-enhanced cell can go as low as 0 V when $I_{REF} = 0$ A.

Figure 5.10: Implemented envelope Detector.



Source: The author.

In Fig. 5.10, C_1 is used to block the DC voltage, M_5 is used to bias M_4 with a relatively small current (10 μA). M_4 is used as an amplifier and its gain is also controlled by its gate-to-source voltage (v_{gs4}). If v_{gs4} is a large signal, the transconductance of M_4 is higher when this signal is on its positive cycle than when it is on its negative cycle. This makes the voltage on the drain of M_4 (v_{D4}) more sensitive to the positive cycle of v_{gs4}. Then, we can say that M_4 acts like a diode when it forwards high level signals and blocks the low level ones. In this case, we have on v_{D4} the upper part of the envelope of v_{LC} shifted to the bottom part of the v_{d4} signal.

M_8 is configured as a source follower. It is used to increase the impedance seen by the drain of M_4 isolating it from the capacitive-resistive load, composed by $C_2 - R_2 - C_3$, required to obtain the envelope.

The presented RC network implements a low-pass filter with the following transfer function:

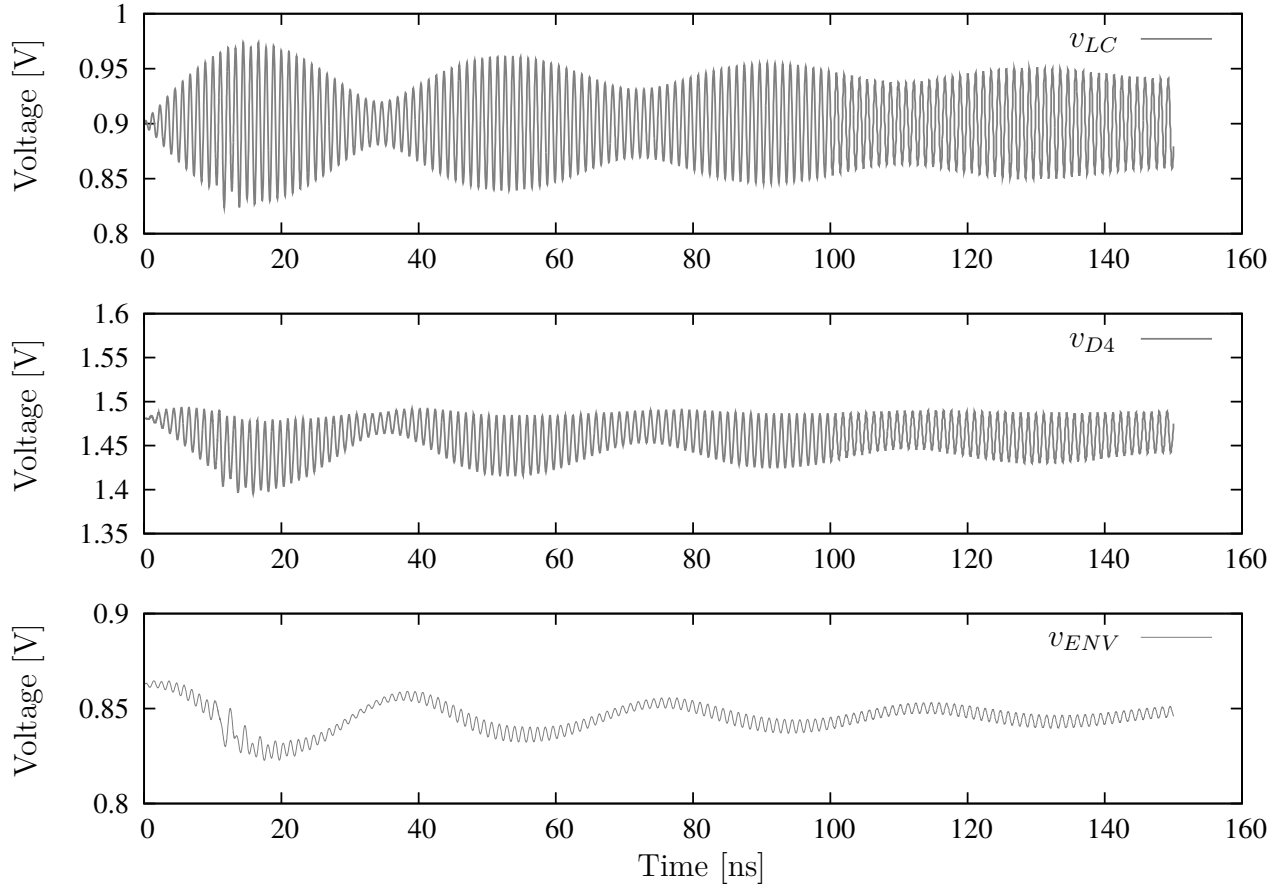
$$A_{RC} = \frac{v_{ENV}}{v_{ci}} = \frac{1}{R_F\left(s^2 R_2 C_2 C_3 + s(C_3 R_2/R_F + C_2 + C_3) + 1/R_F\right)}, \tag{5.20}$$

where it is considered that the input signal (v_{ci}) has a series resistance equal to R_F. We set the first pole frequency at 120 MHz and the second one at 2 GHz. In this design, it is considered that the detected envelope has a maximum frequency equal to 100 MHz.

We plot the main signals of the envelope detector in Fig. 5.21. We can say that the LC network is detuned with the signal source frequency, as it is seen by the v_{LC} curve. In this

example, it is easy to see that one part of the envelope of v_{LC} (the upper part as mentioned above) is passed to v_{D4}. Lastly, we filter v_{D4} to obtain its envelope (v_{ENV}).

Figure 5.11: Time domain response of the main signals of the envelope detector.



Source: The author.

5.3.2.1 Component Sizing

It is possible to view the used component sizes/values of the implemented envelope detector in table 5.2.

Table 5.2: Component sizes/values of the implemented envelope detector.

Component	Value	Additional data
M_1	$W_{tot}/L = 20\,\mu\text{m}/.4\,\mu\text{m}$	fingers = 10, multiplicity = 1
M_2, M_3	$W_{tot}/L = 10\,\mu\text{m}/.4\,\mu\text{m}$	fingers = 10, multiplicity = 1
I_{DC1}	$40\,\mu\text{A}$	
C_1	680 fF	Dual MIM
R_1	$8\,\text{k}\Omega$	
M_4, M_5	$W_{tot}/L = 35\,\mu\text{m}/.4\,\mu\text{m}$	fingers = 10, multiplicity = 1
M_6, M_7	$W_{tot}/L = 4\,\mu\text{m}/.8\,\mu\text{m}$	fingers = 4, multiplicity = 1
M_8	$W_{tot}/L = 20\,\mu\text{m}/.4\,\mu\text{m}$	fingers = 10, multiplicity = 1
I_{DC3}	$100\,\mu\text{A}$	
C_2	150 fF	MIM capacitor
R_2	$1.6\,\text{k}\Omega$	
C_3	1 pF	Dual MIM capacitor

Source: The author.

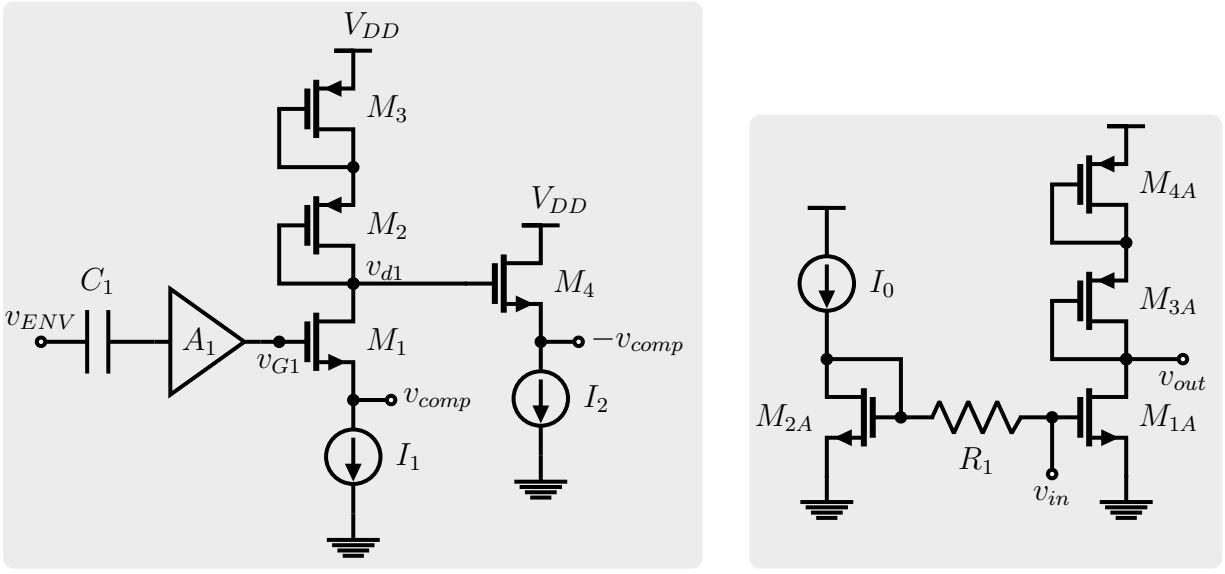
5.3.3 Implemented Balun

The balun is one of the key blocks of the measurement system. With this circuit we turn the unbalanced envelope into a balanced one. So, we can easily count the envelope peaks if the outputs of the balun are compared.

The implemented balun can be seen in Fig. 5.12(a). C_1 is used as a DC blocker and A_1 is an amplifier. M_1 is the core of the balun and the signals on its drain and source are ideally shifted by 180 degrees. M_4 is configured as source-follower amplifier and it is used to match the output impedances of the balun and reduce the load seen by the drain of M_4. M_2 and M_3 are configured as active loads and are used to bias M_1.

A_1 is implemented as a common-source amplifier with active load and its schematic is depicted in Fig. 5.12(b). We set the gain of this amplifier equal to 6 to compensate the losses of v_{LC} due to the buffers and to the RC network.

Figure 5.12: (a) Balun circuit and (b) A_1 implemented as a common-source amplifier.

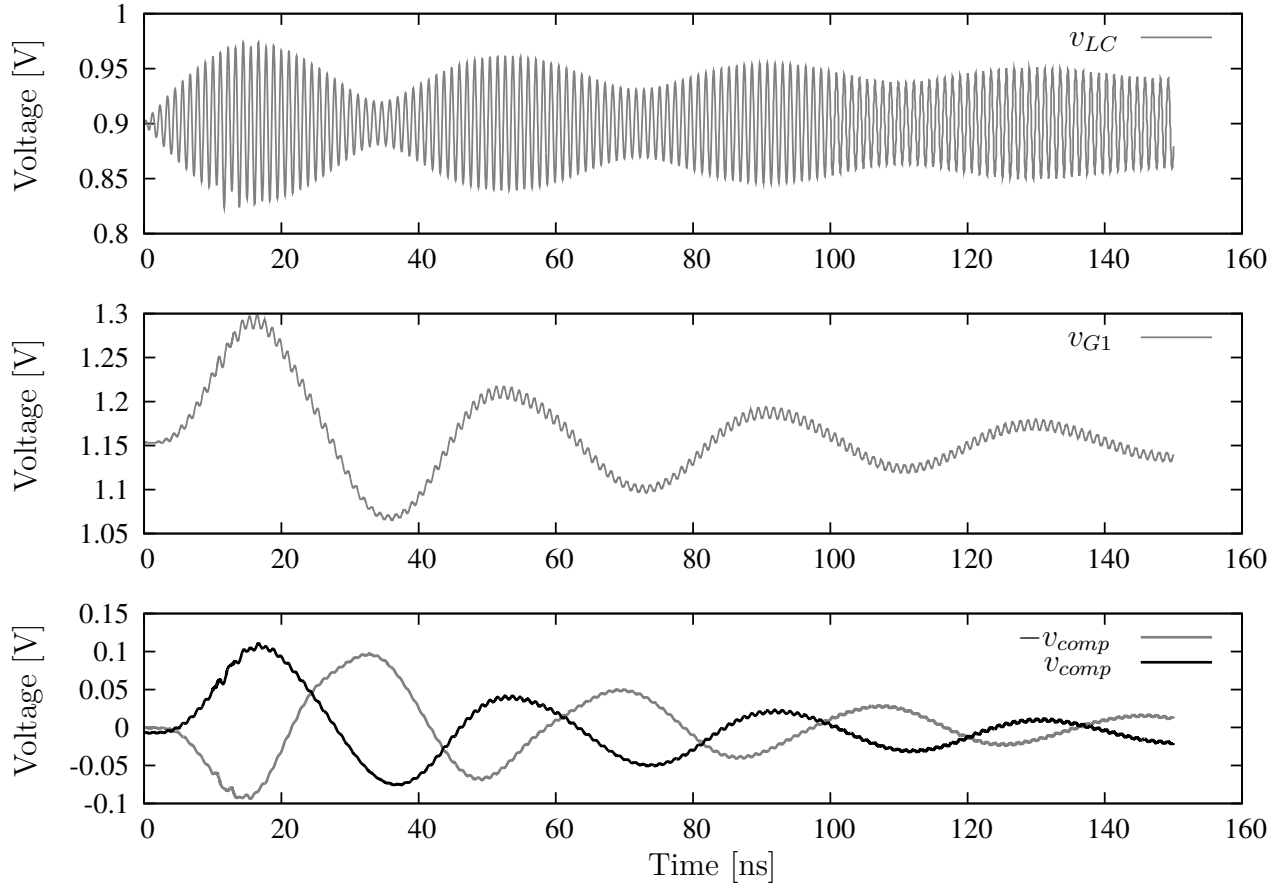


(a) (b)

Source: The author.

The transient response of the main signal of the balun is shown in Fig. 5.13. v_{LC} is also shown to aid with the analysis of the balun signals. v_{G1} is the signal on M_1 gate. The output of the balun is represented by $-v_{comp}$ and v_{comp}. We note that the average voltage of these signals is removed and that they are not exactly shifted by 180 degrees, but this does not impose any issue when the envelope peaks are counted.

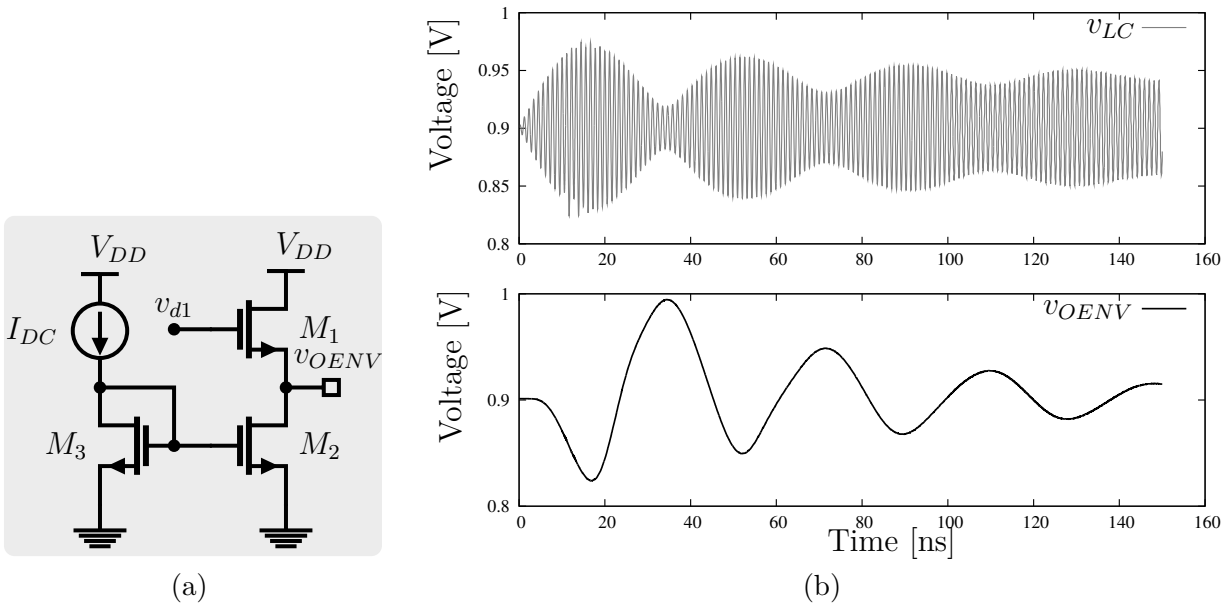
Figure 5.13: Time domain response of the main signals of the balun.



Source: The author.

The envelope is one of the main signals of this parameter extractor and we should be able to measure it outside the chip. Hence, another buffer is connected to v_{d1} and its output is connected to a pad. The schematic of this buffer can be seen in Fig. 5.14. In the circuit simulation, the buffer is loaded with $1\,\mathrm{M\Omega}//13\,\mathrm{pF}$, which is a pessimistic load considering that a passive 10x probe is used for the measurement. The resulting buffer waveform can be seen in Fig. 5.14(b).

Figure 5.14: (a) Schematic of the buffer and (b) simulated buffered envelope signal considering a 1 MΩ//13 pF load.



Source: The author.

5.3.3.1 Component Sizing

It is possible to view the used component sizes/values of the balun circuit in table 5.3.

Table 5.3: Component sizes/values of the implemented balun circuit.

Component	**Value**	**Additional data**
M_2, M_3	$W_{tot}/L = 4\,\mu$m/.8 μm	fingers = 4, multiplicity = 1
M_1, M_4	$W_{tot}/L = 10\,\mu$m/.4 μm	fingers = 10, multiplicity = 1
I_1, I_2	20 μA	
C_1	680 fF	Dual MIM
M_{1A}	$W_{tot}/L = 20\,\mu$m/.4 μm	fingers = 10, multiplicity = 1
M_{2A}	$W_{tot}/L = 10\,\mu$m/.4 μm	fingers =5, multiplicity = 1
I_0	20 μA	
R_1	9.4 kΩ	
M_{3A}, M_{4A}	$W_{tot}/L = 5\,\mu$m/.6 μm	fingers =4, multiplicity = 1

Source: The author.

In table 5.4 we present the component sizes/values of the output buffer presented in this subsection.

Table 5.4: Component sizes/values of the implemented output buffer.

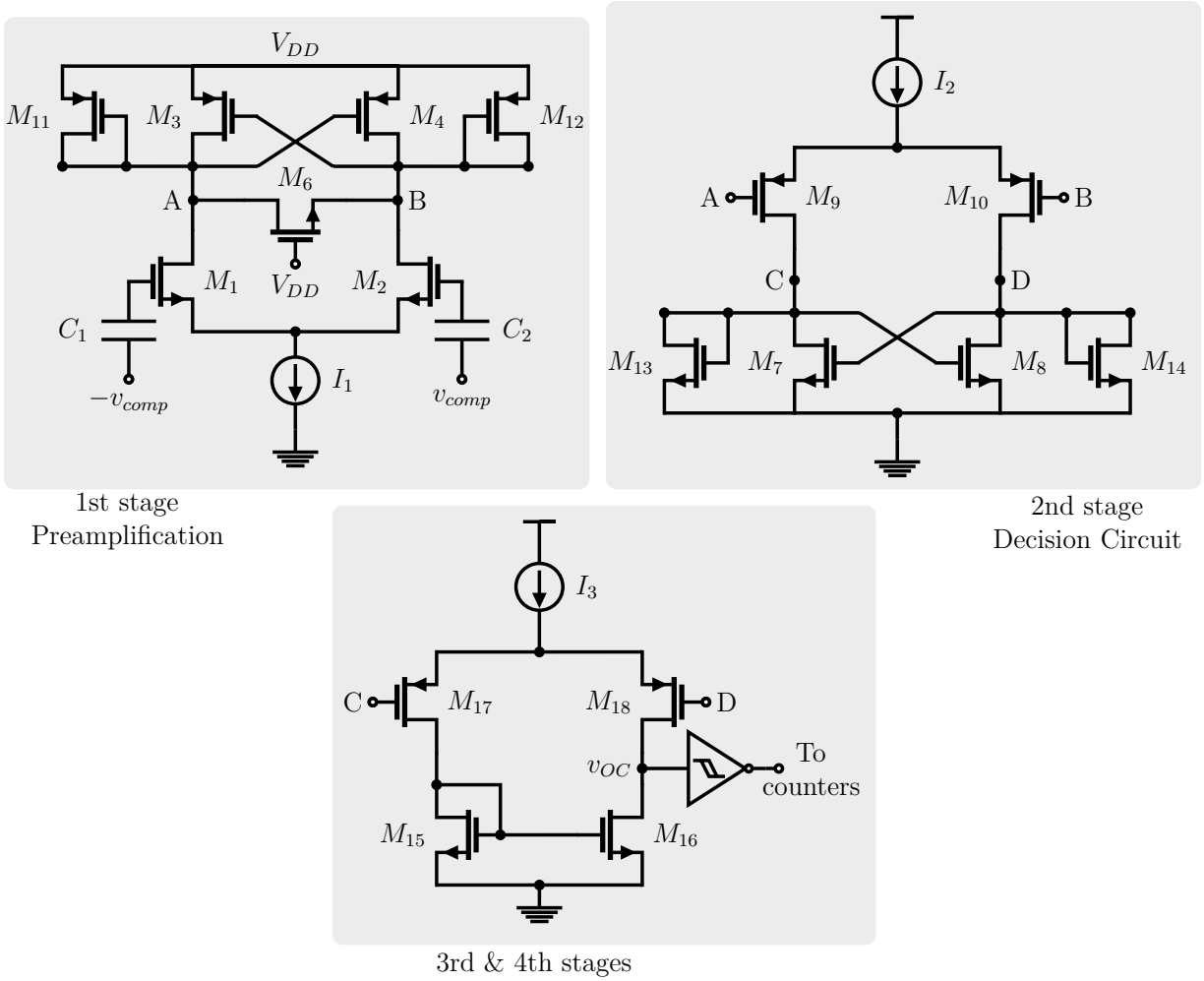
Component	**Value**	**Additional data**
M_1	$W_{tot}/L = 50\,\mu$m/.4 μm	fingers = 10, multiplicity = 1
M_2	$W_{tot}/L = 20\,\mu$m/.4 μm	fingers = 10, multiplicity = 1
M_3	$W_{tot}/L = 5\,\mu$m/.4 μm	fingers = 5, multiplicity = 1
I_{DC}	50 μA	
I_{M_1}	230 μA	

Source: The author.

5.3.4 Comparator

For the comparator stage, we choose the circuit of Fig. 5.15. This comparator can be divided in the input preamplifier, a decision stage, and a circuit that converts the analog voltage to the digital domain. The preamplifier increases the comparator sensitivity, prepares the input signal for comparison and isolates its input from the switching noise that comes from the next stage. The second stage decides which signal input is larger. Lastly, the last stage converts the analog signal to the digital domain, so the counters are able to store the number of peaks. The last stage of the comparator is composed by a differential amplifier, that gives a small gain to the output signal of the second stage, and it is followed by a Schmitt trigger.

Figure 5.15: Implemented comparator.



Source: The author.

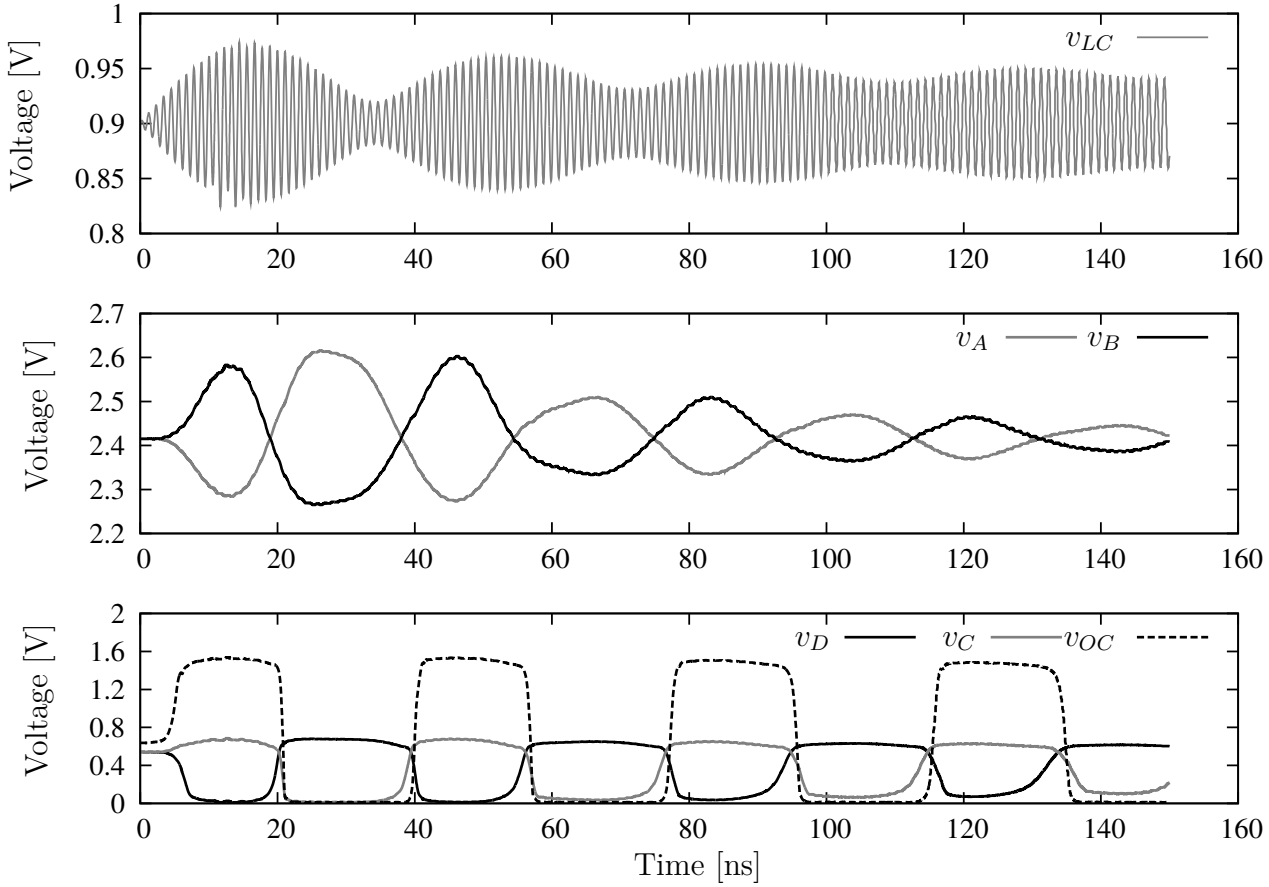
The pre-amp stage receives the signal from the balun. Capacitors $C1$ and C_2 blocks their common-mode voltage. The biasing of M_1 and M_2 is not shown for simplicity. The cross-coupled pair is used to speed-up the signals on A and B. The diode connected transistors are used to avoid that A and B get stuck to either 0 V or V_{DD} when the pre-amp should amplify [43]. M_6 is used to keep the same DC voltage on A and B, even if the transistors of the pre-amp are mismatched. We get the statistical mismatch results of the pre-amp and obtain the DC offset between V_A and V_B. Then, we use this data to size M_6 and reduce the estimated offset.

The second stage of the comparator is the decision circuit and it also uses a cross-coupled pair and diode connected transistors as its loads. It is a good idea to use this stage with hysteresis to reject noise on the incoming signal. We can do this by keeping the aspect ratio of the cross-coupled pair transistors and reducing the W/L relationship of the diode connected

transistors [20].

The main signals of the comparator can be seen in Fig. 5.16. We keep the v_{LC} curve as a reference. The voltage on nodes A and B of the pre-amp and the voltages of the decision stage V_C and V_D can be seen. We note that the maximum voltage on nodes C and D are limited by the diode connected transistors.

Figure 5.16: Time domain response of the main signals of the comparator.



Source: The author.

5.3.4.1 Component Sizing

It is possible to view the used component sizes/values of the comparator in table 5.5.

Table 5.5: Component sizes/values of the implemented comparator.

Component	**Value**	**Additional data**
C_1	400 fF	MIM capacitor
M_1, M_2	$W_{tot}/L = 25\,\mu$m/.6 μm	fingers = 5, multiplicity = 2
M_6	$W_{tot}/L = 1.36\,\mu$m/.5 μm	fingers =2, multiplicity = 1
M_{11}, M_3, M_4, M_{12}	$W_{tot}/L = 8\,\mu$m/1 μm	fingers =2, multiplicity = 1
I_1	100 μA	
I_2	80 μA	
M_9, M_{10}	$W_{tot}/L = 16\,\mu$m/1 μm	fingers = 4, multiplicity = 1
M_{13}, M_{14}	$W_{tot}/L = 3.5\,\mu$m/0.4 μm	fingers = 2, multiplicity = 1
M_7, M_8	$W_{tot}/L = 5\,\mu$m/0.6 μm	fingers = 4, multiplicity = 1
M_{15}, M_{16} [a]	$W_{tot}/L = 4\,\mu$m/0.6 μm	fingers = 4, multiplicity = 1
I_3	20 μA	
R_{Bias} [b]	5 kΩ	each resistor

Source: The author.

[a] This aspect ratio was updated to W/L=10/0.6 after the measurements results.

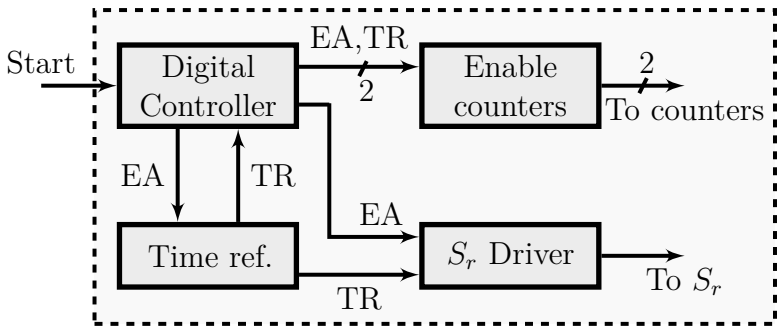
[b] Resistors used to bias M_1 and M_2 and omitted for simplification.

5.3.5 Controller

The *LC* tuning method requires that the controller has to turn on S_r and enable one counter for a certain amount of time. After that, the controller should open S_r, disable the first counter, and enable the second counter for the same amount of time. With the given information, we show the block diagram of the implemented controller in Fig. 5.17.

When the digital controller receives a rising start signal, the time reference circuitry is enabled with the EA signal going to high (a good mnemonic for EA is Enable All). After 1 μs, the time reference circuitry responds to the digital controller by changing TR (Time Response) to 0 V. After another 1 μs, TR goes to V_{DD} (or digital '1') and the digital controller disables the timer. One counter is enabled when EA and TR are high and the other one is enabled when EA=1 and TR=0. The S_r driver closes S_r when EA=TR=1 and it opens this switch when TR goes to 0.

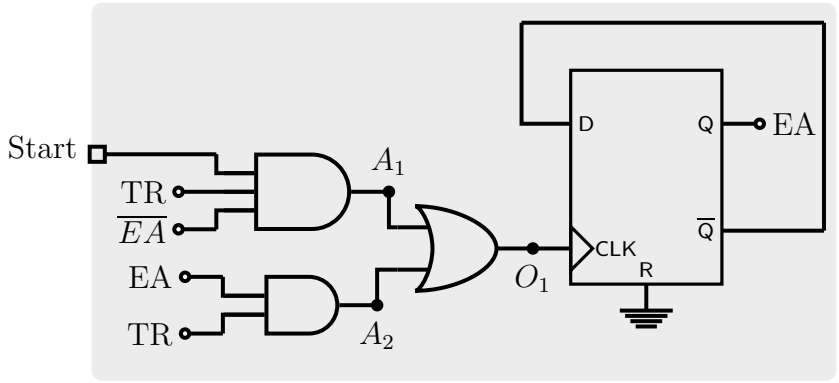
Figure 5.17: Block diagram of the controller.



Source: The author

The digital controller can be seen in Fig. 5.18. EA signal toggles when there is a rising edge on the CLK input of the the D flip-flop. This signal goes to 1 every time that A_1 goes to 1. A_1 goes to 1 when $\overline{\text{EA}}$=TR=1 and the start signal goes to 1. The digital controller disables the other blocks of the controller when EA goes to 0. This happens on the second rising edge of A_2. The first rising edge of A_2 happens when TR=1 and EA rises to 1 and its second rising edge occurs when TR returns to 1.

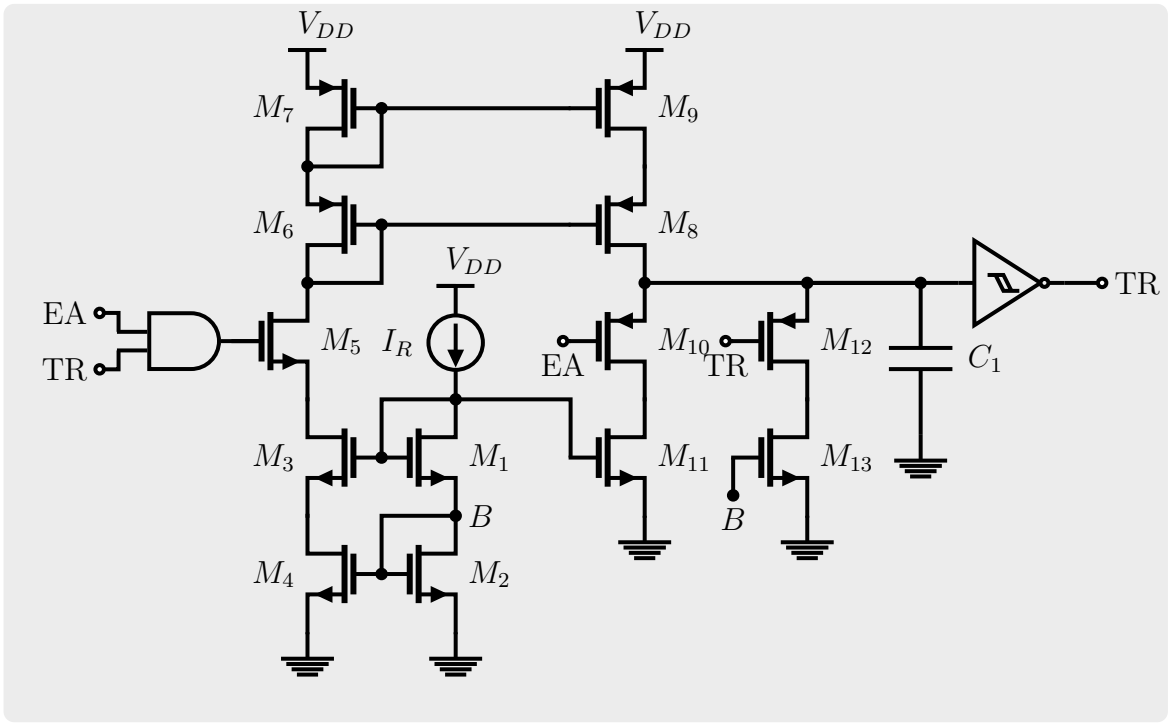
Figure 5.18: Circuit of the digital controller.



Source: The author.

The circuit that generates TR can be seen in Fig. 5.19. TR goes to 0 when the voltage on C_1 crosses the high to low voltage threshold of the Schmitt trigger. In this case, C_1 is charged with a current equal to I_R when TR=EA=1. When TR goes to 0, M_{11} closes, M_5 opens, and C_1 is discharged with a with a current that is fraction of I_R until C_1 reaches the low to high voltage threshold of the Schmitt trigger. The discharge of C_1, while TR=0, should take the same time of the high to low transition of TR after EA rises. This time is obtained by simulation and it can be changed with the aspect ratio of M_{12}. When the counting process is finished, C_1 should be fully discharged, then M_9 closes and another start pulse can be given to the controller.

Figure 5.19: Implemented time reference.

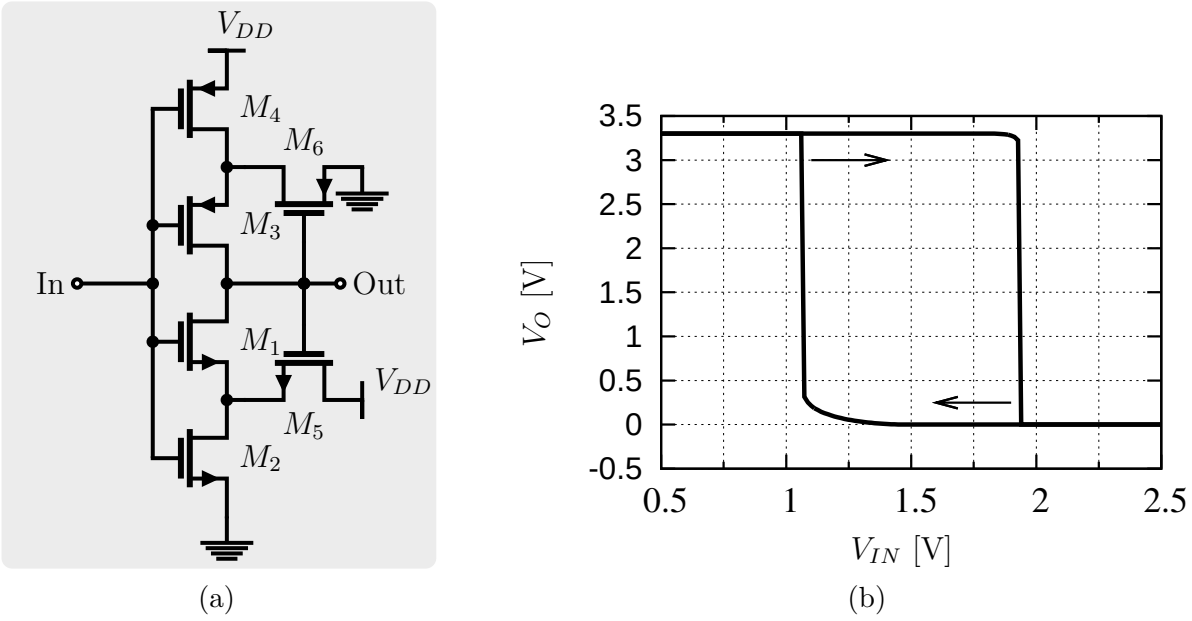


Source: The author.

We also show the schematic and the hysteresis curve of the implemented Schmitt trigger used in the counter in Fig. 5.20(a) and (b), respectively. Note that in this case the hysteresis is approximately equal to 900 mV and the high-to-low voltage threshold is approximately equal to 1.9 V. So, if we want the charging time of C_1 equal to the time that it takes to reach the low-to-high voltage threshold, we discharge C_1 with approximately half of the current necessary

to charge it to reach the high-to-low voltage threshold.

Figure 5.20: Schematic of the Schmitt trigger and its transfer characteristics in (a) and (b), respectively.



(a) (b)

Source: (a) Extracted from [32] and (b) the author.

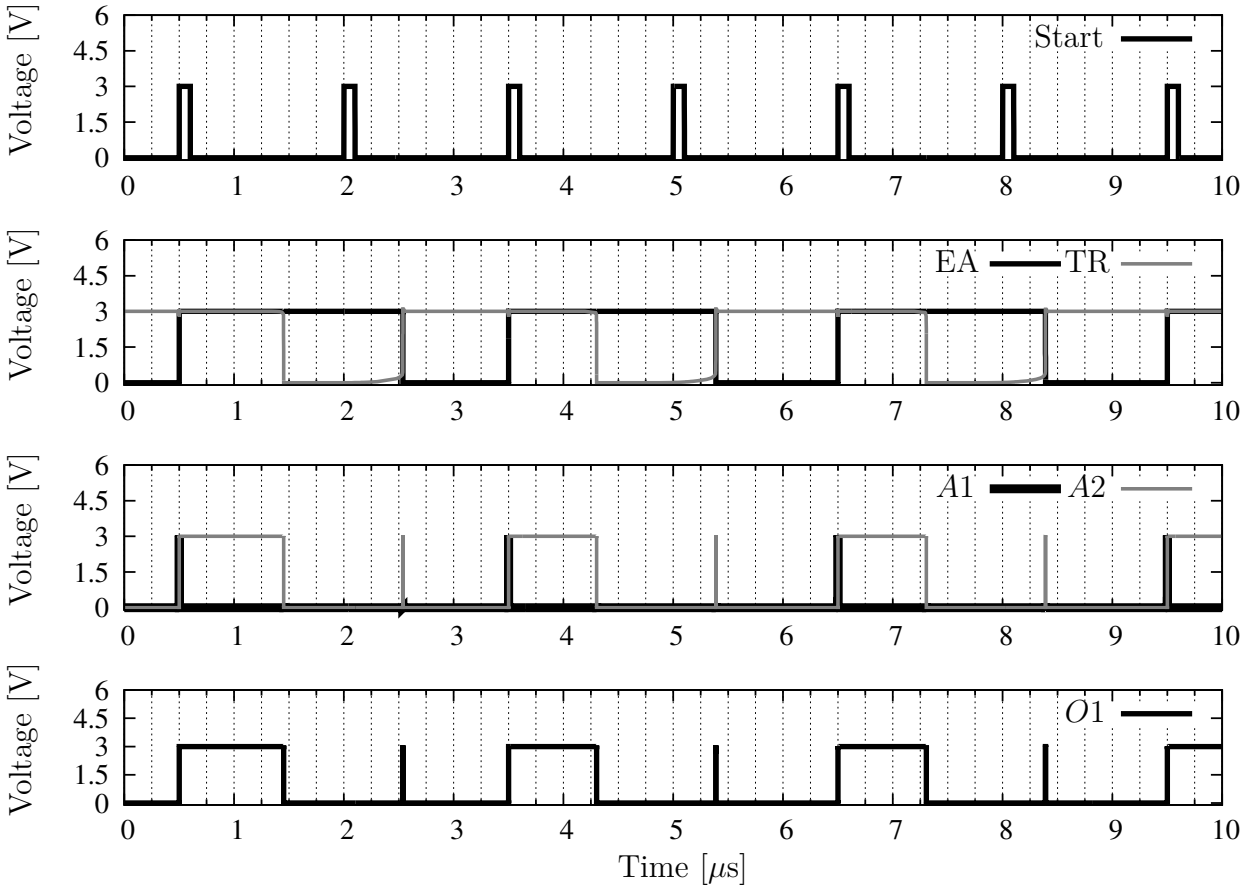
The main signals of the controller are shown in Fig. 5.21. The external start signal has a period of 1.5 μs. 1.0 μs after that the start signal went to 1 for the first time, the time reference circuit changes TR to 0. While EA=1, an start pulse does not have any effect on the controller. We also show A_1, A_2 and the OR operation with these signals ($O1$) in the same figure. When the start signal rises to 1, A_1 and EA rises to 1. $A1$ has a short width because this signal is responsible to set EA=1 and by its turn, EA resets $A1$. The second A_2 pulse resets EA and it makes the controller able to restart the counting process.

The circuit that is used to close and open S_r is shown in Fig. 5.22. As commented previously, S_r closes when TR=EA=1. S_r must have a fast switching with respect to the input signal frequency and we designed a chain of inverters to obtain a relative fast switching. TR and EA can also be equal to 1 for a short period, when the low-to-high voltage threshold of the Schmitt trigger of the timer reference circuit is crossed and the flip-flop of the digital controller is keeping EA=1. This situation can be seen in Fig. 5.21 at 2.5 μs. Then, we need to delay TR so that EA can go to zero after the complete counting process and S_r is closed only when it is required. This delay is done with the two inverters seen in Fig. 5.22. To do this delay we make the first inverter with the minimum allowed dimensions and the aspect ratio of the second inverter 5 times the aspect ratio of the first inverter.

The inverters of the 3-chain inverters have the width of their pMOS transistors 3 times higher than the width of their nMOS transistors. The width of the first nMOS transistor is the 1.5 times the minimum allowed by the technology and they increase 2.7 times to next stage. The length of the MOS transistors is the minimum allowed by the PDK, in this design we are using $V_{DD} = 3.3\,\text{V}$ and the minimum length of the 3.3-V transistor is equal to 400 nm. S_r [2] has an equivalent capacitance approximately equal to 150 fF seen by the driver . With 3 inverting stages, it is possible to drive S_r and obtain a rising time close to 1 ns, as seen in the circuit simulation result presented in Fig. 5.23. We also plot a relatively slow Start signal to confirm

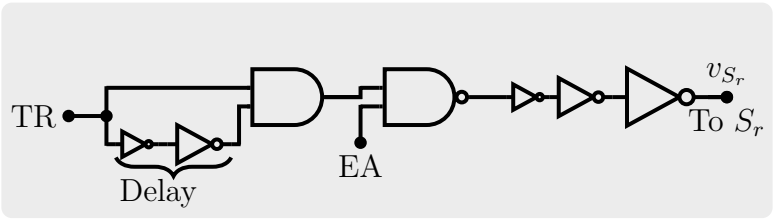
[2]Implemented using an NMOS transistor with W_{tot}/L=100/0.4 with 20 fingers and multiplicity equal to 4.

Figure 5.21: Time domain response of the main signals of the controller.



Source: The author.

Figure 5.22: S_r driver circuitry.

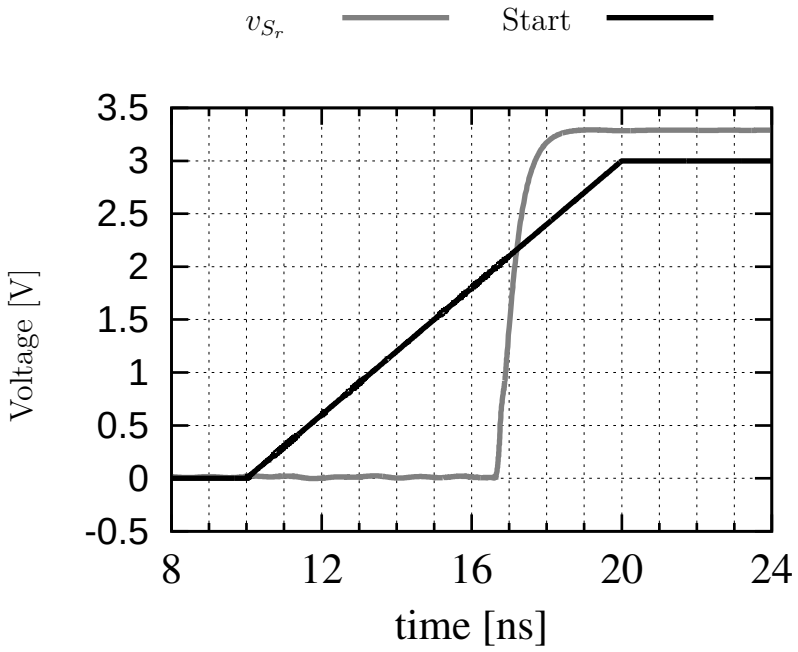


Source: The author.

that S_r can close within 1 ns.

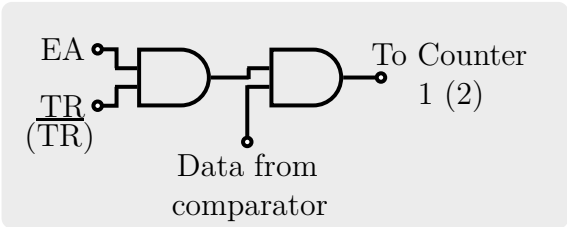
The two circuits that enable the counters can be seen in Fig. 5.24. The difference between them is that counter 1 is enabled by TR and EA, and counter 2 is enabled by $\overline{\text{TR}}$ and EA. Then, the digital data from the comparator is passed to either counter 1 or counter 2.

Figure 5.23: Rising of v_{S_r} and a relatively slow start signal.



Source: The author.

Figure 5.24: Circuit that enables the counters.



Source: The author.

5.3.5.1 Component Sizing

It is possible to view the used component sizes/values of the implemented time reference in table 5.6.

Table 5.6: Component sizes/values of the implemented time reference circuit.

Component	Value	Additional data
C_1	680 fF	Dual MIM capacitor
M_1, M_2, M_3, M_4, M_5	$W_{tot}/L = 25\,\mu$m$/.6\,\mu$m	fingers = 1, multiplicity = 1
M_6, M_7, M_8, M_9, M_{10}, M_{12}	$W_{tot}/L = 1\,\mu$m$/.5\,\mu$m	fingers = 1, multiplicity = 1
M_{13}	$W_{tot}/L = .8\,\mu$m$/.8\,\mu$m	fingers =1, multiplicity = 1
M_{11}	$W_{tot}/L = 1\,\mu$m$/.5\,\mu$m	fingers =1, multiplicity = 1
I_R	$10\,\mu$A	
M_{Sch} [a]	$W_{tot}/L = .68\,\mu$m$/.4\,\mu$m	fingers =1, multiplicity = 1

Source: The author.

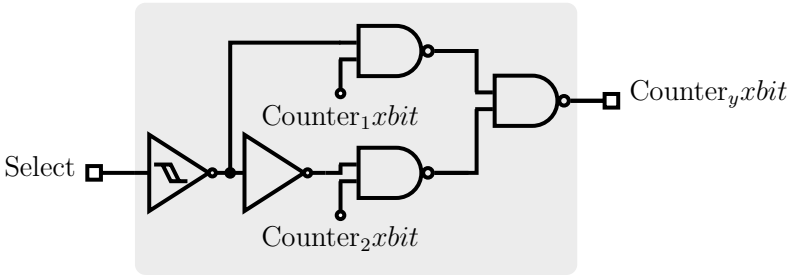
[a]Transistor size of the Schmitt trigger circuit shown in Fig. 5.20. All the transistors were built with the same dimensions.

5.3.6 Counter and MUX

We are interested to read the number of pulses that are stored by the 4-bit counters. So, each bit of the counter must be read. To reduce the number of on-chip pads, each bit of one counter is multiplexed with the same equivalent bit of the other counter. The implemented multiplexer can be seen in Fig. 5.25 and we note that the output of the multiplexers are connected to pads.

To further reduce the number of pads one can use a shift register and serially read the bits of the counter. The chosen method for reading the bits may require a larger number of pads, but the bits are easier to be read, making the prototype faster to measure.

Figure 5.25: Implemented multiplexer.



Source: The author.

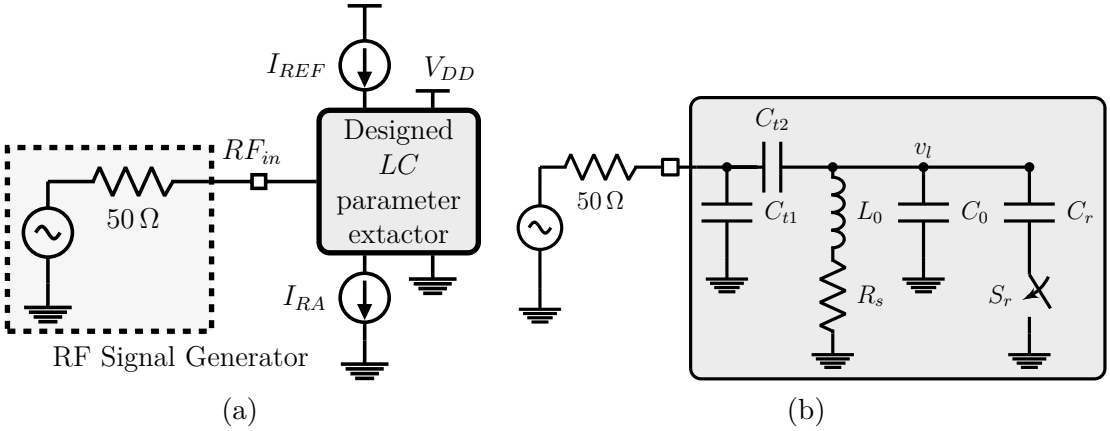
5.4 SIMULATED SYSTEM

Now we can test the system using the test bench of Fig. 5.26(a). In this figure I_{REF} is the current that sets the value of the negative resistance and I_{RA} is a DC current that is mirrored to the blocks that need a current reference. The start, reset, and select inputs are omitted as well as the multiplexer outputs. The main passive components used on the input of the designed system are redrawn in 5.26(b), for convenience.

The input impedance, seen by the RF signal generator, is plotted in Fig. 5.27. We note that when $I_{REF} = 3\,$mA, the LC network has a very high quality factor ($\cong 1000$) as it is expected after analyzing Fig. 5.8, which relates I_{REF} with the series resistance of the inductor.

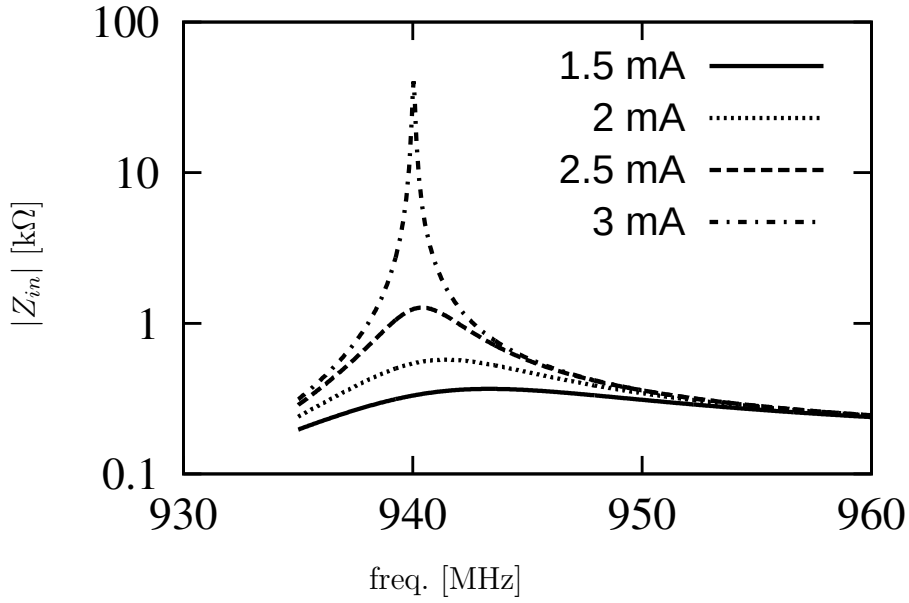
In the next step, we simulate a complete sequence of the designed parameter extractor, as seen in Fig. 5.28. To obtain this figure we used $I_{REF} = 3\,$mA, a signal frequency equal

Figure 5.26: (a) Test bench used to simulate the unloaded parameter extractor and (b) passive components that forms the *LC* network.



Source: The author.

Figure 5.27: Input impedance of the unloaded *LC* network for different I_{REF} values.

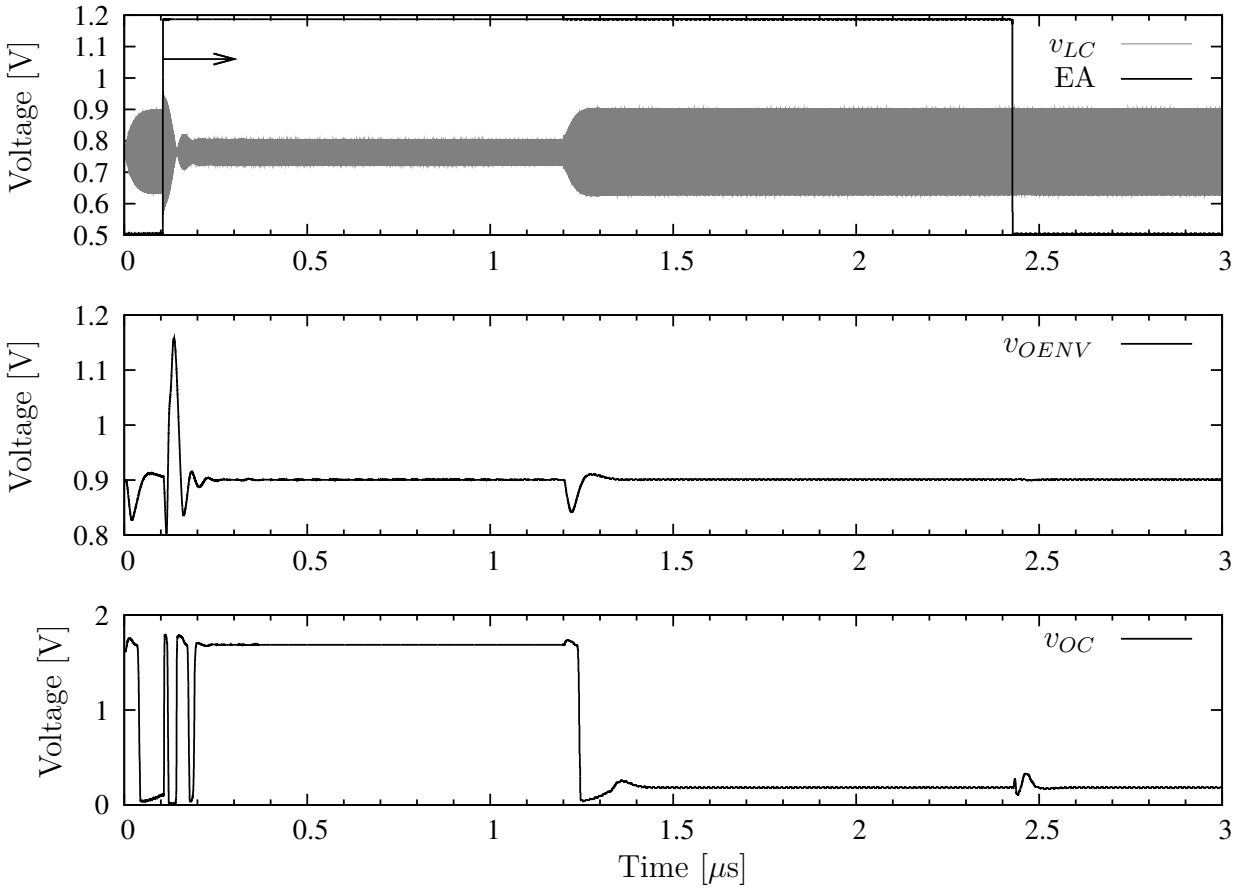


Source: The author.

to 920 MHz, and an input signal power equal to −27 dBm. At 100 ns EA rises and the Q is measured. At 1.2 μs S_r opens, only one falling pulse is seen in v_{OC}, and we note that the system is tuned with the incoming signal.

C_r is designed to be equal to $C_0/10$, so the number of pulses seen in v_{OC} should be higher than the observed in Fig. 5.28. This is due to the high Q ($\cong$ 1000) observed when $I_{REF} = 3$ mA. With 3 pulses we have that $Q \cong 100$ according to what is calculated previously. Hence, something is decreasing the Q of the *LC* network. It turns out that the RF signal source has an equivalent output impedance equal to 50 Ω. This impedance is in parallel with C_{t1} and seen from L_0, it seems that C_{t2} is a lossy capacitor that decreases the Q of the L_0-C_0-C_r network. Hence, the losses inserted by either the signal source or the system that the *LC*

Figure 5.28: Complete sequence of the LC parameter extractor for $I_{REF} = 3\,\text{mA}$.



Source: The author.

network is inserted, should be compensated by the negative resistance to further increase the Q of the resonating circuit.

The frequency response of the designed LC network can be seen in Fig. 5.29 using different I_{REF} values. It is considered that the LC tank is loaded with $50\,\Omega$ and that the signal source has an output power equal to $-27\,\text{dBm}$. To obtain these curves, the terminal is placed on v_l node, seen in Fig. 5.26(b), and the RF_{in} node is loaded with $50\,\Omega$ only. Here we note that I_{REF} almost had to be doubled to obtain an input impedance as high as the one seen in Fig. 5.27.

We plot the complete tuning sequence of the LC parameter extractor in Fig. 5.30, using the test bench of Fig. 5.26(a) for $I_{REF} = 5\,\text{mA}$. This is done to confirm that the LC network has a high Q when it is loaded by the RF signal generator. In this case, a signal frequency equal to 925 MHz is used. This frequency is tuned with the LC network as it is seen in Fig. 5.29.

I_{REF} is related with the Q of the loaded LC network and with the number of pulses of v_{OC} in table 5.7. We also plot in Fig. 5.31 the simulated and calculated number of pulses versus the Q of the LC tank. We note that eq. (5.15) can predict well the number of pulses, but there is a small deviation from the simulated results of 1 pulse when Q is between 200 and 400. This is due to the assumption that after 2τ, we would not be able to distinguish the envelope peaks.

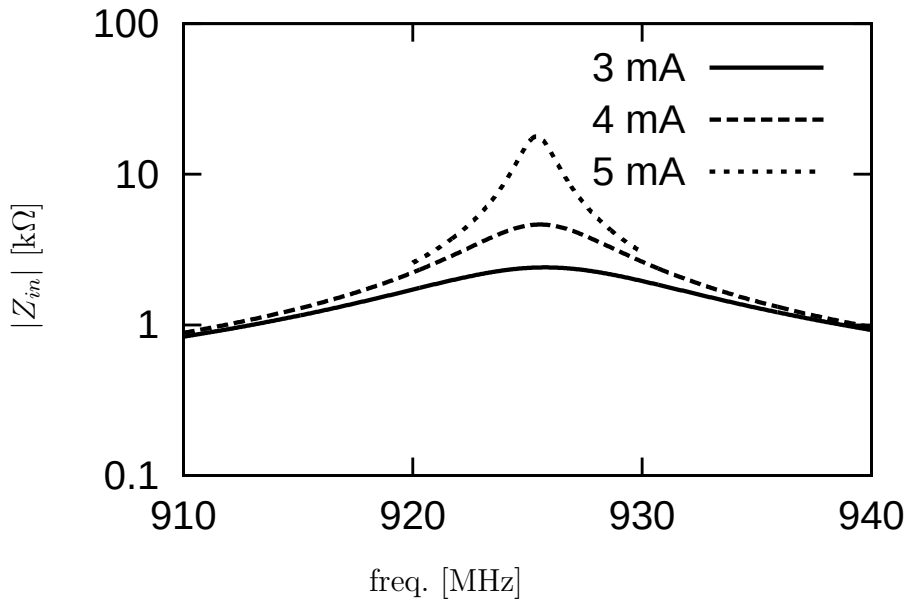
Using (5.15) and the designed f_r of this LC parameter extractor, we have that:

$$\frac{\partial N_d}{\partial Q} = 0.63(1.05 - 1). \tag{5.21}$$

The first integer of (5.21) can be found as:

$$I = \frac{1}{0.63(1.05 - 1)} = 31.7. \tag{5.22}$$

Figure 5.29: Input impedance of the loaded LC network for different I_{REF} values.



Source: The author.

Table 5.7: Table relating I_{REF}, Q and the number of pulses of v_{OC} for the designed LC network.

I_{REF} (mA)	Q	v_{OC} pulses
0	10.7	0
1	27	1
2	46	1
3	78	2
3.5	106	3
4	150	5
4.5	247	9
4.75	356	12
4.85	425	13
4.9	468	14
5	578	16

Source: The author.

Hence, the sensitivity of the designed LC parameter extractor is equal to 31.7, which means that this is the minimum ΔQ that creates a detectable output change.

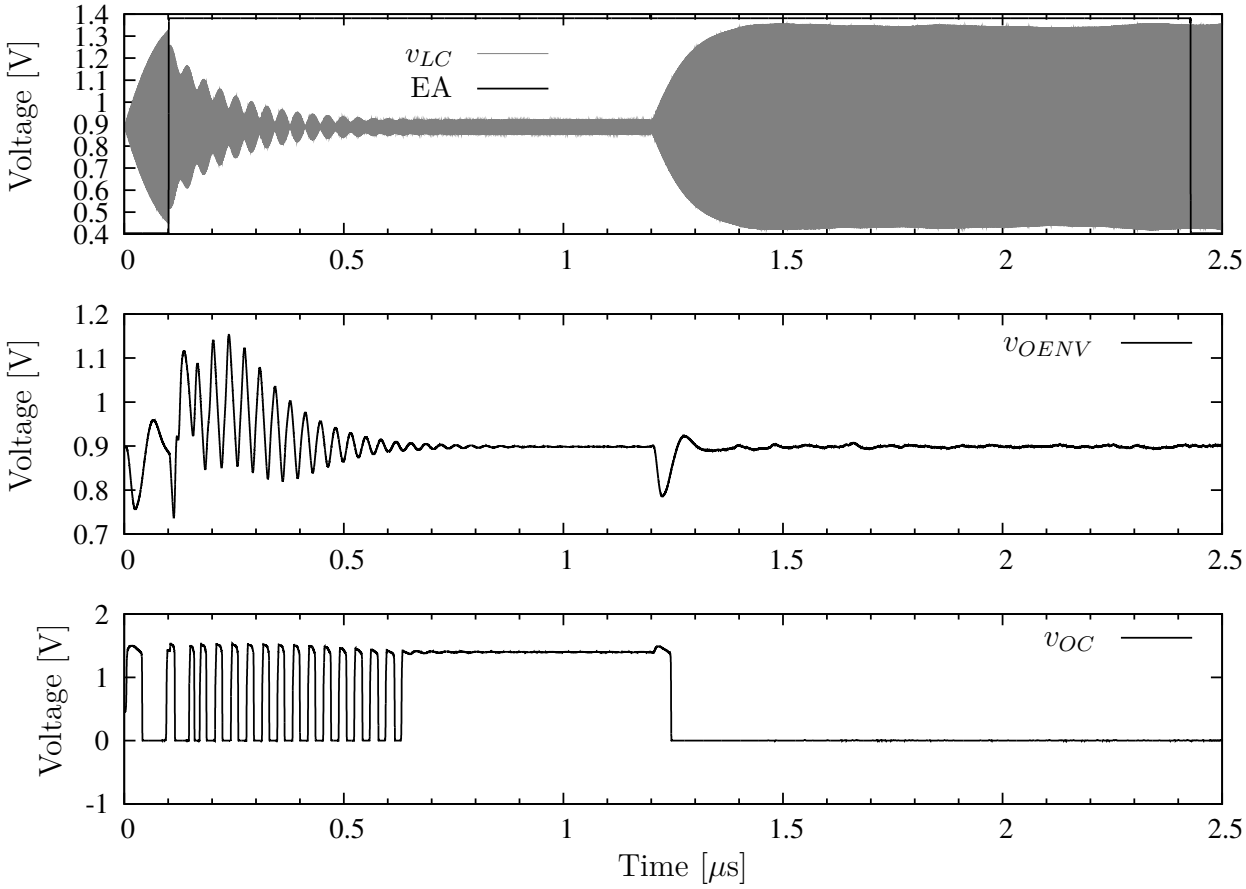
Since the designed LC parameter extractor can detect if the resonating network is detuned with the signal source, we calculate the minimum frequency deviation from f_0 that creates a detectable output change. Based on (5.15), this frequency deviation can be obtained as:

$$\Delta freq(\%) = \frac{f_{rmin}}{f_0}(\%) = \frac{1}{1 + 0.63Q_0} \times 100, \tag{5.23}$$

where f_{rmin} is the minimum frequency deviation that produces a detectable output. Equation (5.23) is potted in Fig. 5.32 versus Q. We note that the resonant frequency sensitivity decreases with Q.

The designed prototype have a total current consumption equal to 1.6 mA, considering

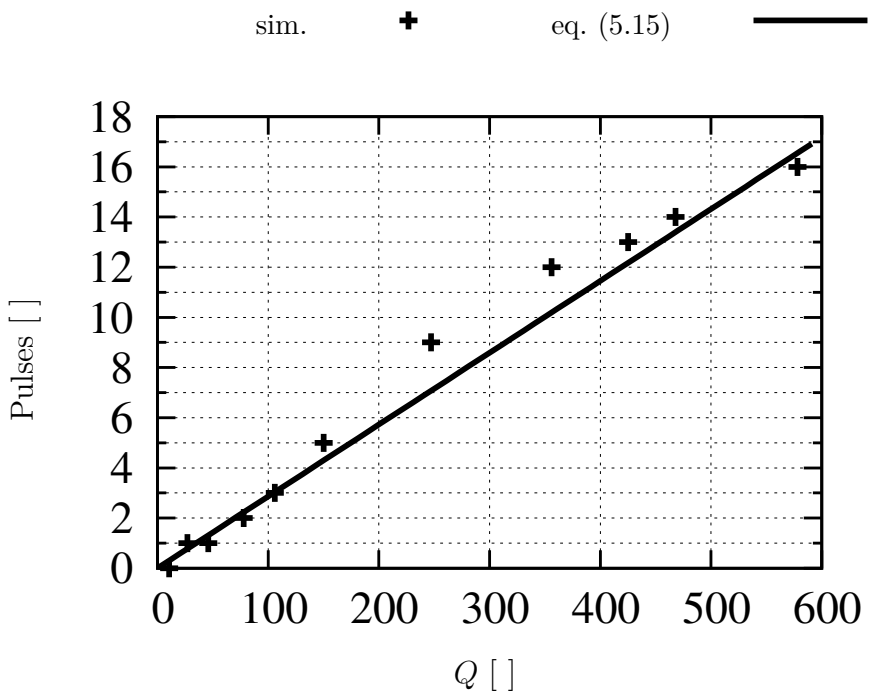
Figure 5.30: Complete sequence of the LC parameter extractor for $I_{REF} = 5\,\text{mA}$.



Source: The author.

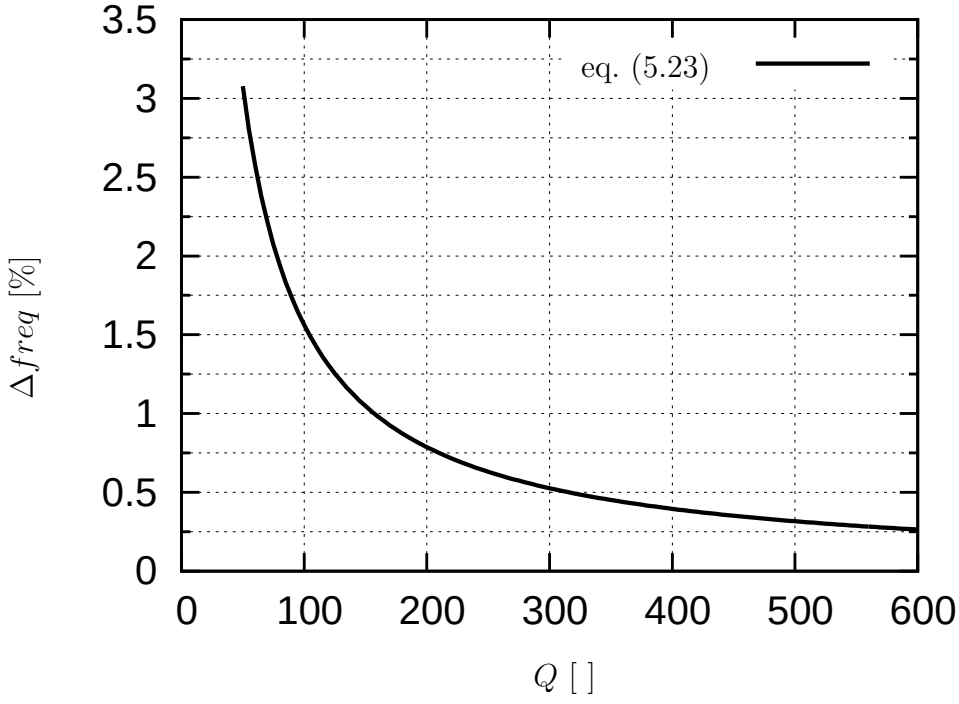
that $I_{REF} = 0\,\text{mA}$. From this 1.6 mA, the output buffer uses $300\,\mu\text{A}$.

Figure 5.31: Comparison between the simulated and calculated number of pulses versus the Q of the loaded LC network.



Source: The author.

Figure 5.32: Detectable frequency deviation from f_0 versus Q.



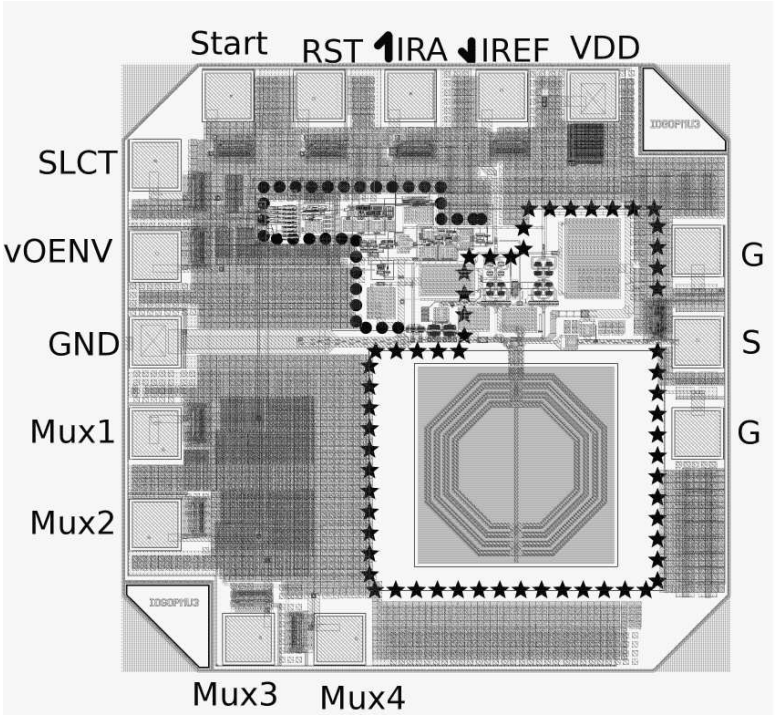
Source: The author.

5.5 MEASUREMENT RESULTS

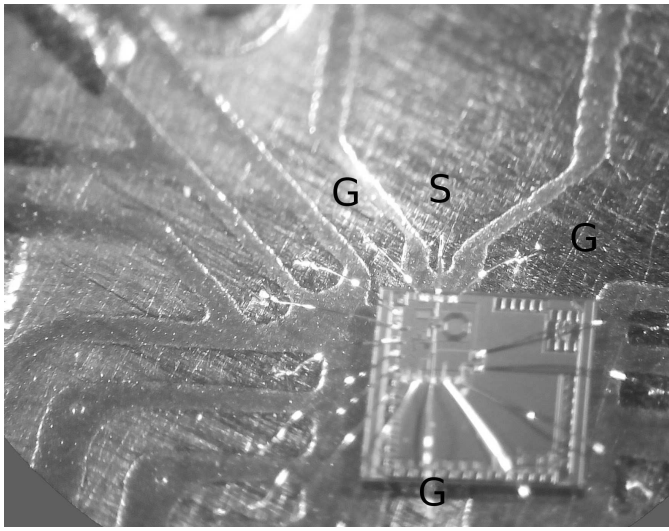
The presented system is implemented in standard a 130-nm CMOS process and the layout of the IC can be seen in Fig. 5.33(a). The LC network and its Q-enhancing circuit are enclosed by the stars and it occupies 0.26 mm^2. The other blocks of this system are enclosed by the dots and they have an equivalent area of 0.034 mm^2.

We wire-bonded the prototype on an FR-4 PCB, as it is seen in Fig. 5.33(b). A gold wire bonding is used with a wire diameter of 25 μm. The 900-MHz signal goes to the chip guided by a coplanar microstrip line and by the wire bond (S).

Figure 5.33: Layout and fabricated LC parameter extractor wirebonded on an FR-4 PCB in (a) and (b), respectively.



(a)



(b)

Source: The author.

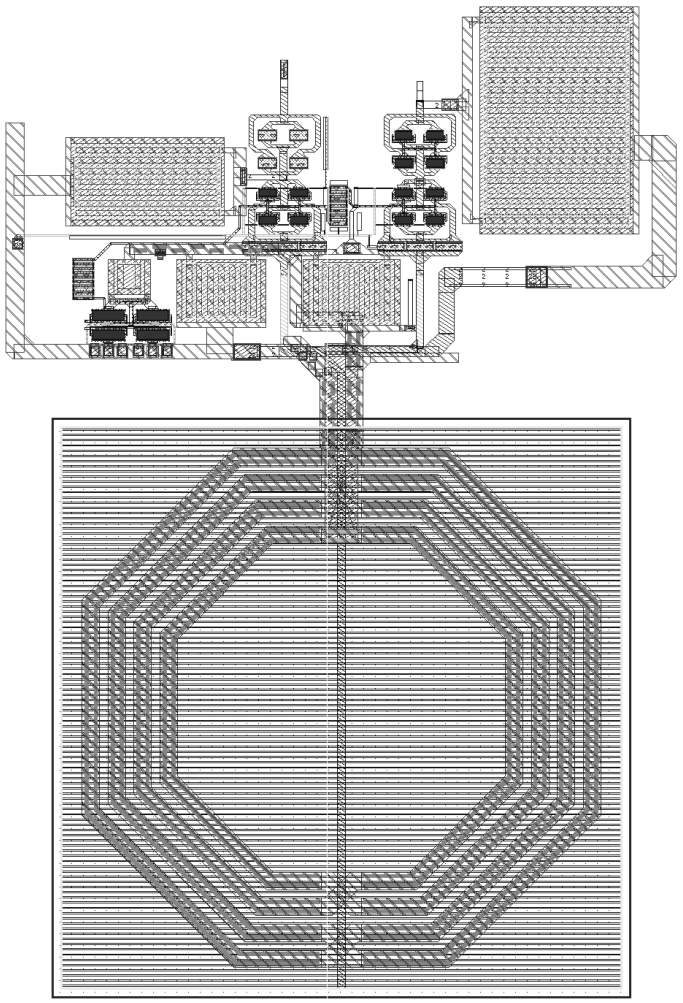
In Figs. 5.34 and 5.35 the reader can see the layout zoom of the designed enhanced Q cell, envelope detector, comparator, and digital cells (controller, counters, and mux).

The frequency response of the input impedance measured with a vector network analyzer (VNA) can be seen in Fig. 5.36, for different values of I_{REF}. We note that the measured resonant frequency decreased from the simulated results. This deviation is expected and it is due to the added parasitics from the pads, wirebondings, PCB, and it can also be credited to process variation. Also note that the resonant frequency decreases as I_{REF} increases. This is due to the capacitance variation of the transistor that is responsible for the negative resistance. Here we can see that is difficult to predict all of these uncertainties, and then we understand the importance of frequency tuning.

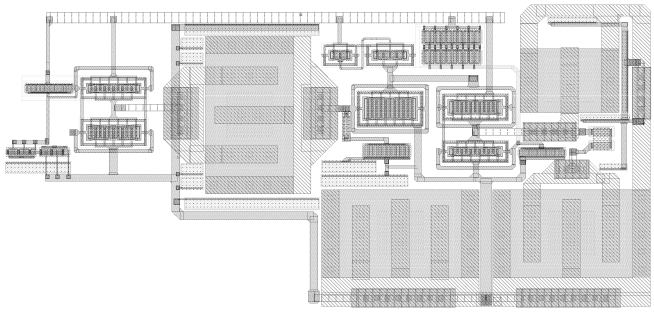
In table 5.8, we relate I_{REF} with the simulated and measured Q of the designed parameter extractor. It is observed that the measured Q is higher than the simulated, for currents above 2.5 mA.

The detected envelope measured when S_r closes can be seen in Fig. 5.37. The start signal, that we see in gray, is externally generated and it is used to trigger the oscilloscope. We note that something different happens with the envelope when the start signal is higher than 0.5 V,

Figure 5.34: Layout of the designed enhanced Q cell and the envelope detector in (a) and (b), respectively.



(a)



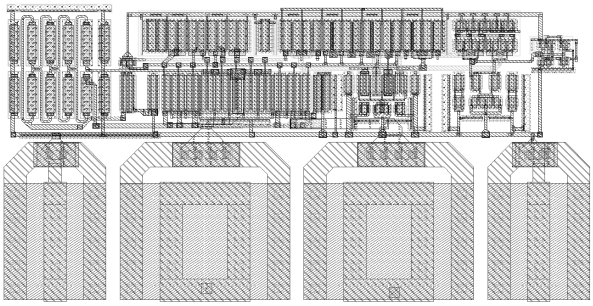
(b)

Source: The author.

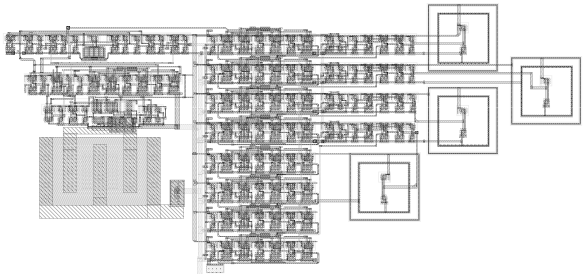
as it is shaded in gray. This behavior is the one that we look for and it is possible to measure the Q of the LC network with it. However, it is also seen an infinite sequence of peaks before the start signal and after it. These extra peaks do not allow us to have a correct peak counting. We also have these extra peaks when the RF signal is off and I_{REF} is equal to 0 mA.

In table 5.9 we report the lab. equipment used to make the presented measurement results.

Figure 5.35: Layout of the designed comparator and the designed digital cells in (a) and (b), respectively.



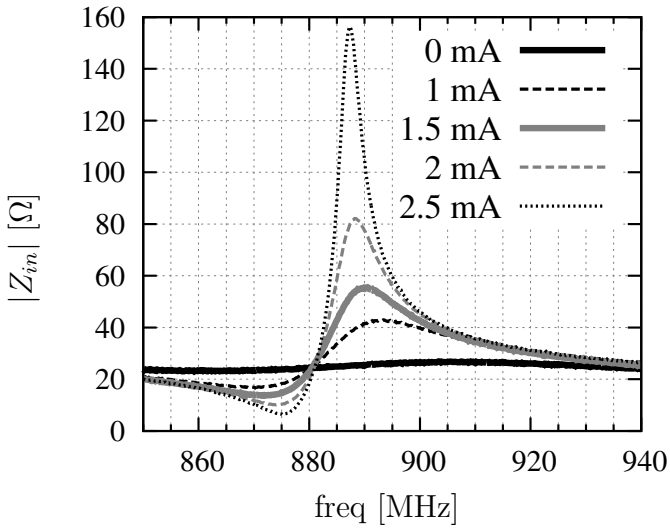
(a)



(b)

Source: The author.

Figure 5.36: Measured input impedance of the *LC* parameter extractor.



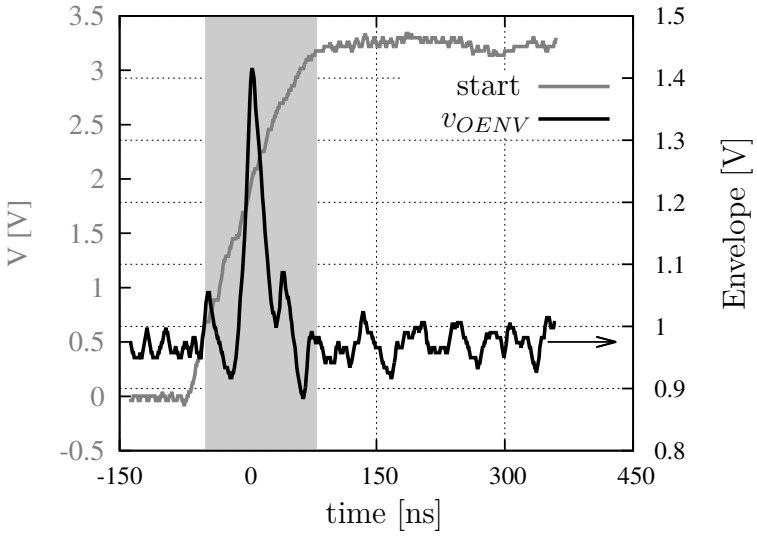
Source: The author.

Table 5.8: Table relating I_{REF} with the simulated and measured unloaded Q.

I_{REF} (mA)	Q sim.	Q meas.
1	23.9	23.7
1.5	49	46.8
2	100	94.5
2.5	253	216
2.7	341	593
3	1680	>4000

Source: The author.

Figure 5.37: Measured envelope using $I_{REF} = 3\,\text{mA}$.



Source: The author.

Table 5.9: Equipment used in the laboratory to obtain the presented measurement results.

Equipment	**Seller**	**Additional data**
Signal generator	Rohde & Schwarz	SMA 100A, 9 kHz to 6 GHz
Voltage Source	Agilent	E3634A
Source Measurement Unit (SMU)	Agilent	B2902A
Oscilloscope	Agilent	DSO-x-2014, 1 Gsample/s, 4 channel scope
Probe	Agilent	N2862B, 10:1, 150 MHz, passive, 10 MΩ//15 pF
VNA	Rohde & Schwarz	ZVB8, 300 kHz to 8 GHz

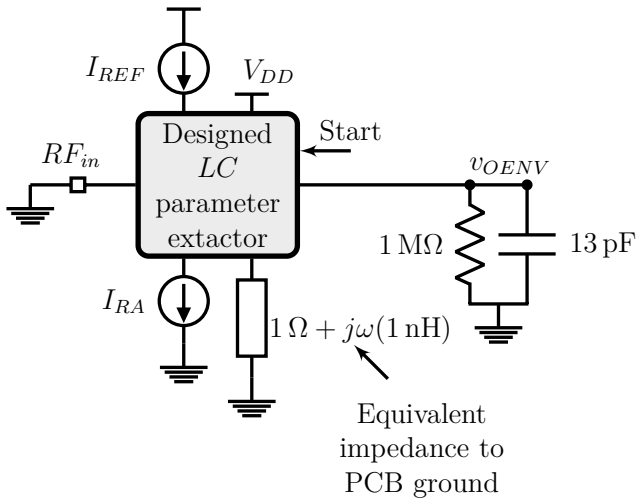
Source: The author.

5.5.1 Debugging

It is necessary to know what caused those extra peaks observed on the detected envelope. After we received the prototype, a similar test bench of the one shown in Fig. 5.38, was used to find in the simulator what caused the measured oscillations. In this test bench, no signal is placed on the RF_{in} port and a 1-nH inductor with a 1-Ω series resistance, that emulates a

wirebond [44], is placed between the IC's ground pad and the PCB ground.

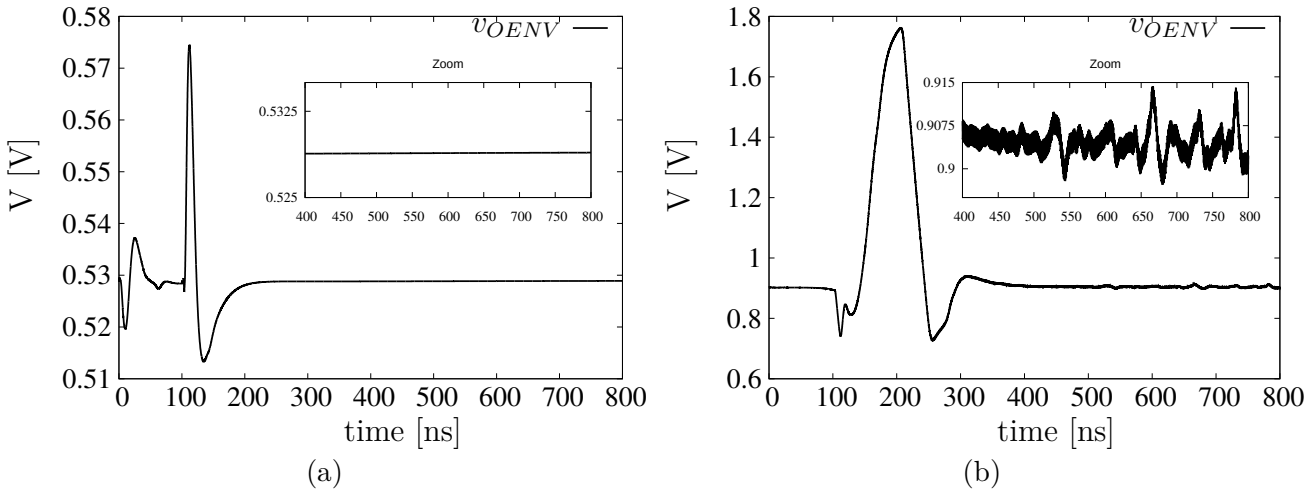
Figure 5.38: Test bench used to validate the designed prototype.



Source: The author.

The test bench of Fig. 5.38 is used to simulate the detected envelope presented in Fig. 5.39(a) and (b). The difference between these curves is that (a) shows the simulated envelope with the extracted RLC parasitics, while (b) presents the envelope obtained by a schematic simulation. The start signal has a rising slope at 100 ns, and we note that the simulated result using the schematic has a noisier transient response compared to the one simulated using the extracted parasitics.

Figure 5.39: (a) Simulated envelope with the extracted RLC parasitics and (b) envelope obtained with a schematic simulation.



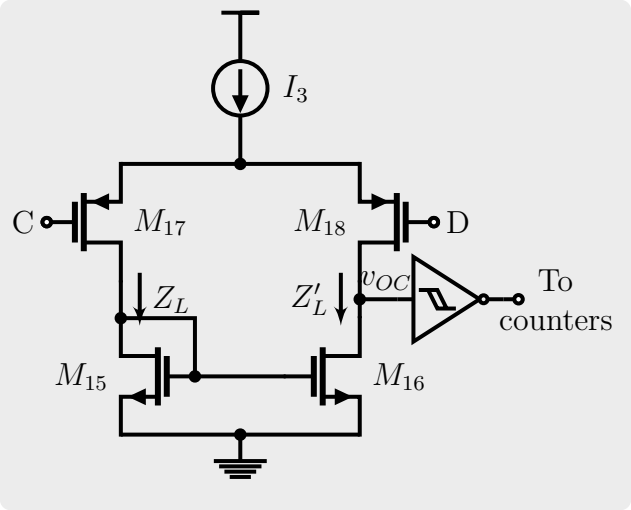
Source: The author.

Hence, in the presented case we concluded that the simulated schematic can predict the measured noise better than the test bench using the extracted parasitics. Probably, the extracted test bench have a high estimated filtering capability that was not seen on the fabricated chip.

This noise response was tracked down and we found that the 3rd stage of the comparator, that is shown in Fig. 5.40, is responsible for it. The presented noisy response was canceled by

decreasing the impedance of the load transistors (Z_L) used by this stage. We note that in the 'Simulation system' section, the transient curves are obtained using the new impedance of the 3rd stage of the comparator and considering the wirebond impedance to the ground.

Figure 5.40: 3rd and 4th stages of the comparator repeated for the reader convenience.



3rd & 4th stages
Conversion to digital domain

Source: The author.

Another possible source of noise is the flicker ($1/f$) noise. To minimize this kind of noise we redesigned the presented system using transistors with a higher area. To overcome eventual noisy signals we increased the hysteresis effect of the 2nd stage of the comparator.

5.6 SUMMARY

In the presented chapter we reviewed some self-tuned LC filters based on the Master-Slave tuning method. These self-tuned filters require a large area because the inductor is usually orders of magnitude bigger than other passive components and at least two of them are required. Hence, we present a solution for extracting the parameters of an LC network without the need of extra inductors. With the obtained data, the designer can easily know the Q of the resonating network and it is also possible to know how close the LC network is tuned with the input signal source.

We also modeled the step response of the voltage on an LC network, while it is connected to a sinusoidal voltage source. With this model, we proposed a method for estimating the parameters of an LC tank. Then, the LC parameter extractor system was conceived and the chip was designed using a 130-nm CMOS process.

The measurements results of the prototype is shown and we have seen that the prototype is almost fully working as expected. The problem may be the designed 3rd stage of the comparator and the $1/f$ noise.

6 CONCLUSIONS

From the motivations presented in the introduction, it was possible to conceive three novel on-chip LC tuning circuits for RFID systems, as presented in the thesis. Hence, hypothesis H1 is validated.

In the following sections we present the performance of the tuners conceived in this thesis with conclusions. The LC parameter extractor is also compared with some automatic tuners used in filters and it is also compared with a Q measurement system.

6.1 RFID TUNERS PERFORMANCE

The current-based tuner presented in chapter 4 was conceived to overcome eventual limitations imposed by the negative-resistance tuner, which has a voltage limit of approximately V_{DD} on the LC network.

Using the tuner based on negative resistances, the designer can be sure that the chosen capacitance configuration is at or very close to the resonant frequency. Using the current-based tuner, the chosen capacitance configuration might not be close to the resonance frequency. This is caused by the search routine that is used by this tuner. So, if the designer did not choose carefully the capacitance regions, the current-based tuner might choose a capacitance value that is far away from the resonant frequency.

It is important to note that the other RFID tuners, that were presented in chapter 2, do not report their performance. We are not able to see the tuner performance even in [45] that precedes [9]. Hence, we build table 6.1 to make a comparison among the designed systems in this thesis. We note that although the LC parameter extractor is not designed as a tuner, a simple digital control method can be integrated to implement this function.

Table 6.1: Performance of the tuners conceived in this thesis.

Method	**CMOS Process**	V_{DD}	I_{avg}	**Time for tuning**	**Area**	**Frequency**
Neg Res chapter 3	130 nm	3.3 V	$12\,\mu A/V$	250 ms	0.022 mm^2	125 kHz
RF current chapter 4	130 nm	3.3 V	$10\,\mu A$	32 ms	0.015 mm^2	125 kHz
Transient chapter 5	130 nm	3.3 V	1.6 mA	$> 2\,\mu s$	0.034 mm^2	900 MHz

Source: The author.

The LC parameter extractor presents the highest power consumption and it occupies the largest area among the systems presented in table 6.1. However, it has the advantage to digitally report the quality factor of the LC network and how close it is tuned with the input signal frequency. This characteristic makes this tuner a good candidate to be implemented in software-defined radio systems. As it is described in chapter 5, the frequency sensitivity of the LC parameter extractor is large ($\Delta freq > 3\,\%$), if the resonating network has a low Q. Then, this system alone may not be as accurate as the other methods for finding the resonance point of an LC network.

We note that the current consumption of the negative resistance method depends on the quality factor of the LC network and on the voltage on its terminals. The tuning time of the negative-resistance based tuner can be reduced by 8 times without any loss, in the designed

system. With this reduction, the time for tuning using the low frequency methods become similar.

One parameter of that may also be relevant to the reader is the required time to design these systems. The negative-resistance based tuner is more time consuming, compared to the others. This is due to the requirement to control the negative resistance over a wide voltage range. Then, with the given information in this section, the designer can choose among one of the proposed methods for tuning an RFID tag.

6.2 PERFORMANCE OF AUTOMATIC *LC* TUNERS AND *Q* MEASUREMENT SYSTEMS

The *LC* parameter extractor can be used to tune RFID tags, but it can also be compared to automatic *LC* tuners used in filters and to systems that perform *Q* measurements. Hence, we use table 6.2 to make this comparison.

Table 6.2: Table containing systems that either automatic tune their *LC* network or measure their *Q*.

Ref.	**Method**	**Process**	**Freq.**	**Area**	V_{DD}	**Current**	**Time for tuning / measuring**
[36]	MS	75-GHz SiGe Bipolar	5.5 GHz	$> L$	1.8 V	< 19 mA	NA
[14]	MS	0.25-μm BiCMOS	1.9 GHz	$> L$	2.7-3.3 V	18 mA	NA
[15]	3 dB	0.35-μm CMOS	2 GHz	$<.0725$ mm^2	1.3 V	< 3.6 mA	9 it.
[39]	Transient	x	10 kHz	Off chip	5 V	NA	$\cong 10Q/\omega_0$
chapter 5	Transient	130-nm CMOS	0.9 GHz	.034 mm^2	3.3 V	1.6 mA	2 μs

Source: The author.

References [36] and [14] are classical references that use a master-slave structure. If we consider that their slave inductor has an area of $200\,\mu\text{m} \times 200\,\mu\text{m}$, the master will occupy at least this area ($0.04\,\text{mm}^2$). From the information given in [36] it is estimated that their master structure uses less than 19 mA. The "time for tuning" requirement does not apply to [36] and [14], because they do not have a minimum time for tuning. Considering that the power-up phase has passed and no noise is inserted into the master, these filters are always tuned.

It is easy to see that if it is necessary to implement a very high Q circuit, as the one seen in [36], the master filter should be always on. However, if it is required a filter with $Q \cong 10$, as seen in [14], the designer should look for another tuning structure that reduces area and current consumption. Or at least, the designer should sample and hold the DC output voltages obtained from the master and turn it off.

In [15], the proposed automatic Q tuner takes 9 "iterations" for setting a $Q = 120$. This 'time' is due to two interacting loops that are associated with the value of Q and the amplitude of the filter at f_0. In the paper, the authors do not comment about the required time taken for each interaction, but we remark that this system requires two different test tones at its input. One signal must have a frequency equal to f_0 and another signal should have a frequency equal to the desired -3-dB cutoff frequency of the filter. This imposes one requirement to the test equipment that must switch between these frequencies whenever it is required by this integrated system.

The work presented in [39] uses a transient method for finding the Q of a resonating network, which is similar to the system designed in chapter 5. It is conceived an off-chip system

that operates at 10 kHz and measures very high quality factors as such as 10^5. For this Q, the authors mentioned that the measurement time for one sample was around 12 s (roughly, we can estimate it from chapter 5 as $10Q/\omega_0 = 15.9\,\text{s}$). They also have a generated data, that is used to obtain the value of Q, of 10^7 samples. We know that it is not required, in most filter applications, to obtain such high Q and also that when ω_0 increases the measurement time decreases proportionally to it.

A filter with $Q = 100$ and with its center frequency at 900 MHz, has a time constant $\tau = 35\,\text{ns}$, which results in 160 voltage peaks for an oscillation time equal to 5τ. It would be required to have an 8-bit counter to store these number of peaks, which is feasible. From what is shown in [39], we see that it is required to have either a clock extractor or a built-in time reference to estimate the Q.

The LC parameter extractor presented in chapter 5 does not require any time reference circuitry (excluding that simple one that is used to open S_r), since the Q measurement is realized by an analysis of the resulting envelope obtained from the signal source and the detuned LC network. This system also decreases the signal frequency that contains the Q information. It is obtained an envelope frequency equal to 43 MHz, considering a filter with $f_0 = 900\,\text{MHz}$ and a 10-% detuning capacitance. Then, the detuned envelope of a filter with $f_0 = 2.4\,\text{GHz}$ and with a 10-% detuning capacitor, reaches only 117 MHz. This characteristic also makes the conceived system capable to operate in multiple bands, without major modifications on its design. Thus, the obtained area of $0.034\,\text{mm}^2$ would almost be the same for a multi-band LC parameter extractor. In a first order analysis, it is only required to add another detuning capacitor and more counters to store the information of the second filter.

6.3 SUMMARY OF CONTRIBUTIONS

The main contributions proposed in this thesis are:

- An LC network tuner based on negative resistances that is intended to be used in RFID applications operating at 125 kHz. Although other automatic filter tuners use negative resistances, we proposed a novel application for this Q-enhancing block that considerably decreases the complexity of the tuning decision circuitry. As the reader can see in the appendix, we explained with details the behavior of a cross-coupled pair using MOS transistors over a wide voltage range. Then, we propose a circuit to automatically control the value of the negative resistance over different voltage levels, as the reader can see in chapter 3. We also proposed the on-chip design of this tuner using a CMOS process;

- An LC network tuner also intended to be used in RFID applications that is based on a sample of the RF limiter short-circuit current. This current is processed by a variable-gain current amplifier and compared with a moving reference current. This novel method can have the lowest power consumption among the presented tuners. This is partially due to the possibility to scale the reference current by the WTA. As far as the author is aware, the proposed WTA current scaling using the aspect ratio of the transistors is also a novel contribution. We also proposed the on-chip design of this tuner using a CMOS process;

- A parameter extractor, operating at 900 MHz, for LC filters that digitally reports their quality factor and their resonance values. In this parameter extractor, we presented a novel method for measuring the quality factor of the LC network by using a detuning capacitor. We also proposed a method for counting the detected envelope peaks and we integrated the system using a CMOS process;

6.4 FUTURE WORK

In a short term we are going to resubmit the designs that were presented in chapter 4 and chapter 5 with the required corrections. We have an LC tuner based on the RF limiter current that was designed using Ceitec 0.6-μm process that probably will behave as expected. We do this assumption because we have previously tested a translinear loop with an on-chip current source and both worked as expected. So, when this LC tuner arrives, we will be able to have good tuning results to report.

Also, a slightly modified version of the tuner presented in chapter 4 is being prepared to be patented.

In a longer term, it would be interesting to propose a digital control circuitry for the LC parameter extractor. Then, the system conceived in chapter 5 could be programed to behave as required by the user.

6.5 PUBLICATIONS

We have publised the tuning technique presented in chapter 3 in [16]. The paper is entitled as “Automatic LC network tuner based on negative resistances” and it was published by the Electronics Letters in 2015.

We have also submitted a paper containing the on-chip system presented in chapter 3 to "TCASII: Express Briefs". This paper was accepted for publication in the end of 2017 and it is entitled “On-chip automatic LC tuner for RFID tags based on negative resistances".

Appendices

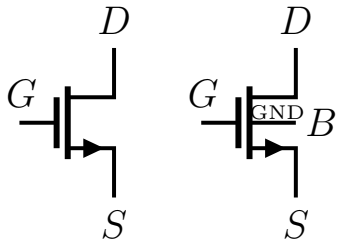
A GENERAL CONSIDERATIONS

In this appendix we discuss about general considerations made during the thesis.

A.1 TRANSISTORS

Standard components of the foundry's kit were chosen in every system designed in this thesis. The nMOS transistors, for instance, share the same substrate. Due to this, the chosen schematic representation of this transistor is shown in Fig. A.1(a) without the bulk contact. A more complete schematic of this transistor can be seen in Fig. A.1(b) with an explicit bulk contact connected to GND. Adding the bulk contact of the nMOS transistors would not add any additional information, then this contact was suppressed in the schematics seen in this thesis. The pMOS transistors does not share the same substrate, but they have their substrate connected to V_{DD}, unless it is stated otherwise.

Figure A.1: Schematic of a nMOS transistor (a) without the bulk contact and (b) with this terminal connected to ground.



(a) (b)

Source: The author.

A.2 MONTE CARLO

A Monte Carlo statistical simulation requires many iterations, usually > 100, in order to see the effect of multiple process extremes. Corner simulations on the other hand are faster because the corner model is already defined and it is not stylistically varied. Hence it can not obtain the combinations in the process extremes, seen in the Monte Carlo case.

It is possible to set the simulator to use Monte Carlo methods to investigate the influence of statistical variations in the values of components. In this thesis all the systems were validated using Monte Carlo runs. Depending on the user PDK more than one Monte Carlo option will be available. In this thesis we used the setting that according to the PDK manual gives: "full statistical process variation; best representation of long term manufacturing performance".

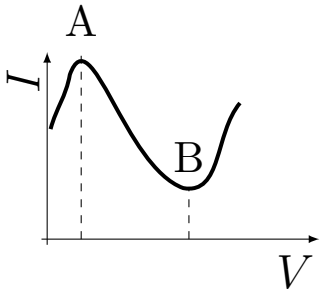
B MORE ABOUT NEGATIVE RESISTANCES

B.1 NEGATIVE RESISTANCES

As defined in [46], the negative resistance is an electrical property observed on some circuits and devices in which an increment of the voltage brings a decrement of the current on its terminals. The devices with negative resistance are usually limited in the energy that they can handle and exhibit a very specific region where this effect is seen.

Using the given definition, we can plot in Fig. B.1, the expected $I \times V$ curve of a device with negative resistance. We note that between points **A** and **B** we have the negative resistance effect and its equivalent conductance can be calculated using the slope of the curve.

Figure B.1: Typical IxV curve observed in devices with negative resistance.



Source: Adapted from [46, 47].

We can find the design of devices using negative resistances in the 1910s in [47] with the dynatron, which is a vacuum tube electronic device. The author comments that the dynatron could be used as an oscillator at audio and radio frequencies or as a voltage or current amplifier. Actually, this negative-resistance device was used as an oscillator for radio receivers until the 1940s when it was replaced by the transitron [48, 49].

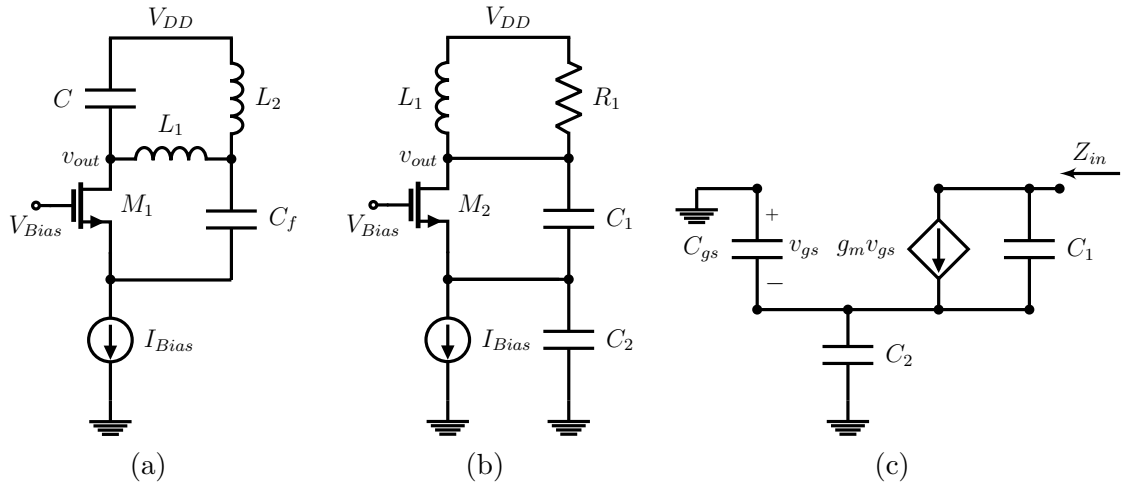
In addition to the dynatron and transitron, we can find devices with negative resistance in tunnel diodes (TDs) and in resonant tunnel diodes (RTDs). The TDs, which are formed by a heavily doped p-n junction, were proposed in 1958 by Esaki and were used in oscillators up to 100 GHz [50]. The RTDs, which are double-barrier structures having a thin GaAs sandwiched between two GaAlAs (gallium aluminum arsenide) barriers [51], were proposed in 1974 by Esaki. They have a better speed index and higher speed oscillators can be built, as we can see in [52] where an 1.5 THz oscillator is presented. The RTDs can also be used in digital circuits. According to [53], the RTDs are suited for the design of highly compact, self-latching logic circuits. This becomes evident when the authors compare the number of components to implement digital functions.

The Gunn diodes are also worth to mention. Their negative resistance effect were observed by Gunn, in 1962, when he was having a 'noisy' response of the reflected signal coming from a $50\,\Omega$ transmission line that was terminated by his devices [54]. His diodes are unipolar devices with no p-n junction and were firstly made of n-type GaAs and n-type InP [55]. Millions per year of Gunn diodes were sold in the 1980's, however they lost part of the market due to the use of field-effect transistors in radios [54]. Nowadays, we can easily buy Gunn diodes suited for frequencies up to 110 GHz [56]. We can see an attempt to increase the Gunn diode oscillation frequency in [57]. In this citation the authors grow a layer of InGaAs on a InP substrate and

measure an oscillation of 164 GHz.

Not only the aforementioned devices present the negative resistance effect. We can see this effect in the classics Hartley [58] and Colpitts [59] oscillators, invented in the 1910s. In these oscillators, the losses of the LC network are compensated through a positive feedback achieved due to an active-passive configuration as we can see in Fig. B.2. In other words, the negative resistance effect is observed when we increase v_{out} and, as a result, we see that the drain to source current of the transistor is decreased due to an increase of the transistor's source voltage.

Figure B.2: Hartley and Colpitts oscillators using nMOS transistors in (a) and (b), respectively. (c) Small-signal model for the Colpitts common-gate negative resistance cell.



Source: (a) and (b) are extracted from [60] and [61], respectively. (c) the author.

It is also possible to estimate the negative resistance of these oscillators using the small-signal model of the MOS transistor. In Fig. B.2(c) we show the small-signal model for the Colpitts common-gate negative resistance cell and its input impedance can be equated as:

$$Z_{in}(\omega) = \frac{-g_m}{\omega^2 C_p C_1} + \left[\frac{1}{j\omega C_p} + \frac{1}{j\omega C_1}\right], \tag{B.1}$$

where $C_p = C_2 // C_{gs}$ and g_m is the transistor's transconductance. Here we confirm that the negative resistance of the Colpitts oscillator is due to the transistor (g_m, mainly) and the passive components.

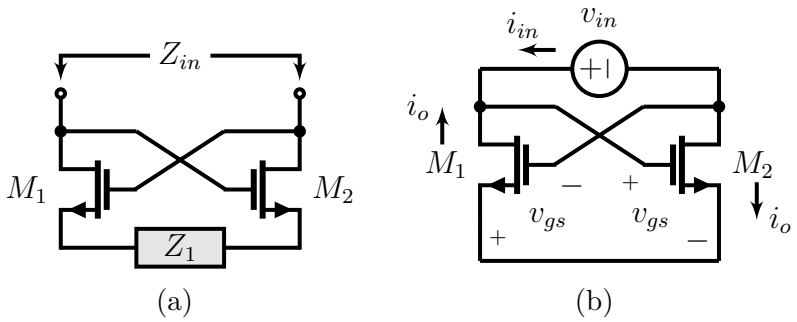
Throughout the years we have seen the integration and improvements on the Colpitts oscillators. Among them, we can cite [62] and [61] in their attempt to extend the phase noise of Colpitts oscillators using new circuit techniques in differential versions. These circuits were presented using integrated BiCMOS and CMOS processes in 1997 and 2002, respectively.

Traditionally, Colpitts oscillators were considered easier to be integrated than Hartley oscillators because the latter needs a tapped inductor to be implemented. However, with the advances in the CMOS technology, in 2007 we see a fully-integrated differential Hartley oscillator [60] oscillating with a maximum frequency of 4.5 GHz.

A very interesting and elegant circuit that presents negative resistance is the cross-couped pair. It has evolved for almost 100 years and it is seen in inumerous applications. It is not a surprise that the 'Circuit For All Seasons' column reserved 3 issues to talk only about this circuit and its applications [63, 64, 65]. We can also see, in the same column, the cross-coupled pair being used in a 'StrongARM' latch and in a bridged T-coil in [43] and [66], respectively.

We can see a basic nMOS cross-coupled cell in Fig. B.3(a). Note that the biasing circuitry is omitted for simplicity and that the input impedance of this cell is seen accross the drain of

Figure B.3: (a) Basic nMOS cross-coupled cell and (b) circuit used to estimate its input resistance.



Source: (a) Extracted from [63]. (b) The author.

the transistors. If we take the circuit of Fig. B.3(b), we have that when the drain voltage of M_1 increases, its drain to source current decreases because its gate to source voltage decreased. Then, if $Z_1 = 0$ and with the aid of Fig. B.3(b), the resistance seen across the cross-coupled pair can be found as:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{2v_{gs}}{-i_o} = \frac{-2}{g_m}. \tag{B.2}$$

If Z_1 is a capacitor, Z_{in} contains a positive capacitance ($Z_{in} = -2/g_m + j/(\omega C)$), allowing the cancellation of positive capacitance at the drains of the cross-coupled pair [63, 66].

The cross-coupled pair using CMOS has been used in many analog applications shuch as: Q-enhancing circuits for LC filters [15], impedance negators [66], sense amplifiers [64] and oscillators [67]. Recently, we have seen in CMOS a 300-GHz fundamental oscillator in [67] and an 1.3-THz 6th order oscillator in [68] both citations use the cross-coupled pair as its negative-resistance cell.

According to the Barkhausen criteria, the circuit can oscillate if the total phase shift around the loop is 360º and the absolute value of the open loop gain is equal to 1, both at the oscillation frequency. Hence, if the losses of an LC network are not fully compensated by a cross-coupled pair, the system will not oscillate, as it is seen in chapter 3.

The advantages of using CMOS are its large scale integration capability and its lower price compared to other technologies. Unfortunately, the aforementioned devices with negative resistance such as the Gunn diodes and the RTDs can not be implemented in CMOS technology, yet. However, we can copy some characteristics of these devices and use them in digital circuits. One example can be seen in [69], where the authors mimic the negative resistance behavior of an RTD with a CMOS cell. In the same paper it is shown a cell that is configured to realize threshold logic gates operations, as it occurs with RTDs.

B.2 LARGE SIGNAL ANALYSIS OF THE CROSS-COUPLED PAIR

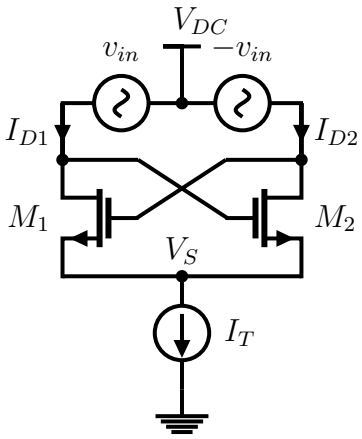
Considering the cross-coupled pair of Fig. B.4 and that the transistors are operating in ther exponential regime, I_D can be written as:

$$\begin{aligned} I_D =& I_{D1} - I_{D2} = I_{S1}\left(e^{\left(\frac{V_{G1}-V_{TH}}{n_1}-V_S\right)\frac{1}{U_T}}\right)\left(1-e^{(-V_{D1}+V_S)\frac{1}{U_T}}\right) \\ &- I_{S2}\left(e^{\left(\frac{V_{G2}-V_{TH}}{n_2}-V_S\right)\frac{1}{U_T}}\right)\left(1-e^{(-V_{D2}+V_S)\frac{1}{U_T}}\right). \end{aligned} \tag{B.3}$$

And I_T can be obtained as:

$$I_T = I_{D1} + I_{D2} = I_{S1}\left(e^{\left(\frac{V_{G1}-V_{TH}}{n_1}-V_S\right)\frac{1}{U_T}}\right)\left(1-e^{(-V_{D1}+V_S)\frac{1}{U_T}}\right) + I_{S2}\left(e^{\left(\frac{V_{G2}-V_{TH}}{n_2}-V_S\right)\frac{1}{U_T}}\right)\left(1-e^{(-V_{D2}+V_S)\frac{1}{U_T}}\right). \tag{B.4}$$

Figure B.4: NMOS cross-coupled pair used in this section.



Source:The author.

It is possible to equate V_S from (B.4), supposing that $I_{S1} = I_{S2}$, $n = n_1 = n_2$, $V_{G1} = V_{DC} - v_{in} = V_{D2}$ and $V_{G2} = V_{DC} + v_{in} = V_{D1}$ as:

$$e^{\frac{-V_S}{U_T}} = \frac{I_T}{I_S}\frac{1}{e^{\frac{V_{DC}-V_{TH}}{nU_T}}2\cosh\left(\frac{v_{in}}{nU_T}\right)} + \frac{e^{\frac{-V_{DC}}{U_T}} + \cosh\left[v_{in}(\frac{n+1}{nU_T})\right]}{\cosh(v_{in}/(nU_T))} = \frac{I_T + 2I_S\cosh\left[v_{in}(\frac{n+1}{nU_T})\right]e^{\left(\frac{V_{DC}-VT}{n}-V_{DC}\right)\frac{1}{U_T}}}{2I_S\cosh\left(\frac{v_{in}}{nU_T}\right)e^{\frac{V_{DC}-V_{TH}}{nU_T}}}. \tag{B.5}$$

We plot V_S versus v_{in} can be seen in Fig. B.5. We note that the simulated behavior of V_S is the same obtained using (B.5).

If it is required to implement a current source to obtain I_T, it is important consider the value of V_S. Otherwise, the MOS transistor used as a current source may operate outside its saturation region. We used the following parameters to obtain the curve presented in Fig. B.5: nMOS transistors, $I_S = 0.6\,\mu$A, $V_{DC} = 1.0\,$V, $V_T = 0.6\,$V, $I_T = 1\,$nA, $n = 1.2$ and $U_T = 25\,$mV. The reader may notice that a pMOS cross-coupled pair is used in chapter 3 to implement the negative resistance. With this cell the signal can go below 0 V and 'close' to V_{DD} so that the transistor that operates as a current source and does not leave its saturation region.

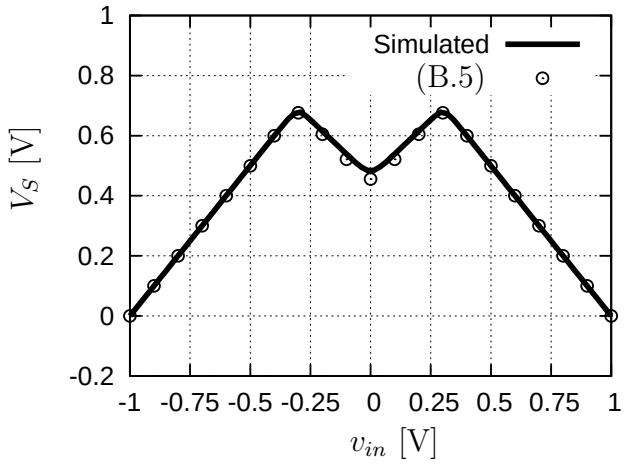
I_D/I_T can be written as (supposing the same conditions used to obtain V_S):

$$\frac{I_D}{I_T} = \frac{-\sinh\left(\frac{v_{in}}{nU_T}\right) + \sinh\left(\frac{v_{in}}{U_T}+\frac{v_{in}}{nU_T}\right)e^{(-V_{DC}+V_S)\frac{1}{U_T}}}{\cosh\left(\frac{v_{in}}{nU_T}\right) - \cosh\left(\frac{v_{in}}{U_T}+\frac{V}{nU_T}\right)e^{(-V_{DC}+V_S)\frac{1}{U_T}}}. \tag{B.6}$$

By an analysis of the cross-coupled pair we have that V_S is smaller than V_{DC}, due to a voltage drop on the transistors. If this difference is higher than 0.2 V the terms multiplied by the exponential are reduced by at least 6 orders of magnitude. Hence, (B.6) can be rewritten as:

$$\frac{I_D}{I_T} = -\tanh\left(\frac{v_{in}}{nU_T}\right). \tag{B.7}$$

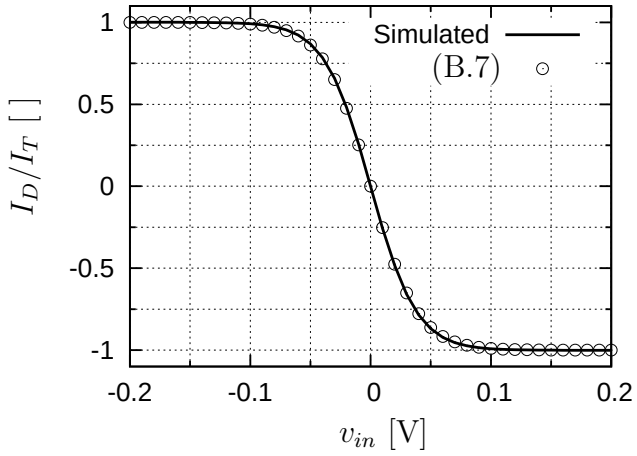
Figure B.5: V_S obtained by circuit simulation and using (B.5).



Source: The author.

The behavior voltage of I_D/I_T can be seen in Fig. B.6. We also see that the calculated behavior of I_D/I_T agrees with circuit simulation.

Figure B.6: I_D/I_T versus v_{in} obtained by circuit simulation and using (B.7).



Source: The author.

From (B.7) we can write that:

$$\begin{aligned} \frac{2I_1 - I_T}{I_T} &= -\tanh\left(\frac{v_{in}}{nU_T}\right) \\ \frac{I_1}{I_T} &= \frac{-\tanh\left(\frac{v_{in}}{nU_T}\right) + 1}{2}, \end{aligned} \tag{B.8}$$

and

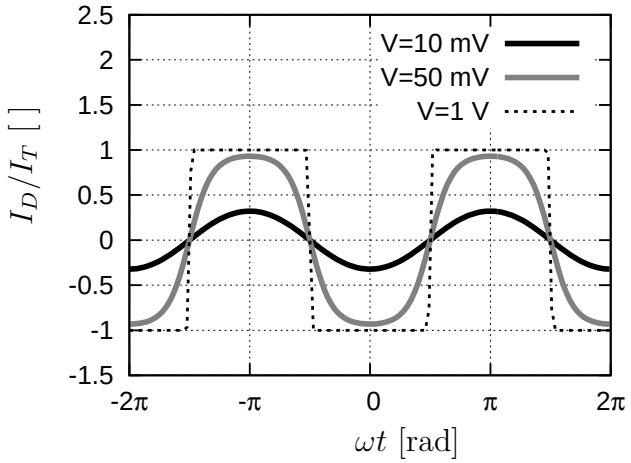
$$\frac{I_2}{I_T} = \frac{\tanh\left(\frac{v_{in}}{nU_T}\right) + 1}{2}. \tag{B.9}$$

For a time-varying signal (B.7) can be rewritten as:

$$\frac{I_D}{I_T} = -\tanh\left(\frac{V_{PK}\cos(\omega t)}{nU_T}\right). \tag{B.10}$$

Then, we can predict the behavior of the time-varying signal, as it is shown in Fig. B.7. We can note that there are no harmonics for signals with smaller amplitudes, but as V_{in} increases, odd harmonics are added making the I_D/I_T transient curve look like a square signal.

Figure B.7: I_D/I_T when the circuit is excited by a cosine and for 3 different values of V_{PK}.



Source: The author.

Since the cross-coupled pair is a non-linear circuit and we have to use it for high voltage levels (>10 mV), it is required to expand I_D in a Fourier series that can be written as:

$$\begin{aligned} I_D &= I_{h1}\cos\omega t + I_{h3}\cos 3\omega t + I_{h5}\cos 5\omega t + ... \\ &= I_T \sum_{h=1}^{\infty} a_{2h-1}\cos(2h-1)\omega t. \end{aligned} \tag{B.11}$$

The coefficients of the Fourier series (a_h) can be written as:

$$a_h = \frac{1}{\pi}\int_{-\pi}^{\pi} -\tanh\left(\frac{V}{nU_T}\cos(\theta)\right)\cos(h\theta)d\theta, \tag{B.12}$$

as we see in chapter 3.

BIBLIOGRAPHY

[1] C. S.A., "CEITEC S.A. Webpage." [Online]. Available: http://www.ceitec-sa.com

[2] M. Roberti, "RFID journal." [Online]. Available: http://www.rfidjournal.com/articles/view?1338

[3] A. Al-Fuqaha, M. Guizani, M. Mohammadi, M. Aledhari, and M. Ayyash, "Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications," *IEEE Communications Surveys & Tutorials*, vol. 17, no. 4, pp. 2347–2376, 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7123563/

[4] J. W. Nilsson and S. Riedel, *Electric Circuits*, 10th ed. Pearson, 2014.

[5] K. Finkenzeller and Wiley InterScience, *RFID handbook : fundamentals and applications in contactless smart cards, radio frequency identification and near-field communication*. Wiley-Blackwell, 2010.

[6] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, mar 1996. [Online]. Available: http://ieeexplore.ieee.org/document/494195/

[7] T. Ohira, "What in the World Is Q?" *IEEE Microwave Magazine*, vol. 17, no. 6, pp. 42–49, jun 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7464980/

[8] B. Razavi, *RF microelectronics*, 2nd ed. Prentice Hall, 2012.

[9] M. Stoopman, S. Member, and S. Keyrouz, "Co-Design of a CMOS Recti fi er and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, 2014.

[10] S. Srinivas, J. Kuhn, R. A. Oliver, J. D. Hyde, and C. J. Diorio, "SELF TUNING RFID TAGS," US 9,349,090 B1, 2016.

[11] G. Seigneuret, E. Bergeret, and P. Pannier, "Auto-tuning in passive UHF RFID tags," in *NEWCAS Conference (NEWCAS), 2010 8th IEEE International*, no. 1, 2010, pp. 181–184.

[12] R. L. Copeland, G. M. Shafer, and B. Raton, "Techniques for tuning an antenna to different operating frequencies," US7,202,790 B2, 2007. [Online]. Available: https://patentimages.storage.googleapis.com/pdfs/d3a083c39a9de6e22785/US7202790.pdf

[13] H. Wegleiter, B. Schweighofer, C. Deinhammer, G. Holler, and P. Fulmek, "Automatic Antenna Tuning Unit to Improve RFID System Performance," *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 8, pp. 2797–2803, aug 2011.

[14] D. Li and Y. Tsividis, "A 1.9GHz Si Active LC Filter with On-Chip Automatic Tuning," *IEEE International Solid-State Circuits Conference*, vol. 47, no. 3, pp. 2000–2002, 2001.

[15] F. Bahmani, T. Serrano-Gotarredona, and E. Sánchez-Sinencio, "An accurate automatic quality-factor tuning scheme for second-order LC filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, pp. 745–756, 2007.

[16] R. Rottava, P. Silva, and F. de Sousa, "Automatic LC network tuner based on negative resistances," *Electronics Letters*, vol. 51, no. 1, pp. 25–27, jan 2015. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/el.2014.3800

[17] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, jul 1995.

[18] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Addison-Wesley, Ed., 1971.

[19] I. Pappas, C. Theodorou, S. Siskos, and C. A. Dimitriadis, "A new linear voltage-to-current converter with threshold voltage compensation for analog circuits applications in polycrystalline silicon TFT process," in *2009 16th IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009)*. IEEE, dec 2009, pp. 599–602.

[20] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design (Oxford Series in Electrical and Computer Engineering)*, 3rd ed. Oxford University Press, 2011.

[21] G. K. Balachandran and R. E. Barnett, "A Passive UHF RFID Demodulator With RF Overvoltage Protection and Automatic Weighted Threshold Adjustment," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2291–2300, sep 2010. [Online]. Available: http://ieeexplore.ieee.org/document/5582118/

[22] U. Kaiser and W. Steinhagen, "Low-power transponder IC for high-performance identification systems," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 306–310, 1995.

[23] F. P. Cortes, J. P. Martinez Brito, R. Cantalice, E. Ghignatti, A. Olmos, F. Chavez, and M. Lubaszewski, "A low-power RF/analog front-end architecture for LF passive RFID tags with dynamic power sensing," in *2014 IEEE International Conference on RFID, IEEE RFID 2014*, 2014, pp. 60–66.

[24] B. Gilbert, "Translinear circuits: a proposed classification," *Electronics Letters*, vol. 11, no. 1, p. 14, 1975. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/el_19750011

[25] ——, "A DC-500MHz amplifier/multiplier principle," in *1968 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. IEEE, 1968, pp. 114–115. [Online]. Available: http://ieeexplore.ieee.org/document/1154642/

[26] ——, "Translinear circuits: An historical overview," *Analog Integrated Circuits and Signal Processing*, vol. 9, no. 2, pp. 95–118, mar 1996. [Online]. Available: http://link.springer.com/10.1007/BF00166408

[27] S.-C. Liu, *Analog VLSI : circuits and principles*. MIT Press, 2002.

[28] A. G. Andreou and K. A. Boahen, "Translinear circuits in subthreshold MOS," *Analog Integrated Circuits and Signal Processing*, vol. 9, no. 2, pp. 141–166, mar 1996. [Online]. Available: http://link.springer.com/10.1007/BF00166411

[29] T. Serrano-Gotarredona, B. Linares-Barranco, and A. Andreou, "A general translinear principle for subthreshold MOS transistors," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 5, pp. 607–616, may 1999. [Online]. Available: http://ieeexplore.ieee.org/document/762926/

[30] J. Lazzaro, S. Ryckebusch, M. A. Mahowald, and C. A. Mead, "Winner-take-all networks of O(N) complexity," *Advances in neural information processing systems 1*, pp. 703–711, 1989. [Online]. Available: http://dl.acm.org/citation.cfm?id=89944

[31] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, jun 1977. [Online]. Available: http://ieeexplore.ieee.org/document/1050882/

[32] R. Baker, *CMOS: Circuit design, layout, and simulation*, 3rd ed. Wiley-IEEE Press, 2010.

[33] J. A. Macedo and M. A. Copeland, "A 1.9-GHz silicon receiver with monolithic image filtering," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 378–386, 1998.

[34] H. Samavati, H. R. Rategh, and H. Lee Thomas, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 765–772, 2000. [Online]. Available: http://ieeexplore.ieee.org/document/841505/

[35] M. Koroglu and P. Allen, "LC notch filter for image-reject applications using on-chip inductors," *Electronics Letters*, vol. 37, no. 5, p. 267, 2001. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/el_20010207

[36] J. Rogers and C. Plett, "A 5-GHz radio front-end with automatically Q-tuned notch filter and VCO," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 9, pp. 1547–1554, sep 2003. [Online]. Available: http://ieeexplore.ieee.org/document/1225798/

[37] R. Schaumann and M. Tan, "The problem of on-chip automatic tuning in continuous-time integrated filters," in *IEEE International Symposium on Circuits and Systems*, 1989, pp. 106–109. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=100302

[38] S. Li, N. Stanić, and Y. Tsividis, "A VCF loss-control tuning loop for Q-enhanced LC filters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, pp. 906–910, 2006. [Online]. Available: http://ieeexplore.ieee.org/document/1705064/

[39] M. Zhang and N. Llaser, "Exploiting Time-Domain Approach for Extremely High Q-Factor Measurement," *IEEE Transactions on Instrumentation and Measurement*, vol. 64, pp. 2730–2737, 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7086308/

[40] K. Kundert and I. Clifford, "Achieving Accurate Results With a Circuit Simulator," Tech. Rep. [Online]. Available: https://kenkundert.com/docs/eda+t93-preso.pdf

[41] S. Wang and R.-X. Wang, "Q-enhanced CMOS inductor using tapped-inductor feedback," *Electronics Letters*, vol. 47, no. 16, p. 921, 2011. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/el.2011.1165

[42] A. M. Niknejad, *Electromagnetics for High-Speed Analog and Digital Communication Circuits*. Cambridge University Press; First edition, 2007.

[43] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7130773/

[44] J. W. M. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, 2nd ed. Artech House Publishers, 2010.

[45] M. Stoopman, W. A. Serdijn, and K. Philips, "A robust and large range optimally mismatched RF energy harvester with resonance control loop," in *2012 IEEE International Symposium on Circuits and Systems*. Seoul: IEEE, may 2012, pp. 476–479. [Online]. Available: http://ieeexplore.ieee.org/document/6272068/

[46] E. Herold, "Negative Resistance and Devices for Obtaining It," *Proceedings of the IRE*, vol. 23, no. 10, pp. 1201–1223, oct 1935. [Online]. Available: http://ieeexplore.ieee.org/document/1685775/

[47] A. Hull, "The Dynatron: A Vacuum Tube Possessing Negative Electric Resistance," *Proceedings of the IRE*, vol. 6, no. 1, pp. 5–35, feb 1918. [Online]. Available: http://ieeexplore.ieee.org/document/1646086/

[48] C. Brunetti, "The Transitron Oscillator," *Proceedings of the IRE*, vol. 27, no. 2, pp. 88–94, feb 1939. [Online]. Available: http://ieeexplore.ieee.org/document/1686838/

[49] "Radio-Craft Magazine," www.americanradiohistory.com/Archive-Radio-Craft/1940s/Radio-Craft-1940-03.pdf , Date Acessed: 2017/02/02.

[50] G. Haddad and R. Trew, "Microwave solid-state active devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 760–779, mar 2002. [Online]. Available: http://ieeexplore.ieee.org/document/989960/

[51] L. L. Chang, L. Esaki, and R. Tsu, "Resonant tunneling in semiconductor double barriers," *Applied Physics Letters*, vol. 24, no. 12, pp. 593–595, 1974.

[52] J. Lee, M. Kim, and K. Yang, "A 1.52 THz RTD Triple-Push Oscillator With a -Level Output Power," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 2, pp. 336–340, mar 2016.

[53] P. Mazumder, S. Kulkarni, M. Bhattacharya, Jian Ping Sun, and G. Haddad, "Digital circuit applications of resonant tunneling devices," *Proceedings of the IEEE*, vol. 86, no. 4, pp. 664–686, apr 1998. [Online]. Available: http://ieeexplore.ieee.org/document/663544/

[54] J. Voelcker, "The Gunn effect," *IEEE Spectrum*, vol. 26, no. 7, p. 24, jul 1989. [Online]. Available: http://ieeexplore.ieee.org/document/29344/

[55] J. B. Gunn, "Microwave oscillations of current in III-V semiconductors," *Solid State Communications*, vol. 88, no. 11-12, pp. 883–886, 1993.

[56] Microsemi, "MG1001 – MG1061 Microsemi Microwave Products," 2009. [Online]. Available: https://www.digchip.com/datasheets/download_datasheet.php?id=7048312&part-number=MG1010-11

[57] A. Khalid, C. Li, V. Papageogiou, G. M. Dunn, M. J. Steer, I. G. Thayne, M. Kuball, C. H. Oxley, M. Montes Bajo, A. Stephen, J. Glover, and D. R. S. Cumming, "In0.53Ga0.47As planar gunn diodes operating at a fundamental frequency of 164 GHz," *IEEE Electron Device Letters*, vol. 34, pp. 39–41, 2013.

[58] R. V. L. Hartley, "Oscillation Generator," 1920.

[59] E. H. Colpitts, "Oscillation generator," 1918. [Online]. Available: https://www.google.com/patents/US1624537

[60] S. H. Lee, Y. H. Chuang, S. L. Jang, and C. G. Chen, "Low-phase noise Hartley differential CMOS voltage controlled oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 17, pp. 145–147, 2007.

[61] R. Aparicio and A. Hajimiri, "A noise-shifting differential Colpitts VCO," in *IEEE Journal of Solid-State Circuits*, vol. 37, 2002, pp. 1728–1736.

[62] L. Dauphinee, M. Copeland, and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated LC resonator," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, 1997, pp. 390–391. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=585454

[63] B. Razavi, "The Cross-Coupled Pair - Part I [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 6, no. 3, pp. 7–10, 2014.

[64] ——, "The Cross-Coupled Pair - Part II [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 6, no. 4, pp. 9–12, 2014. [Online]. Available: http://ieeexplore.ieee.org/document/6951438/

[65] ——, "The Cross-Coupled Pair?Part III [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 1, pp. 10–13, 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7036175/

[66] ——, "The Bridged T-Coil [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 4, pp. 9–13, 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7336651/

[67] ——, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 894–903, apr 2011.

[68] Q. J. Gu, Z. Xu, H. Y. Jian, B. Pan, X. Xu, M. C. F. Chang, W. Liu, and H. Fetterman, "CMOS THz generator with frequency selective negative resistance tank," *IEEE Transactions on Terahertz Science and Technology*, vol. 2, pp. 193–202, 2012.

[69] N. J., M. Avedillo, and J. Quintana, "Efficient realisation of MOS-NDR threshold logic gates," *Electronics Letters*, vol. 45, no. 23, p. 1158, 2009. [Online]. Available: http://ieeexplore.ieee.org/document/5325114/