Contributions on the automatic tuning of LC networks using on-chip circuits

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Introduction

- Motivation: Real world problem.

Ceitec's RFID earring used by the cattle.

RFID tag (earring).

Introduction

- Motivation: Real world problem.

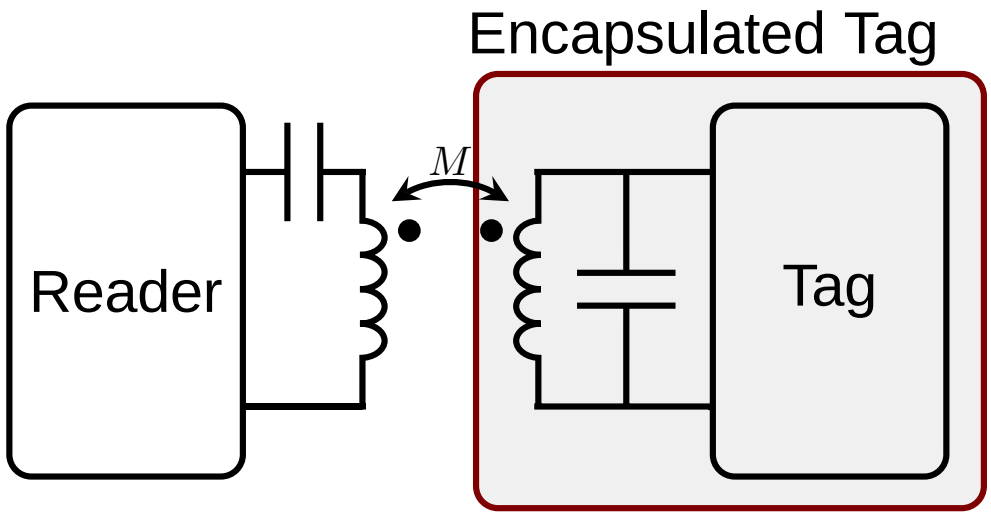


Figure: Block diagram of an RFID system emphasizing the tag and its magnetic coupling with the reader.

Introduction

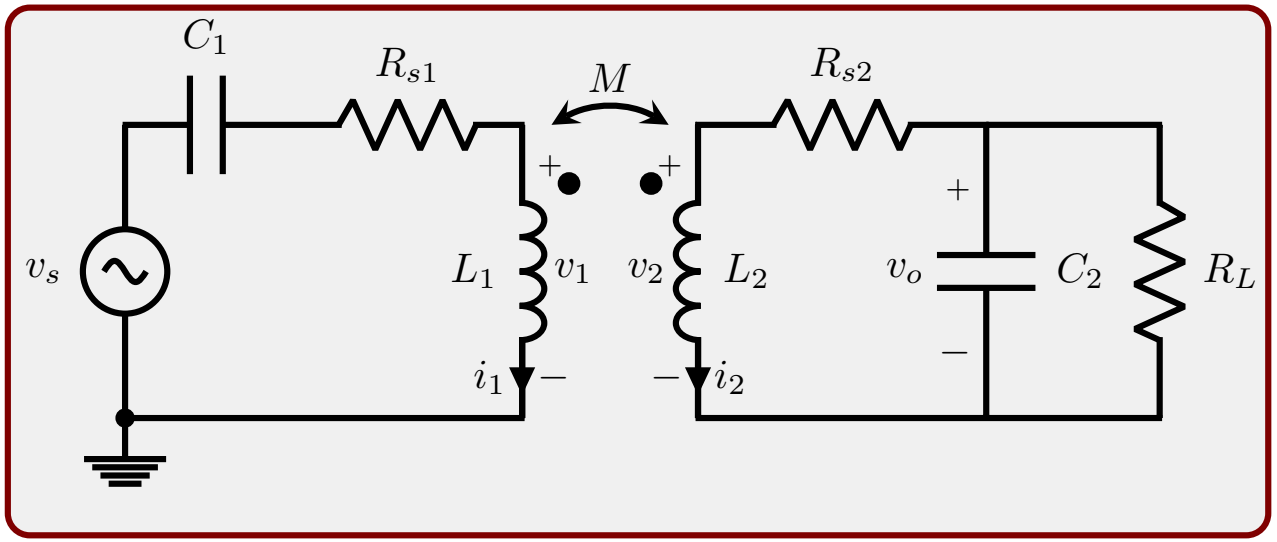


Figure: Two coupled resonating LC networks.

The impedance seen from v_s can be found as:

$$Z_s = \frac{v_s}{i_1} = R_{s1} + \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + R_{s2} + \frac{R_L}{1+j\omega R_L C_2}}. \quad (1)$$

Introduction

$$v_o = \frac{j\omega k\sqrt{L_1 L_2} i_1}{1 + \left(\frac{1}{R_L} + j\omega C_2\right)(j\omega L_2 + R_s)} \quad (2)$$

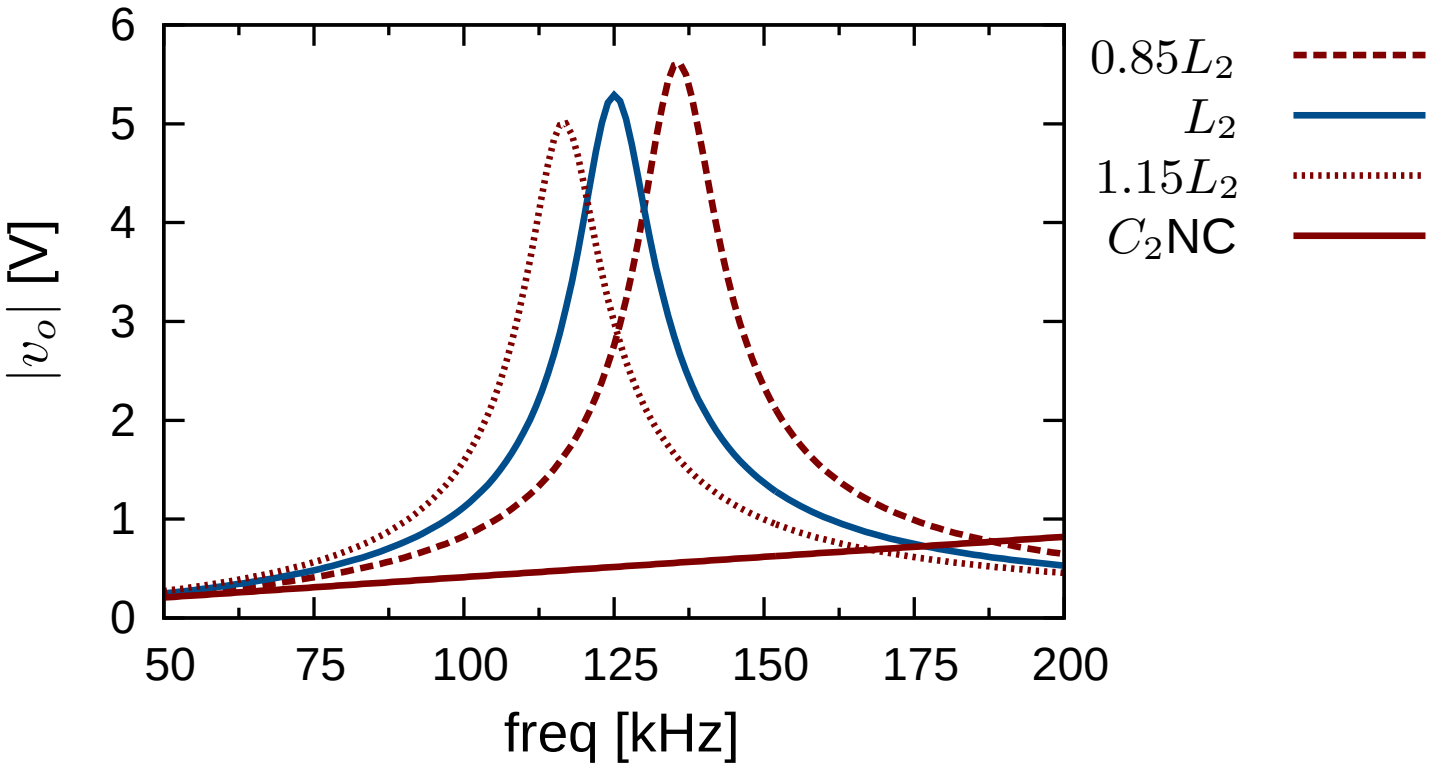


Figure: Frequency response of $|v_o|$ for different values of L_2.

Introduction

Hypothesis:

It is possible to conceive novel LC network tuning systems, that minimizes the required on-chip area, to be integrated on a commercial RFID chip.

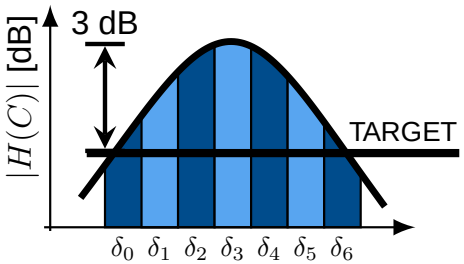
The folowing designs were conceived:

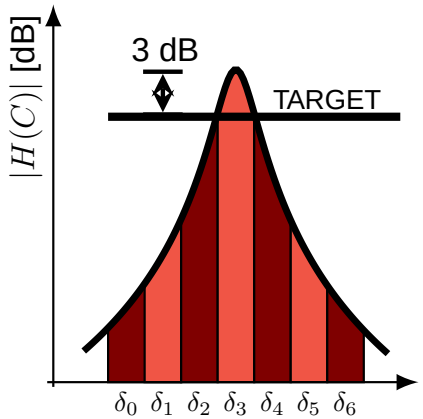
- LC tuner based on negative resistances;
- LC tuner based on the current of an RF limiter;
- LC parameter extractor;

LC tuner based on negative resistances

LC tuner based on negative resistances

- Proposed Tuning Method
- Proposed Architecture
- Negative resistance Control
- Results
- Summary
- Other results





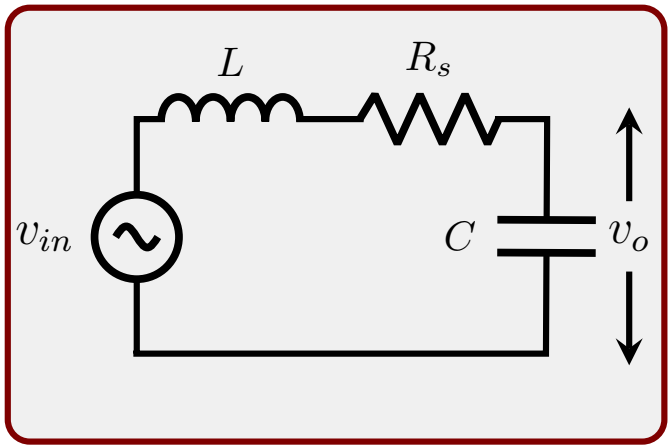


Figure: Equivalent RLC circuit of the tag seen by the induced voltage v_{in}.

$$H(s) = \frac{v_o}{v_{in}}(s) = \frac{1}{sC(sL + R_s) + 1} \tag{3}$$

$$|H(s)|\,\big|_{s=j\omega_0} \cong \frac{\sqrt{L/C}}{R_s} \tag{4}$$

LC tuner based on negative resistances

Proposed Tuning Method

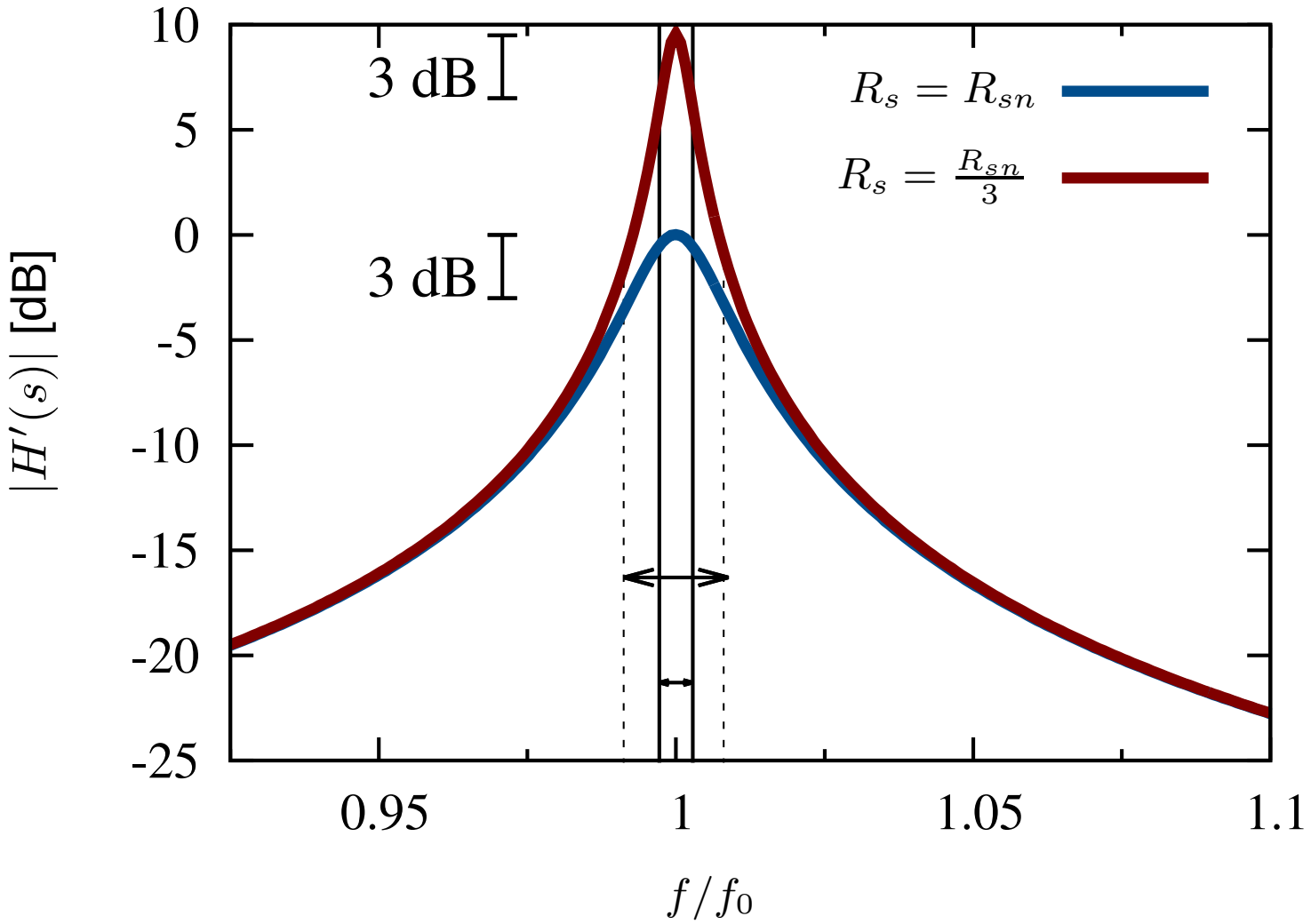


Figure: $|H'(s)|$ considering two values of R_s.

Capacitance response:

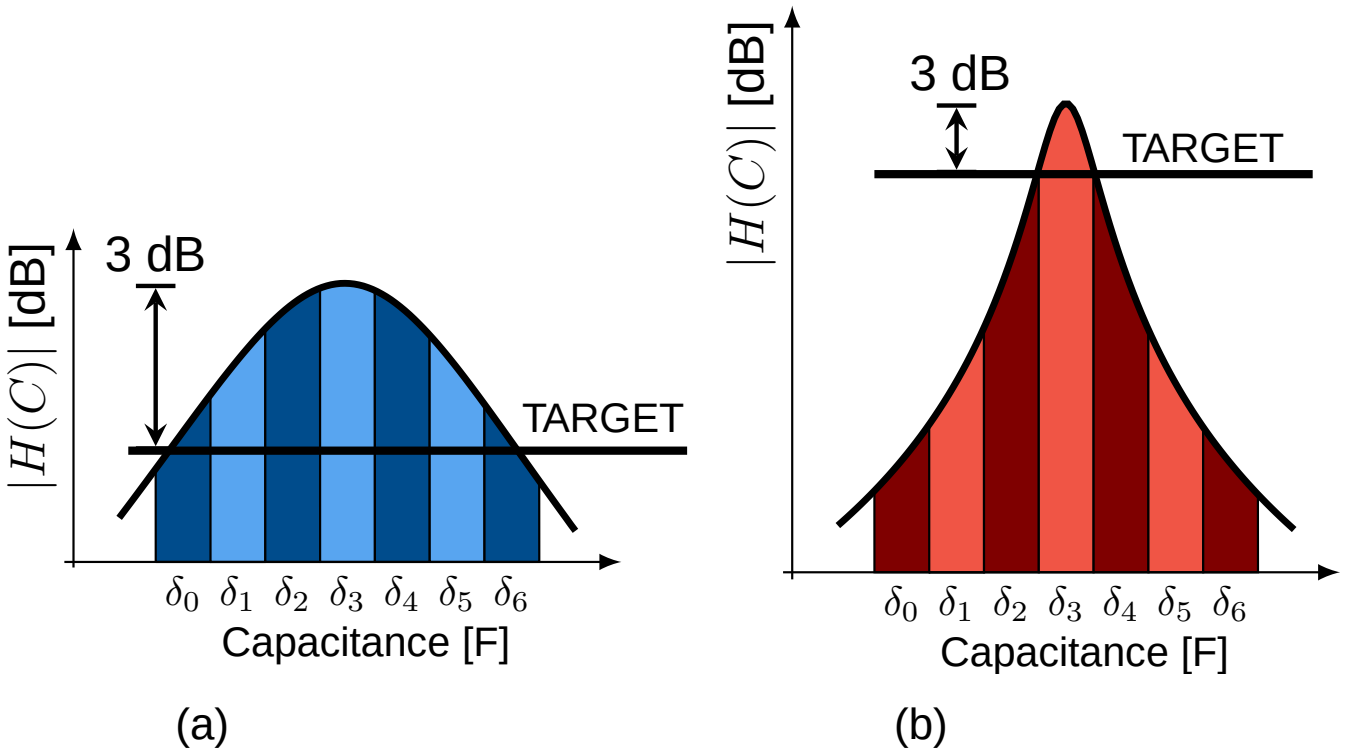
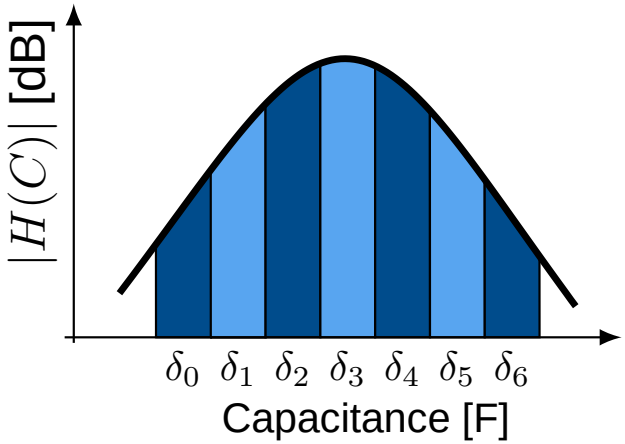
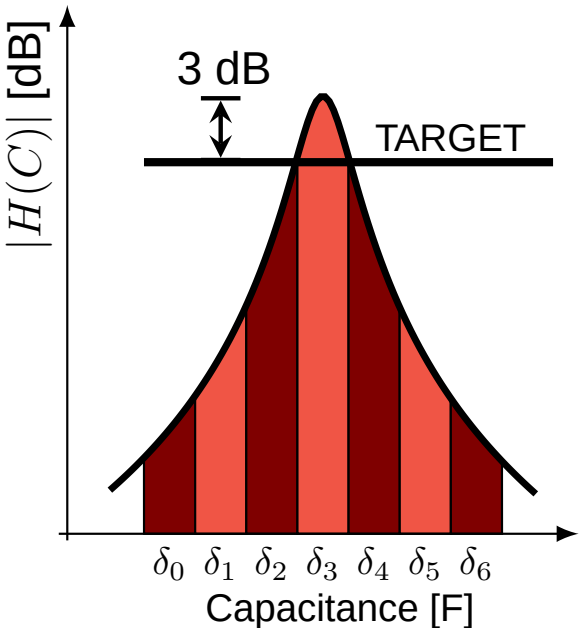


Figure: $|H(C)|$ for different capacitance regions (δ) with a relatively low and high Q in (a) and (b), respectively.

LC tuner based on negative resistances

Proposed Tuning Method





Determine target level and $-R$:

- choose capacitance region;
- use a negative resistance, that is calculated based on the chosen capacitance region;
- set the target voltage so that it covers the desired capacitance region when the negative resistance is enabled;

LC tuner based on negative resistances

Proposed Architecture

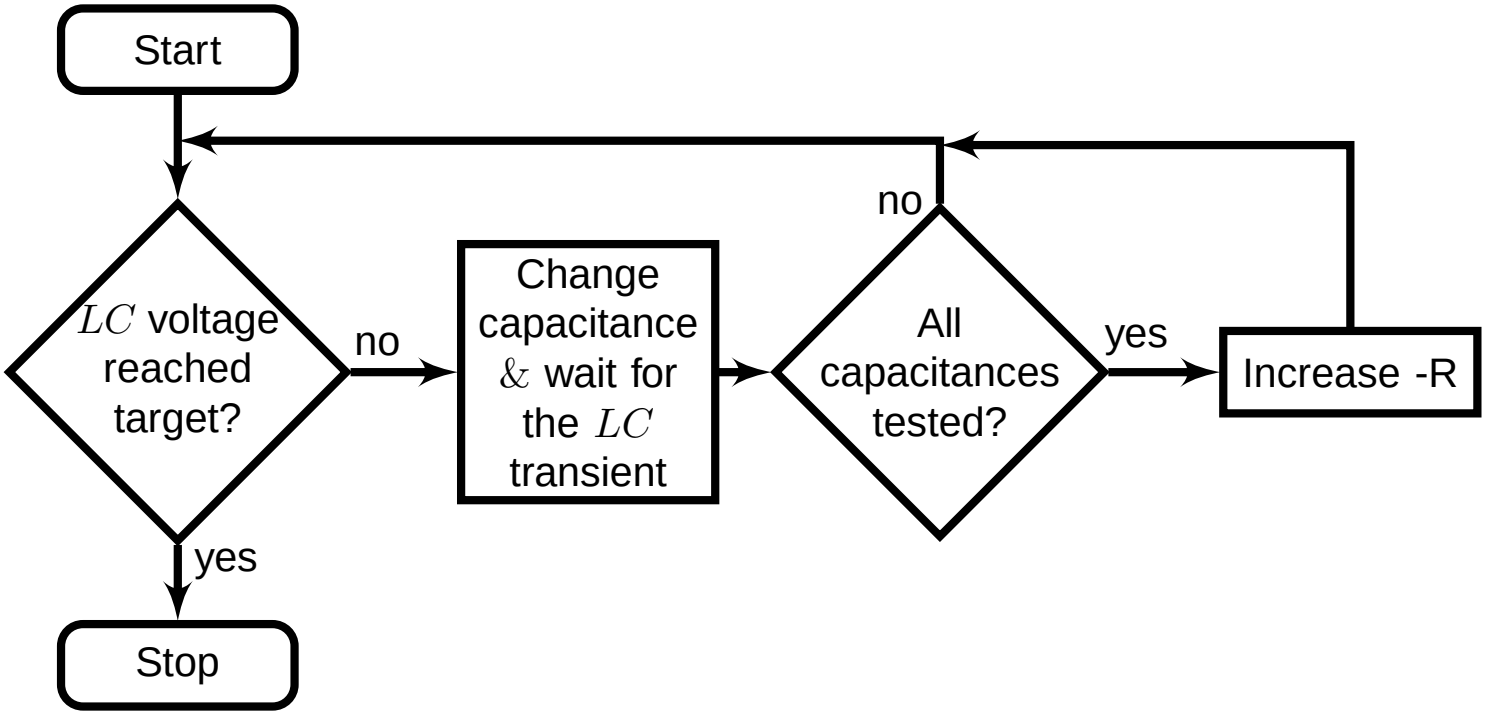
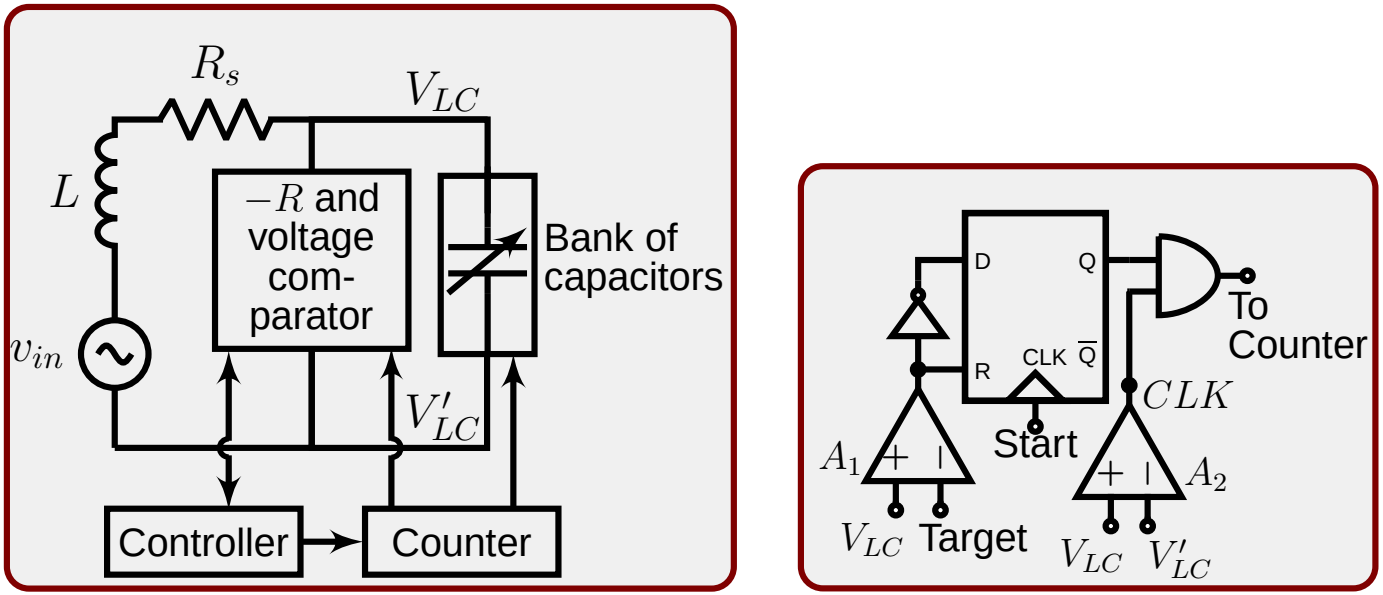


Figure: Proposed flowchart.

LC tuner based on negative resistances

Proposed Architecture



(a) (b)

Figure: (a) Block diagram of the proposed tuner and (b) implemented voltage comparator and controller.

LC tuner based on negative resistances

Proposed Architecture

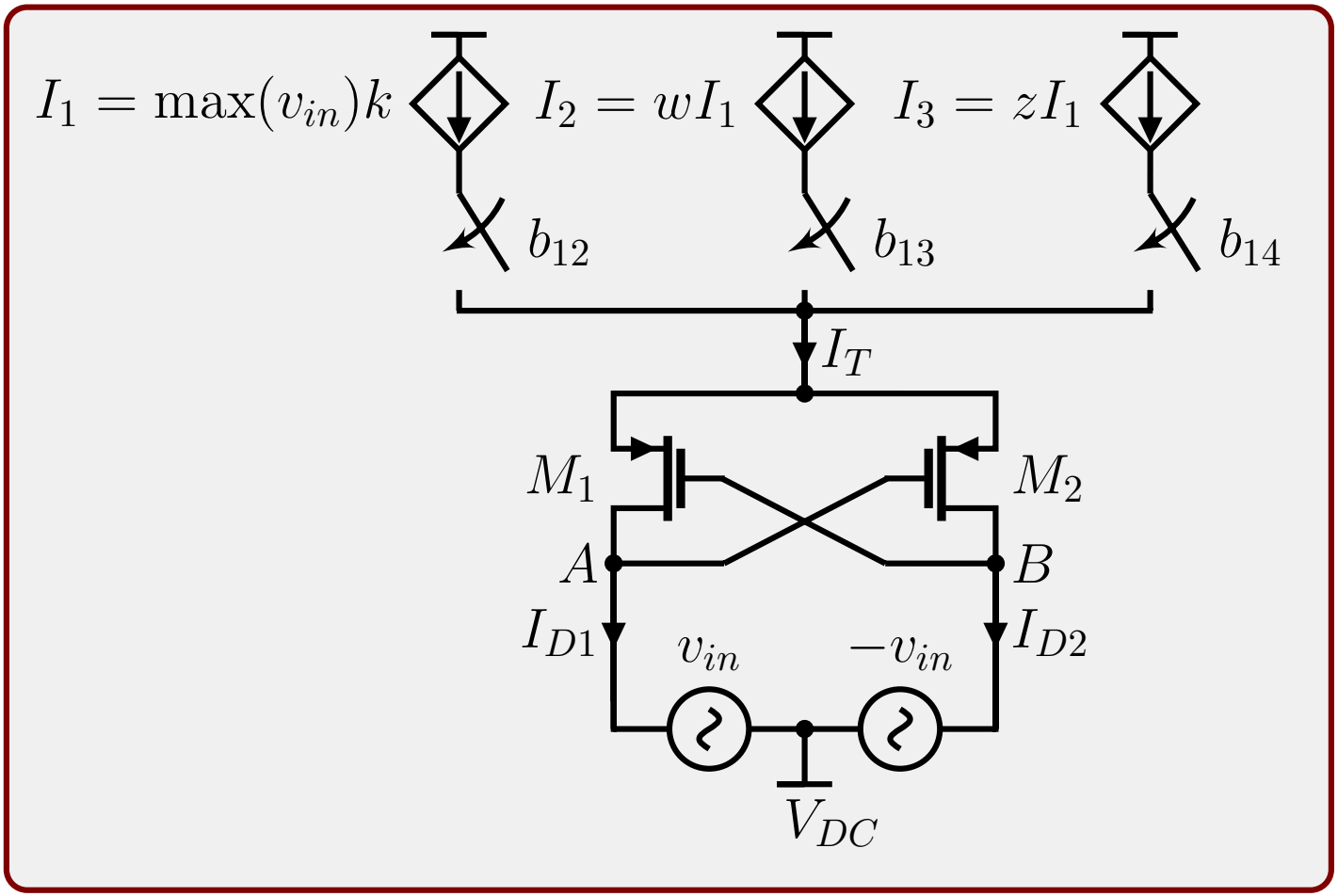


Figure: Implemented PMOS cross-coupled pair used as an adjustable negative resistance.

Large signal behavior of the Cross coupled pair

$$\Re(Z_{in}) = \frac{V_{Diff}}{a_1 I_T} \tag{5}$$

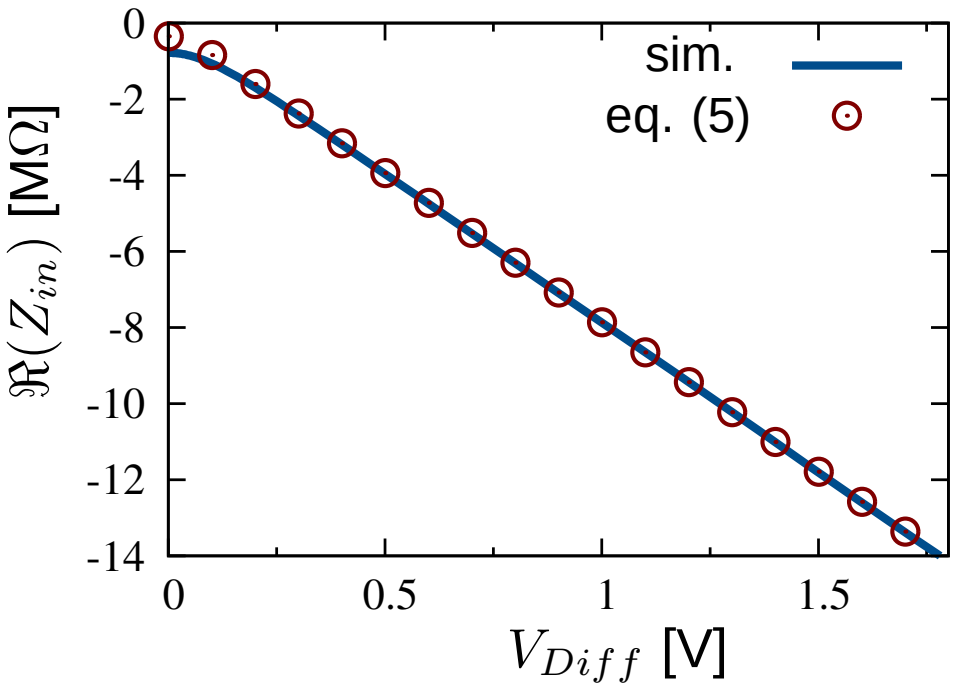
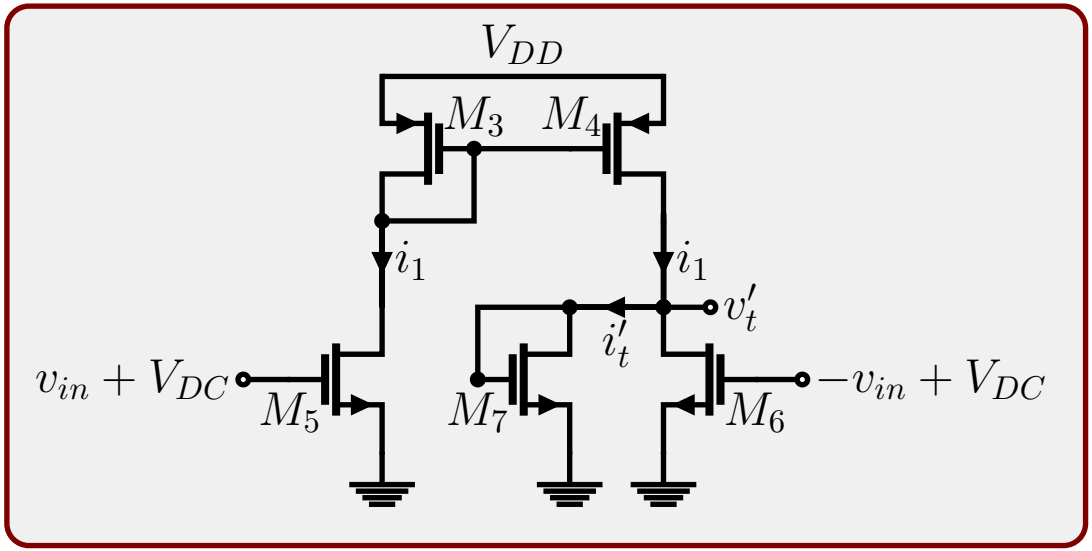


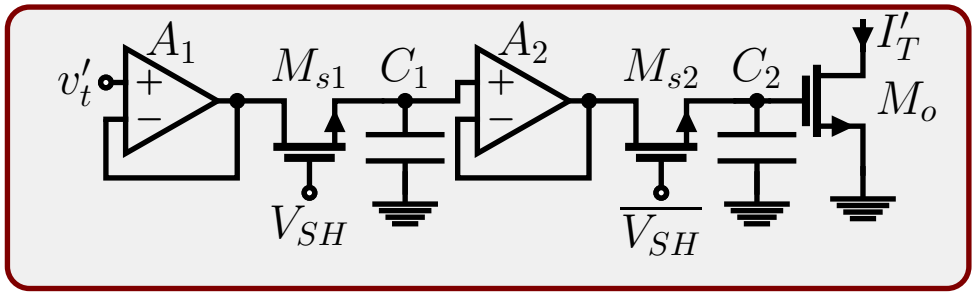
Figure: Equivalent resistance of the cross-coupled pair at $125\,\mathrm{kHz}$.

LC tuner based on negative resistances

Negative resistance Control



(a)



(b)

Figure: (a) Proportional voltage to current converter (b) v_t' peak sampler.

LC tuner based on negative resistances

Negative resistance Control

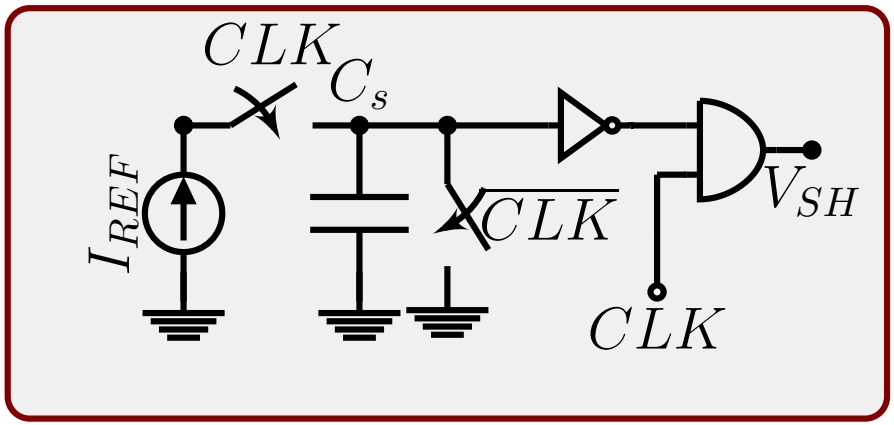
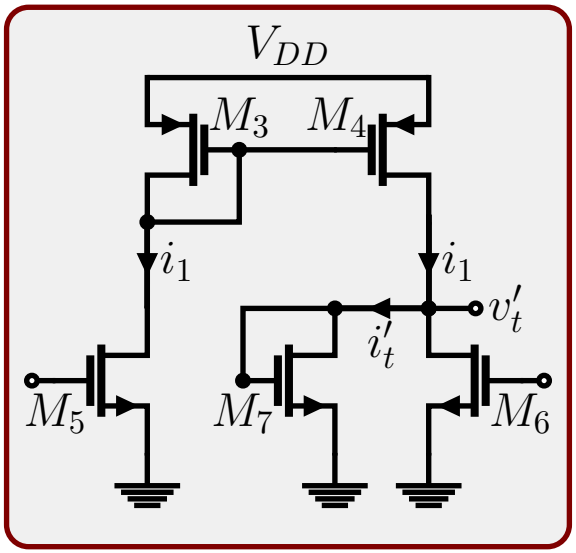
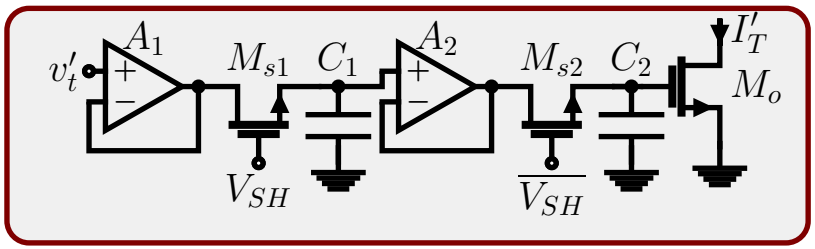


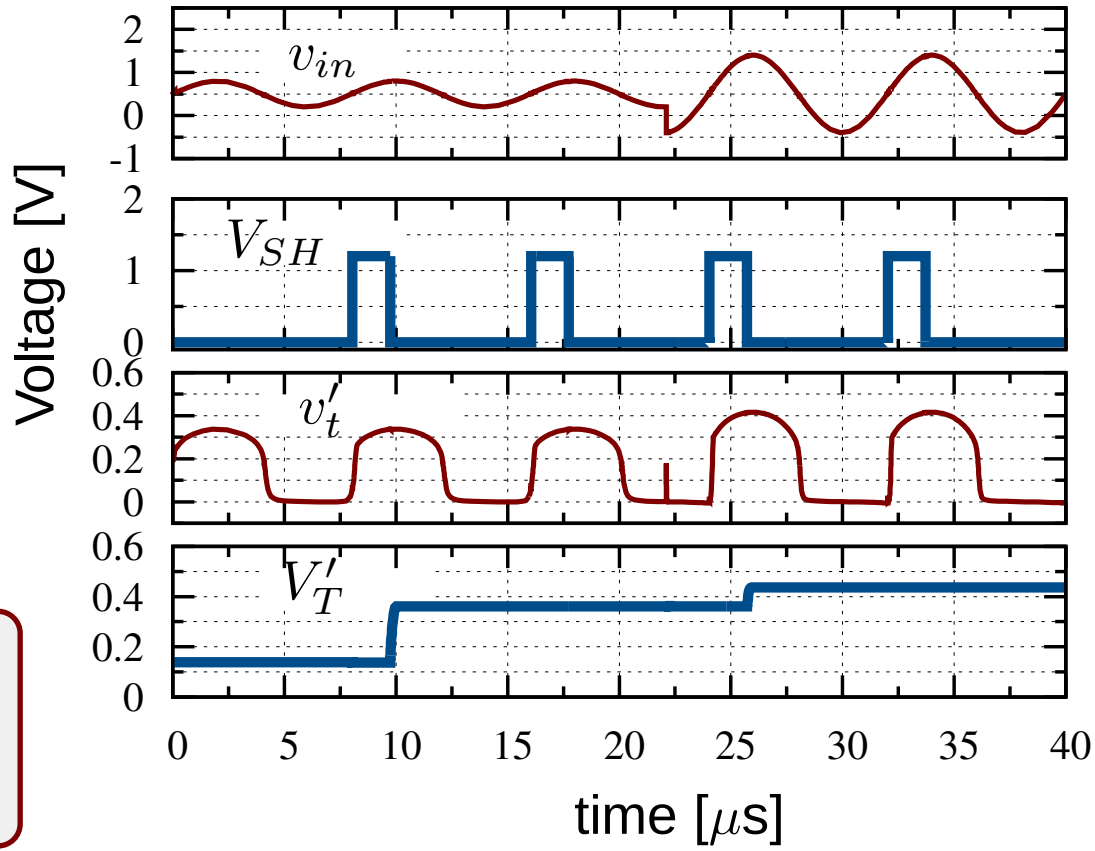
Figure: V_{SH} signal generation.

LC tuner based on negative resistances

Negative resistance Control







LC tuner based on negative resistances

Results

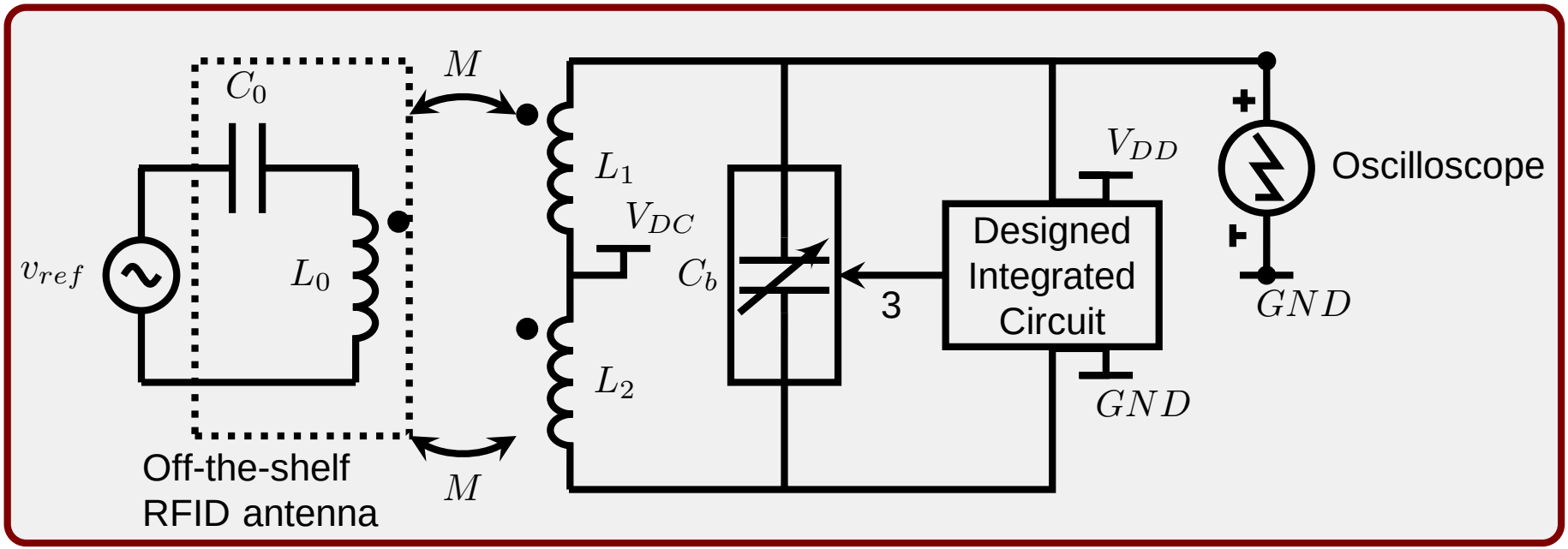
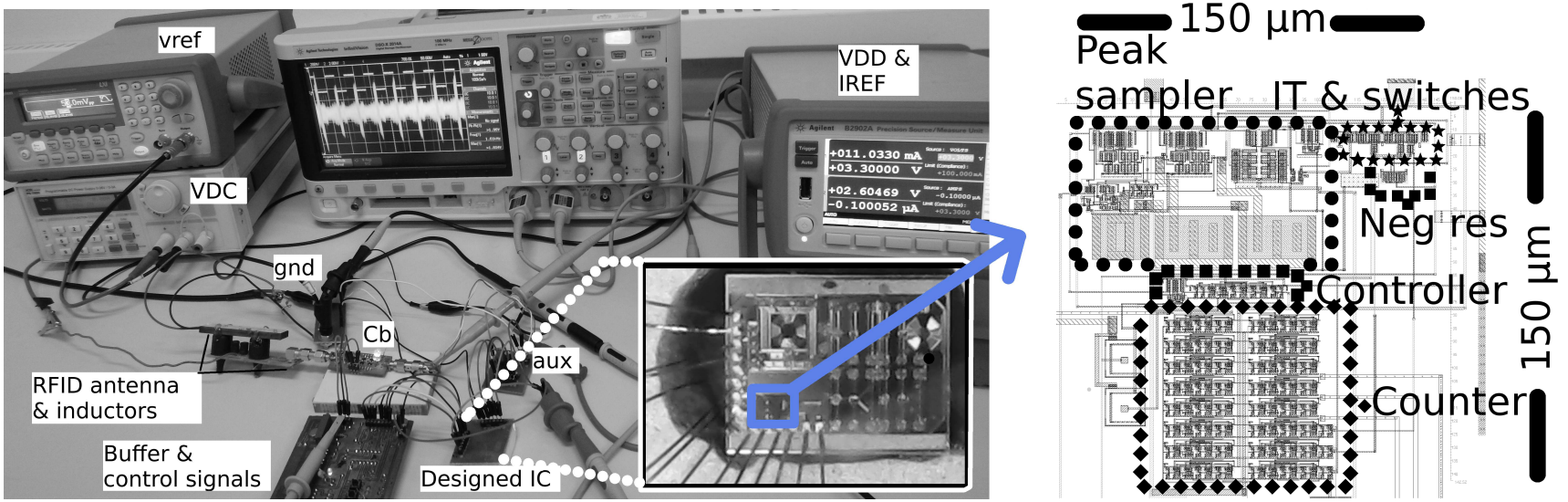


Figure: Simplified schematic of the testbench used to used to validate the integrated tuner.



(a) (b)

Figure: (a) Photograph of the complete testbench including the photo of the designed IC. (b) Layout of the active region of the designed IC

LC tuner based on negative resistances

Results

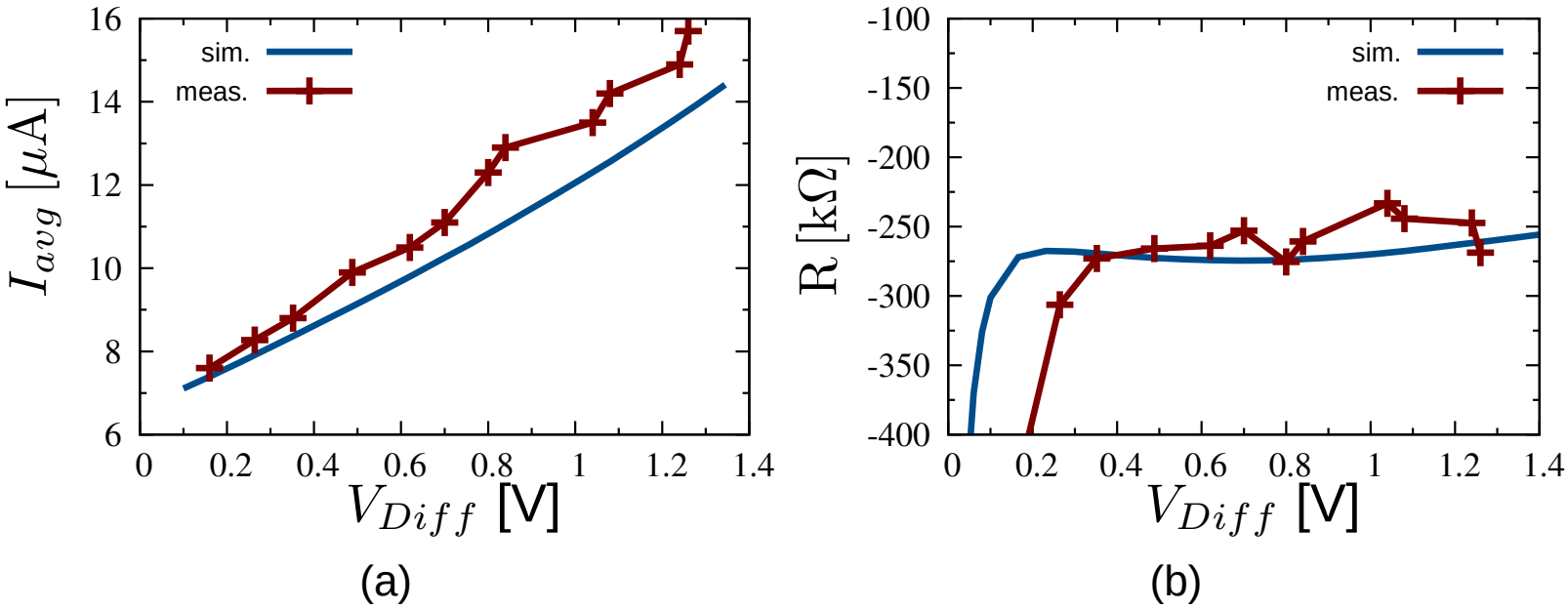


Figure: (a) Average current consumption versus V_{Diff} and (b) equivalent parallel IC negative resistance.

LC tuner based on negative resistances

Results

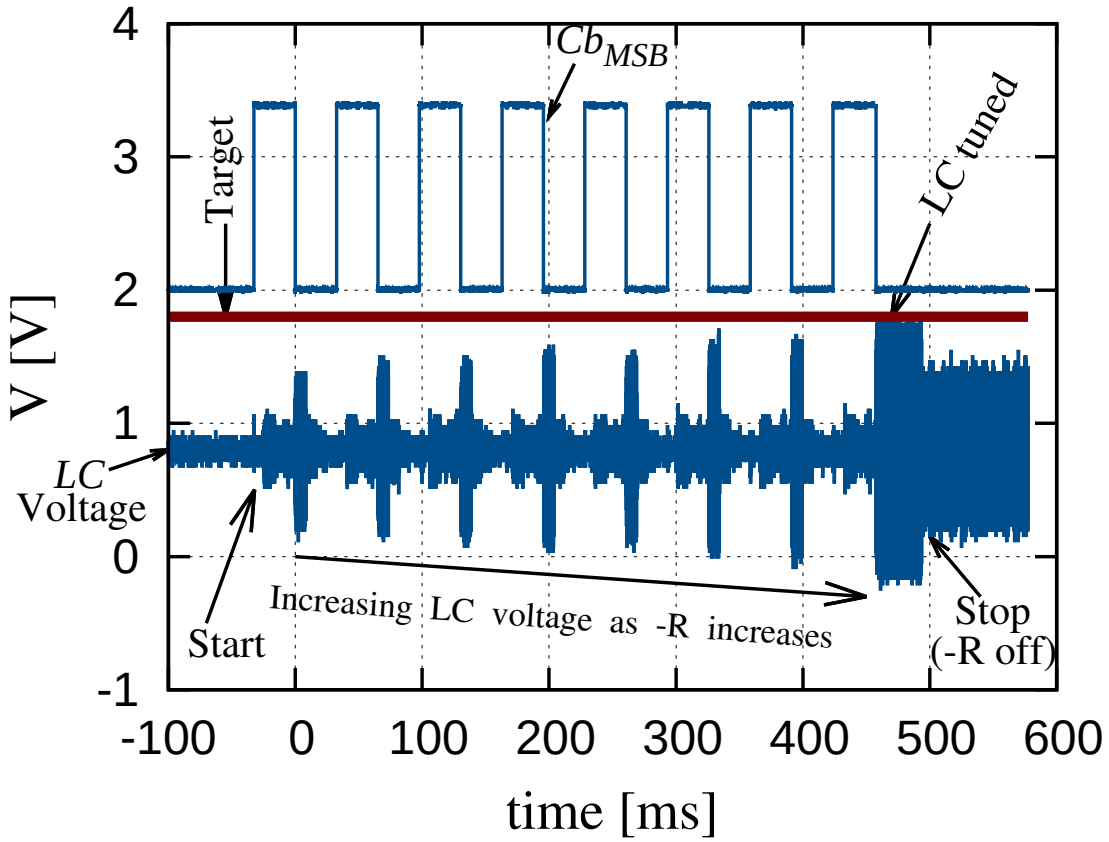


Figure: Waveform of a complete tuning sequence of the integrated tuner.

LC tuner based on negative resistances

Results

Table: Performance summary and comparison with related works.

Ref.	Method	Technology	Area (mm^2)	Power	Time for tuning	Freq.
This work	-R	130 nm	0.022	40 μW	500 ms	125 kHz
[1]	Rect. Voltage	90 nm	0.029	NA	NA	868 MHz
[2]	Master Slave	0.25 $\mu\mathrm{m}$	NA	$\cong$ 18 mW	x	1.9 GHz
[3]	3-dB	0.35 $\mu\mathrm{m}$	0.072	5.5 mW	9 iterations	1.97 GHz

[1] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, “Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters,” IEEE J. Solid-State Circuits, vol. 49, pp. 622–634, 2014.

[2] D. Li and Y. Tsividis, “A 1.9 GHz Si Active LC Filter with On-Chip Automatic Tuning,” IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, vol. 47, no. 3, pp. 2000–2002, 2001.

[3] F. Bahmani, T. Serrano-Gotarredona, and E. Sanchez-Sinencio, “An accurate automatic quality-factor tuning scheme for second-order LC filters,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, pp. 745–756, 2007.

- We proposed a novel application for the negative resistance that considerably decreases the complexity of the tuning decision circuitry;
- We explained with details the behavior of a cross-coupled pair using MOS transistors over a wide voltage range;
- We also proposed a circuit to automatically control the value of the negative resistance over different voltage levels;

LC tuner based on negative resistances
Other results

Publications:

- “Automatic LC network tuner based on negative resistances”. Electronics Letters, January 2015.
- “On-chip automatic LC tuner for RFID tags based on negative resistances". Accepted by the Transaction on Circuits and Systems II: Express Briefs, October 2017.

LC tuner based on the RF limiter current

LC tuner based on the RF limiter current

- Introduction
- Results
- Summary

At Ceitec the tag is tested very close to the reader.

LC tuner based on the RF limiter current

Introduction

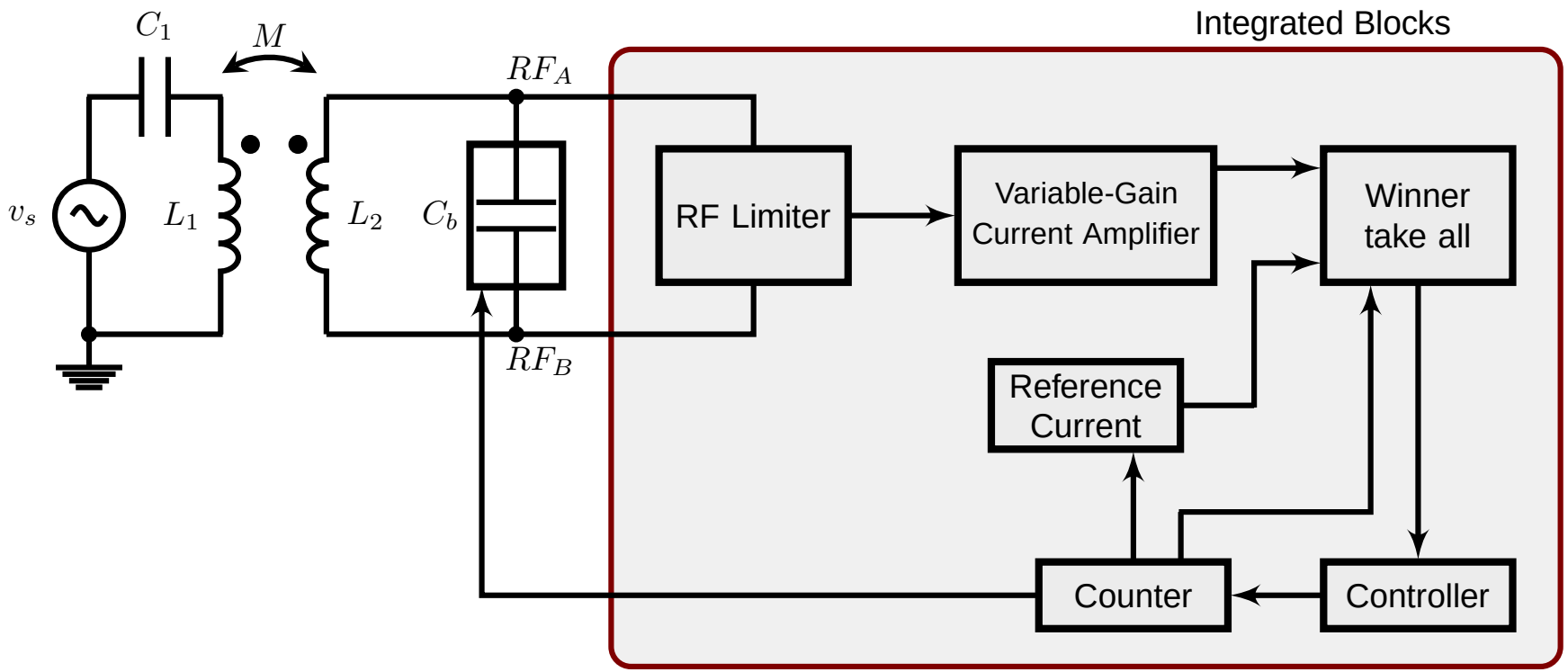


Figure: Block diagram of the LC tuning technique based on the current of the RF voltage limiter.

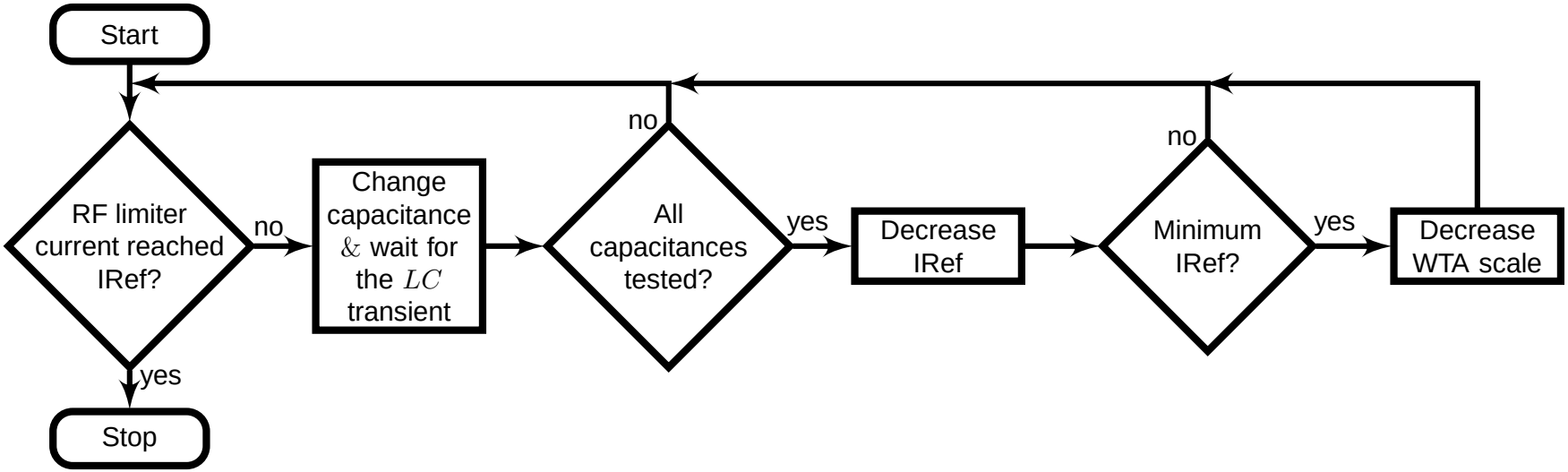


Figure: Proposed flowchart.

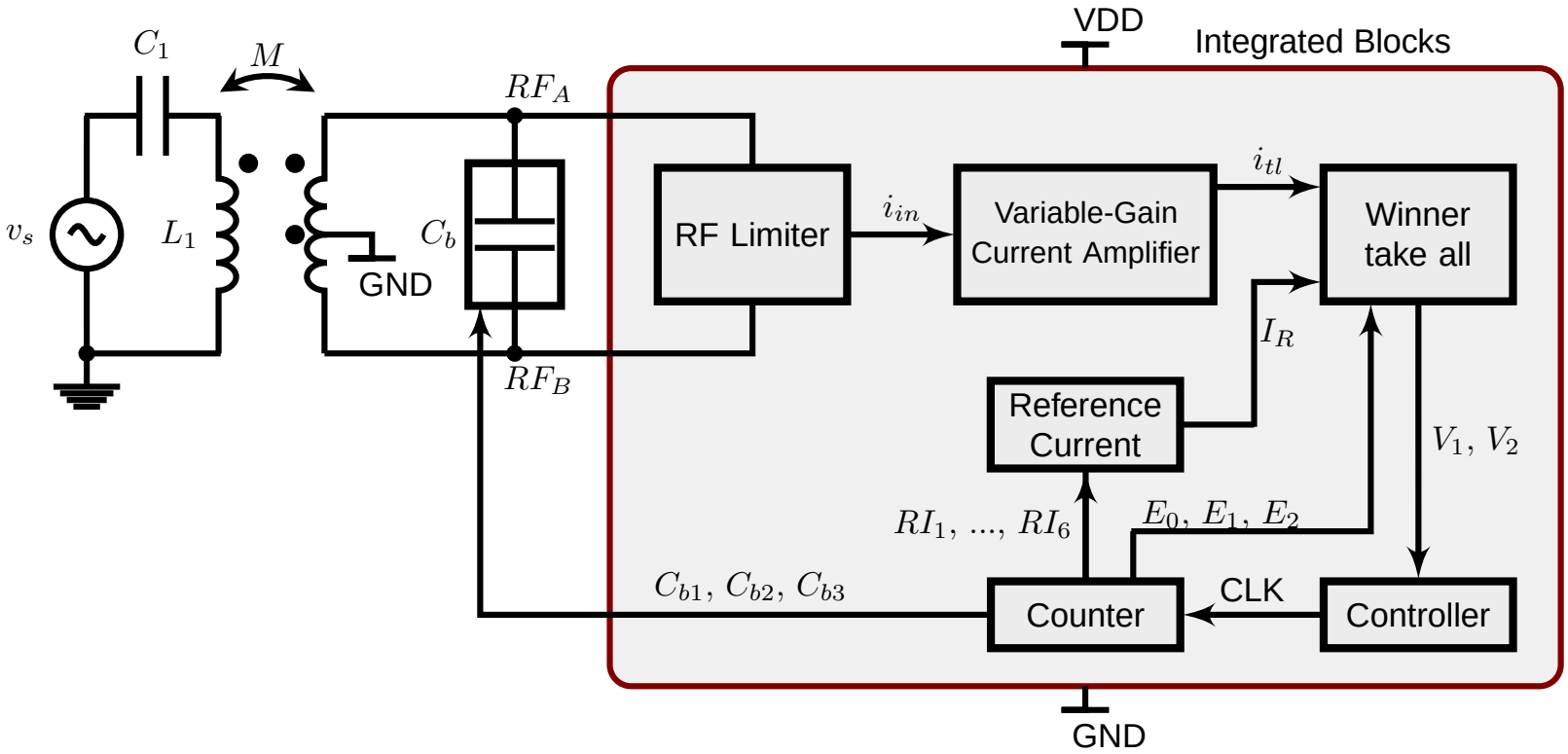


Figure: Circuit used to simulate the designed tuner and its main nets and current names.

LC tuner based on the RF limiter current

Results

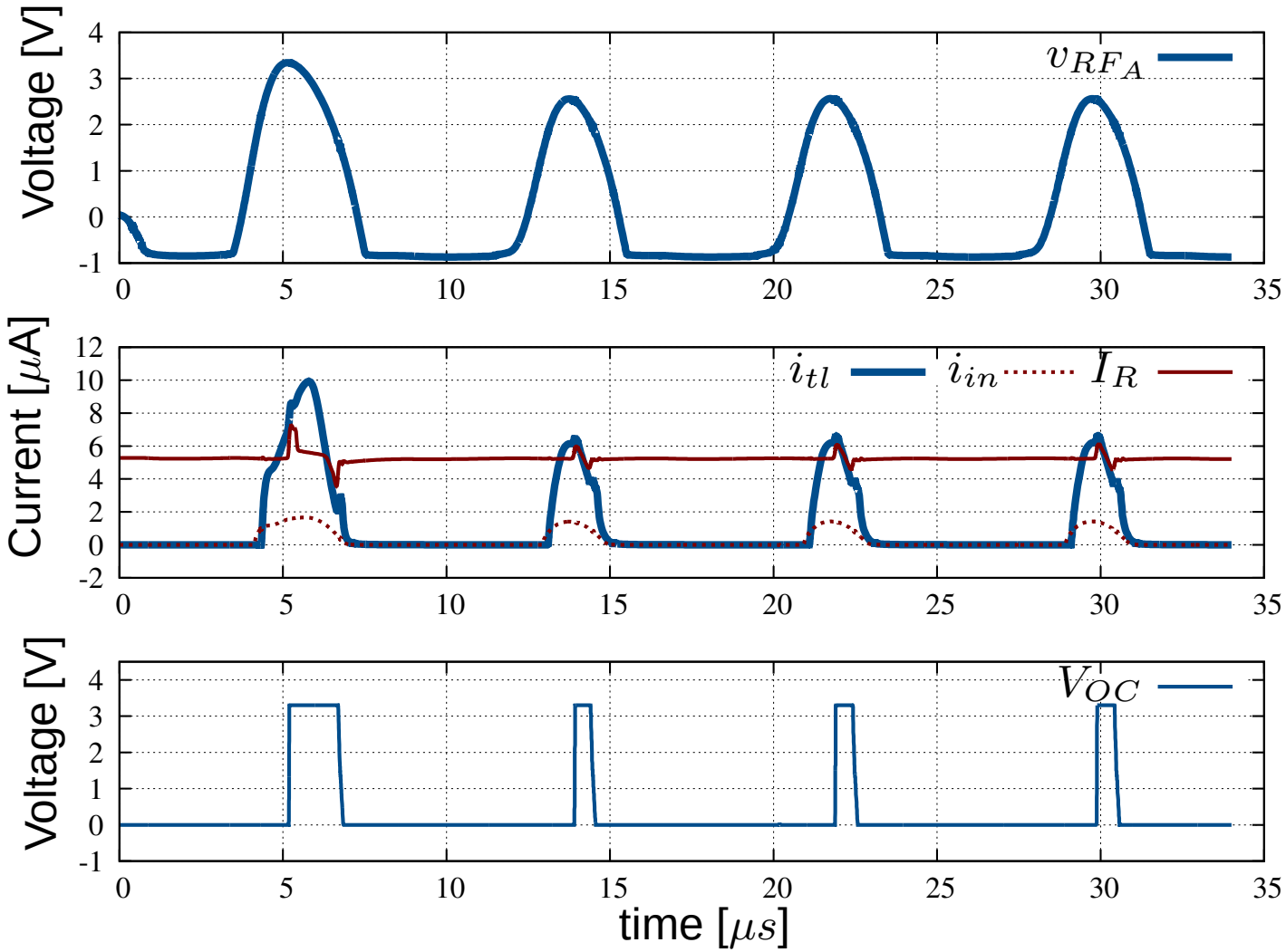
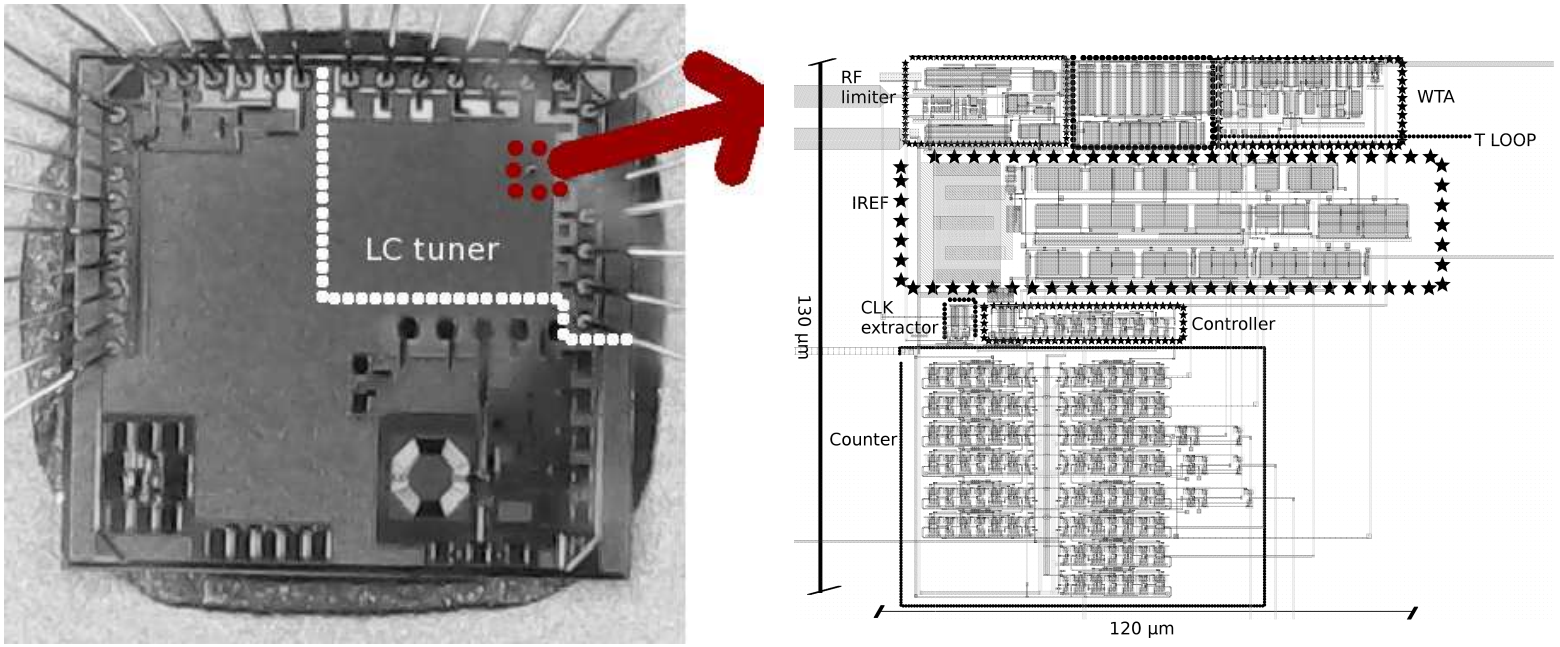


Figure: Main signals of the tuner when I_R is lower than the peak of i_{tl}.

LC tuner based on the RF limiter current

Results



(a) (b)

Figure: (a) Designed 2 mm x 2 mm chip and (b) layout of the proposed LC tuning system.

LC tuner based on the RF limiter current

Results

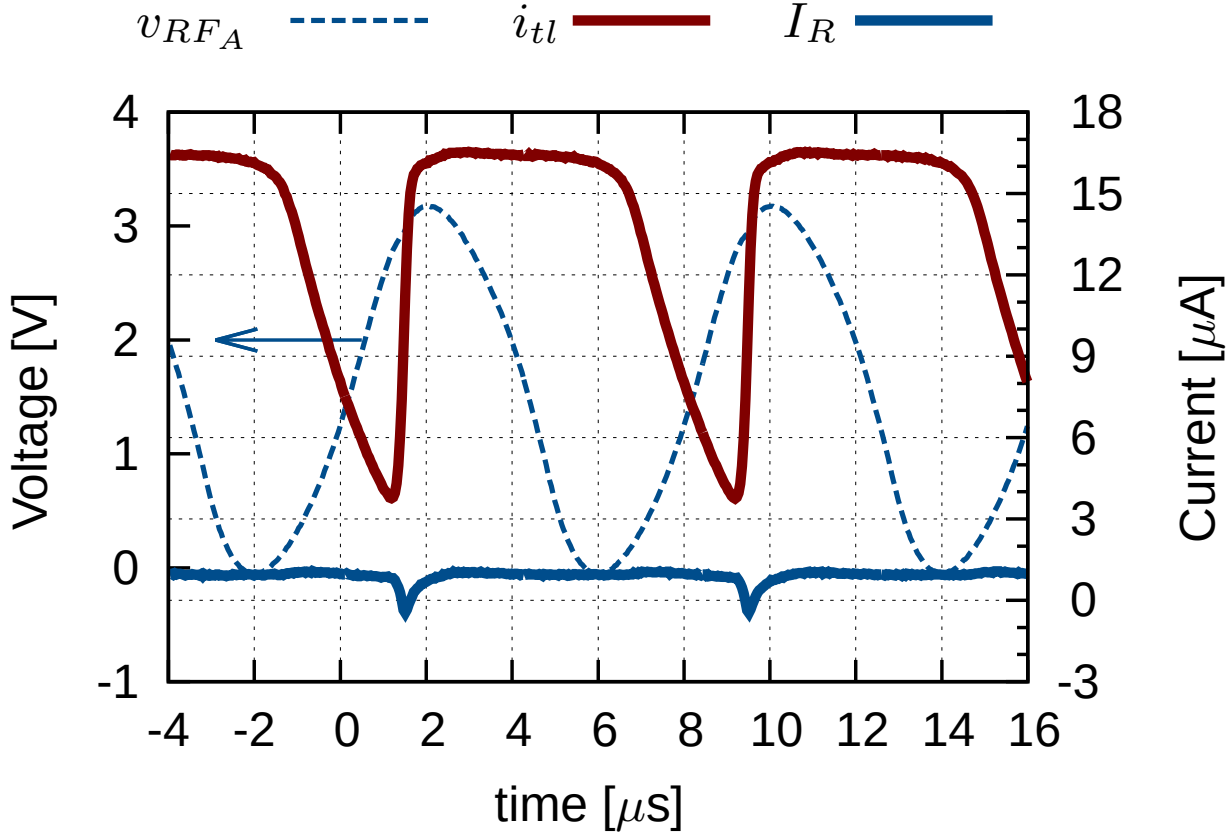


Figure: Main measured signals of the presented LC tuner.

LC tuner based on the RF limiter current
Summary

- A novel method that has the lowest power consumption among other tuners was presented;
- We have shown how to decrease power consumption by scaling the aspect ratio of the transistors of the WTA;
- Another chip was designed (Nov-13th) without the current reference core. So we will be able to analyze the system's behavior for different current values;

LC parameter extractor

LC parameter extractor

- Commonly implemented self-tuned LC filters
- Transient behavior of LC networks
- Implemented System
- Results
- Summary

LC parameter extractor

Systems that either automatic tune their LC network or measure their Q

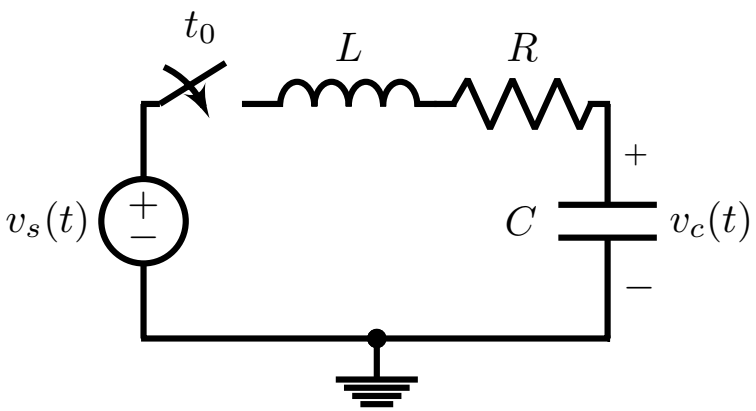
Ref.	Method	Process	Freq.	Area	V_{DD}	Current	Time for tuning / measuring
[1]	MS	75-GHz SiGe Bipolar	5.5 GHz	> L	1.8 V	< 19 mA	NA
[2]	MS	0.25-μm BiCMOS	1.9 GHz	> L	2.7-3.3 V	18 mA	NA
[3]	3 dB	0.35-μm CMOS	2 GHz	<.0725 mm^2	1.3 V	< 3.6 mA	9 it.
[4]	Transient	x	10 kHz	Off chip	5 V	NA	$\cong 10Q/\omega_0$

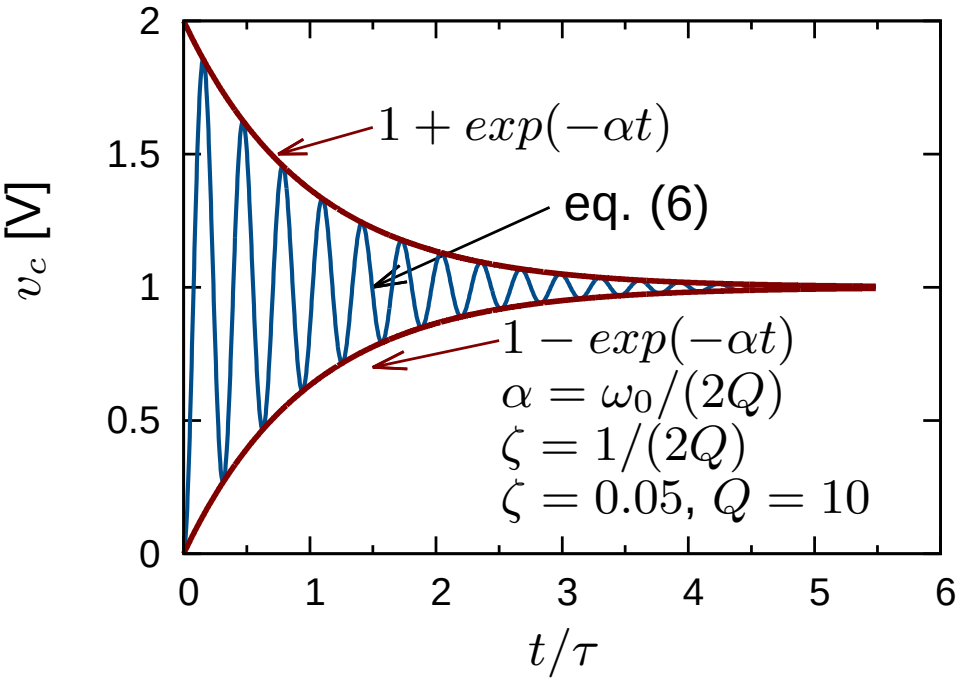
[1] J. Rogers and C. Plett, “A 5-GHz radio front-end with automatically Q-tuned notch filter and VCO,” IEEE Journal of Solid-State Circuits, vol. 38, no. 9, pp. 1547–1554, Sep. 2003.

[2] D. Li and Y. Tsividis, “A 1.9 GHz Si active LC filter with on-chip automatic tuning,” in 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177), vol. 47, no. 3, 2001, pp. 368–369.

[3] F. Bahmani, T. Serrano-Gotarredona, and E. Sánchez-Sinencio, “An accurate automatic quality-factor tuning scheme for second-order LC filters,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54, pp. 745–756, 2007.

[4] M. Zhang and N. Llaser, “Exploiting Time-Domain Approach for Extremely High Q-Factor Measurement,” IEEE Transactions on Instrumentation and Measurement, vol. 64, pp. 2730–2737, 2015.





Voltage source connected to a series RLC network after $t = 0$. We also see the transient response of an underdamped RLC network when the switch closes at $t = 0$.

$$v_c(t) = V_S + e^{-\frac{t}{\tau}}(A_1 e^{j\omega_d} + A_2 e^{-j\omega_d}) \qquad (6)$$

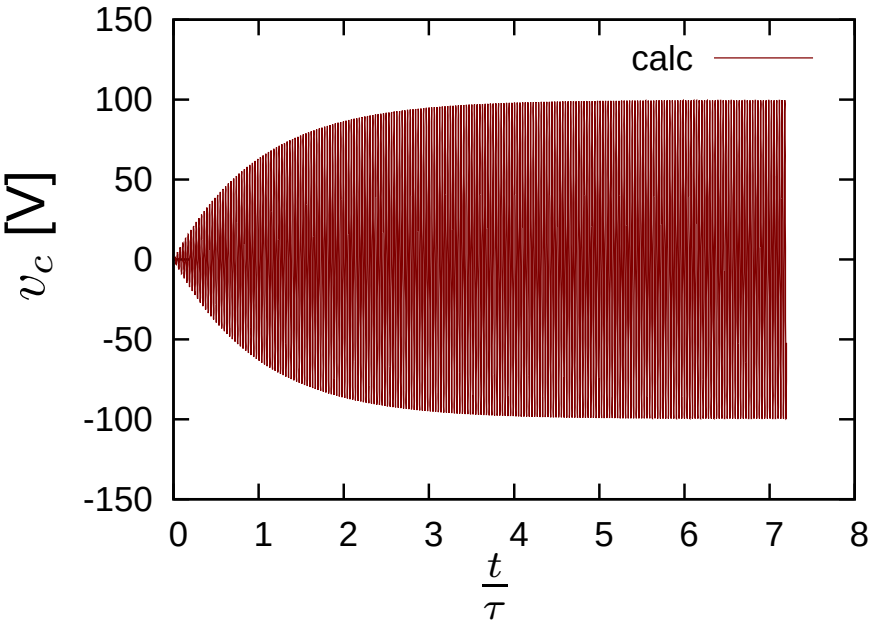
Supposing that $v_s(t)$ is a sinusoid:

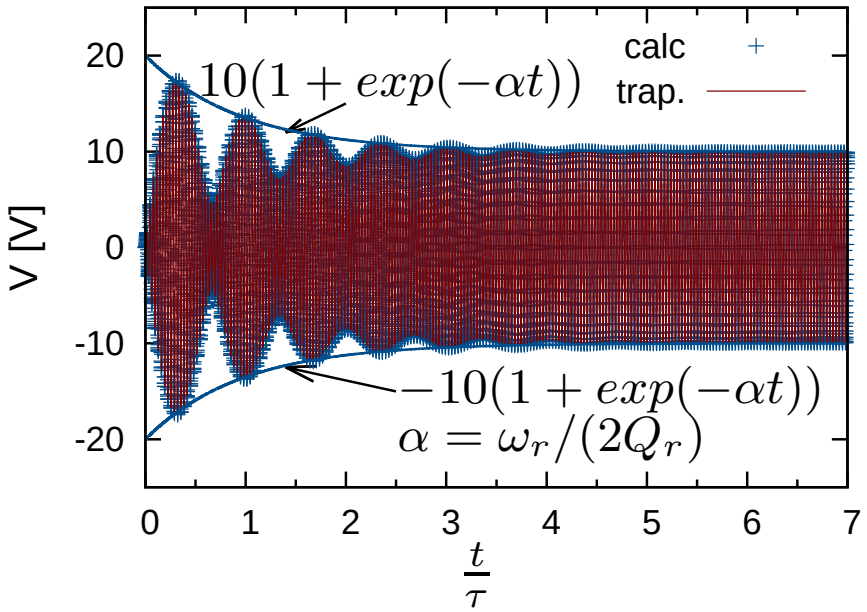
$$v_c(t) = \frac{-A\omega^2 \sin\omega t + \sin\omega t - B\omega\cos\omega t}{A^2\omega^4 + B^2\omega^2 - 2A\omega^2 + 1} + \frac{e^{-\frac{t}{\tau}}\omega\left[(2A^2\omega^2 + B^2 - 2A)\sinh(\theta t) + B\sqrt{B^2 - 4A}\cosh(\theta t)\right]}{(A^2\omega^4 + B^2\omega^2 - 2A\omega^2 + 1)\sqrt{B^2 - 4A}}, \quad (7)$$

where $A = LC$, $B = RC$ and $\theta = \sqrt{B^2 - 4A}/2A$.

LC parameter extractor

Transient behavior of LC networks





Cases considering a tuned LC network and a detuned one.

$$N = 5\tau(f_0 - f_r) \cong 1.6\,Q_r\left(\frac{f_0}{f_r} - 1\right) \qquad (8)$$

LC parameter extractor

Implemented System

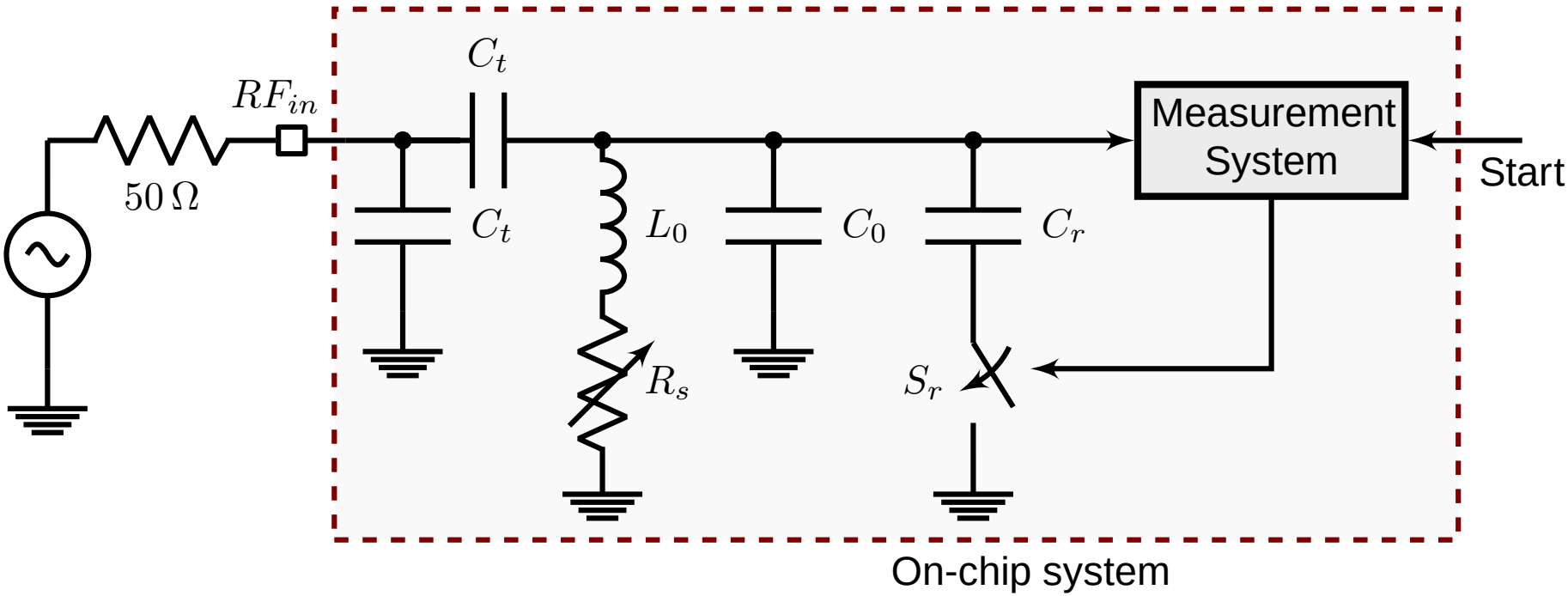


Figure: Simplified on-chip system implemented to extract the properties of L_0, C_0 and R_s.

LC parameter extractor

Implemented System

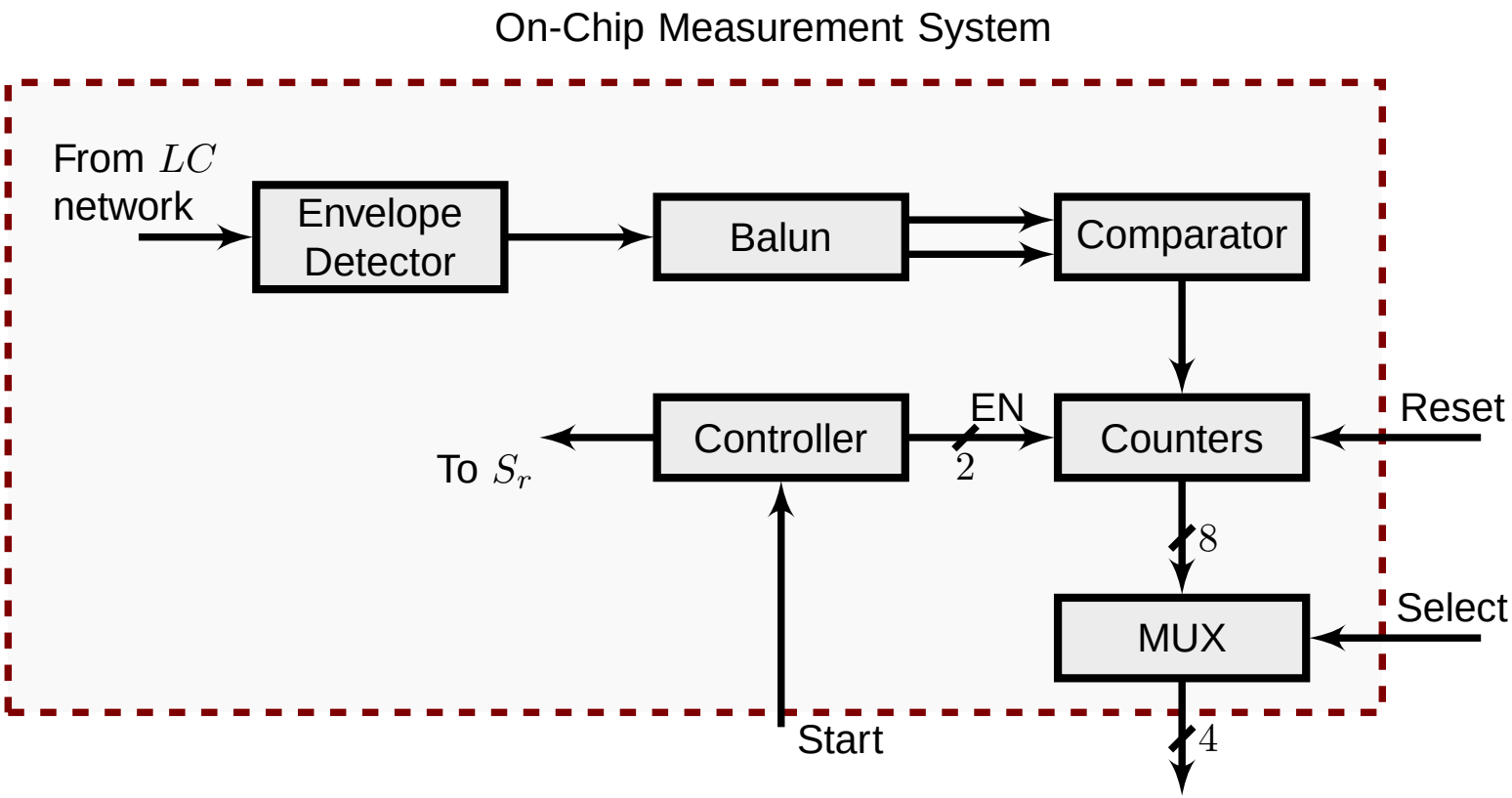
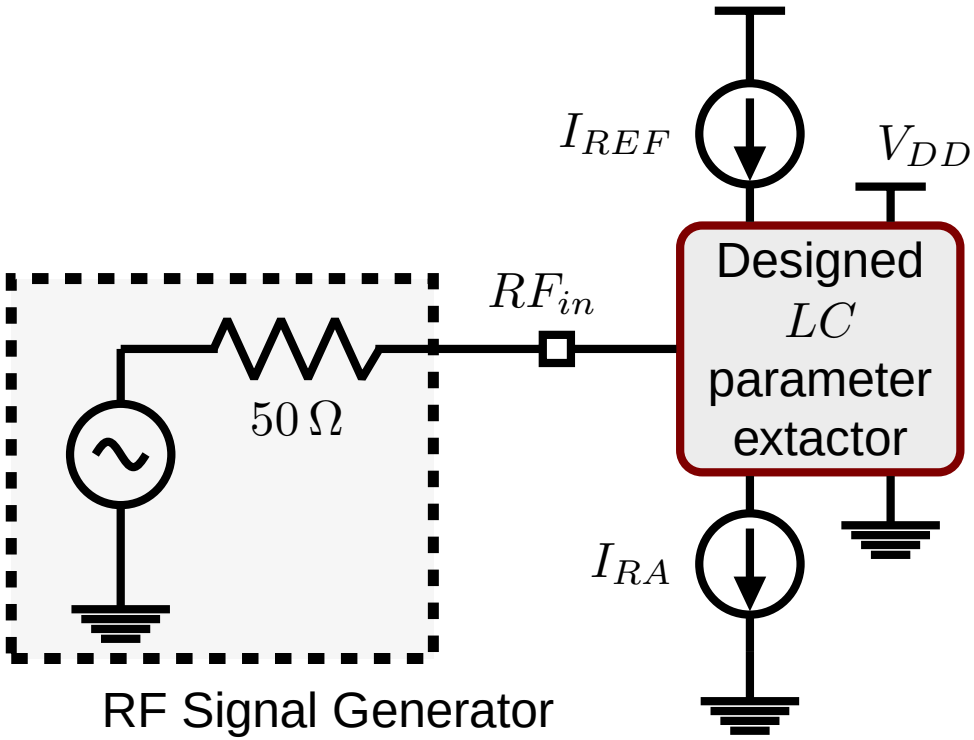


Figure: Block diagram of the designed LC-parameter-extractor system.



Testbench used to simulate the parameter extractor

LC parameter extractor
Results (Simulated)

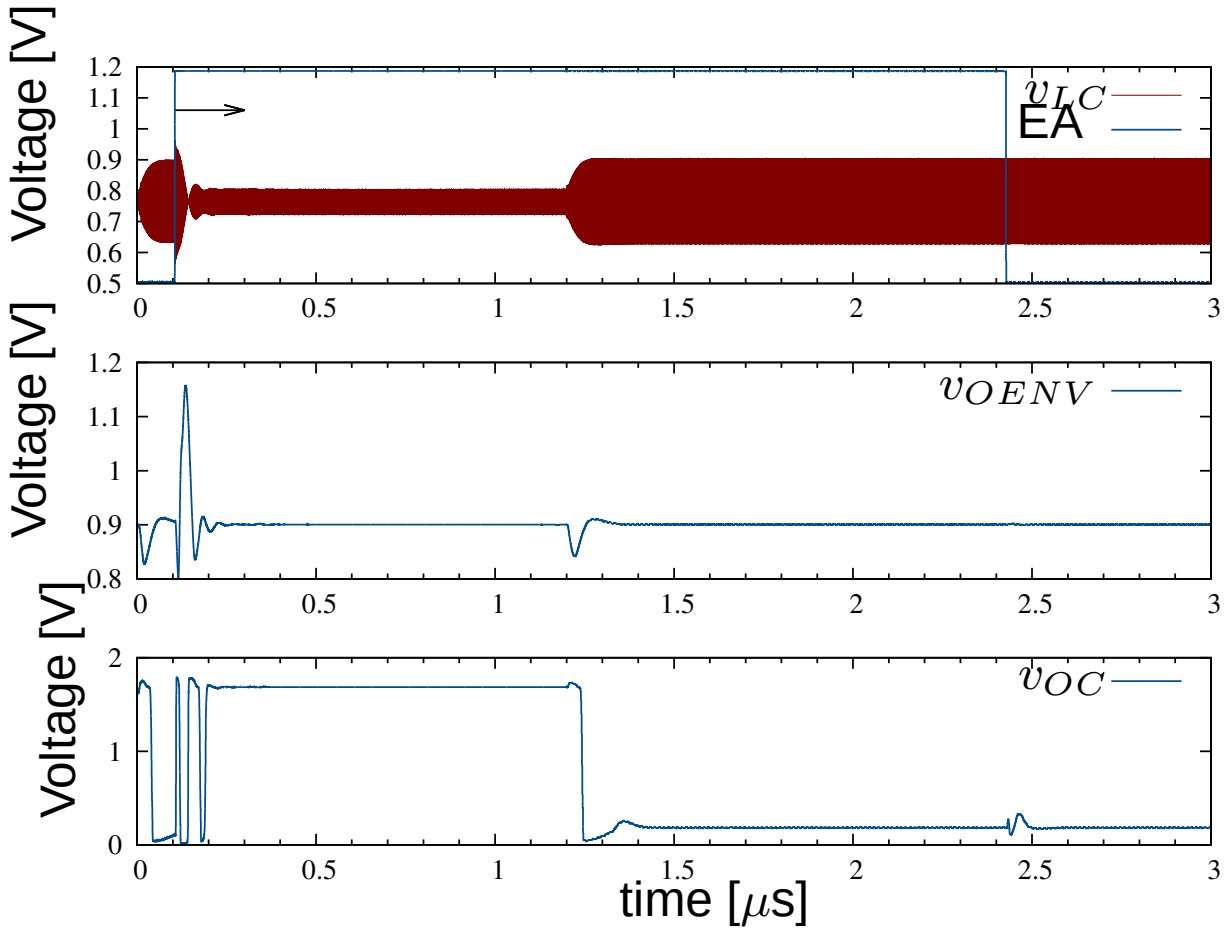
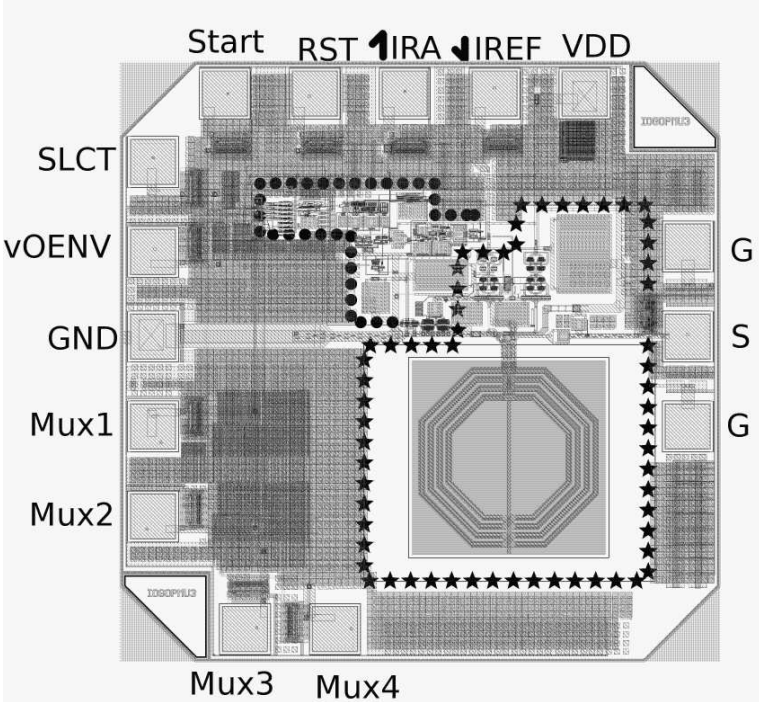
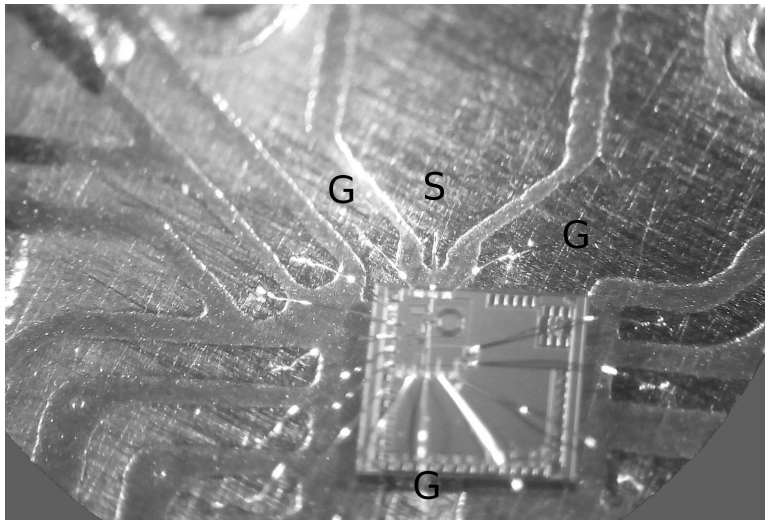


Figure: Complete sequence of the LC parameter extractor.

LC parameter extractor
Results



(a)



(b)

Figure: Layout and fabricated LC parameter extractor wirebonded on an FR-4 PCB in (a) and (b), respectively.

LC parameter extractor
Results

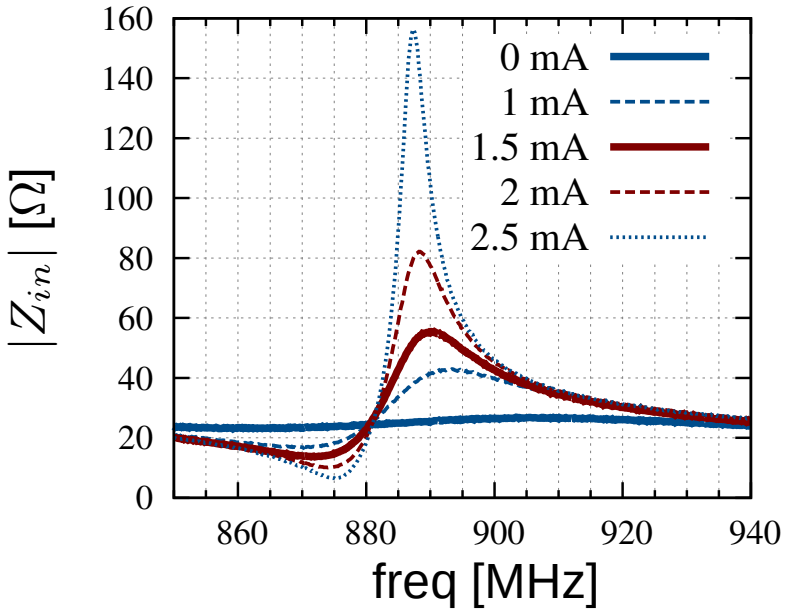


Figure: Measured $|Z_{in}|$.

I_{REF} (mA)	Q sim.	Q meas.
1	23.9	23.7
1.5	49	46.8
2	100	94.5
2.5	253	216
2.7	341	593
3	1680	>4000

Table: I_{REF} and the simulated and measured unloaded Q.

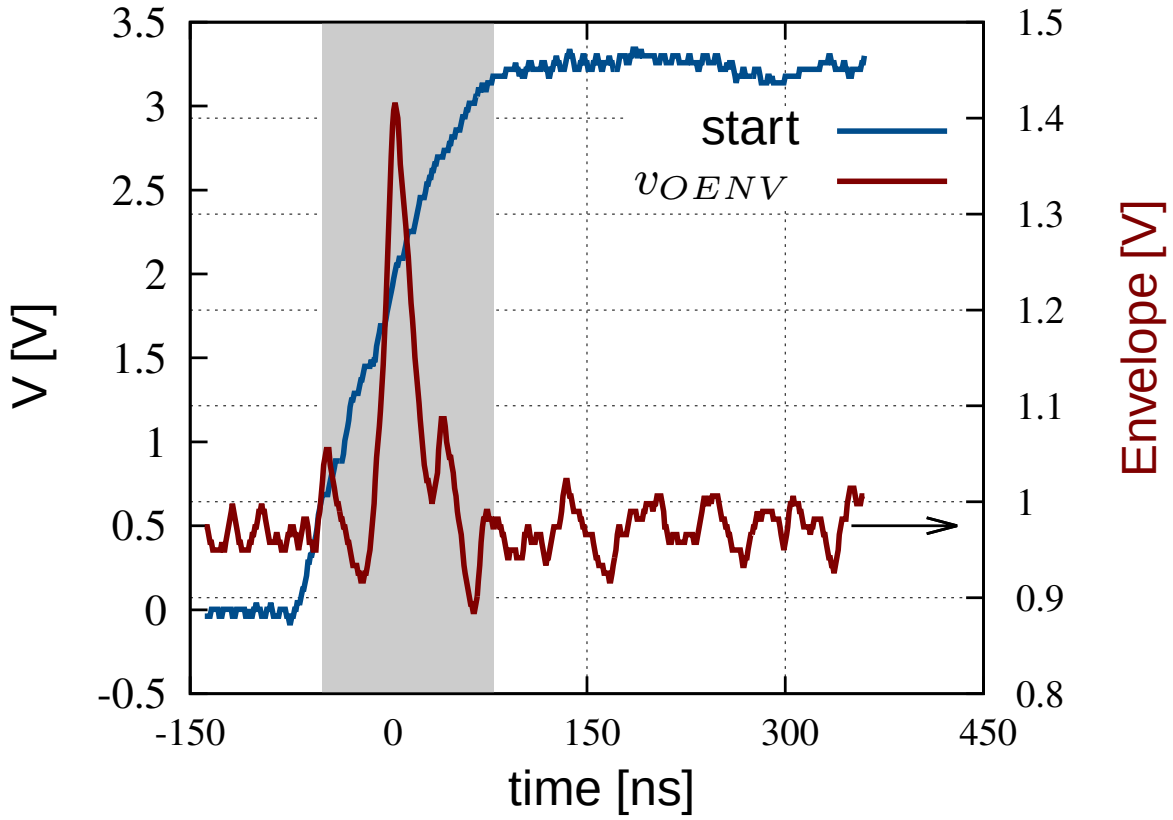


Figure: Measured envelope using $I_{REF} = 3\,\mathrm{mA}$.

LC parameter extractor

Systems that either automatic tune their LC network or measure their Q

Ref.	Method	Process	Freq.	Area	V_{DD}	Current	Time for tuning / measuring
[1]	MS	75-GHz SiGe Bipolar	5.5 GHz	> L	1.8 V	< 19 mA	NA
[2]	MS	0.25-μm BiCMOS	1.9 GHz	> L	2.7-3.3 V	18 mA	NA
[3]	3 dB	0.35-μm CMOS	2 GHz	<.0725 mm^2	1.3 V	< 3.6 mA	9 it.
[4]	Transient	x	10 kHz	Off chip	5 V	NA	$\cong 10Q/\omega_0$
LC p. ext	Transient	130-nm CMOS	0.9 GHz	.034 mm^2	3.3 V	1.6 mA	$2\,\mu$s

[1] J. Rogers and C. Plett, “A 5-GHz radio front-end with automatically Q-tuned notch filter and VCO,” IEEE Journal of Solid-State Circuits, vol. 38, no. 9, pp. 1547–1554, Sep. 2003.

[2] D. Li and Y. Tsividis, “A 1.9 GHz Si active LC filter with on-chip automatic tuning,” in 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177), vol. 47, no. 3, 2001, pp. 368–369.

[3] F. Bahmani, T. Serrano-Gotarredona, and E. Sánchez-Sinencio, “An accurate automatic quality-factor tuning scheme for second-order LC filters,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54, pp. 745–756, 2007.

[4] M. Zhang and N. Llaser, “Exploiting Time-Domain Approach for Extremely High Q-Factor Measurement,” IEEE Transactions on Instrumentation and Measurement, vol. 64, pp. 2730–2737, 2015.

- We present a solution for extracting the parameters of an LC network without the need of extra inductors;
- With the transient modeling, we proposed a method for estimating the parameters of an LC tank (Q and the tuning);
- The measurements results of the prototype was shown and we have seen that the prototype is almost fully working as expected;
- Another version of this system was sent to fabrication (Nov-13th);

Conclusions

- We can say that we designed 3 different tuners for one port devices.

Table: Performance of the tuners conceived in this thesis.

Method	CMOS Process	V_{DD}	I_{avg}	Time for tuning	Area	Frequency
Neg Res tuner	130 nm	3.3 V	$12\,\mu\mathrm{A}/V$	250 ms	0.022 mm^2	$125\,\mathrm{kHz}$
RF **current limiter**	130 nm	3.3 V	$10\,\mu\mathrm{A}$	32 ms	0.015 mm^2	$125\,\mathrm{kHz}$
Transient LC **p. extract.**	130 nm	3.3 V	$1.6\,\mathrm{mA}$	$> 2\,\mu\mathrm{s}$	0.034 mm^2	$900\,\mathrm{MHz}$

Conclusions
Main contributions

- We present two novel methods for tuning LC networks;
- We proposed a circuit for controlling the negative resistance of a cross-coupled pair;
- We show how we are able to decrease the power consumption of the LC parameter based on the RF limiter current.
- A novel LC parameter extractor, operating at $900\,\mathrm{MHz}$, that digitally reports the parameter of the LC network is presented.

Conclusions

Future work:

- In a longer term, it would be interesting to propose a digital control circuitry for the LC parameter extractor. Then, an LC filter could be programed to behave as required by the user.

Thank You

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