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Low-cost impedance meter using a digital lock-in amplifier

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Low-cost impedance meter using a digital lock-in amplifier

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“Man is nothing else but that which he makes of himself.”

Jean-Paul Sartre, 1946

RESUMO

A Tomografia por Impedância Elétrica (TIE) é uma técnica de imagem não invasiva amplamente utilizada em aplicações biomédicas, como no monitoramento da ventilação pulmonar e no imageamento de culturas celulares, porém sua aplicação é comumente limitada pelo alto custo dos medidores de impedância necessários para seu funcionamento. Para facilitar o acesso a esta tecnologia, este trabalho apresenta o desenvolvimento de um medidor de impedância de baixo custo utilizando um microcontrolador. A solução proposta utiliza o RP2040 em conjunto com um inovador algoritmo de amplificador lock-in digital (LIA) baseado em subtração. Essa abordagem elimina a necessidade de processadores de sinal digital (DSPs) caros ao substituir operações de ponto flutuante por simples subtrações. O sistema foi validado experimentalmente medindo capacitâncias na faixa de 2.2 nF a 47 μ F, e comparando os resultados com um medidor LCR comercial devidamente calibrado. Os resultados demonstraram um erro relativo mínimo de 1,21% na faixa de operação avaliada, com a maior precisão ocorrendo próximo ao ponto ideal projetado teoricamente de 32 nF. Embora a prova de conceito tenha sido bem-sucedida, o desempenho atual do dispositivo possui limitações em relação à resolução efetiva limitada (ENOB de 8,7 bits) do conversor analógico-digital (ADC) do RP2040 e ao atraso de fase na amostragem induzido pelo modo sequencial (*round-robin*). O trabalho conclui que, com a implementação de um ADC dedicado e o aumento da frequência de referência utilizada para o LIA, a arquitetura é altamente promissora para futuras aplicações na escala de picofarads.

Palavras-chave: Tomografia por Impedância Elétrica. Amplificador Lock-In Digital. RP2040. Medição de capacitância. Sistemas Embarcados.

ABSTRACT

Electrical Impedance Tomography (EIT) is a widely used noninvasive imaging technique in biomedical applications, such as lung ventilation monitoring and cell culture imaging, but its application is commonly hindered by the high cost of the impedance meters required for its operation. To facilitate access to this technology, this work presents the development of a low-cost impedance meter using a microcontroller. The proposed solution utilizes the RP2040 alongside an innovative subtraction-based digital lock-in amplifier (LIA) algorithm. This approach eliminates the need for expensive digital signal processors (DSPs) by replacing floating-point operations with simple subtractions. The system was experimentally validated by measuring capacitances ranging from 2.2 nF to 47 μ F, and comparing the results with a properly calibrated commercial LCR meter. The results demonstrated a minimum relative error of 1.21% across the evaluated operating range, with the highest accuracy occurring near the theoretically projected optimal point of 32 nF. Although the proof of concept was successful, the current performance of the device has limitations regarding the limited effective resolution (8.7-bit ENOB) of the RP2040's analog-to-digital converter (ADC) and the sampling phase delay induced by the sequential (*round-robin*) mode. The work concludes that, with the implementation of a dedicated ADC and an increase in the reference frequency used for the LIA, the architecture is highly promising for future applications on the picofarad scale.

Keywords: Electrical Impedance Tomography. Digital Lock-In Amplifier. RP2040. Capacitance Measurement. Embedded Systems.

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LIST OF ABBREVIATIONS AND ACRONYMS

DC	Direct current
DSP	Digital signal processor
DUT	Device under test
EIT	Electrical Impedance Tomography
ENOB	Effective Number of Bits
LIA	Lock-in amplifier
PSD	Phase-sensitive detector

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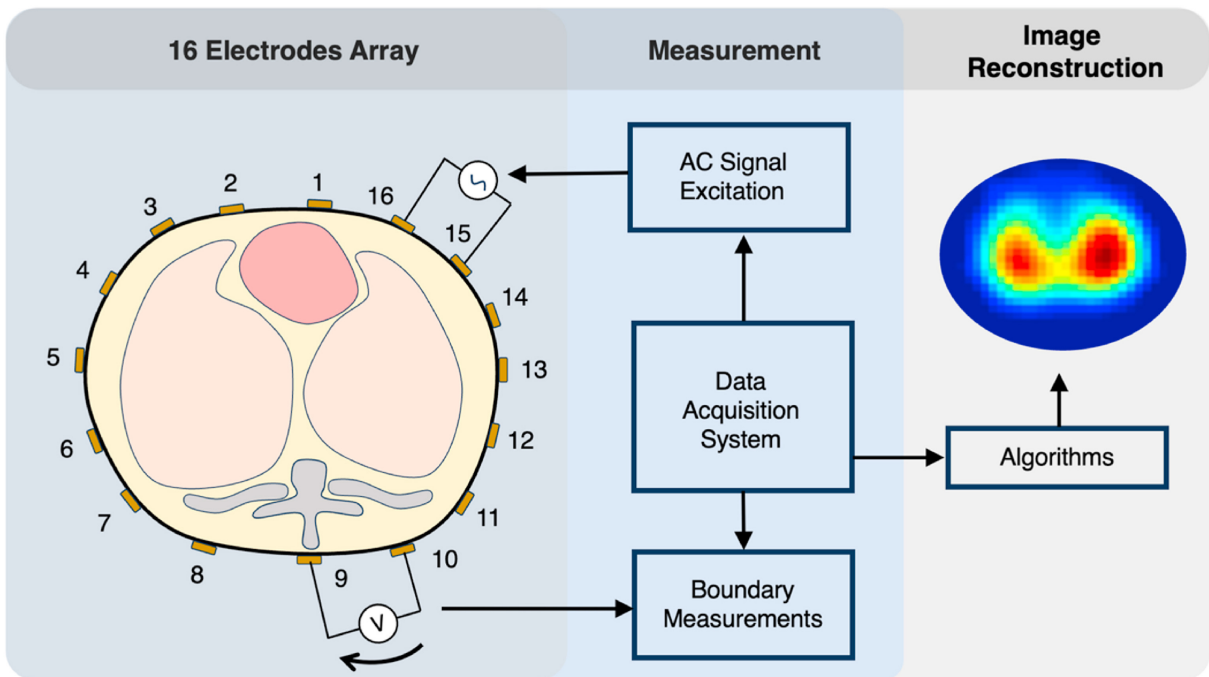
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1 INTRODUCTION

1.1 CONTEXT AND BACKGROUND

Electrical Impedance Tomography (EIT) is a noninvasive imaging technique based on measuring the test subject response to a known current or voltage and identifying the corresponding impedance. Through the use of multiple electrodes placed equidistantly around the object to be imaged, the alternating current (or voltage) is sequentially injected between pairs of electrodes, allowing the creation of a conductivity map that forms a tomographic image (WU et al., 2021), as illustrated in Figure 1.

Figure 1 – Working principle of EIT, highlighting the steps in the process of constructing an image.



Source: Adapted from Yu et al. (2024).

This technique is a staple of the biomedical imaging arsenal, since the frequency of the injected stimulus can be chosen according to the desired application: high frequencies are used to detect liquid trapped inside the tissue, while low frequencies are useful for identifying its general shape and size. For example, lung ventilation monitoring typically uses frequencies around 50 kHz to allow the imaging of the gas (air) and fluid (blood) inside the organ (WU et al., 2021). EIT also finds use in a myriad of other applications, such as industrial imaging for gas and oil pipes (KWON; CHOI; SEO, 2015), cell imaging for developing and monitoring cell cultures (MORCELLES; BERTEMES-FILHO, 2021), and even geophysics, through electrical resistivity tomography, a subtype of EIT that utilizes direct current to monitor the resistivity of soil (DICKIN; WANG, 1996).

To make a clear image of the underlying object, many electrodes are needed, each one providing more resolution to the final image. However, the impedances being measured are small, involving capacitances in the order of femtofarads to picofarads. The stray capacitances present throughout the whole measuring system are often larger in value than the ones being measured, which can lead to loss of information if not taken into account. Due to the low currents and voltages, noise is also a big factor that has to be carefully handled, especially at lower frequencies, where Flicker noise dominates the spectral density (FERLITO et al., 2020).

If the test subject is moving or has moving fluids inside of it, measurement speed is also a factor. There are various ways of approaching the sequence in which the electrodes will be measured, but at a minimum, $n \times n$ measurements will be needed, being n the number of electrodes. To define the necessary requirements for the project, it is important to note that EIT systems typically inject safe alternating currents of low amplitude, generally below 1 mA, while measuring the resulting boundary voltages (WU et al., 2021). The collection of all the electrode data is used to make a single frame of the output image, with multiple acquisitions needed per second to allow for the imaging of moving subjects. Depending on the physiological target, the required measurement speed can range from 10 frames per second for standard lung monitoring to over 100 frames per second for fast cardiac or thorax vital sign tracking (WU et al., 2021). Failure to fulfill these requirements will lead to a blurred image or other artifacts.

Commercial impedance meters are available, but are generally ill-suited for this kind of application, being too bulky, slow, or expensive. The best approach is an embedded measurement system, allowing for portability and tailored for each application's needs. However, designing a system for this use is not trivial, requiring careful consideration and design on each step along the way. The current paradigm in measurement technology reflects all of the above, using microcontrollers for their unmatched flexibility and affordability, as well as ease of design (REVERTER, 2012).

1.2 MOTIVATION

As discussed previously, EIT is a valuable technique for noninvasive imaging. Since it requires carefully designed circuits and is very sensitive to interference, the current paradigm usually uses expensive measurement devices to offer its full potential. To democratize access to EIT and popularize its usage, it is essential to offer a robust, low-cost alternative to these devices.

The embedded measurement system approach is promising, being an accessible option to measure the small capacitances required. Modern microcontrollers can fulfill the hardware and timing requirements of the task at hand, offering good ADCs, high clock speeds, and ease of development.

More specifically, the RP2040, a 32-bit dual-core ARM microcontroller designed by

Raspberry Pi and released in 2021, demonstrates the necessary capabilities for these tasks. By combining the flexibility and availability of this microcontroller with the speed and accuracy of modern data processing algorithms, it is theoretically possible to implement a sub-picofarad impedance measurement device that can be used for EIT applications.

1.3 OBJECTIVES

The primary goal of this work is to develop a low-cost, flexible impedance meter using a microcontroller and optimized programming, as a proof-of-concept for future EIT applications. The measuring device will target not the sub-picofarad range needed for EIT, but a higher, nanofarad range, while still aiming to achieve a low relative error in a wide range of capacitance values. The results will then be analyzed and the possibility of adapting the architecture to the needed range will be discussed.

This task will require a custom prototype board to interface all the necessary parts, such as the microcontroller and analog filtering stages, as well as the development of specialized firmware. Performance will be evaluated by measuring known capacitances and comparing the results against a properly calibrated LCR meter.

2 THEORETICAL BACKGROUND

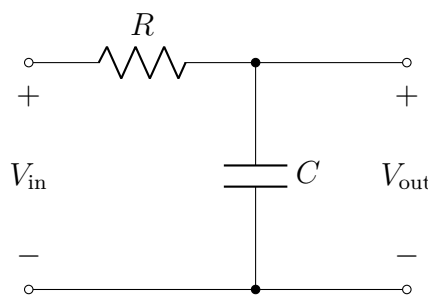
This chapter will elaborate on the theoretical background that will be used in the following chapters, as well as providing a review of the current state of the art. As stated previously, most of the current measurement systems utilize microcontrollers to handle the sensor reading and data manipulation needed. The following sections are based on these systems, being the most technologically advanced.

2.1 DIRECT MICROCONTROLLER INTERFACING

The simplest method of measuring an impedance, such as a capacitance or an inductance, is measuring its time constant τ . For capacitors, it represents the time needed to charge the capacitor from 0 V to $1 - e^{-1}V \approx 63.2\%$ of the applied Direct current (DC) voltage, being defined as $\tau = RC$, where R is the series resistance through which the capacitor will be charged, and C is the capacitance. Alternatively, it is also the time needed to discharge the capacitor through the resistor to $\approx 36.8\%$ of the initial charge voltage (REVERTER, 2012).

To illustrate this, Figure 2 shows a simple RC circuit, while Figure 3 shows its charging curve in the case where a DC voltage V_{in} of 1 V is applied, with $R = 10 k\Omega$, $C = 1 \mu F$. By designing a system where V_{in} and R are previously known, it is possible to determine the value of C by measuring the time needed for V_{out} to reach $\approx 63.2\%$ of V_{in} , equal to one time constant τ .

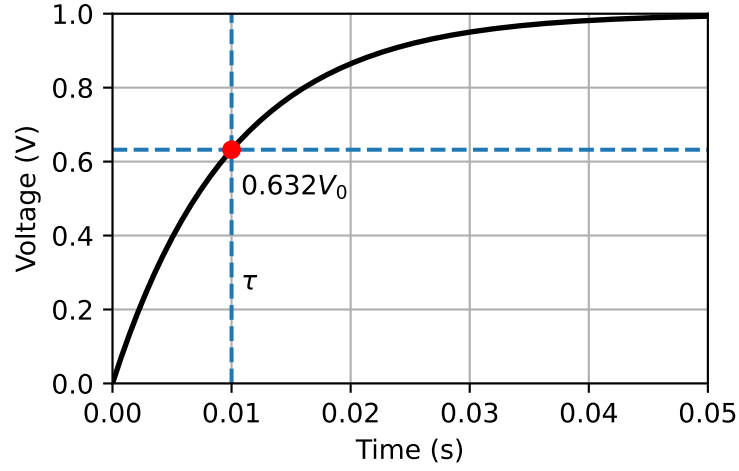
Figure 2 – Schematic of a simple series RC circuit used for demonstrating direct microcontroller interface measurement of the time constant τ .



Source: The author.

Reverter (2012) proposes a direct interface circuit based on a microcontroller to measure the time constant of a single capacitive sensor, as represented in Figure 4. Measuring the discharge time once would be the simplest way of carrying out the measurement, but the author does so three times through the use of an auto-calibration technique, eliminating both additive and multiplicative offsets of the circuit. The order in which the

Figure 3 – Simulated transient charging response of a series RC circuit, highlighting the exponential voltage rise towards the 1 V DC input step over time.



Source: The author.

auto-calibration measurements are taken is not important. As such, in no specific order, they are:

- a) Parasitic offset measurement: measures the discharge time of the parasitic capacitance C_s , removing its undesired offset.
- b) Reference measurement: measures discharge time of the reference capacitance C_{ref} , eliminating variability caused by component's tolerances and low-frequency power-supply noise.
- c) Sensor measurement: measures the discharge time of the sensor capacitance C_x .

The first part of the process, the charging step, is to charge the desired capacitance to the logic-high voltage V_1 . This is done by setting Pin 1 to output '1' and changing the other pins according to the desired measurement, as shown in Table 1. This configuration should be kept until the charging is fully finished.

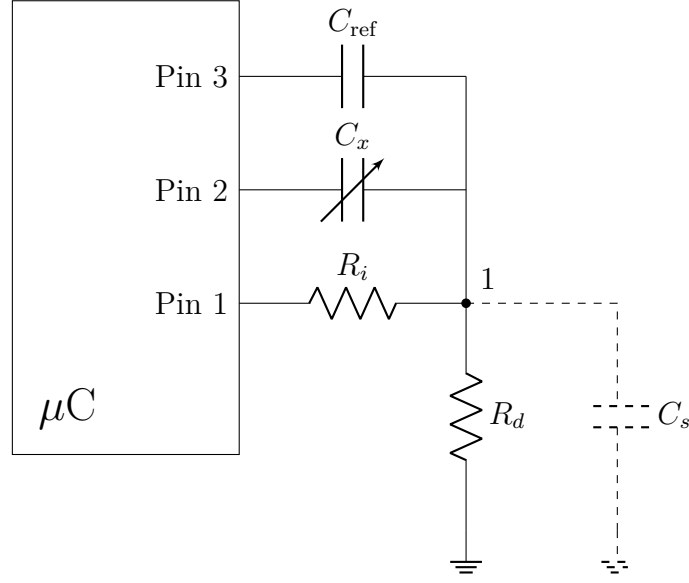
Table 1 – Pin configurations for the charging stage.

Measurement	Pin 2	Pin 3
Reference	High-Z	'0'
Offset	High-Z	High-Z
Sensor	'0'	High-Z

Source: Reverter (2012).

The second part, the discharging step, maintains the same configuration as the first part, except for Pin 1. Instead of discharging the capacitances until their voltage reaches the ground potential, it is more efficient to utilize the integrated Schmitt trigger buffer commonly found on GPIO pins. This way, Pin 1 can be set as a High-Z input with an

Figure 4 – Direct interface circuit for a single capacitive sensor.



Source: Adapted from Reverter (2012).

associated interrupt on state change. At the start of the discharging process, a timer is set to start. When the voltage threshold from a logic '1' to a logic '0' is crossed, the interrupt fires and the timer is then read and its value saved.

After each measurement, the cycle repeats until all three have been obtained. Then, the sensor capacitance can be estimated as

$$C_x = \frac{T_x - T_{\text{off}}}{T_{\text{ref}} - T_{\text{off}}} C_{\text{ref}} \quad (1)$$

where T_x is the discharge time of the sensor, T_{off} is the discharge time of the parasitic offset capacitance, and T_{ref} is the discharge time of the reference capacitance (REVERTER, 2012).

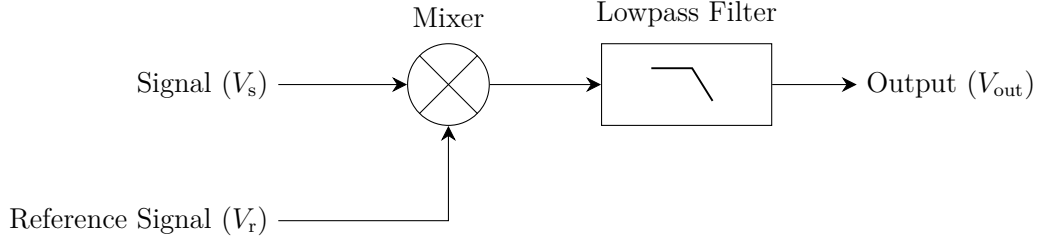
This measuring technique works remarkably well, but only for capacitances larger than 1 pF, since parasitic capacitances start having a big effect on the outcome for values lower than that. Still, it proves itself valuable, considering how simple and cheap it is.

2.2 LOCK-IN AMPLIFIER

A Lock-in amplifier (LIA) is a useful way of filtering the desired signal selectively, removing much of the noise affecting the measurement. It is very well-suited for measuring low value impedances, such as the ones present in capacitive sensors. Figure 5 shows the usual structure of a LIA (BENGTSSON, 2012).

For a LIA to work, it is required to have a fixed frequency reference, hereby given as $V_r \sin(\omega_r t + \theta_r)$, where V_r is the reference signal's amplitude, ω_r its frequency, and θ_r

Figure 5 – Signal processing block diagram of a basic analog lock-in amplifier (LIA), showing the mixing of the input signal (V_s) with a reference wave (V_r) followed by low-pass filtering to extract the DC component (V_{out}).



Source: The author.

its phase. The desired signal is assumed to be of the form $V_s \sin(\omega_s t + \theta_s)$.

The first essential part of the LIA topology is the Phase-sensitive detector (PSD), which will lock the output of the amplifier in a specific frequency. If the above signals are the LIA reference and input, respectively, the PSD's output is the product of the sine waves (SYSTEMS, 2006).

$$\begin{aligned}
 V_{psd} &= V_s V_r \sin(\omega_s t + \theta_s) \sin(\omega_r t + \theta_r) \\
 &= \frac{1}{2} V_s V_r \cos([\omega_s - \omega_r] t + \theta_s - \theta_r) - \\
 &\quad \frac{1}{2} V_s V_r \cos([\omega_s + \omega_r] t + \theta_s + \theta_r)
 \end{aligned} \tag{2}$$

This output has two signals: one at the difference frequency ($\omega_s - \omega_r$), and another one at the sum frequency ($\omega_s + \omega_r$). The next step in the topology is to run this resulting signal through a low-pass filter, which will filter the AC signals. This seems counter-intuitive, since it would filter out both signals. However, in the case that $\omega_s = \omega_r$, the filtered output will be a DC signal, proportional to the signal amplitude, of value

$$V_{out} = \frac{1}{2} V_s V_r \cos(\theta_s - \theta_r) \tag{3}$$

Traditionally, this signal multiplication was done using analog circuitry, requiring complex circuits and being oftentimes expensive and/or bulky. This limitation led to the rise of digital LIAs, first introduced by using a dedicated Digital signal processor (DSP), allowing the use of floating and fixed-point multiplication directly at hardware level. Multiplication in a general purpose microprocessor is a costly operation, taking many cycles to complete. So, for standard applications, a DSP is required (BENGTSSON, 2012).

Li et al. (2011) proposes a high-speed algorithm for a digital LIA that avoids the cost of multiplications by oversampling the signal and performing subtractions. The

authors sample the signal with a sampling frequency four times the signal's frequency, obtaining samples at 0° , 90° , 180° , and 270° . At these specific phase angles, the sine (or cosine) reference signal evaluates to $\{0, 1, 0, -1\}$, removing the need for more complex multiplications. This way, the real and imaginary parts of the signal become

$$\begin{aligned} I &= \frac{1}{4} (X[1] - X[3]) \\ Q &= \frac{1}{4} (X[0] - X[2]) \end{aligned} \tag{4}$$

allowing a much faster calculation without the use of a DSP, which in turn minimizes system complexity and cost.

This technique has great results, including in the cases where the measured capacitance is of small value. It is, however, dependent on a precise reference signal and, for the fast algorithm above, also dependent on accurate timing for the samples.

2.3 COMPARING TECHNIQUES

The direct interfacing technique is the most basic among the discussed methods, present in Table 2. It allows for good measuring performance with the least amount of system and computational complexity of the three. Conversely, it fares poorly with regards to accuracy when the capacitance values dip below 1 pF, and may be influenced heavily by parasitic capacitances and external noise.

Both LIA approaches perform better when dealing with the sub-picofarad measurements required for EIT, but also have stricter requirements that need to be met. For the DSP-based architecture, the primary limitation is the DSP itself, since cheap microcontrollers do not typically integrate DSP hardware. The subtraction-based architecture proposed by Li et al. (2011) eliminates this requirement, but substitutes it with the need for more precise timing.

2.4 CHOOSING THE MEASUREMENT RANGE

The range of capacitances that the microcontroller LIA will be able to measure depends on several factors. The lower range, consisting of small capacitances, is limited primarily by the ADC's speed and any external phase delay introduced during the measurement. The subtraction LIA utilizes the difference in phase between the reference and the output signal to obtain the real and imaginary parts of the voltage wave, which works well for capacitance values that induce a noticeable phase shift. However, as the capacitances get smaller, this phase shift is overshadowed by the time delay between consecutive ADC samples, causing complete loss of measurement accuracy.

Table 2 – Comparison of impedance measurement techniques for embedded systems.

Technique	Hardware Requirements	Computational Cost	Primary Limitations
Direct Interfacing	General-purpose microcontroller	Minimal (Simple timers)	Inaccurate below 1 pF, highly susceptible to parasitic capacitance and low-frequency noise.
Classic Digital LIA	DSP or FPGA, high-speed ADC	High (Floating-point math)	Higher financial cost, higher power consumption, and increased physical footprint.
Subtraction Digital LIA	General-purpose microcontroller, fast ADC	Low (Additions and subtractions)	Requires precise ADC timing and synchronization with the reference signal.

Source: The author.

The upper range is limited by the voltage resolution of the ADC. Between the reference and the DUT, a resistor R_s is placed to limit the current and act as a voltage divider of previously known value. However, as the capacitances grow, their reactance becomes smaller, which leads to less voltage applied in the DUT. Eventually, the voltage levels are so low that the ADC can't measure it anymore, causing again loss of measurement accuracy.

The operating point of the measurement device can be set by determining the reference frequency and the resistance R_s . To maximize the excursion of the phase shift and the voltage in the DUT over the desired range, the operating point, which is also the capacitance value with the best measurement accuracy, should be in the valley created by the superposition of both limitations. A phase shift of 45° is the middle point of the excursion of the phase angle and optimal value for detection, happening when the capacitive reactance equals the resistance. For the voltage range, the middle point and optimal value happens when both impedances share the same value. Both points end up being the same, and the capacitance value with the best accuracy can be expressed as

$$C = \frac{1}{2\pi f R_{eq}} \quad (5)$$

where R_{eq} is the equivalent resistance seen by the DUT, consisting of a parallel circuit between R_s and the ADC input impedance.

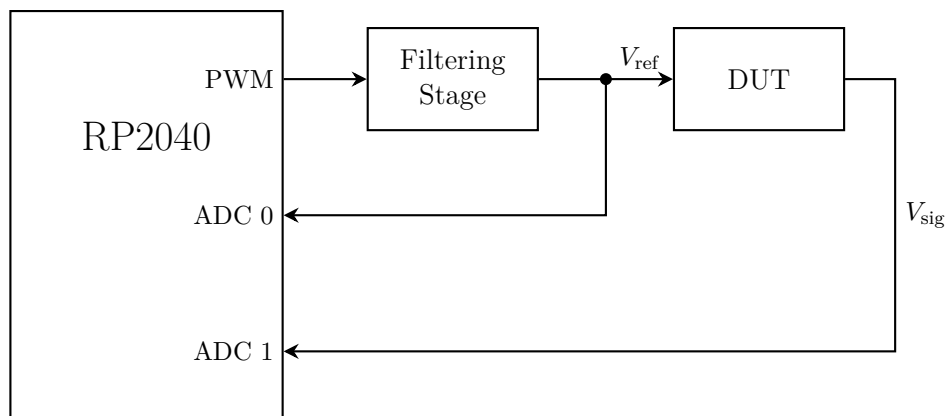
3 SYSTEM DESIGN AND IMPLEMENTATION

This chapter aims to describe the system design choices made during the project's development, as well as how these choices were implemented both in hardware, and software.

3.1 HARDWARE ARCHITECTURE

The hardware needed for the impedance measurement device consists of the microcontroller and its voltage supply, a signal filtering stage to deliver a clean sinusoidal signal to the load, and a voltage reference. Figure 6 shows a system block diagram of the hardware architecture.

Figure 6 – Proposed system hardware architecture block diagram, detailing the signal flow from the RP2040 PWM generator, through the active filter front-end, down to the DUT, and back to ADC channels 0 and 1.



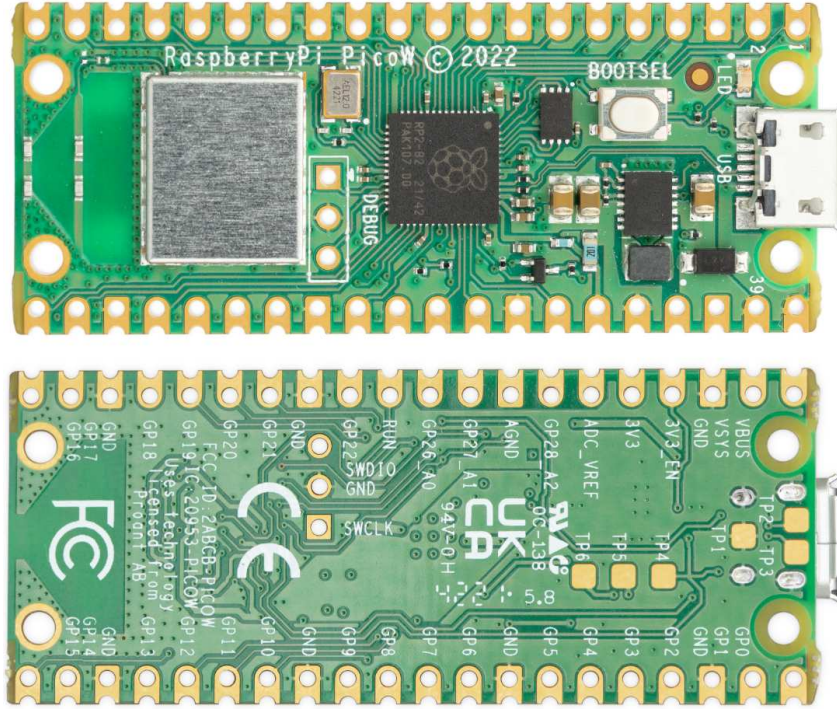
Source: The author.

3.1.1 Microcontroller

As stated previously, the microcontroller was chosen to be the Raspberry Pi RP2040. This decision was heavily influenced by its accessibility and low-cost, significantly lowering the entry barrier for this project, while also fulfilling all the needed requirements.

The RP2040 is powered by a dual-core ARM Cortex-M0+ clocked at 133 MHz (capable of overclocking), 264 kB of embedded SRAM and 30 GPIOs, 4 of which can be used as analog inputs. It also has a 4 channel 12-bit ADC capable of 500 ksps, and 16 PWM channels. The chip itself is powered by a voltage of 3.3 V, but the Pico W board can be powered by 5 V, supplied through a micro-USB port, which eliminates the need for an external power supply unit.

Figure 7 – Raspberry Pi Pico W microcontroller board.



Source: Raspberry Pi Ltd (2024).

Unfortunately, even though the RP2040's ADC is 12-bit, the Effective Number of Bits (ENOB) is limited to 8.7, showing peaks of non-linearity in specific values caused by a design error in the chip. This limitation reduces the accuracy of the measurement and must be accounted for.

One of the GPIO pins is used to output a PWM signal with a frequency f_s , which will serve as input to the filtering stage. The output of the filter, a sine signal of the same f_s frequency, is sampled by one of the ADC inputs, and is also used as a input V_{ref} to the Device under test (DUT) stage. This final signal, now influenced by the voltage divider consisting of the impedance under test and R_s , is again sampled by an ADC input.

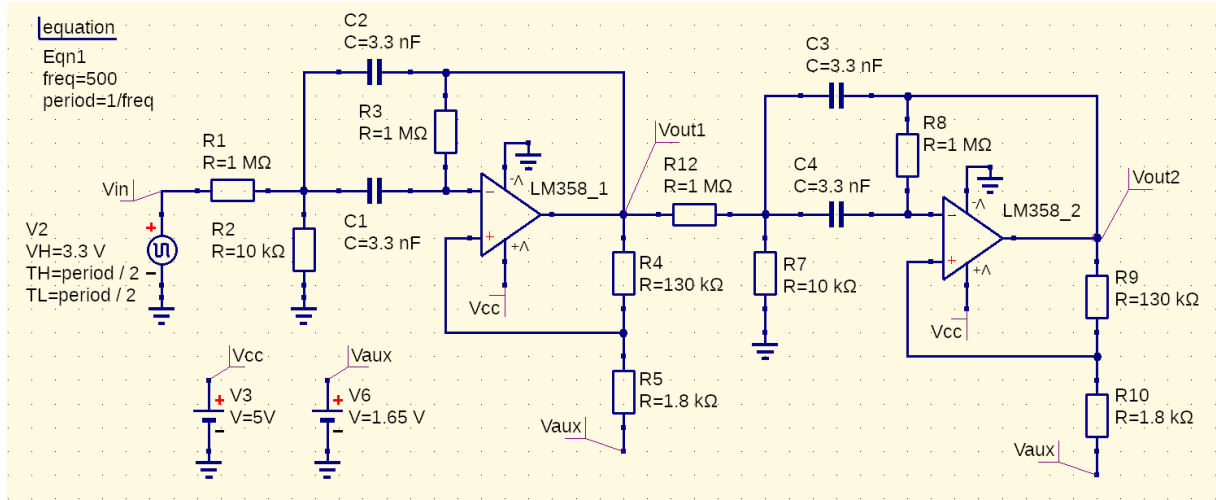
3.1.2 Signal filtering

The signal filtering block is based on a two-stage 4th order Butterworth band-pass active filter, using a LM358N chip as the op-amp, owing to its availability and acceptable performance, set around a 500 Hz center frequency. This frequency was chosen alongside a R_s of $10\text{ k}\Omega$, resulting in an optimal capacitance measurement value of approximately 32 nF when considering the ADC input resistance to be $1\text{ M}\Omega$. For the filter specifications, a -3 dB passband was used, with width equal to 10% of the center frequency, while the stopband was set to -40 dB with a width double the center frequency.

This configuration was simulated using the 'uSimmics' software (previously known

as 'QucsStudio'). The circuit schematic is shown in Figure 8, and the simulation results in Figure 9. The output of the first stage showed a slight distortion, which was mostly corrected by the second stage, resulting in a sine wave with an acceptable amount of higher-order components.

Figure 8 – Circuit schematic of the filtering stage with a center frequency of 500 Hz.



Source: The author.

3.1.3 Voltage reference

For added stability to the DC operating point, the signal filtering circuit requires an auxiliary DC voltage in its feedback system. To supply this voltage reference, a LM358N op-amp was used in a voltage follower configuration, buffering the voltage from a simple resistive voltage divider. By using the Pico W's VBUS pin as a 5 V voltage source when the board is powered via USB, and two resistors – one 10 kΩ and the other one 4.7 kΩ, the voltage divider outputs around 1.6 V, which is close to half of the 3V3 supply used by the RP2040 chip. Figure 10 shows a circuit schematic of the voltage reference stage, as well as the results of the DC simulation.

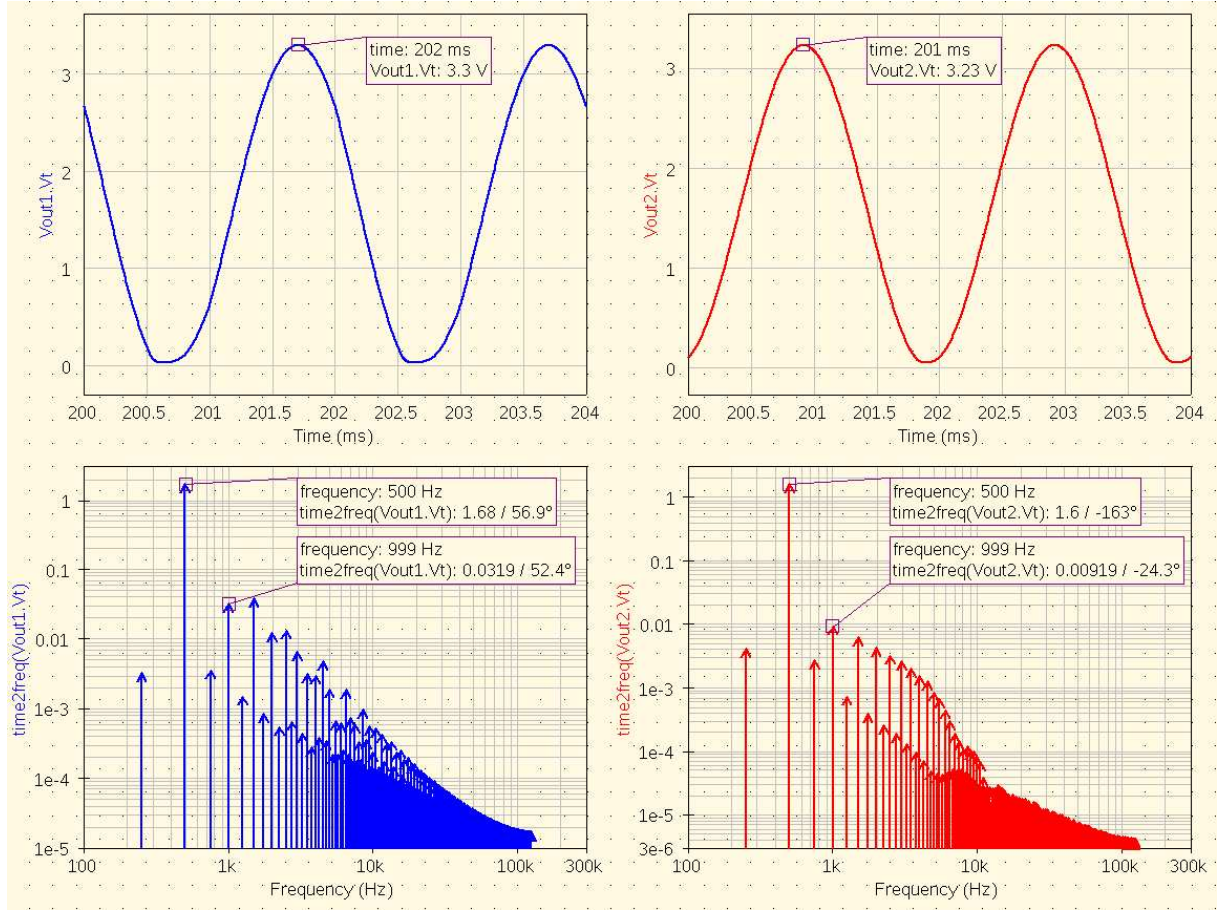
3.2 SOFTWARE

The following subsections will elaborate on the software implementation, specifying the trade-offs taken along the way and providing an overview of the algorithm used.

3.2.1 Algorithm flowchart

The algorithm execution follows a sequential state machine, adapted from Miyazaki et al. (2019) and illustrated in Figure 11. This code flow is independent of the language implementation and will now be analyzed in detail.

Figure 9 – Simulation results for the filtering stage with a center frequency of 500 Hz.



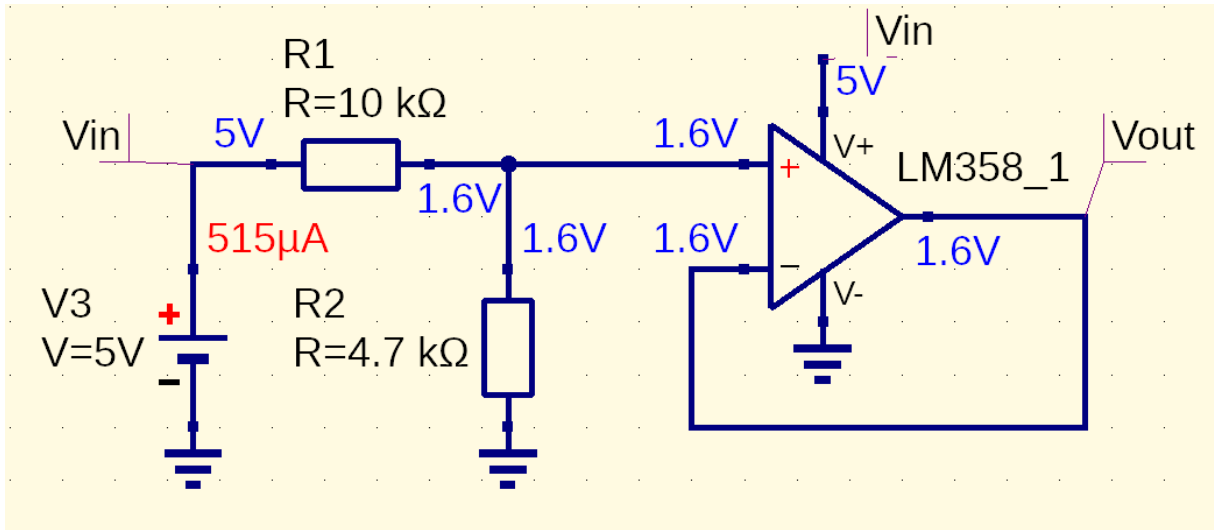
Source: The author.

The first step, after the board is powered on and performs its own startup routine, is to initiate all the necessary peripherals. This includes: the internal clock, performing any necessary CPU or ADC overlocks; the PWM signal, that will be then used to generate the sine signal at the specific measuring frequency; the ADC, for measuring the samples; and the serial communication for interfacing with the user.

The second step consists in calibrating the circuit using a two-step technique: first by measuring the open-circuit voltage, where the DUT is disconnected; then the short-circuit voltage, where the DUT is shorted. For each of the two measurements, a complex voltage is obtained by using Li et al. (2011) algorithm of sampling the output signal every 90° in relation to the reference signal, and converting the values to a real and an imaginary part, which is then saved for later use.

In the third step, the device is already calibrated and the actual DUT measurement is carried out. The technique is the same as the one used in the calibration step, sampling the output signal every 90° . It is necessary to wait for a zero-crossing event on the reference signal to synchronize the samples and start the process. Instead of sampling only 4 times,

Figure 10 – Circuit schematic of the voltage reference stage.



Source: The author.

it is more accurate to sample every point multiple times and take the average of the results. The results are stored in variables for later use.

The fourth step uses the variables obtained in the previous step to obtain a complex value representing the DUT impedance. This result may be interpreted as a pure resistance by taking the real part only, or a capacitance by taking the imaginary part.

The fifth and last step prints the results to the serial interface and prepares for a new measurement round. The calibration step is skipped, since the device has already been calibrated before.

3.2.2 Language implementations

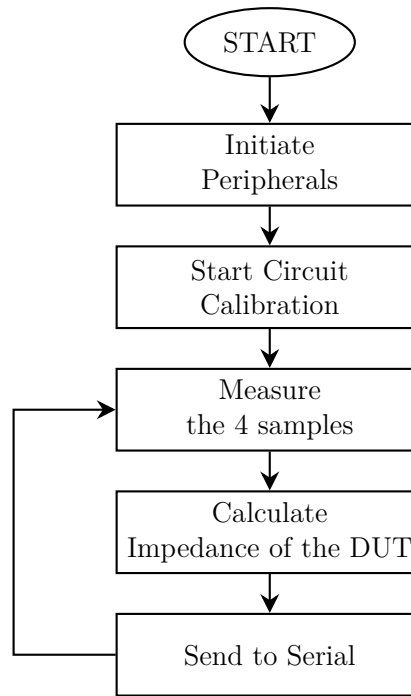
The algorithm above was first implemented through the use of MicroPython, an efficient implementation of Python 3 for microcontrollers, which allowed for quick prototyping and testing. Due to performance issues, it was later ported to the C language, empowering the use of the full capabilities of the RP2040. The following subsections will provide an overview of the implementations. Since both of them follow the algorithm flowchart very closely, the focus will be on a few differences between the two.

3.2.2.1 MicroPython

To extract maximum performance from the RP2040 microcontroller, it is over-clocked to 270 MHz right at the start of the script. Then, the GPIO pins, ADC, and PWM are initialized.

The sampling function uses polling of the ADC value to detect the zero-crossing event on the reference, comparing between the current value and the previous one. After the

Figure 11 – Impedance measurement firmware operational flowchart, illustrating peripheral startup, dual-step open/short circuit calibration, and the continuous $4f$ sampling loop.



Source: Adapted from Miyazaki et al. (2019).

event is detected, the samples are taken every 90 degrees using calls to a sleep function to maintain synchronicity. There are two major limitations to this measurement methodology.

The first flaw is in how the zero-crossing is detected: since Python is an interpreted language, it introduces noticeable overhead on variable assignments and function calls. This translates into a slower sampling speed, with a sample every $13\mu\text{s}$, introducing error in the determination of the zero-crossing.

The second flaw is in the timing for the samples: using calls to a sleep function results in lower accuracy and control of the timing, since it is hard to account for the overhead caused by the interpreter.

These issues were quickly identified and the development of a C implementation turned into a high priority task.

3.2.2.2 C

Just as the previous MicroPython implementation, the microcontroller is first overclocked to 270 MHz. The serial stack is initialized, as well as the PWM. Before initializing the ADC, the internal clock source is changed from the typical internal 48 MHz clock to the system clock, running now at 270 MHz, with a frequency divider of 2. This allows the ADC clock to run at 135 MHz, with a sampling speed of approximately

1.4Msps, compared to the original 500ksps. Clock speeds over 135 MHz showed distortions in sample data around half of ADC's 12-bit range, which greatly affected accuracy. The ADC is also set to round-robin mode, reading one sample of the reference pin followed by one sample of the input pin. Finally, every sample is written to the ADC FIFO and transferred to a buffer on memory using the RP2040 DMA controller automatically.

Using this method, the sampling function can now start the ADC and let it run continuously until the memory buffer is full. Since the signal frequency and the sample resolution is previously known, the buffer size can be set to fit two periods: one from the reference, and one from the input. By setting the ADC to round-robin mode, the buffer should now contain the reference samples in the even indices, and the input samples in the odd indices. Through the use of modular arithmetic, the samples can be iterated over without fear of overflow, looping from the end of the buffer back to the start, enabling the determination of the zero-crossing much more accurately. The obtaining of the 90-degree separated samples also becomes trivial, since the buffer is of known size.

This approach eliminated the synchronization and timing issues and resulted in a sample being taken on average every $0.71\mu\text{s}$, 18 times faster than by using MicroPython. This optimization improved the measurement accuracy greatly, so the C implementation became the default one.

4 RESULTS

This chapter will discuss the results obtained using the digital subtraction LIA for capacitance measurement, as well as how the data was gathered.

4.1 EXPERIMENTAL SETUP

The RP2040 was powered by a laptop's internal battery, avoiding power supply noise and allowing serial communication with the device. A range of capacitances from 2.2 nF to 47 μ F was measured with a properly calibrated LCR meter and measured again using the LIA. Each capacitance value was measured 1024 times and the average was taken to calculate the results.

4.2 RESULTS AND DISCUSSION

Table 3 contains the capacitance measurement results achieved. The value measured with the LCR meter and the one measured with the LIA was used to calculate the absolute relative error. As expected from theory, the absolute error curve, present in Figure 13, exhibits a concave behavior. The optimal measurement value can be calculated using the theoretical formula seen previously. Given the system's reference frequency of $f = 500$ Hz, the series resistor $R_s = 10$ k Ω , and the ADC input impedance of approximately $R_{adc} = 1$ M Ω , the equivalent resistance R_{eq} seen by the DUT is:

$$R_{eq} = \frac{R_s \cdot R_{adc}}{R_s + R_{adc}} = \frac{10 \times 10^3 \cdot 1 \times 10^6}{10 \times 10^3 + 1 \times 10^6} \approx 9901 \Omega \quad (6)$$

Thus, the theoretical optimal capacitance point is:

$$C_{opt} = \frac{1}{2\pi f R_{eq}} = \frac{1}{2\pi \cdot 500 \cdot 9901} \approx 32.15 \text{ nF} \quad (7)$$

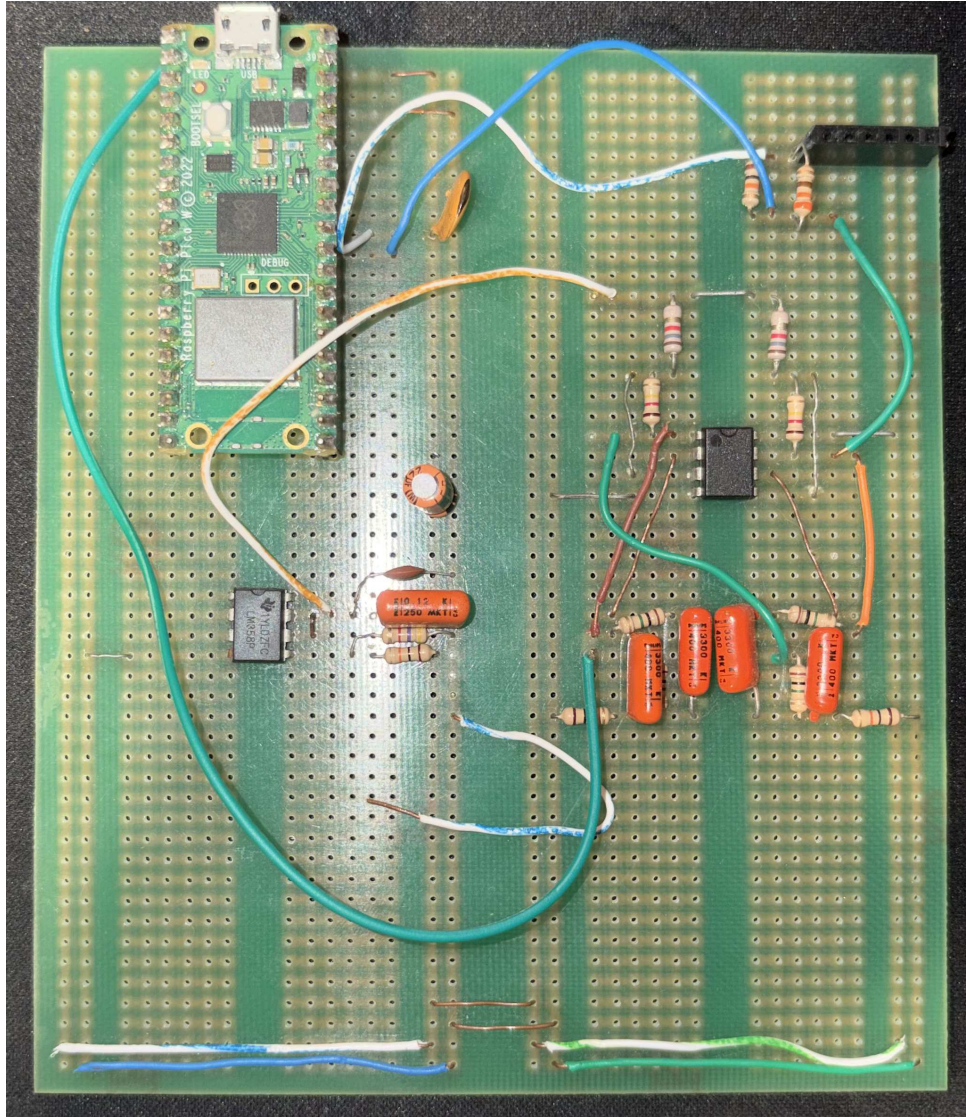
The valley in the measured points is accurately located at the measured capacitance closest to this theoretical 32 nF value. The curve is asymmetrical, indicating that the LIA fares worse in the lower range than the upper one.

The theory successfully predicted the measurement behavior, and the absolute relative error was acceptably low in a wide range of capacitances.

To validate the proposed theory, the value of R_s was changed from 10 k Ω to 680 Ω . Following the same theoretical prediction, the new equivalent resistance becomes $R_{eq} \approx 679.5 \Omega$, which results in a new optimal measuring point of:

$$C_{opt} = \frac{1}{2\pi \cdot 500 \cdot 679.5} \approx 468.4 \text{ nF} \quad (8)$$

Figure 12 – Photograph of the custom-designed board prototype, featuring the Raspberry Pi Pico W board and the dual-stage analog active filtering front-end.



Source: The author.

The capacitances were measured again using the LIA, and the results are shown in Table 4 and Figure 14. The theoretical measurement point once again coincides with the best accuracy point, but the whole range exhibits a high absolute relative error when compared to the original LIA. This degraded accuracy is caused by the lower value of R_s , which overloads the output of the filtering stage and causes voltage sag and distortion. For use in this range, it is recommended to change the reference frequency instead, or a more robust output to the filtering stage.

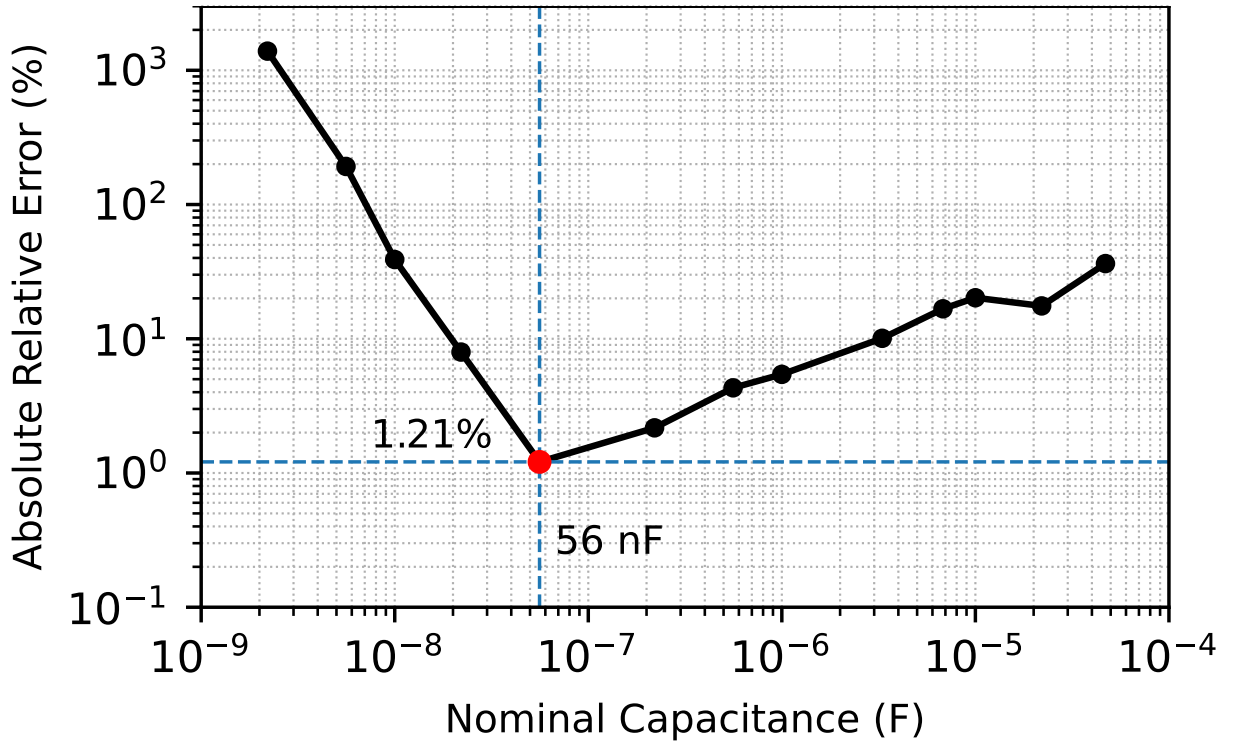
Although an absolute relative error exceeding 200% would be considered unacceptable from the point of view of a general-purpose commercial impedance meter, its impact must be contextualized within the scope of EIT image reconstruction. In EIT

Table 3 – Capacitance measurement results comparing the LIA against a LCR meter.

Nominal Value	Measured Value (LCR)	Measured Value (LIA)	Absolute Relative Error
2.2 nF	2.22 nF	33.1 nF	1389.09%
5.6 nF	5.9 nF	17.2 nF	192.19%
10 nF	10.6 nF	14.7 nF	38.92%
22 nF	22.6 nF	20.8 nF	7.96%
56 nF	56.3 nF	55.6 nF	1.21%
220 nF	213 nF	218 nF	2.17%
560 nF	552 nF	575 nF	4.31%
1 μ F	1.02 μ F	1.07 μ F	5.43%
3.3 μ F	3.0 μ F	3.3 μ F	10.08%
6.8 μ F	5.9 μ F	6.89 μ F	16.72%
10 μ F	8.6 μ F	10.3 μ F	20.21%
22 μ F	17.6 μ F	20.7 μ F	17.57%
47 μ F	65 μ F	41.4 μ F	36.31%

Source: The author.

Figure 13 – Absolute relative error curve for capacitance measurements.



Source: The author.

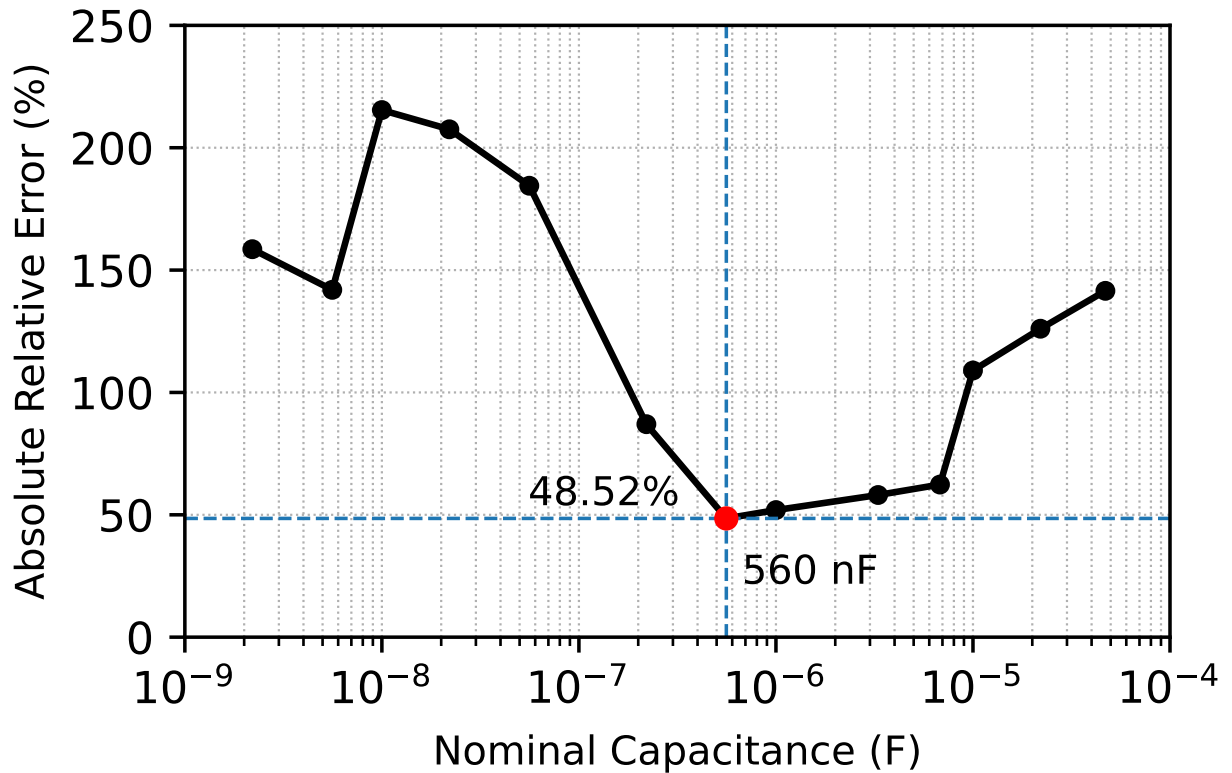
applications, image generation relies heavily on the relative variation of impedances over time or frequency, rather than their absolute static values. Furthermore, the observed error exhibits a highly systematic and predictable behavior across the measured range. Because this error is systematic, it can be computationally corrected through software calibration or normalization algorithms prior to the image reconstruction phase.

Table 4 – Capacitance measurement results of the modified range LIA.

Nominal Value	Measured Value (LCR)	Measured Value (LIA)	Absolute Relative Error
2.2 nF	2.22 nF	5.75 nF	158.54%
5.6 nF	5.9 nF	14.3 nF	141.93%
10 nF	10.6 nF	33.3 nF	215.39%
22 nF	22.6 nF	69.5 nF	207.53%
56 nF	56.3 nF	160 nF	184.47%
220 nF	213 nF	398 nF	87.03%
560 nF	552 nF	819 nF	48.52%
1 μ F	1.02 μ F	1.54 μ F	51.93%
3.3 μ F	3.0 μ F	4.74 μ F	58.09%
6.8 μ F	5.9 μ F	9.58 μ F	62.36%
10 μ F	8.6 μ F	18 μ F	108.97%
22 μ F	17.6 μ F	39.8 μ F	126.04%
47 μ F	65 μ F	157 μ F	141.52%

Source: The author.

Figure 14 – Absolute relative error curve for capacitance measurements of the modified LIA.



Source: The author.

5 CONCLUSION

5.1 LIMITATIONS

While the system successfully validated the design of the subtraction-based digital LIA using a microcontroller, the proof-of-concept was limited to a range not suitable for EIT applications. As for the limitations in the current design, the RP2040 ADC is a major bottleneck point: it has a low ENOB due to non-linearity peaks, which limits the voltage resolution, as well as sub-par sampling speed, requiring an overclock to be usable. The round-robin mechanism utilized is also a point of concern, since the reference voltage and the signal voltage are not sampled simultaneously, which introduces a phase delay between consecutive samples. The device was also very sensitive to power supply noise, yielding the best results only when it was powered from a battery.

5.2 ENHANCEMENT POSSIBILITIES

To scale the measuring range to the pF needed for EIT, a combination of increasing the reference frequency and the series resistor to the DUT can be applied. For an optimal measuring point of 1 pF, a frequency of 150 kHz and a resistor value of $1\text{M}\Omega$ could be used. However, for the calculations to be accurate, the input impedance of the ADC has to be significantly higher than the series resistor.

This brings up the next enhancement possibility: changing the ADC utilized for a higher resolution one, with two simultaneous sampling channels. It can be achieved either with an external ADC chip, or by choosing another microcontroller entirely. Going further, the system would benefit from a more precise sampling alignment. Dedicated hardware can be implemented, which would cause an interrupt to the microcontroller every 90° of the signal, guaranteeing almost zero phase delay in the sample acquisition.

A standalone power supply unit would also be an improvement, turning the device into a more reliable and independent option.

5.3 FINAL THOUGHTS

This work aimed to develop a low-cost, embedded impedance meter using a general-purpose microcontroller as an important step toward more accessible EIT applications. By implementing a subtraction-based digital Lock-In Amplifier on the RP2040 microcontroller, it was possible to bypass the need for expensive DSPs while maintaining a simple hardware architecture.

Quantitatively, the measurement results closely matched the theoretical predictions. The system was evaluated across a capacitance range from 2.2 nF to $47\text{ }\mu\text{F}$, demonstrating a concave error curve with its highest accuracy near the theoretically calculated 32 nF

optimal design point, where the relative error reached values as low as 1.21%.

Qualitatively, the transition from an interpreted MicroPython environment to a low-level C implementation utilizing DMA and round-robin ADC sampling significantly improved the system's timing behavior. This optimization proved the feasibility of high-speed synchronous $4f$ sampling on a low-cost ARM Cortex-M0+ architecture.

While the current setup operates effectively in the nanofarad and microfarad ranges, the enhancement possibilities highlighted above provide a clear path for future iteration. By addressing the ADC limitations and scaling the reference frequency, this architecture is promising for eventual application in the sub-picofarad range required for medical EIT.

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