LATIN AMERICAN CUBESAT WORKSHOP
SALVADOR, BR
OCTOBER 2024

The NASCERR Mission – An University/Private Sector Cooperation with Cubesat *

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Abstract

NASCERR stands for Radiation Hard Electronics Nanosatellite (Nanosatélite Com Eletrônica Robusta à Radiação, in Portuguese). It was proposed and accepted in a call issued by the Brazilian National Research Council – CNPq for Brazilian universities and public research institutes for the development of CubeSats and their equipment/subsystems. One of the requirements of the call was the mandatory participation of private companies in the proposal and development of the CubeSat. Qualification testing at these levels will be performed at the Integration and Testing Lab (LIT) of the National Institute for Space Research (INPE). The CubeSat will communicate with ram frequencies and its coordination is being requested by IARU. It is a 2U cubesat where 1U holds the bus and the other U is for the payloads. NASCERR, as required by the CNPq call, is a cooperation between the university and Brazilian companies. The attitude determination and control subsystem, the solar panels, the electronic power subsystem, the structure, and the onboard and ground software were developed by these companies, while the onboard computer, the transceiver, and the onboard antenna set were imported. All the subsystems were already either delivered or contracted with delivery within the coming six months. Students from UFC and UFSM participate in the project with scholarships from

*Acknowledgment: This study was financed in part by CNPq and partially supported by Fundação Cearense de Apoio ao Desenvolvimento Científico e Tecnológico (FUNCAP) under grant ITR-0214-00041.01.00/23.

its budget. Only a proto-flight model will be developed. Qualification testing at these levels will be performed at the Integration and Testing Lab (LIT) of the National Institute for Space Research (INPE). The CubeSat will communicate with ham frequencies and its coordination is being requested to IARU. This is the first CubeSat mission managed and developed by UFC. The mission was presented to the Brazilian Space Agency and its Space Mission Selection and Acceptance Process – ProSAME for habilitation in the official space mission portfolio of the country. The schedule of the call requests the cubesat be ready for delivery to launch by the end of 2025. Launching and ground station and operation are not included in the CNPq provided budget. The NASCERR launch is planned to 2026. This is the first CubeSat mission managed and developed by UFC. The paper presents the CubeSat's operating range, electrical schematics, and other technical details.

Keywords: radiation hardening, public/private cooperation, cubesat use, experiments.

1 Introduction

This project results from a public call (CNPq/MCTI/FNDCT Nº 19/2022) from the National Council for Research - CNPq to develop cubesat space missions. It required that Brazilian research groups team up with Brazilian companies for its development. The proposal put together different research and experienced groups in electronics and computer systems applied to space, with new technological companies dedicated mostly to space projects. It involved three states in Brazil distant hundreds of kilometers from each other in the country's South, Southeast, and Northeast. And one French group associated with the two research groups. NASCERR (Radhard Electronic Nanosatellite) [1] is a 2U technological Cubesat with 1U dedicated to the platform and the other U to the experiments. The platform is modular and used in the nanoMIRAX mission[1], from the National Institute for Space Research – INPE like LECX[2] mission.

The NASCERR mission is the continuation of the work done by these research groups in other Brazilian CubeSats and an opportunity to test in space other components and equipment developed by them with radiation hardening to improve the reliability of CubeSats and their useful life in space.

2 Payloads

The NASCERR project consists of four experiments: (i) ROBOC – Robust On-Board Computer; (ii) Radiation Hard Error-Correcting Code; (iii) Implementations of Machine Learning (ML) Algorithms; and (iv) an amateur point-to-point radio communication software, now in its third version, after the first two flew in other Brazilian cubesats. Of the four experiments, the first three involve hardware and software integration, while the last is predominantly a software experiment. The overall architecture of Nascerr can be seen in Figure 1

2.1 ROBOC – Robust On-Board Computer

ROBOC aims to study and validate dynamic error correction code (ECC) algorithms

[1] http://www.das.inpe.br/publicacoes/pdfs/braga_mirax.pdf

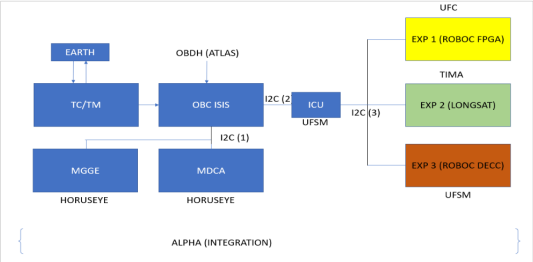

Figure 1: NASCERR Architecture.

for protecting data in external memory. The NASCERR implementation uses a SmartFusion2 025 FPGA from Microsemi. An RTL was developed in SystemVerilog to implement the described ECC models, ensuring that all operations requested by the processor to the memory are handled transparently. This means that, when reading from or writing to memory, the processor is unaware that the data is passing through the FPGA, which acts as a "Man-in-the-Middle." The entire communication process happens invisibly to the processor, maintaining system performance without any interference.

As illustrated in Figure 2, the FPGA intermediates the communication between the main processor and the SRAM. Every time the processor writes data, the FPGA encodes it using an ECC, generating redundant bits. The DATA + redundancy set is then stored in the SRAM. When the data is read again, the FPGA reads the set, decodes the data using the ECC, corrects any detected errors, and then passes the corrected data back to the processor. This process occurs without introducing additional latency, as the operation is conducted using only combinational circuits, ensuring that the MATM (Man-in-the-Middle) block does not degrade the read and write performance to external memory. The ECC mechanism implemented in NASCERR is not only responsible for detecting errors but also for correcting them, working to prevent information loss by correcting errors according to the capabilities of each ECC algorithm.

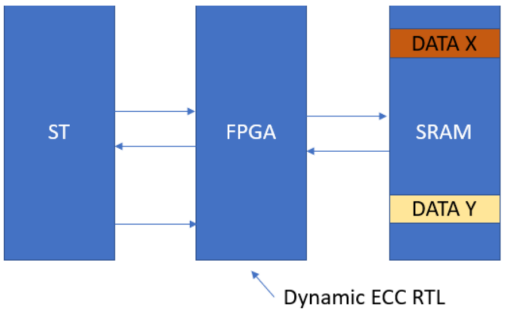

Figure 2: Dynamic ECC protection in SRAM

The MATM block implemented on the FPGA supports up to four modes of operation: (i) without ECC; (ii) MRSC; (iii) eMRSC; and (iv) TBEC-RSC.

- he MRSC (Matrix Region Selection Code) is an efficient and low-cost error correction code (ECC) for microcontroller units (MCUs) that uses a 2-D parity encoding scheme. It divides data bits into regions and utilizes logic equations to pinpoint error locations, implementing a region selection algorithm (RSA). This code corrects up to two-bit errors per data word and handles several adjacent error patterns with lower synthesis costs compared to other robust ECCs.

- The eMRSC (Extended MRSC) extends the original 16-bit version of the MRSC to a new 32-bit format. It offers two code versions: one with a lower increase in redundancy and another with higher

correction capability. The eMRSC introduces a new data matrix region scheme that reduces the number of redundant bits generated, providing a tradeoff between area, power overhead, and reliability.

- The TBEC-RSC (Triple Burst Error Corrector based on Region Selection Code) is a 2-D ECC scheme mapped onto a 1-D physical structure. It builds on the MRSC algorithm but with modifications to enhance its error correction efficacy, particularly for burst errors. The TBEC-RSC is designed to correct 100% of triple burst errors and more than 40% of eight-bit burst errors. The code has been tested with 16-bit data, but it can be easily extended to larger base-2 data words, such as 64 bits.

Each of the four modes of operation of the MATM block can function either in a static or dynamic manner. In static mode, the experiment's software, running on the main processor (ST Processor), selects the protection mode to be used. In dynamic mode, the MATM block automatically chooses the most appropriate mode based on pre-set criteria. For instance, if the number of errors within a given time window exceeds a certain threshold, the algorithm with the highest correction capability will be selected. Otherwise, an algorithm with lower correction capability, which uses less redundancy, will be chosen. It is important to note that algorithms with higher correction capacity require more redundant bits, which increases data overhead in the SRAM. Therefore, memory efficiency criteria can also be selected, resulting in data protection that is tailored to system needs.

2.2 Radiation Hard Error-Correcting Code

2.2.1 Radiation Problem in Integrated Circuits

Over the past decade, TID[2] radiation [3] hardening in commercial CMOS technology [4] [5] has been evolving rapidly due to the continuous reduction of gate oxide thickness. However, there is no guarantee that the same level of radiation tolerance among different manufacturers will work for the same technology node, since radiation hardening is not a factory-monitored parameter. In addition, TID effects for a given CMOS technology are closely linked to the exact gate oxide thickness, the imperfection levels in the Si02 insulation region, etc. Unfortunately, these parameters are usually not modeled in CMOS devices, which makes predicting the radiation impact of a CMOS circuit very difficult. They are often not disclosed by the manufacturer, which complicates the modeling of radiation effects at the semiconductor level. Therefore, in addition to choosing a more advanced CMOS technology for radiation-hardened designs, RHBD techniques [6] are also required in the circuit to ensure its reliability and performance even under extreme radiation levels. RHBD techniques can be used throughout the design phase of a CMOS chip. In general, they can be separated into four hierarchical levels: system level, circuit level, device level, and layout level. See

[2]TID (Total Ionizing Dose) effects refer to the cumulative damage caused to electronic devices by prolonged exposure to ionizing radiation, impacting their performance and reliability over time.

Figure 3.

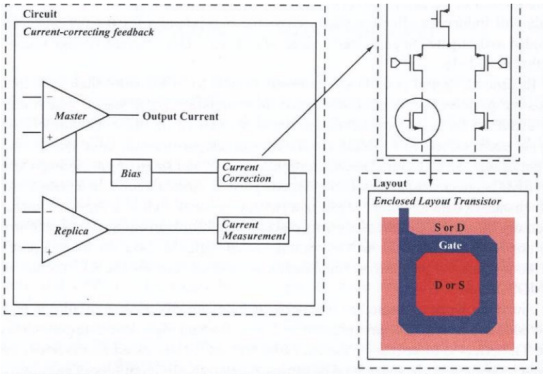

Figure 3: Dynamic ECC protection in SRAM

A) System Level

RHBD at the system level is the most effective way to ensure radiation hardening of an electronic device. When an electronic system is required to perform certain functions in a radiation environment, the first consideration should be to choose a system structure that provides the highest radiation tolerance. A good example is the selection of an analog-to-digital converter (ADC) suitable for radiation-tolerant applications [7]. ADCs have various architectures, such as flash, pipeline, successive approximation (SAR), dual-slope integration, and Sigma-Delta. For a given specification in terms of resolution, power consumption, and dynamic range, all these types of ADCs may be suitable. However, they have different radiation tolerance levels. Commercial ADCs from different manufacturers were compared to verify their performance against gamma radiation. Interestingly, a tested Sigma-Delta ADC (ADS 1210) showed a higher level of radiation tolerance (about 25 kGy) when an external reference voltage is used for it (if the internal bandgap circuit is used to provide a reference voltage, the converter will fail after reaching 200Gy). Flash ADCs are more vulnerable to the TID effect.

b) Circuit Level

Although there is adequate radiation tolerance at the system architecture level, radiation-induced failures can occur at the circuit level, as in the case of the bandgap circuit of the Sigma-Delta ADC. Therefore, radiation-sensitive components throughout the system must be identified and ensured that they can achieve the required radiation tolerance level. Due to this, RHBD techniques must be applied at the circuit level. As an example, an RHBD approach is presented at the circuit level to improve the radiation hardening of a CMOS VCSEL driver. The driver is implemented in 0.7µm CMOS technology. Radiation induces changes in the threshold voltage of the MOS transistor in the driver, causing a change in the VCSEL current. This is addressed with a current feedback mechanism for correction, as shown in Figure 4. The purpose of this feedback circuit is to maintain a constant current through the VCSEL. An extra replica of the driver is employed to reproduce the same current. The replica and main drivers are identical devices, so any performance changes in the main driver due to the effects of TID will be reflected in the replica device as well. A control loop continuously monitors this process to keep the output current constant.

c) Device Level

RHBD at the device level addresses radiation hardening issues by choosing appropriate transistor types and geometries (width and length) in the implementation of CMOS circuits. For example, in older CMOS technologies, PMOS transistors are preferred for radiation-tolerant designs, since varying the threshold voltage causes only performance changes rather than functional failures. Furthermore, TID effects

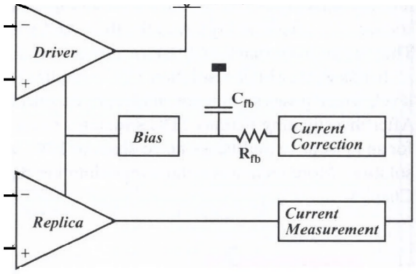

Figure 4: ELT transistor and its geometric parameters

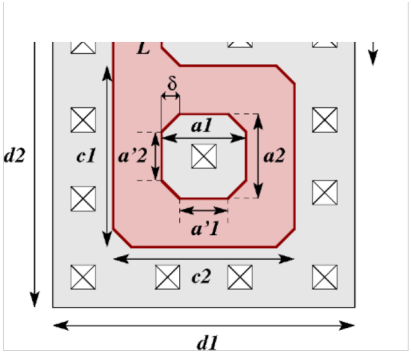

Figure 5: ELT transistor and its geometric parameters

in a transistor have dependencies on the geometry in which it is designed.

d) Layout Level

RHBD techniques at the layout level have proven to be very effective in eliminating the latch-up effect and preventing radiation-induced leakage currents. One example is the Enclosed Layout Transistor (ELT) technique for very high radiation hardening applications. An ELT has a closed gate design, which separates the drain and source regions of a CMOS transistor. An ELT is shown in Fig 5. This design eliminates the parasitic transistors that were originally located on two edges of a conventional CMOS device. The radiation-induced leakage current of the MOS transistor is greatly reduced. The main drawbacks of the ELT transistor are increased area and greater difficulty in electrical modeling.

2.2.2 Radiation Hard Cell Library

The Santa Maria Design House (SMDH) project linked to the Federal University of Santa Maria has developed a radiation hard digital cell library (SMDH-RH) using RHBD techniques for the standard 180nm XFAB CMOS technology. The library is presented in 5 types with 24 cells for each library type, as shown below. RH (Radiation Hard) library type with 24 cells each:

- library typical voltage: 1.8v; temperature: 25c;
- slow library with voltage: 1.62v; temperature: -55c;
- slow library with voltage: 1.62v; temperature: 125c;
- fast library with voltage: 1.98v; temperature: -55c;
- fast library with voltage: 1.8v; temperature: 125c

Cells contained in the libraries are the following: ANTENNACELLRH3: "protection cell against antenna effects (net charge) at manufacture, PIMP diode in NWELL", see Table 1 and Figure 6.

2.2.3 Error Correction Code (ECC)

In computing, telecommunications, information theory, and coding theory, an Error Correction Code (ECC) is a software-implemented

Table 1: Code Pin Antenna

BURHX1: "Buffer X1"	BURHX2: "Buffer X2"
BURHX4: "Buffer X4"	DECAPRH3: "DECAP cell"
DFFRHRSX1: "negedge D-Flip-Flop with Reset and Set"	DFRRHX1: "posegedge D-Flip-Flop"
DLHRHX1: "high active transparent D-latch"	DLYRH2X1: "Delay cell, typical 1ns"
EORH2X1: "2-Input XOR"	FEEDRH1: "FEED cell"
INRHX1: "Invert"	INRHX2: "Invert"
INRHX4: "Invert"	LOGIC0RH: "Constant logic 0"
LOGIC1RH: "Constant logic 1"	MAJRH3X1: "3-Inputs Majority cell"
MURH2X1: "2:1 Multiplexer"	NARH2X1: "2-Input NAND"
NARH3X1: "3-Input NAND"	NORH2X1: "2-Input NOR"
NORH3X1: "3-Input NOR";	SDFRRHX1: "posegedge D-Flip-Flop with Scan"
XDLHRHX1: "SEE hardened high active transparent D-latch"	

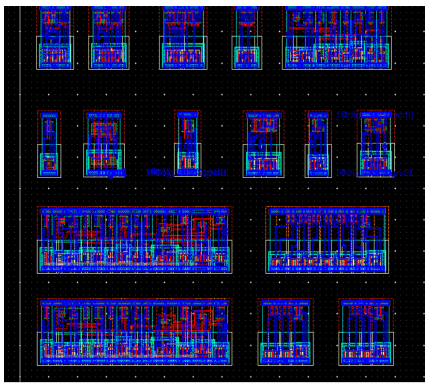

Figure 6: Cell Design (XFAB 180nm Technology)

technique used to control data errors in unreliable or noisy communication channels. This technique can be successfully used in the space environment. It is important to consider that systems need to be prepared for errors arising from radiation effects in the environment. The disturbances that occur can be detected and even corrected by ECCs depending on how they occur. The inversion of one or more bits can occur during transmission or storage within the memory. If the error is detected during transmission, but there is no way to correct it, simply retransmit. However, if data inconsistency is detected during memory reading, there is a need for correction, since there is no way to extract the information again from its source. One of the techniques used to protect memories applied in satellite OBCs is the use of ECC. The integrated circuit that performs the interface between the onboard computer and the memory can be an FPGA or a specific circuit prototyped for this purpose. An ECC is the circuit to be analyzed aiming at the development of a specific integrated circuit (ASIC) and robust to radiation since radiation-tolerant FPGAs are not used in nanosatellites. Radiation-robust FPGAs have a very high cost.

2.3 Implementations of ML Algorithms

In the advent of new generations of electric self-driving cars, autonomous drones, airplanes, and satellites, artificial intelligence (AI) applications, and machine learning (ML) algorithms have been rising in popularity thanks to the constant technological evolution of electronic computing systems, autonomous taking decisions in situations that are usually of high risk in case of failure. Those applications necessarily face harsh environmental conditions, being

considered safety-critical because unexpected failures in their systems may lead them to catastrophic situations such as a loss of navigation control, harming users and people around. Hence, computing systems and their sensors in safety-critical applications must safely and reliably operate under environmental perturbations by mitigating their harmful effects and minimizing risks for human beings and related surroundings, even under simple impacts of single subatomic particles released by radiation effects of cosmic rays coming from space to ground levels. In this context, several scientific challenges are raised. For instance, how reliable to radiation effects are the more and more complex firmware embedded in applications such as nanosatellites that usually are built with low-cost commercial-off-the-shelf (COTS) components? The Université Grenoble Alpes (UGA/TIMA) will design, implement, and test a nanosatellite payload board based on COTS components. The scientific goals of the UGA payload board are to assess the reliability of ML algorithms as well as attitude estimation (AE) algorithms facing low Earth orbit (LEO) radiation effects, correlating spaceflight-level results with data collected in ground-level accelerated radiation tests.

The actions for specifying, designing, implementing, testing, and reporting the UGA payload board were organized into 17 milestones/deliverables. The UGA payload board will be integrated into the Brazilian nanosatellite "NASCERR" planned to be launched by our international partners in 2026. The actions will be executed by 4 interns, 3 PhD students, a senior engineer, and a professor. The procedures for performing the UGA payload board's scientific experiments and transmitting data from space to ground will be aligned with the University of Santa Maria (UFSM) team. Essentially, the on-board computing systems will be composed of software (firmware), ML and AE algorithms, and COTS components. One of the deliverables will be an interface control document (ICD) following the standards of space agencies.

2.4 Amateur point-to-point radio communication software

This is a point-to-point amateur radio communication software. It is an advanced version of the previous one that flew in ITASAT-1. The experiment consists of reception, storage, and retransmission of short (64 bytes maximum) text messages following the format: Origin|Locator|Destiny|Message, where the character "|" separates each field, and:

- Origin: Callsign of transmitter station (6 characters maximum);
- Locator: QTH Locator (6 characters maximum);
- Destiny: Callsign of receiver station (6 characters maximum).

To store a message, the satellite includes a date-hour field with the satellite hour such as: *Date-hour*|*Origin*|*Locator*|*Destiny*|*Message*. A station can request the last 20 messages for a certain destiny. The messages are stored in the memory of the satellite during a time interval and are deleted after this period. The experiment does not require any additional hardware to the platform or the other payloads.

3 Plataform

The platform for the NASCERR cubesat will have a 2U structure (10cm x 10cm x 20cm)

with 1U made available for the payloads described in the previous item and 1U made available for the service subsystems. Among these, five are developments made by national companies in the country for the project, and three are imported from companies that produce them abroad. Two of these can also be developed by national companies, but to mitigate further risks to the mission, they will be imported from companies that already produce them with significant space heritage.

3.1 Power Subsystem (MGGE)

Performs the following functions:

- Optimizes the transfer of the energy captured by the solar panels;
- Controls the distribution of energy to the system;
- Manages the generation, storage, and consumption of energy by the system;
- Makes all information available for processing by the main on-board system;
- Performs battery protection (voltage and current) by hardware and software;
- Allows the configuration of parameters inherent to battery charging and energy distribution;
- Controls the temperature of batteries by hardware and software.

The energy conversion of the solar panels is carried out by BOOST converters (voltage lifters) with MPPT (Maximum Power Point Tracking) operating mode. Each converter with two inputs for solar panels. It uses the MPPT operation to maximize the use of the energy that the panels can generate when the system needs to recharge the batteries and does not consume the full capacity of the panels. In this case, all excess consumption is directed to storage. The circuit operates in two MPPT modes: constant voltage and maximum power

Batteries are Lithium-ion with a total supply of 7.56 +/-0.2V and operating temperature between -20 and + 50 degrees Celsius. The circuit allows the change of the working voltage of the panel, around a default value, so that, according to previous configuration, it can operate in any mode. The working voltage value can be changed to constant voltage mode (microcontrol dependent) by software. When there is no destination for the surplus energy that the panels can generate, the converter operates in constant voltage output mode, extracting from the panels only what the system needs.

Control is made with an Atmel microcontroller, ARM 32bits, M4, from the SAMG55 family, supported by several external function blocks, with high performance and low consumption. Operating frequency around 24MHz for minimum consumption, with external crystal for clock stability. Internal RTC for "time stamping" of operational analysis and availability of last event window with occurrence accuracy. External flash memory (IC2) with a capacity of 128kbytes, with an SPI interface.

3.2 Attitude Determination and Control Subsystem (MDCA)

It uses an Atmel microcontroller, ARM 32bits, M7, from the SAME70 family, supported by several external functional blocks, high performance with moderate consumption,

being able to operate up to 300MHz of internal clock (use of the lowest allowable clock for processing for minimum consumption). It can completely turn off the microcontroller without loss of the onboard time reference. Memory capacity for internal flash code with at least 2 Mbytes and for work (internal RAM) at least 384 kbytes. Forecast for NOR flash with a capacity of 16 Mbytes and for two units of FRAM memories (SPI interface) with a capacity of 512 kBytes each, totaling 1 Mbyte of resource (IC2 and IC3). Interface for SDCard available on the microcontroller using external 8 kbyte E2prom (I2C interface). It communicates with the subsystem's internal attitude-sensing devices, through an SPI bus with several selector lines and an I2C Master bus, and with external devices or systems via I2C Slave bus, SPI bus, two asynchronous serial interfaces, one USB interface, and one CAN interface. Firmware load is done via the JTAG interface, accessed by JTAG connector.

It uses as attitude sensors a three-axis magnetometer and gyroscopes, both of the MEMS type (for reading in eclipse), and solar sensors, these placed in the CubeSat panels. As actuators, three torque coils, one air core, and two ferrous cores, are arranged on the two sides of the subsystem board. The air core coil and the ferrous core coils are mounted on opposite faces on the subsystem board, completing the control trihedron. The electronics are assembled in the space enclosed by the torque coils on the board. Configuration does not require the solar panels to have magnetic actuators and allows the determination of the attitude throughout the entire orbit.

It has a GPS receiver for onboard orbit determination. GPS antenna placed on the top face of the CubeSat. Orbit is obtained autonomously on board, without the need, for this definition, to receive the TLEs (two lines elements) obtained by the earth station via the internet through NORAD. The data read on board, from the platform and the payload, can be associated on board with the point in the orbit at which it was obtained and transmitted to the ground with this identification.

3.3 Transceiver, onboard computer and onboard antenna set

These three subsystems were imported from ISISpace for the reasons explained above. The transceptor was imported from ISISpace. It is a VHF uplink/UHF downlink full duplex transceiver that can operate in commercial amateur radio bands in the VHF/UHF frequency spectrum with flexibility of transmit rate and frequency change during flight. TMTC and Beacon are on the same board.

The data management module (OBDH) has an MSP430 20MHz ultra-low power microcontroller with I2C, UART, and SPI interfaces. With antenna release control and 2G bytes flash memory. It performs housekeeping operations and allows the management of payloads. Electronic components with flight heritage and with communication with the other modules. Includes the operating software and library.

The antenna system contains four ribbon spring antennas up to 55 cm long. The system has a thermal knife composed of a wire and two redundant heating elements per tape. RF phasing/BalUn circuits join the antennas in a spool configuration. Depending on the configuration, one or two radios in the CubeSat can connect to the antenna system via miniature RF connectors. The top face of the antenna system can accommodate a two-cell

solar panel and can be customized to accommodate sensors or other systems that protrude outward. The antenna is compatible with any UHF and/or VHF radio system. It can be mounted on all the frames of the main suppliers of CubeSats frames on the market. For custom-made structures, that follow the standard CubeSat mechanical envelope, assembly is also possible.

3.4 Structure

2U aerospace aluminum alloy structure in 7075-T6 alloy with qualified corrosion protection for the environmental conditions of space and vibration at launch. Surface treatment (black sulfuric anodizing 16 to 20 microns); Worm shafts and screws in 304 stainless steel. Kill switch mechanisms to activate the opening of the on-board antennas in stainless steel 316 and aerospace aluminum 7075-T6. External dimensions (width X length X height) of 100 X 100 X 227 millimeters. Weight up to 400 grams.

3.5 Software

- Management of onboard data for the NASCERR flight model platform and communication with the platform's subsystems and payloads.
- Mission application software for acquiring and processing telemetry from the satellite and for formatting and sending telecommands to the satellite
- Integration of onboard software and mission application software.
- On-board computer interfaces and platform subsystems.
- On-board management software in binary format (installable).

3.6 Solar panels

Solar Panels for 2U Cubesat, in +-X, Y and Z with temperature sensor and solar with four solar cells assembly (SCA), except in Z where there are 2 SCA in each. Triple-junction solar cells, InGaP/GaAs/Ge, with spatial qualification by ECSS E ST20-08C standard for low orbit, mass between 80-90 mg/cm2 and area between 26 and 27 cm2. Efficiency greater than 29%, external by-pass protection diode and high radiation resistance.

4 Coordination of Attendance, Launch and Operation

The CubeSat will operate with amateur radio frequency in VHF (145.9 MHz) for uplink and UHF (436.5 MHz) for downlink. The main ground station will be in the campus of the University of Ceará – UFC. The auxiliary ground station will be located and the National Space Research Northeast Regional Center – INPE/CRN, in the city of Natal, RN. Both stations will be able both to send commands and receive telemetry from NASCERR, from the payloads and the platform performance data. Amateur radio stations around the globe will also be able to receive telemetry data and so track the CubeSat in its entire orbit. Therefore being an important auxiliary element to provide information about its health, performance, and operation planning.

The launch will be piggyback, All the experiments on board are independent of the orbital

plane inclination angle. Thus, NASCERR may be suited to be launched from the Alcantara Launching Center, in Brazil, in low-inclination planes, if this launch site is available.

5 Conclusion

All the subsystems for the NASCERR platform are done and delivered. Those developed in Brazil were qualified at the Integration and Testing Laboratory of the National Institute for Space Research – LIT/INPE. Those imported have many hours in space. The payloads are being developed and are continuation or spin-offs from other projects and research. Due to their different requirements and complexities, they have different conclusion schedules but all are feasible within the mission schedule. This is mostly due to the foundry process of the hardware and the very tight schedule and lead time of the companies abroad that will be hired to do this process. Also, two payloads are interdependent and have to be developed partially in sequence. The mission software, both for on board and for the ground station are being developed with the participation of students from the Federal University of Ceará (UFC). The project sponsors these students. There are different options for the ground station at the UFC campus that are being studied.

NASCERR will be delivered for launch in 2025. Its launch is forecasted to 2026.

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