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An Endured On-Board Computer for Small Satellites, using Low Cost COTS Combined with Radiation-Hardened Devices and Fault-Tolerance Strategies

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Abstract

Space radiation is harmful to electronic devices, leading to transient and permanent faults in the on-board systems of a satellite. In traditional satellites, radiation-hardened (rad-hard) devices are employed to mitigate the radiation effects on the electronics. However, in Cubesat based missions, a solution based entirely on rad-hard components is not always feasible due to its high costs, and the limited availability of this type of devices. Therefore, in low-budget small satellite missions, alternative development approaches are needed to mitigate the radiation effects on their systems. One such approach is the combination of rad-hard devices and commercial-off-the-shelf (COTS) components in order to create a cost-effective, fault-tolerant system for use in the satellite's subsystems and payloads. This paper describes the design of a processing module for Cubesats, employing a rad-hard SoC FPGA device combined with COTS components. Additionally, it outlines strategies for the mitigation of radiation effects, resulting in a new fault-tolerant computing platform for

CubeSat missions. The work shares decisions, considerations, and studies made during the ongoing project. Furthermore, the research and development activities are conducted in the context of a cooperation between Spacelab at the Federal University of Santa Catarina (UFSC), Brazil and the European Space Agency (ESA), The Netherlands. The anticipated outcome is the expansion of possibilities for CubeSat missions allowing, for instance, deep-space missions. Initially, the proposed processing system is expected to be used as the on-board computer of an endured version of the FloripaSat platform.

1 Introduction

CubeSats typically use only COTS components, that is, instead of using specific and customized components for each mission, components commonly used in the industry and available in large quantities are employed. This characteristic increases development speed and reduces costs, but it brings new challenges to satellite reliability since COTS are not typically designed for applications in space environments where they are exposed to radiation and vacuum, and their behavior may not be predictable or reliable.

Several strategies have been developed and employed in CubeSats to overcome radioactive effects and increase the survivability of their electronic components. Components that use radiation techniques or strategies are known as "radiation-hardened" or "rad-hard." Currently, there are several techniques to mitigate the effects of radiation, ranging from manufacturing processes to printed circuit board design. These techniques are not centralized and are usually grouped by research lines in certain areas, such as microelectronics and systems engineering.

Currently, we have commercially available radiation-resistant components, such as power converters and even FPGAs. However, besides the fact that these components can cost up to twenty times more [1], this market is focused in the United States, which, due to military potential, restricts external sales through ITAR and EAR regulations [2].

The Space Systems Research Laboratory at UFSC, SpaceLab, in partnership with ESA, has developed payloads (CubeSat modules that carry the experiment or final application of the CubeSat, i.e., the mission's objective) for CubeSats using FPGAs and SoC FPGAs rad-hard from the French startup NanoXplore. Two payloads have been developed for use in missions, Payload-X and Payload-XL, which will be launched in the GOLDS-UFSC and Cassini missions.

This work aims to describe the architecture of a fault-tolerant computational platform developed to be used in CubeSat missions using the NanoXplore NG-ULTRA SoC FPGA along with COTS and radiation mitigation techniques.

2 Radiation on Electronic Devices

Electronic components are sensitive to radiation effects, especially semiconductors. In a space environment, there are highly energetic particles (heavy ions, protons, and electrons). When these particles collide with electronic components, they generate various effects, ranging from performance loss and abrupt shutdowns to catastrophic failures. When an en-

ergetic particle collides with a semiconductor, part of the particle's energy is transferred to the electronic component. This transferred energy is called LET, which is expressed as the energy deposited per unit length along the path of the ionizing particle.

The radiation effects resulting from this energy transferred by the energetic particle to the semiconductor device can be divided into transient effects and long-term effects.

Transient effects can occur in electronic components through SEEs or due to high radiation doses. Their susceptibility increases as the device size decreases and as circuit signal speeds increase [3]. The effects of SEE are so impactful in small-scale technologies that they are becoming an issue in terrestrial applications with sub-$65nm$ CMOS technology [4].

Exposure to a radioactive environment causes progressive degradation of the component in a stable and predictable manner. These effects tend to produce long-term changes in the operational characteristics of devices. Long-term radiation will cause the threshold voltage curve to shift and generate leakage currents. The first effect is more relevant for larger transistors, and the latter for smaller devices [5].

3 Component selection criteria

In Fig. 1, a suggested classification criterion for TRL, based on [6] is presented, developed for the context of CubeSat submodules. According to this criterion, it is mandatory that the component has at least TRL-3. Tests in a space or similar environment may include flight heritage, radiation effects testing, or tests in a thermal vacuum chamber.

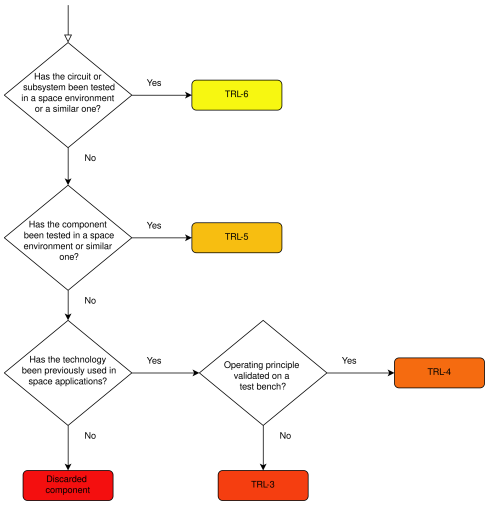


Figure 1: TRL classification criteria

In [7], recommended derating factors for various component families are provided. These factors represent the percentage difference between, for example, the absolute maximum voltage specified in the datasheet and the application voltage. Table 1 presents a compilation of the most relevant factors for CubeSat module design.

4 Design

Since this is a module following CubeSat standards (i.e., an area of $10cm$ x $10cm$ and power constraints) [8], in some cases, solutions were prioritized that were not necessarily the most robust but provided a good balance between reliability, space, and power consumption.

To parallelize the development of firmware applications while the hardware is being developed, the goal was to maintain compatibility

Table 1: Derating techniques grouped by component categories.

Component group	**Derating (load ratio or limit)**	**Factor**
Capacitors (Ceramic Chip)	Voltage	60%
Resistors (Chip)	Voltage	80%
Resistors (Chip)	Power (rms)	50%
Non-volatile memories	Supply voltage	$\pm$ 5%
Switching regulators	Output current	80%
Switching regulators	Maximum input voltage	90%
MOSFET	Power dissipation	65%
MOSFET	Voltage (VDS)	80%
MOSFET	Drain current	75%

with the DevKit version 1.1 [9], especially in the parts of the SoC responsible for storing and loading the bitstream. By reusing parts of the DevKit hardware, we ensure the functionality of the circuit, raising the reliability level to TRL-4 and enabling compatibility with the development and debugging tools provided by NanoXplore.

Since this computational platform is not developed for a specific mission, it is not possible to define an orbit and, consequently, a LET spectrum to select components based on their cross-section. Therefore, the performance of the central component of the module, the NG-ULTRA SoC FPGA, will be used as a reference, and components with similar performance in terms of radiation tolerance will be chosen. In terms of SEE, the NG-ULTRA is immune to up to $65\frac{MeV \cdot cm^2}{mg}$, and in terms of TID, it withstands up to $50krads$ [10].

For the selection of COTS, derating factors were used, as well as the TRL criteria (Section 3).

4.1 Processing System

The architecture of the SoC is available in [11]. A specific BSCAN bank is provided for configuration. In it, it is possible to define, through exclusive pins: operation mode, bitstream loading configurations, reset pins, status reading, among others.

To facilitate the configuration of the FPGA SoC, I^2C converters capable of interfacing with the configuration pins of the BSCAN were used. Additionally, there is a JTAG interface for configuring the internal registers and isolated pins for configuring the FPGA mode. These resources are made available on a dedicated connector to be compatible with NanoXplore tools.

The BSCAN also features a UART interface for debugging. This interface is connected to one of the channels of a Silicon Labs CP2105-F01-GM converter for RS-485 and is externalized.

To store the bitstream intended for loading, four Infineon S25FL512 NOR memories were selected. The memories can be configured for sequential reading or, using only three, in TMR mode. Additionally, it is possible to load the bitstream directly via SpaceWire, which is externalized.

For the four R-52 processors in the PS, six IS43DR16640C DDR2 memories from ISSI are available. These are connected to the SoC's DDR controller. This controller provides protection to the DDR2 memory devices using Reed-Solomon coding and can tolerate up to one faulty device.

With the exception of the memories, these circuits are used only for configuration and debugging and are therefore not designed to be used in a space environment. Thus, a connector capable of disconnecting them from

the power bus has been added. The RS-485 converter is powered directly by the external connector and therefore poses no risk to the power bus. The memories were chosen with compatibility with the DevKit in mind. In the case of the bitstream memories, NanoXplore recommends specific part numbers to ensure compatibility with their programming tools, and the DDR2 memories were selected to allow the reuse of validated circuits from the DevKit, which allows us to consider a TRL-4 level for both types of memory.

4.2 Processing Logic

The NG-ULTRA features 4 direct banks (24 I/O per bank), 10 complex banks (34 I/O per bank), 8 HSSL banks, and 7 PLL clock generators.

The 4 direct banks and 2 complex banks were used. The HSSL banks and clock generators were not utilized as they were deemed unnecessary within the scope of CubeSats. The following subsections detail the components connected to the PL.

4.2.1 Memories

For data storage, memories were selected to provide different degrees of the trade-off between reliability, capacity, and speed to enhance application possibilities in various mission types.

A NAND *flash* memory of the eMMC type was chosen for the storage of Linux-based operating systems and mass data storage, providing high capacity and speed. The Kingston EMMC128-IY29-5B111 memory, with $128GB$, features an eMMC 5.1 HS400 interface allowing up to $400MB/s$. This memory does not have radiation testing, flight heritage, or validation in other projects, thus it does not offer high reliability; however, this type of memory technology has been employed in CubeSat modules, as in [12], and we can assign it a TRL-3 level.

For critical data, a MRAM EM064LXQADG13IS1T from Everspin, with $64Mb$, operating at $133MHz$ and featuring SPI interface up to Octal SPI, is provided. This specific memory has not yet been tested against radiation effects or in other CubeSat applications, but as described in [13], its immunity against radiation effects is high, ensuring a TRL-3 level.

Finally, to provide an alternative that offers medium capacity and latency but high reliability, three MT29F4G08ABADAWP NAND *flash* memories were selected to operate in TMR. This memory has been characterized in [14], [15], and [16]. With accumulated TID, this memory begins to show errors in memory blocks at approximately $38krad$, but it remains functional even after $100krad$. No SEL was observed with LET up to $67.7\frac{MeV \cdot cm^2}{mg}$; SEU may occur starting from $1.1\frac{MeV \cdot cm^2}{mg}$, which are mitigated by TMR. We can classify it as TRL-5.

4.3 Sensing System

For this application, several sensors were chosen for system management, telemetry collection, and satellite management.

To monitor the power systems, two INA226AQDGSRQ1 power sensors from Texas Instruments were selected to monitor the $3V3$ and $5V$ buses. This sensor does not have flight heritage and has not been tested against radiation effects; however, it is widely used

in SpaceLab projects, and its operation has been proven in vacuum and vibration chambers through tests conducted on the CubeSat GOLDS-UFSC, which utilizes the TTC 2.0 submodule that, in turn, employs this sensor [17]. Thus, we sought to leverage the circuit used in TTC 2.0, ensuring a TRL-6 level for the circuit.

For temperature monitoring, the TMP112AQDRLRQ1 sensor was chosen, which has flight heritage from the CubeSat GRIDS-2 [18], guaranteeing a TRL-5 level. Additionally, two sensors were selected to ensure redundancy in case one of the modules fails.

The temperature and power sensors share the same I^2C serial bus. This type of bus is often problematic and susceptible to failures; therefore, *buffers* were used to isolate the bus from the individual branches in case of failures, as shown in Fig. 2.

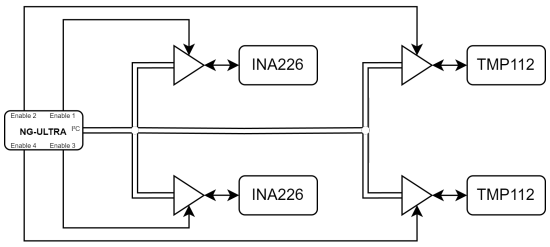


Figure 2: Node isolation system using *I2C* buffers.

To enhance the module's ability to act as an onboard computer, a magnetometer MMC5983MA from Memsic and a gyroscope IAM-20380 from TDK InvenSense were included for attitude control. They are configurable, allowing the choice between using I^2C or SPI buses. To increase reliability, a dedicated SPI bus was implemented solely for these two sensors. The magnetometer is being employed for the CubeSat of the CLIMB mission, which will monitor radiation from the Van Allen belts, and space environment simulation tests have already been conducted. Therefore, we can assign a TRL-5 level. So far, no missions have directly used the gyroscope; however, there are proposals for ADCS systems, as in [19], leading us to assign a TRL-3 level.

Finally, an ADC was implemented to allow reading of simple analog pins. The chosen converter was the ADC128S102 from Texas Instruments. It features a 12-bit resolution SPI interface and up to 8 channels. The project is illustrated in Fig. 3. To avoid the need to design an isolated power supply for the analog supply, an RC filter was used to eliminate ripple in the analog power. Five channels were made available with a bandwidth of up to $BW_{signal} = 48kHz$ and a Fs_{clk} of up to $16MHz$; its use must meet Nyquist's criterion expressed in Inequality 1, where N corresponds to the number of channels being sampled.

$$Fs_{clk} > 32 \cdot BW_{signal} \cdot N \tag{1}$$

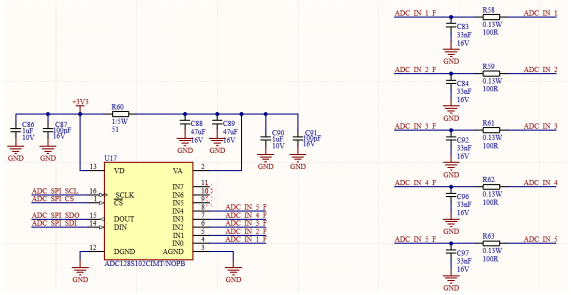


Figure 3: ADC design for reading external analog pins.

The ADC was characterized concerning TID and SEE, as described in [20]. SET was ob-

served starting from $18.5\frac{MeV \cdot cm^2}{mg}$, SEFI and changes in the *step current* were observed starting from $32.1\frac{MeV \cdot cm^2}{mg}$, and SEL was noted from $60\frac{MeV \cdot cm^2}{mg}$. The component was tested up to $30krad$ and showed promising results with only changes in power currents. It can be classified as TRL-5.

4.3.1 Interfaces

As there is no defined and exclusive mission for this module, its communication system was designed to offer great flexibility and alternatives for communication buses. Below are the interfaces connected to the banks of the FPGA available for communication with other satellite modules.

- 3 SpaceWire channels connected to the optimized banks of the FPGA.
- 1 CAN channel.
- 1 bus of LVDS pins available for implementation.
- 1 bus of generic pins available for implementation.
- 1 bus externalizing the 5 channels of the ADC.
- 1 UART channel for debugging connected to the second channel of the RS-485 converter.

For the implementation of the CAN bus, a SN65HVD232 transceiver from Texas Instruments was used. This transceiver is extremely popular and was chosen because it has been extensively tested in SpaceLab projects; however, no studies were found that mention it has flight heritage, thus it has a reliability level of TRL-4.

SpaceWire was implemented without routers, using the pins of the optimized complex banks for SpaceWire, which feature dedicated controllers, thereby simplifying and increasing the efficiency of the application.

4.4 Power System

The consumption estimate followed the procedure described in [21]. The power of the external ICs is presented therein, estimating an average consumption without any type of burst readings from the memories or sensors, and the maximum power estimate considers the most power-consuming operational mode for the IC (disregarding latch-up states). The total estimated power is $1.366W$ and $5.408W$, respectively. All these components were selected with a supply voltage of $3V3$, except for the DDR2 memories, which use $1V8$.

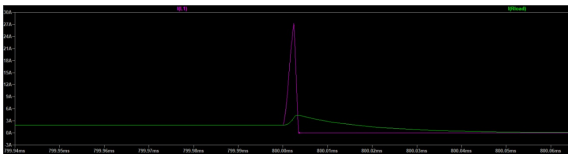


Figure 4: Simulation of the operation of the LTC4361-2 surge stopper against current surges.

To estimate the consumption of the FPGA SoC, the NXPowerEstimator tool was used. Since the project does not yet have a defined mission, there are no planned applications to be executed on the FPGA SoC. Thus, to estimate a consumption, a resource-intensive application was considered, using about 75% to 80% of the resources.

The expected current consumption for the FPGA SoC is shown in Table 2, specified for each power rail. The total power was $4.62W$.

Table 2: Current Consumption in Different Power Rails

Voltage (V)	**Ultra Consumption (mA)**	**ICs Consumption (mA)**	**Total Consumption (mA)**
3.3	31	745	776
1.8	277	690	967
1.0	4014	-	4014

4.4.1 Power Cascade

With the consumption estimate, we can develop the power cascade. Due to limited space for the CubeSat module, this design will prioritize area.

The $3V3$ voltage will serve only as power for the simple banks of the FPGA and for the external ICs. Due to physical limitations, we can save area on the PCB by directly receiving this voltage from the EPS bus; however, a maximum tolerance of no more than 5% is stipulated to comply with derating rates.

The voltages of $1V8$, $1V$, and $0V9$ will be converted directly on the module as they are more sensitive and power the logic of the FPGA, the SoC, and the DDR2 memories, in addition to not being buses commonly available in the EPS. To minimize the high current, an additional input voltage of $5V$ was chosen for the conversions.

4.5 Latch-up Protection

Although the NG-ULTRA supports up to $2000V$ on its pins, the external ICs are COTS and must therefore be protected in the event of SEL occurrences. To achieve this, we can add surge stoppers in series with the converters; specifically, the LTC4361-2 from Analog Devices is an excellent option and is widely used in CubeSat missions ([22], [23], [24], [25], among others). Its circuit is simple and similar in different implementations, ensuring TRL-6. Its operation occurs through monitoring the bus via the terminals of a shunt resistor. The device then controls the switching of an N-channel MOSFET, which can open the power circuit, preventing damage. After $130ms$, the bus is reconnected. In Fig. 4, the LTC4361 can be seen activating and disconnecting the bus in response to a current spike of $28A$, thus protecting the bus. Surge stoppers will be added to the $3V3$ and $1V8$ supplies of the COTS ICs. In Fig. 5, the implementation of the protection circuit on the $1V8$ power bus can be visualized.

4.6 Power Converters

To implement the power cascade, it is necessary to convert $5V$ to $1V$, $1V8$, and generate the reference voltages for the memories and the SoC.

The converter chosen for the $1V8$ conversion was the ST1S10 from STMicroelectronics, which has the advantage of integrating its MOSFETs within the chip, saving space. This buck converter supports up to $2A$ of current and is synchronous, which increases conversion efficiency. However, the second MOSFET tends to reduce the converter's lifespan due to cumulative effects of TID. Despite this, in [26],

this converter was characterized and supports up to $125krads$ without damage. In [27], the ST1S10 was characterized under SEE, showing resistance to SEL and SEFI for LETs greater than $67.7\frac{MeV \cdot cm^2}{mg}$; however, SETs may occur from $1\frac{MeV \cdot cm^2}{mg}$. Another positive aspect of choosing this converter is its flight heritage from the KySat-2 mission [22], which guarantees it a reliability level of TRL-5. The converter's design was made using the tool provided by the manufacturer for designing DC-DC sources. A maximum input voltage variation of 10% was considered. In Fig. 5, we can see the designed circuit; in Fig. 6, the efficiency of the converter is presented. At a maximum predicted consumption of $1.92A$, the converter achieves an efficiency of 83.7% and a ripple of 0.14%.

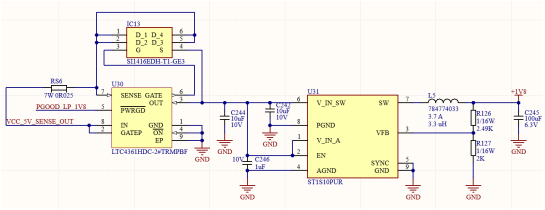


Figure 5: $1V8$ voltage conversion circuit with latch-up protection.

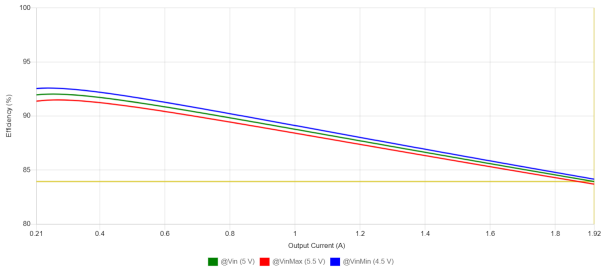
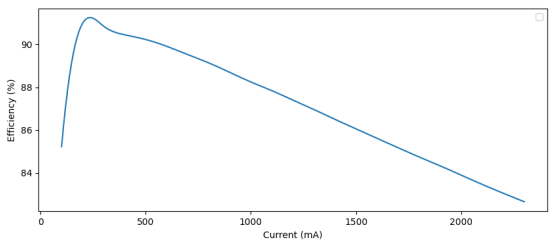


Figure 6: Efficiency of the $1V8$ power supply.

The $1V$ voltage is intended to power the cores of the SoC and the FPGA, and it is recommended by the manufacturer to dedicate two isolated buses. Thus, the LTM4619 buck converter from Analog Devices was chosen, which provides two outputs of up to $4A$ each and features such as power good and soft start. It was characterized against radiation in [28] and survived up to approximately $200krad$. In this same work, it was tested against SEEs of $200\frac{MeV \cdot cm^2}{mg}$, but it did not survive and was not tested near the NG-ULTRA resistance values ($\leq 65\frac{MeV \cdot cm^2}{mg}$). Thus, this result is not relevant for this application, and a new test with a LET value closer to this should be proposed. The design of this converter was made using the component's datasheet as a reference, and its design was validated using the SPICE model provided by the manufacturer. Both channels were designed to have a soft start of $1.4ms$ and a ripple of approximately 0.2%. The efficiency is shown in Fig. 7; at maximum predicted consumption, the efficiency is approximately 81.9%. This converter has flight heritage from the 12U CubeSat of the Aoxiang-Sat1 mission [29] and for the COVE payload to power the rad-hard Xilinx Virtex-5QV FPGA [30], ensuring TRL-5.

Figure 7: Efficiency of the $1V$ power supply.

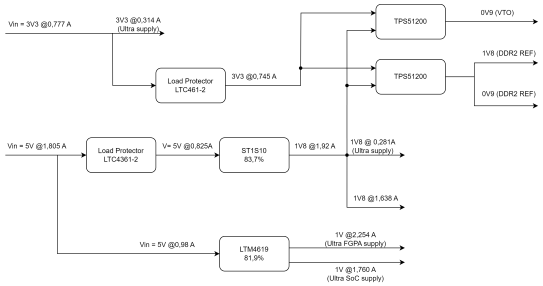


Finally, LDOs are needed to obtain the reference voltages for the memories and the DDR

bank of the SoC. Specifically, the TPS51200 was chosen, which is designed for this functionality. In [31], SEE tests were conducted, establishing a threshold LET between $11\frac{MeV \cdot cm^2}{mg}$ and $18\frac{MeV \cdot cm^2}{mg}$ for the occurrence of SEL. To circumvent the problem, the supply for these LDOs will also be protected by the LTC4361-2 surge stoppers. The TPS51200 is used in the NG-Ultra DevKit and in Payload-XL [32], allowing us to classify it as TRL-5.

Finally, the resulting power cascade is illustrated in Fig. 8.

Figure 8: Resulting power cascade.



5 Conclusion

In this work, it was possible to develop the architecture of a platform with fault tolerance characteristics by integrating a SoC FPGA with COTS components.

The next step in the development of the module consists of designing the physical layout of the PCB for the computational platform and testing the PDN. For this, the works of [32] and [21] will be used as a basis, describing radiation mitigation techniques focused on layout using the ECSS standards developed by the ESA. Due to the planned compatibility with the DevKit, it is expected that firmware work can be carried out with some parallelism through it.

There are currently no confirmed missions for the developed module. However, it is anticipated that it will be integrated into the Persistent-1 and ROCUS-1 missions of SpaceLab.

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