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Design of a 16 GHz Voltage-Controlled Oscillator with control and output stages using 12 nm FinFET Technology

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Supervisor:: Prof. Fernando Rangel de Sousa, Dr.
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Aquilles Pedro Grisa Santana

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O presente trabalho em nível de graduação foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Bacharel em Engenharia Eletrônica.

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Dedico este trabalho aos meus pais, amigos e colegas de trabalho.

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RESUMO

Este trabalho foca no projeto e análise de um oscilador controlado por tensão (VCO) destinado à integração em um loop de travamento de fase (PLL) utilizado na geração de referência temporal digital. Uma fundamentação teórica é desenvolvida para orientar a escolha das topologias de projeto e analisar os resultados, comparando-os com osciladores de alta velocidade de última geração. O projeto implementa um VCO de 16 GHz utilizando tecnologia FinFET de 12 nm, com um oscilador em anel de cinco estágios, um buffer para isolamento do sinal e uma fonte de corrente controlada por tensão (VCCS) para regular a corrente de polarização. O oscilador opera com tensão de alimentação de 0,8 V, utilizando transistores de ultra-baixo limiar. Simulações em malha aberta indicam um consumo médio de potência de 919,27 µW e demonstram um ruído de fase médio de -83,41 dBc/Hz a 1 MHz de offset em relação à portadora, refletindo baixas variações de ruído de fase.

Palavras-chave: Oscilador controlado por tensão. 16 GHz. FinFET. Ruído de fase. Oscilador em anél.

ABSTRACT

This work focuses on the design and analysis of a voltage-controlled oscillator (VCO) intended for integration within a phase-locked loop (PLL) used in digital clock generation. A theoretical foundation is developed to guide the selection of design topologies and to analyze the results by comparing them with state-of-the-art high-speed oscillators. The design implements a 16 GHz VCO using 12 nm FinFET technology, featuring a five-stage ring oscillator, a buffer for signal isolation, and a voltage-controlled current source (VCCS) to regulate the starving current. The oscillator operates at a supply voltage of 0.8 V using ultra-low threshold voltage transistors. Open-loop simulations indicate an average power consumption of 919.27 μW and demonstrate an average phase noise of -83.41 dBc/Hz at 1 MHz offset from the carrier, reflecting low phase noise fluctuations.

Keywords: Voltage-controlled oscillator. 16 GHz. FinFET. Phase noise. Ring oscillator.

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LIST OF ABBREVIATIONS AND ACRONYMS

ACM	Advanced compact MOSFET
Cgs	Gate-to-source parasitic capacitance
CTRL	Control
FDBK	Feedback
FinFET	Fin field-effect transistor
FLL	Frequency-locked loop
F-V	Frequency-to-voltage
I/O	Input and output
ISF	Impulse sensitivity function
KCL	Kirchoff current law
OTA	Operational transconductance amplifier
Planar FET	Planar field-effect transistor
PLL	Phase-locked loop
PN	Phase noise
Q	Quality factor
Rds	Drain-to-source resistance
RF	Radio-frequency
RO	Ring oscillator
TIA	Trans-impedance amplifier
V2I	Voltage-to-current converter
VCCS	Voltage-controlled current source
VCO	Voltage-controlled oscillator
VDD	Positive supply voltage
VSS	Reference supply voltage

CONTENTS

1 INTRODUCTION

1.1 MOTIVATION

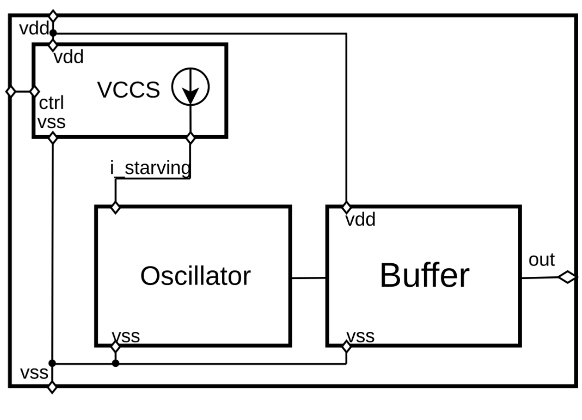
In recent decades, data traffic has increased significantly across society and industry, driven by the growing number of connected devices and the vast amount of information available. As a result, some technologies are shifting to higher frequency ranges to avoid congestion and enable higher data rates. This shift has made the design of circuits capable of operating at GHz frequencies increasingly important.

However, reaching these frequencies poses challenges due to the physical size, limitations, and parasitic effects of the components, which become more significant at high frequencies.

The voltage-controlled oscillator (VCO) generates signals whose output frequency varies in response to an input control voltage. They are essential in various applications, including waveform generation, RF modulation and demodulation and phase-locked loops (PLL). Because the control input may represent a communication channel selection or an error signal from a feedback loop, VCOs are used in devices such as smartphones, computers, radios, radars, and clock generation circuits (ROGERS; PLETT; DAI, et al., 2006).

As technology continues to scale down, there is a growing demand for circuits with faster switching speeds. These circuits must be designed using increasingly smaller transistor nodes to allow integration with other system components. This work addresses some of the challenges in designing a current-starved voltage-controlled oscillator using 12 nm FinFET technology for future high-speed digital clock generation. The design includes a voltage-controlled current source (VCCS), the current-starved ring oscillator, and a buffer stage optimized for high-frequency operation.

Figure 1 – Voltage-controlled oscillator proposed diagram



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1.2 STATE OF ART REVIEW

This section analyzes and discusses recent works related to similar applications, evaluating their design strategies and performance to inform the development of this project. Although a direct comparison is not always feasible due to differences in the technology nodes, configurations, and final applications of VCOs, these studies offer valuable insight into achievable performance and design trade-offs.

In (LI et al., 2024), the authors propose a compact, low-power, low-jitter PLL for telecommunications applications. To reduce area and eliminate the need for bulky passive components, they replaced the traditional LC-VCO with a ring oscillator based on CMOS delay cells. This choice enables a compact design and wide tuning range, at the expense of increased noise. Implemented in 12 nm FinFET technology, the VCO achieves a tuning range from 0.7 to 12.5 GHz, with a power supply of 0.8 V, power consumption of 1.08 mW, and phase noise of -81.45 dBc/Hz at 1 MHz.

In (SUN et al., 2024), a dual-core LC-VCO is presented as part of a low-noise PLL operating from 8.5 to 17.8 GHz. The design uses two parallel oscillators: a Low VCO (LVCO) for the lower frequency range and a High VCO (HVCO) for the upper range, with overlapping coverage in between. This architecture offers a wide tuning range and reduced phase noise. The VCO operates at 1.2 V with a maximum power consumption of 30.07 mW, implemented in 65 nm CMOS technology. Although this dual-core LC-VCO topology differs significantly from the single-core ring oscillator proposed in this work, it provides a useful point of comparison in terms of performance and design trade-offs.

In (XIA; WU; TIAN, 2024), the authors design a ring-based PLL using a current-controlled oscillator (CCO). This CCO shares the same ring structure as the topology proposed in this work but incorporates a voltage-to-current converter (V2I), following a similar control principle. The design, implemented in 6 nm CMOS, achieves a tuning range from 4 to 16 GHz with a supply voltage of 0.75 V and power consumption of 4.95 mW.

Earlier works such as(TURKER et al., 2018) and (LIU; GOH; SIEK, 2005) present both LC-based and ring oscillator designs. These studies serve as historical benchmarks that illustrate the evolution of oscillator performance over time and the improvements made in power efficiency, tuning range, and noise characteristics.

Table 1 – State of art comparison

Work	Power supply (V)	Power consumption (mW)	Frequency (GHz)	Phase Noise @ 1 MHz (dBc/Hz)	Tech. (nm)	Topology
LI et al., 2024°	0.8	1.08	0.7 - 12.5	-81.45	12	RO
SUN et at., 2024	1.2	30.07	0.05 - 17.8	-109.9	65	Dual LC
XIA; WU; TIAN; 2024	0.75	4.95	4-16	-	6	RO
TURKER et al.,2018	-	45	7.4 - 14	-123.2	16	LC
LIU; GOH; SIEK, 2005	1.8	50	8.4 - 10.1	-99.9	180	RO

Source: Author

° VCO Only

1.3 ORGANIZATION

This work is structured as follows. Chapter 2 presents the fundamental concepts required to understand the design, including the key performance metrics and parameters analyzed throughout the project. It also introduces possible oscillator topologies, outlining their advantages, disadvantages, and the techniques applied in the proposed design. Topics covered include the benefits of FinFET technology, oscillator operating principles, performance metrics such as phase noise and jitter, and the core design equations.

Chapter 3 outlines the design specifications and performance targets of the project. It discusses the application of previously introduced equations, the design decisions taken, and preliminary simulation results for each developed subcircuit.

Chapter 4 presents the results of the complete VCO design, including open-loop and closed-loop simulations. The chapter also provides an analysis of the system's overall performance on the basis of these results.

2 THEORETICAL BACKGROUND

This chapter provides the theoretical foundation necessary for the design of the voltage-controlled oscillator (VCO). It aims to establish a solid understanding of high-speed circuit design by exploring key parameters and examining how design decisions influence each building block. This background equips the reader to better understand the design choices and performance targets of the proposed VCO.

2.1 FINFET

The article (MAURYA; BHOWMICK, 2022) describes the FinFET as one of the best Multi-Gate Field Effect Transistor technologies available, due to its improved stability, better short channel performance, and smaller intrinsic gate capacitance.

The primary physical difference between planar and FinFET devices lies in the placement of the gates. In planar transistors, the gate controls the channel only from the top (horizontal axis), whereas in FinFETs, the gate wraps around the channel on multiple sides along the vertical axis. This multisided gate control increases the effective channel area influenced by the gate, allowing for stronger electrostatic control. As a result, the channel forms more efficiently, enabling faster switching and better suppression of short-channel effects.

Figure 2 – Planar FET and FinFET 3D representation

(a) Planar FET (b) FinFET

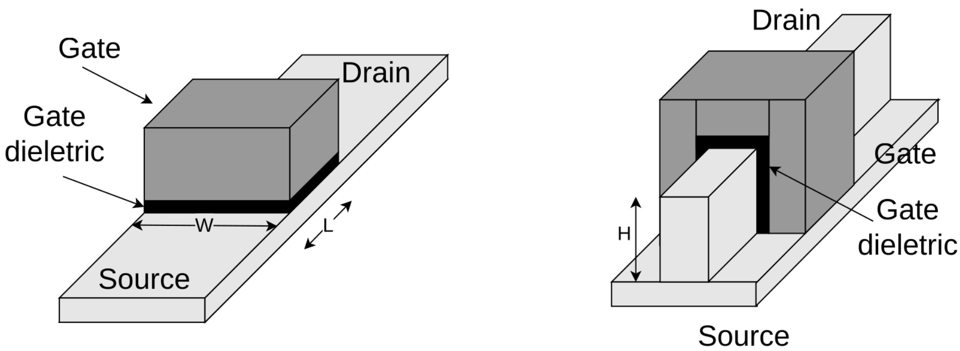

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Figure 2 presents a physical comparison between planar and FinFET technologies. Although both structures share the same basic terminals, gate, drain, and source, and rely on channel formation beneath the gate dielectric.

FinFETs can be classified into two main types: Double-Gate (DG) and Tri-Gate (TG) FinFETs. In the DG FinFET, the channel is controlled by two vertical gate fins on the sides, while a hard mask on the top prevents the horizontal gate from influencing the channel, enhancing structural stability. In contrast, the TG FinFET features not only the side gates but also a top gate, which is separated from the channel only by a dielectric layer. This configuration allows the gate to control the channel from three sides.

Because the gate surrounds more of the channel in FinFETs compared to planar devices, the effective channel width becomes a function of the fin geometry. As a result, key device characteristics such as drive current and switching speed can be tuned by adjusting fin dimensions.

For a double-gate FinFET

$$W_{eff} = 2 \cdot n \cdot Fin_{height} \tag{1}$$

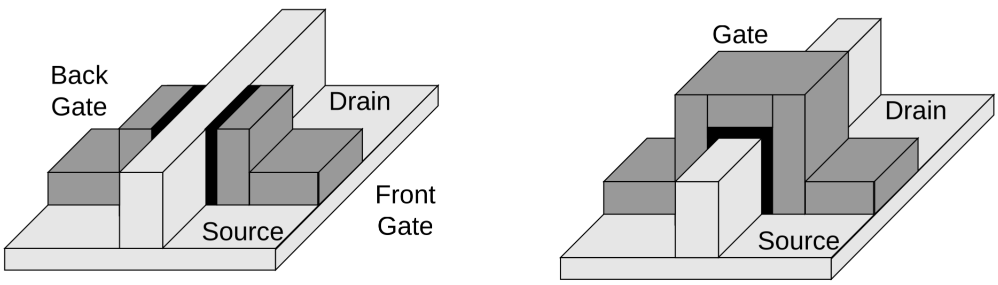
For a tri-gate FinFET

$$W_{eff} = 2 \cdot n \cdot Fin_{height} + Fin_{width} \tag{2}$$

Here, n represents the number of fins in the device. Another way to categorize FinFETs is based on gate connectivity. They can be classified as Shorted-Gate (SG) or Independent-Gate (IG) FinFETs. In SG FinFETs, the front and back gates are electrically connected (shorted), functioning as a single gate. In contrast, IG FinFETs feature physically isolated front and back gates, allowing them to be controlled independently for more flexible operation.

Figure 3 – FinFET gate connectivity representation

(a) Double-gate (b) Tri-gate



Source: Author

In general, the FinFET channel does not require heavy doping. However, light doping may be introduced to improve leakage current control and to fine-tune the threshold voltage. However, the source and drain regions require high doping concentrations to ensure proper carrier injection. However, this high level of doping can lead to an increase in series resistance in the device.

The FinFET has more parasitic capacitance compared to the planar device. As the gate now has a wider coverage area, parasitic capacitances C_{gd} tend to increase for higher fin heights, while narrow fin pitchs tends to interfere with the coupling between fins.

FinFETs exhibit higher parasitic capacitance compared to planar transistors due to their increased gate coverage area. Specifically, the parasitic capacitances from gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) tend to increase with greater fin height (Fin_{height}), as a larger gate surface overlaps the channel. Furthermore, the fin pitch (Fin_{pitch}), the spacing between adjacent fins, affects the electrostatic coupling between fins, influencing the overall capacitance and behavior of the device.

The study in (SINGH et al., 2017) compares the 14 nm FinFET technology with 28 nm planar CMOS for RF applications, focusing on the transition from planar to FinFET nodes to enable higher device density and support emerging technologies. Factors such as design compatibility and cost-efficiency are highlighted as key enablers of this migration. Additionally, the growing trend of replacing traditional analog circuit blocks with digitally assisted analog architectures supports the adoption of FinFET technology, offering reduced area and access to an increasingly mature design ecosystem.

Table 2 – Comparison between FinFET and planar FET technologies

Technology	14 nm FinFET		28 nm FET (planar poly/SiON)	
Device	NFET	PFET	NFET	PFET
L_{gate} [nm]	14		30	
CPP† [nm]	78		126	
V_{DD}[V]	0.8		1.05	
$I_{D_{sat}}$ [µA/µm]*	1523	1433	670	450
$G_{m_{sat}}$ [µS/µm]*	3017	2748	985	395
$f_t.G_m/I_D$ [THz/V]	2650	2053	2000	1150

Note: *Normalized to footprint W_{design}, †CPP: Contacted poly (gate) pitch

Source: (SINGH et al., 2017)

Table 2, adapted from (SINGH et al., 2017), compares device parameters between a 14 nm RF FinFET and a 28 nm high-*k* k metal gate (HKMG) planar RF technology. The FinFET demonstrates superior performance, offering higher drive current (I_D) and transconductance (g_m) for the same footprint. Additionally, it operates at a lower supply voltage and occupies a smaller device area, highlighting its advantages for high-performance and area-efficient RF circuit design.

In the study, key RF performance metrics such as the transition frequency (f_t) and the maximum oscillation frequency (f_{max}) are evaluated for each type of transistor. The parameter f_t represents the frequency at which the current gain between the gate input and the drain output drops to unity, while f_{max} denotes the highest frequency at which the power gain is still achievable, indicating the potential for sustained oscillation.

When comparing NFinFETs with conventional NFETs, and PFinFETs with PFETs, the FinFET devices consistently demonstrate higher values of both f_t and f_{max} than their planar counterparts. These results highlight the superior high-frequency performance of FinFET technology in both NMOS and PMOS configurations.

For a 14 nm node, the obtained values are

Table 3 – 14 nm FinFET f_t and f_{max} extracted from work

	14 nm FinFET	
	NFinFET	PFinFET
$f_t(GHz)$	314	285
$f_{max}(GHz)$	180	140

Source: (SINGH et al., 2017)

To further improve f_{max}, optimization strategies such as increasing the gate length (L_{gate}) and implementing double gate contacts (DGC) can be employed. These enhancements have been shown to raise f_{max} values to 227 GHz for NFinFETs and 195 GHz for PFinFETs, respectively.

Based on the studies referenced, FinFETs represent a viable option for circuit miniaturization and integration with other applications. Their reduced footprint enables higher transistor density on a silicon die, while offering improved performance compared to certain planar technology nodes. Furthermore, design methodologies developed for larger technology nodes can be adapted to FinFET processes, facilitating the transition to advanced technologies.

For RF applications, FinFETs offer higher values for f_t and f_{max}, enabling more efficient operation with reduced signal degradation, as well as lower power consumption and leakage currents. However, it is important to note that despite these advantages, FinFETs are still under evaluation for many applications and may not be the optimal choice for certain circuit blocks due to their inherent non-idealities, such as the increased parasitic capacitance. Furthermore, FinFET layouts are more complex and must adhere to stricter design rules. Consequently, analog and RF circuit designs often encounter challenges during layout, necessitating additional design iterations to achieve desired performance.

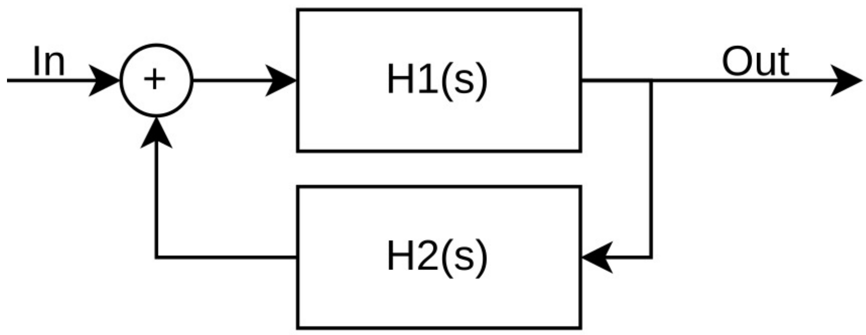
2.2 OSCILLATORS

The book (ROGERS; PLETT; DAI, et al., 2006) defines an oscillator as a circuit that generates a periodic waveform. As mentioned above, oscillators have a wide range of applications, including clock generation for receivers and transmitters, as well as general waveform generation. In the context of this study, the oscillator will be analyzed as the central component of a frequency synthesizer. Key considerations in this context include tunability, the ability to achieve or converge to different frequencies, spectral purity, characterized by low phase noise, and, for integrated circuits, low power consumption.

There are various approaches to oscillator design, but two primary types are discussed in the book. The first is the LC-based oscillator, which uses a resonant circuit composed of inductors and capacitors to generate the desired frequency. The second is the ring oscillator, which achieves oscillation through a series of connected delay cells. In addition, crystal oscillators are discussed, primarily emphasizing their importance as stable reference signals in frequency synthesizers.

2.2.1 Oscillator block diagram

Figure 4 – Oscillator theoretical model



Source: Author

According to (ROGERS; PLETT; DAI, et al., 2006), a system forms an oscillator when its poles lie on the imaginary axis of the s-plane. Substituting $s = j\omega$, if there exists a frequency ω at which the denominator of the transfer function becomes zero, the system will oscillate at that frequency. From a filter perspective, as the poles approach the imaginary axis from the left half-plane, the system's quality factor (Q) tends to infinity. This behavior can be understood by envisioning a negative resistance that cancels the positive resistance responsible for losses and attenuation, thereby allowing the system to sustain oscillations indefinitely. Another viewpoint is that in a feedback system, the loop gain causes the transfer function denominator to become zero at a certain $j\omega$, satisfying the oscillation condition and causing the circuit to oscillate at the corresponding frequency.

The transfer function can be written as

$$\frac{v_{out}}{v_{in}} = \frac{H_1(s)}{1 - H_1(s)H_2(s)} \tag{3}$$

The product of $H_1(s)$ and $H_2(s)$ can be interpreted as the loop gain of the system. When this product approaches unity, the overall transfer function tends toward infinity.

Near this singularity, the system exhibits very high gain, allowing a finite output voltage to be generated from an arbitrarily small input voltage.

For sustained oscillations to occur, the system must satisfy the Barkhausen criteria, which state two essential conditions that must be met.

Loop gain:

$$\left| H_1(s) \cdot H_2(s) \right| = 1 \tag{4}$$

Phase shift:

$$\angle H_1(s) \cdot H_2(s) = 0 \tag{5}$$

or

$$2 \cdot n \cdot \pi$$

With n being an integer, in practice, the loop gain initially exceeds unity, causing the output voltage to grow over time. After a transient period, nonlinearities in the system reduce the effective feedback gain to a level that sustains the oscillation. This balance maintains the feedback signal at a magnitude sufficient to keep the oscillation running continuously.

2.2.2 LC-Based VCO

The LC resonator, composed of inductors and capacitors, determines the oscillation frequency of the oscillator and is often integrated into the feedback mechanism, as seen in Colpitts and Hartley oscillator topologies. The oscillation frequency is approximately given by:

$$\omega_{osc} = \sqrt{\frac{1}{LC}} \tag{6}$$

where L is the inductance and C is the capacitance of the resonant tank circuit. This relation assumes ideal components and neglects loading effects, offering a first-order approximation of the natural oscillation frequency. In practical implementations, however, non-idealities in the components introduce losses that cause the oscillations to decay over time. To compensate for these losses and sustain oscillation, a feedback mechanism is required to continuously supply energy to the circuit.

High-quality inductors are traditionally among the most challenging RF passive components to implement monolithically, primarily due to the lossy substrate, parasitic capacitances between the metal layers and the substrate, and the limited conductivity of on-chip metals. However, extensive research has been dedicated to accurately modeling these devices, with a focus on optimizing geometric structures during fabrication.

Due to modeling and simulation constraints, modern technologies typically do not provide true circular inductors. Instead, they employ polygonal shapes, most commonly octagonal layouts, which can closely approximate the performance of circular structures. In practice, square-spiral inductors are frequently used, but their 90-degree turns contribute additional series resistance. Furthermore, the intrinsic series resistance (R_S) increases with frequency due to the skin effect, an electromagnetic phenomenon that causes current to concentrate near the conductor surface, effectively reducing the cross-sectional area available for conduction.

At lower frequencies, the inductance of an integrated inductor remains relatively constant. However, as the operating frequency increases, parasitic impedances, primarily capacitances between the turns and to the substrate, become increasingly significant. At a certain frequency, these parasitic elements interact with the inductance in such a way that they form a resonant tank, effectively canceling the inductive behavior. This phenomenon defines the self-resonant frequency (SRF) of the inductor, beyond which the component no longer behaves as an inductor and instead exhibits capacitive characteristics.

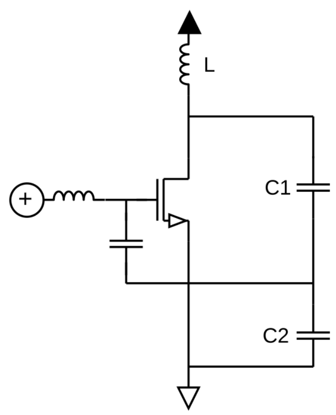
Since parasitic capacitances are strongly dependent on the physical dimensions of the inductor, the self-resonant frequency tends to decrease as the inductor size increases. As a result, the maximum usable size and consequently the maximum achievable inductance of on-chip inductors is inherently limited in high-frequency applications.

The Q for a inductor can be given by the following equation:

$$Q = \frac{|Im(Z_{ind})|}{|Re(Z_{ind})|} = \frac{\omega L}{R_S} = \frac{R_P}{\omega L} \tag{7}$$

Where Z_{ind} is the inductor impedance, L is the equivalent inductance, R_S is the series resistance and R_P is the parallel resistance at frequency ω. This relationship shows that achieving higher quality factors, directly related to the filtering performance of the resonator, requires either a higher inductance or lower series resistance, both of which are influenced by the physical dimensions of the inductor.

Figure 5 – Common-gate Collpits oscillator schematic



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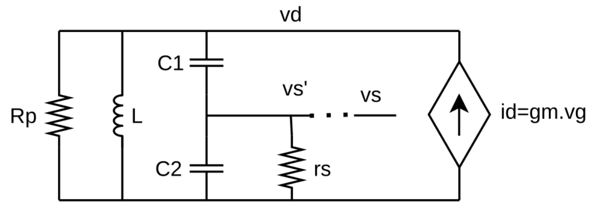
Using a common-gate Collpits topology to analyze a LC-based oscillator. Taking into account the small signal model of Figure 6 (a), the r_s resistor on C_2 can be replaced by a tank-equivalent $r_{s,tank}$ resistor according to

$$r_{s,tank} = \left(1 + \frac{C_2}{C_1}\right)^2 r_s \tag{8}$$

Figure 6 – Small-signal model for a common-gate Collpits oscillator

(a) Collpits common-gate small signals model



(b) Collpits common-gate using capacitive feedback

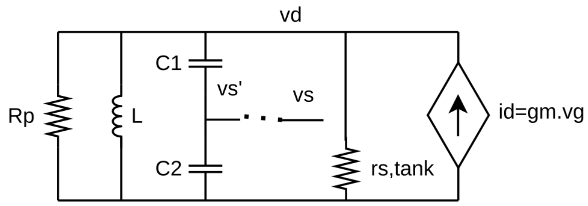


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Figure 6 (b), the equivalent model is obtained. The loop gain now can be expressed as

$$H_1 H_2 = \frac{g_m}{Y_{tank}} \frac{C_1}{C_1 + C_2} = \frac{C_1}{C_1 + C_2} \frac{g_m}{\frac{1}{R_P} + \frac{1}{r_{s,tank}} + j\omega C_T - \frac{j}{\omega L}} \tag{9}$$

To solve for Barkhausen criteria, we can set Equation (9) to one, as the imaginary terms cancel, the resonant frequency will be set as:

$$\omega_o = \sqrt{\frac{1}{C_T L}} \tag{10}$$

With C_T being defined as

$$C_T = C_1 || C_2 = \frac{C_1 C_2}{C_1 + C_2} \tag{11}$$

The remaining terms can be used to obtain the required g_m, setting the loop gain to one in the resonance frequency, but in practice, the small loop gain must be larger than one to guarantee a start-up

$$g_m > \left(\frac{1}{R_P} + \frac{1}{r_{s,tank}}\right)\left(\frac{C_1 + C_2}{C_1}\right) \tag{12}$$

The transconductance g_m compensates for losses that will occur in the inductor R_P and $r_{s,tank}$, so for a decrease g_m, both resistances would need to be as large as possible. A large R_P will be the result of a high Q for the inductor, while a large $r_{s,tank}$ will be the result of a large capacitive transformer relation ($C_2 >> C_1$). As g_m depends on $r_{s,tank}$, so

$$g_m = \frac{\omega^2 L(C_1 + C_2)}{R_P} = \frac{C_1 + C_2}{R_P C_T} \tag{13}$$

To minimize g_m, R_P should be large, and choosing a larger transformer ratio for C_2 and C_1 is not optimum, as it will increase $r_{s,tank}$, but reducing the loop gain, thus requiring a larger g_m. To reduce noise, it is an advantage to increase $r_{s,tank}$ by increasing the transformer ratio, but it requires a larger g_m, which increases power dissipation, being a trade-off between noise and power losses.

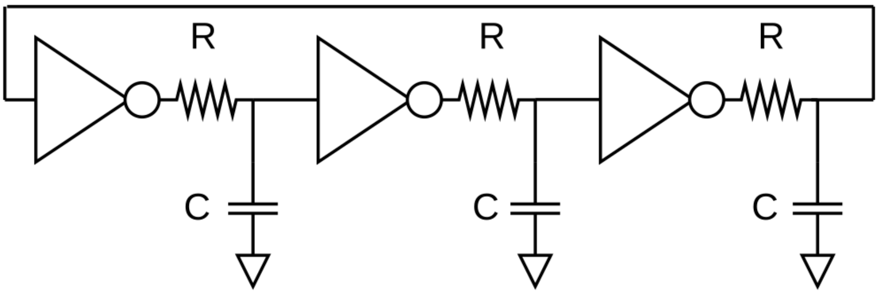
2.2.3 Ring Oscillator VCO

Ring oscillators, like any other type of oscillator, must satisfy the Barkhausen criteria. However, in this case, the phase-shift condition is of greater importance, as the loop gain requirement is typically easily met. Ring oscillators are commonly implemented using an odd number of inverters, with the output of the final stage fed back to the input of the first stage.

When a voltage such as V_{DD} is applied to the input, the signal propagates through the chain of inverters and delay cells. Due to the odd number of inversions and inherent delay, the output eventually becomes V_{SS}, which feeds back to the input and forces it to switch states, initiating a new cycle and propagating the change through all subsequent stages.

In a three-stage ring oscillator, for example, if the input to the first inverter is high, its output will be low. This low signal is then fed into the second inverter, resulting in a high output, which in turn becomes the input to the third inverter, producing a low output. Because this final output is connected back to the input of the first stage,with delay applied, it causes the input voltage to discharge and switch to a low level, restarting the process with the inverted value.

Figure 7 – Three stages ring oscillator diagram



Source: Author

Because they do not rely on inductors, ring oscillators tend to exhibit higher phase noise compared to LC oscillators, although this can vary depending on the chosen topology.

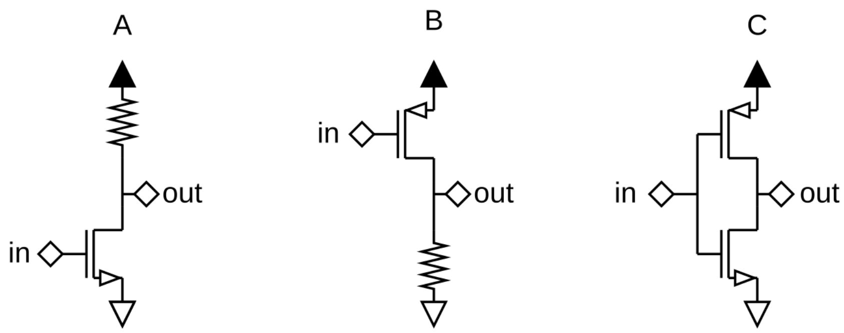
Using a single inverter is insufficient to achieve oscillation. While the input-output behavior may resemble that of a feedback system, the phase shift condition required by the Barkhausen criteria is not met, as it results in only a 180° phase shift rather than the necessary 360°. Additionally, certain topologies may be unstable or fail to function properly.

Although two-stage ring oscillators can theoretically provide the required 360° phase shift, they often result in a latched output, where the final output equals the input and no oscillation occurs. While there are techniques designed to mitigate this behavior and enable oscillation in two-stage configurations, such methods fall outside the scope of this study.

Due to these limitations, the minimum practical implementation for a ring oscillator typically involves three stages, forming the simplest functional configuration. While differential ring oscillator designs exist that can oscillate with an even number of stages, they are generally applied in different contexts and will not be the focus here.

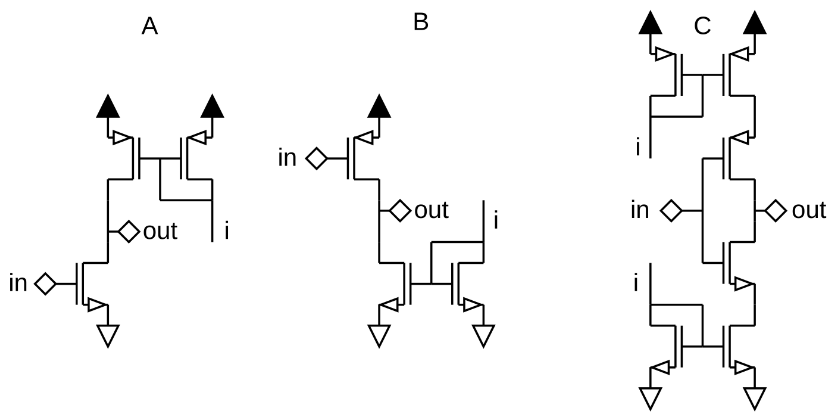
The frequency of oscillation f_{osc} is related to $\frac{I}{C}$, where I is the current of charge and discharge and C is the capacitance size. So, the frequency could be adjusted by controlling both capacitance and current, as the capacitance is a physical dependent parameter, and not so easy to adjust, the oscillation frequency f can be adjusted by the current I.

Figure 8 – Single ended inverters schematic



Source: Author

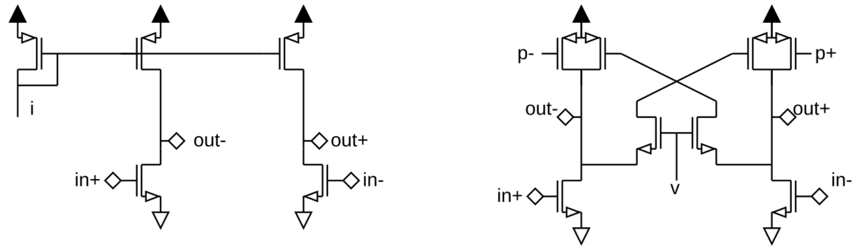
Figure 9 – Single ended inverters with bias current schematic



Source: Author

Different topologies of amplifiers or inverters can make up the structure of a ring oscillator, such as the ones shown in Figure 8. As the oscillation frequency depends on how quickly the capacitance can be charged or discharged, circuits with bias tuning current can be implemented to control the oscillation process, some options are shown in Figure 9.

Figure 10 – Differential inverters schematic



Source: Author

Differential inverters could also be used in an elementary design topology or with cross-coupling, as shown in Figure 10.

For an N-stage ring oscillator, modeling the inverter as a negative transconductor, driving RC cells, as the delay cells

$$G(s) = \frac{v_{out}}{v_{in}} = \frac{-G_m R}{1 + sCR} \tag{14}$$

The open loop gain is defined as

$$H(s) = \left(\frac{-G_m R}{1 + sCR}\right)_1 \cdot \left(\frac{-G_m R}{1 + sCR}\right)_{...} \cdot \left(\frac{-G_m R}{1 + sCR}\right)_N = \left(\frac{-G_m R}{1 + sCR}\right)^N \tag{15}$$

As each stage will add 180°, the phase shift will be $N \cdot 180°$, and the delay cells must complete the phase shift to achieve $2n\pi$

$$\varphi = -tan^{-1}\left(\omega RC\right) \tag{16}$$

Instead of analyzing the inverter by the phase shift, it is possible to characterize it by the time delay it has. The oscillation frequency of an oscillator f_{osc} can be discovered as

$$f_{osc} = \frac{1}{2N\tau} \tag{17}$$

Here τ is the given delay for each cell.

Assuming that the I charging current is constant, an estimate of frequency can be made noting that the output voltage will swing about half V_{DD} before starting the next stage, f_{osc} can be predicted as

$$T = 2N\frac{C \cdot V_{DD}}{I \cdot 2} \tag{18}$$

or

$$f_{osc} = \frac{1}{T} = \frac{I}{N \cdot C \cdot V_{DD}} \tag{19}$$

With N being the number of stages, C the input capacitance of each stage, I the charging/discharging current and V_{DD} the supply voltage for the ring oscillator.

Equation (19) shows that the oscillation frequency f_{osc} depends on the factors discussed above. To achieve a desired oscillation frequency, these parameters can be adjusted accordingly, allowing the oscillator to operate within the specified frequency range.

For a given ring oscillator, the number of stages N is typically considered fixed. Although more complex topologies may implement switching mechanisms to add or remove stages, in most cases, N remains constant. Varying the supply voltage V_{DD} is generally not a viable option, as it may be shared with other circuits. Additionally, reducing V_{DD} may cause transistors to enter the triode or saturation regions improperly, while increasing it beyond the nominal level may risk damaging the device.

The capacitance C is another factor subject to variation due to the fabrication process. Since it depends on device sizing, any deviations caused by the finite precision of the manufacturing equipment can affect the oscillation frequency. Moreover, process variations, such as shifts between slow-slow and slow-fast corners, for example, can further alter the capacitance, thereby affecting the frequency of oscillation.

From basic circuit theory, it is known that the current through a capacitor is given by:

$$I_C = C\frac{dV}{dt} \tag{20}$$

Integrating both sides over time, we obtain:

$$\int_{-\infty}^{t} I_C(t) = C\int_{-\infty}^{t} \frac{dV}{dt}dt \tag{21}$$

Thus, for a given initial time t_0, the voltage across the capacitor can be expressed as:

$$V(\tau) = \frac{1}{C}\int_{t_0}^{\tau} I_C \cdot dt + V(t_0)$$

This equation highlights that the voltage value across a capacitor is directly related to the integral of the current over time. In the context of a current-starved ring oscillator, this relationship becomes critical. In such circuits, the current I_C responsible for charging and discharging the capacitance of the internal node is deliberately limited by current sources. Assuming that the initial voltage $V(t_0)$ is V_{SS} or V_{DD}, the time required to reach a switching threshold, related to the propagation delay, is inherently dependent on both the current magnitude and the capacitance value.

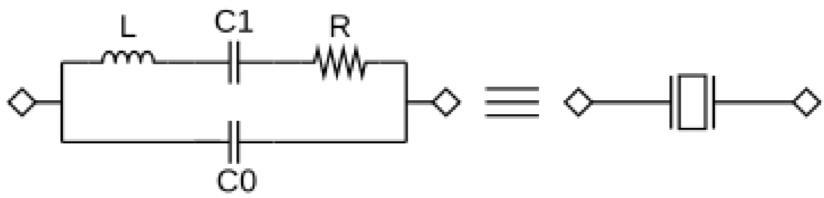
Therefore, in a current-starved ring oscillator, each inverter stage is preceded and/or followed by a current source that restricts the available charging/discharging current, effectively setting the speed at which the output voltage transitions. These current sources are typically implemented as voltage-controlled current sources, where a control voltage modulates the bias current. As a result, the delay per stage, and hence the oscillation frequency, can be finely tuned by adjusting the control voltage.

This architecture enables precise frequency control with relatively low power consumption and is particularly well suited for applications requiring frequency agility and integration efficiency.

2.2.4 Crystal Oscillator

Quartz crystal resonators are primarily used for frequency control and synthesis applications due to their high quality factor Q, excellent long-term stability, and minimal sensitivity to environmental variations, all within a compact form factor. When a voltage is applied across opposing faces of the crystal, it mechanically resonates. Both the quality factor and the temperature coefficients of the resonator are influenced by the crystal's cut orientation.

Figure 11 – Crystal oscillator model



Source: Author

The motional resonance frequency f_S of the crystal oscillator is given by

$$f_S = \frac{1}{2\pi\sqrt{LC}} \tag{22}$$

A figure of merit M is important for crystal oscillators

$$M = \frac{1}{2\pi f_S C_0 R} \tag{23}$$

For M<2, the crystal reactance is never inductive, and an external inductor would be required so it oscillates.

In a crystal resonator, the quality factor of the reactive components is X_1, from the motional inductance or capacitance, divided by the motional resistance.

$$Q = \frac{|X_1|}{R} = \frac{2\pi f_s L_1}{R_1} = \frac{1}{2\pi f_s C_1 R_1} \tag{24}$$

In the vicinity of an isolated mode of vibration, the impedance of a crystal is pure resistive at two given frequencies. The lower frequency is the resonance frequency f_r, which is close to f_s, but not exact due to the presence of C_0, and the higher being the antiresonance frequency f_a. When the resonator is lossless, the antiresonance frequency is approximately equal to the parallel resonance frequency f_p.

$$f_p = f_s\left(1 + \frac{C_1}{2C_0}\right) = f_s\left(1 + \frac{1}{2M}\right) \tag{25}$$

Then M>5, f_r can be approximated by

$$f_r = f_s\left(1 + \frac{1}{2QM}\right) \tag{26}$$

2.2.5 Performance comparison of oscillators

Table 4 – Comparison summary

Parameter	Crystal	LC	Ring
Output frequency	Low	High	Medium
Q	High	Medium	Low
Phase Noise	Best	Good	Poor
Power consumption	Low	High	Highest
Multiphase output	No	No*	Yes
Frequency stability	Best	Good	Poor
Tuning range	Narrow	Medium	Wide
Integrability	No	Large size	Small size
Applications	Reference source	GHz VCO	Multiphase VCO, digital clock generation

Source: (ROGERS; PLETT; DAI, et al., 2006)

Table 4 highlights that crystal oscillators typically offer superior frequency stability and low phase noise compared to other types of oscillators. However, they operate at relatively low frequencies and cannot be fully integrated on-chip, requiring external connection through package pins. As such, they are commonly employed as timing references for other circuits.

LC-based oscillators are capable of reaching frequencies in the hundreds of gigahertz, with favorable performance in terms of phase noise and stability. This makes them suitable for precision applications. Nevertheless, their performance is highly dependent on the quality of the inductor, particularly its Q-factor As high Q inductors are difficult to implement efficiently in integrated circuits due to their large equivalent area, this presents a design challenge.

Ring oscillators, by contrast, offer a compact footprint and a wide frequency tuning range, making them well-suited for fully integrated solutions that require frequency agility. However, they tend to consume more power to achieve acceptable performance and generally exhibit inferior noise and stability characteristics. In some cases, feedback control mechanisms are required to stabilize the oscillation frequency within the desired specifications.

2.3 PHASE NOISE

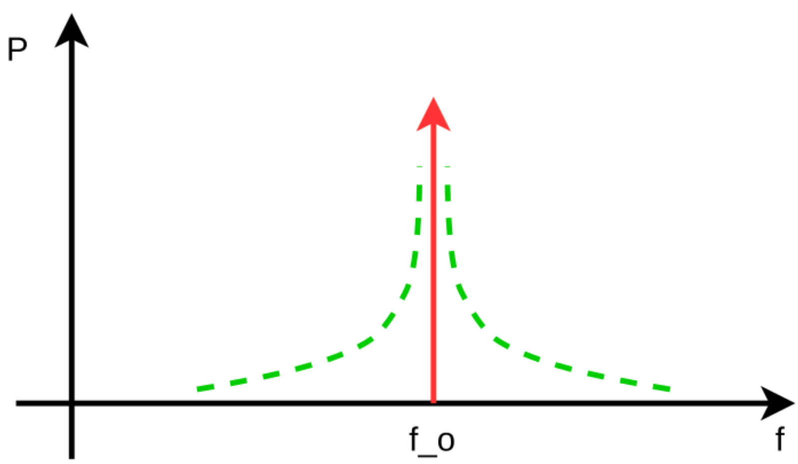
Suppose that there is an ideal oscillator, its frequency response would be represented by an impulse centered at the oscillation frequency. In practice, however, real oscillators exhibit a response that deviates from this ideal, characterized by spectral spreading, known as skirts, around the carrier frequency. This effect arises from instantaneous fluctuations in the waveform magnitude and phase.

The noise responsible for variations in the phase of the waveform is called *phase noise*, which is distinct from the amplitude noise that affects the magnitude of the signal. The waveform of an ideal oscillator can be expressed as:

$$V_{OSC} = A \cdot cos(2\pi f_o t + \varphi_n(t)) \tag{27}$$

Here, f_o is the desired oscillation frequency and $\varphi_n(t)$ is the phase noise of an oscillator. As a variation in phase could be seen as a small variation in frequency, this is the visual representation of what phase noise does to the oscillator in reallity.

Figure 12 – Real oscillator spectrum



Source: Author

Figure 12 illustrates the spectrum of a real oscillator. The red line represents the impulse response of an ideal oscillator, while the green region corresponds to the spectral skirts caused by phase noise. It can be observed that, although the oscillator maintains a dominant frequency component, the presence of phase noise introduces fluctuations in the phase of the output signal over time. These fluctuations result in variations in the exact moments when the signal crosses a reference threshold, due to constructive and destructive interference among the nearby frequency components.

From control theory,

$$\frac{N_{OUT}(s)}{N_{IN}(s)} = \frac{1}{1 - H(s)} \tag{28}$$

Here $H(s) = H_1(s)H_2(s)$, and can also be rewritten as a truncated Taylor series as

$$H(j\omega) \approx H(j\omega_o) + \Delta\frac{dH}{d\omega} \tag{29}$$

And for stable oscillation, $H(j\omega_o) = 1$, then

$$\frac{N_{OUT}(s)}{N_{IN}(s)} = \frac{1}{-\Delta\omega\frac{dH}{d\omega}} \tag{30}$$

As paper (LEE; HAJIMIRI, 2000) describes the phase noise of an ideal oscillator, considering a fully discharged tank circuit, the main source of noise will be the thermal noise present due to the conductance of the tank.

$$\frac{\overline{i_n^2}}{\Delta f} = 4kTG \tag{31}$$

For a relatively small $\Delta\omega$, the offset frequency and the impedance for the tank circuit from a ω_o frequency can be approximated for the tank circuit.

$$Z(\omega_o + \Delta\omega) \approx j\frac{\omega_o L}{2\frac{\Delta\omega}{\omega_o}} \tag{32}$$

The current noise can be transformed in voltage noise if multiplied by the effective impedance seeing from the source. Write the impedance in therms of Q

$$Q = \frac{R}{\omega_o L} = \frac{1}{\omega_o L G} \tag{33}$$

Solving for L

$$|Z(\omega_o + \Delta\omega)| = \frac{1}{G}\frac{\omega_o}{2Q\Delta\omega} \tag{34}$$

This translates the dependency of the inductance L to Q and G

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTR\frac{\omega_o}{2Q\Delta\omega} \tag{35}$$

It can be observed that increasing the tank Q reduces the noise density, as the resonator filtering effect attenuates noise components outside the filter bandwidth, if all other parameters remain constant. This highlights the importance of resonator quality in oscillator design.

As shown in Equation (35), noise affects both the amplitude and phase of the signal. However, as described in (LEE; HAJIMIRI, 2000), comparing with thermodynamics, the noise power associated with amplitude and phase tends to be equal in equilibrium. Since most oscillators incorporate mechanisms that limits the amplitude, the amplitude noise component is suppressed, leaving phase noise as the dominant effect.

It is common practice to normalize the mean square noise voltage density with respect to the mean square carrier voltage and express the result in decibels. This normalized ratio is reported in dBc/Hz, indicating the noise power relative to the carrier power per unit bandwidth. The single-sideband noise spectral density is therefore typically presented in this format.

$$L\{\Delta\omega\} = 10log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right] \tag{36}$$

Equation (36) shows that phase noise at a frequency offset will improve by increasing the carrier power and Q, with k being the Boltzmann constant, the temperature T in Kelvin and the signal power P_{sig}. Increasing power improves the relation because the thermal noise is fixed because the conductance stays almost constant for the region, while improving Q will improve the ratio quadratically, due to the tank impedance falling by a factor $\frac{1}{Q\Delta\omega}$. (LEE; HAJIMIRI, 2000) informs that many simplifications were made, and the calculated results may diverge from the one extracted via simulation or tests, because there is additional noise due to the energy restoration circuit and switching. Furthermore, the ratio will flatten for a large offset rather than just keep dropping indefinably. Due to the details mentioned, Lesson made modifications that consider these simplifications and insert a factor that considers many other aspects, giving the equation

$$L\{\Delta\omega\} = 10log\left[\frac{2FkT}{P_{sig}}\left(1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right)\left(1+\left(\frac{\Delta\omega_1/f^3}{|\Delta\omega|}\right)^2\right)\right] \tag{37}$$

The modification considers F for the increased noise over the $\frac{1}{(\Delta\omega)^2}$ region and a unity addictive factor to consider the noise floor. Also, it includes a multiplicative factor for the behavior of $\frac{1}{|\Delta\omega|^3}$ for small offset frequencies. This equation is known as Lesson's equation and describes the phase noise for a oscillator.

For ring oscillators, the Q factor is poor, as the energy stored in the capacitance of the nodes is discharged each cycle. However, paper (HAJIMIRI; LIMOTYRAKIS; LEE,

1999) describes other equations that can be used to have an overview and calculate phase noise for ring oscillators.

For a single-end ring oscillator, considering that the current source consists of an impulse with area Δq in coulombs occurring at $t = \tau$, this will cause an instantaneous voltage change in the node such that

$$\Delta V = \frac{\Delta q}{C_{node}} \tag{38}$$

Where the C_{node} is the effective capacitance on the node at the injection time. For a small ΔV, the phase shift $\varphi(t)$ will be proportional to the injection charge

$$\Delta\varphi = \Gamma(\omega_o t)\frac{\Delta V}{V_{swing}} = \Gamma(\omega_o t)\frac{\Delta q}{q_{swing}} \tag{39}$$

Where V_{swing} is the voltage swing in the capacitance and $q_{swing} = C_{node} \cdot V_{swing}$. There is a dimensionless function $\Gamma(\omega_o t)$ that is the time-varying periodicity constant with 2π. As it is large when the perturbation causes a large phase shift and small when it causes a small perturbation, $\Gamma(x)$ receives the name of *impulse sensitivity function*, or ISF, which will not be fully covered in this work.

Unlike amplitude noise, phase shifts persist over time, as subsequent signal transitions remain displaced by the same amount. As a result, the phase impulse response of an oscillator takes the form of a time-varying step function. The impulse response of the system can therefore be described as:

$$h_\varphi(t,\tau) = \frac{\Gamma(\omega_o t)}{q_{max}}u(t-\tau) \tag{40}$$

The instantaneous phase of the circuit can be calculated with the following equation.

$$\varphi(t) = \int_{-\infty}^{\infty} h_\varphi(t,\tau)i(\tau)d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_o t)}{q_{max}}i(\tau)d\tau \tag{41}$$

Thus, the single-sideband phase noise of an ring oscillator can be found by

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2} \cdot \frac{\frac{\overline{i_n^2}}{\Delta_f}}{q_{max}^2} \tag{42}$$

With Γ_{rms}^2 being the RMS value of the ISF, $\frac{\overline{i_n^2}}{\Delta_f}$ being the single-sideband power spectral density of the noise current source and f_{off} being the carrier offset frequency.

Increasing the number of stages N will lead to a reduction in the peak of the ISF function, mainly because the waveform transitions become faster with a higher N, since the sensitivity during the transition is inverse to the slope, the peak will drop. The width of the lobes will decrease with greater increase N, since each transition will now occur within a small fraction of the period. Based on this observartions, it is possible to approximate the ISF with a triangular shape. The ISF has a maximum of $\frac{1}{f'_{max}}$, assuming equal rise and fall time,

Increasing the number of stages N results in a reduction of the peak of the ISF, primarily because the waveform transitions become steeper as N increases. Since sensitivity during transitions is inversely proportional to the slope of the waveform, a steeper slope leads to a lower ISF peak. Additionally, the width of the ISF lobes narrows with increasing N, as each transition occupies a smaller fraction of the oscillation period. On the basis of these observations, the ISF can be approximated by a triangular shape. The ISF reaches a maximum of $\frac{1}{f'_{max}}$, where f'_{max} is the maximum slope of the waveform, with the triangular width of approximately $\frac{2}{f'_{max}}$, assuming equal rise and fall times. Under this approximation, the root mean square of the ISF, Γ_{rms} can be estimated as

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(x)dx = \frac{4}{2\pi}\int_0^{\frac{1}{f'}} x^2 dx = \frac{2}{3\pi}\left(\frac{1}{f'_{max}}\right)^3 \tag{43}$$

The stage delay is proportional to the rise

$$\hat{t}_D = \frac{\eta}{f'_{max}} \tag{44}$$

And the period is $2N$ longer than in a single stage delay,

$$2\pi = 2N\hat{t}_D = \frac{2N\eta}{f'_{max}} \tag{45}$$

Here η is a proportionality constant close to unity and $\hat{t}_D$ is the normalized stage delay. It is possible to find a approximate value for the Γ_{rms} as

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}\frac{1}{N^{1.5}}} \tag{46}$$

For a single-ended CMOS ring oscillator, the total channel noise from the NMOS and PMOS devices with input and output in $\frac{V_{DD}}{2}$ is

$$\frac{\overline{i_n^2}}{\Delta_f} = \left(\frac{\overline{i_n^2}}{\Delta_f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta_f}\right)_P = 4kT\gamma\mu_{eff}C_{ox}\frac{W_{eff}}{L}\Delta V \tag{47}$$

With

$$W_{eff} = W_N + W_P$$

$$\mu_{eff} = \frac{\mu_N W_N + \mu_P W_P}{W_N + W_P}$$

$$\Delta V = \frac{V_{DD}}{2} - V_T$$

With the total power dissipation being described as

$$P = 2\eta N V_{DD} q_{max} f_o \tag{48}$$

And assuming simmetry with $\mu_N W_N = \mu_P W_P$, t_D being the delay of each stage and t_r being the rise time and t_f being the fall time,

$$f_o = \frac{1}{2Nt_D} = \frac{1}{\eta N(t_r + t_f)} \approx \frac{\mu_{eff} W_{eff} C_{ox} \Delta V^2}{2\eta N L q_{max}}$$

The phase noise for this topology can be approximated as

$$L\{\Delta f\} \approx \frac{8}{3\eta}\frac{kT}{P}\frac{V_{DD}}{V_{char}}\frac{f_o^2}{\Delta f^2} \tag{49}$$

Where V_{char} is the *characteristic voltage* of the device, for long-channel operation being defined as $V_{char} = \frac{\Delta V}{\gamma}$

For a differential CMOS ring oscillator, considering I_{tail} as the differential pair bias current,the total power dissipation can be described as

$$P = N \cdot I_{tail} \cdot V_{DD} \tag{50}$$

The frequency of oscillation can be approximated by

$$f_o = \frac{1}{2Nt_D} \approx \frac{1}{2\eta N t_r} \approx \frac{I_{tail}}{2\eta N q_{max}} \tag{51}$$

Only the noise of the differential transistors and the load are accounted for. The total current noise is given by

$$\frac{\overline{i_n^2}}{\Delta_f} = \left(\frac{\overline{i_n^2}}{\Delta_f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta_f}\right)_{load} = 4kTI_{tail}\left(\frac{1}{V_{char}} + \frac{1}{R_L I_{tail}}\right) \tag{52}$$

Thus, the expression for the phase noise in differential ring oscillators can be described as

$$L_{min}\{\Delta f\} = \frac{8}{3\eta}N\frac{kT}{P}\left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}}\right)\frac{f_o^2}{\Delta f^2} \tag{53}$$

2.3.1 Discussion

From (DJEMOUAI; SAWAN; SLAMANI, 2001) and (HAJIMIRI; LIMOTYRAKIS; LEE, 1999) perspectives, the oscillator phase noise performance is related to how much the noise sources perturb its phase over time. LC oscillators can achieve better phase noise performance primarily due to their quality factor Q, enabling good energy storage and filtering of noise components that do not align with the resonant frequency. In these circuits, the tank acts as a resonant filter, effectively mitigating phase perturbations caused by noise sources.

In contrast, ring oscillators operate based on cascaded delay stages that inherently exhibit a lower quality factor (Q), making them more susceptible to phase disturbances, especially near signal transitions. As a result, ring oscillators typically show higher phase noise close to the carrier frequency. Despite their benefits, such as compact size, low power consumption, and wide frequency tunability, their architecture limits noise performance when compared to LC-based oscillators.

For ring oscillators producing nearly square wave outputs, phase noise is most critical during the transitions between logic levels, where the output voltage changes rapidly. During these transitions, any variation in the delay of the inverters, caused by any noise source or mismatch, directly affects the time at which the signal crosses a threshold. Since oscillation depends on the precise timing of these transitions, small disturbances can shift the timing unpredictably, leading to phase deviation.

Therefore, the main contributors to phase noise in ring oscillators are fluctuations in the delay of each stage, which are strongly influenced by the charging and discharging currents and transistor characteristics.

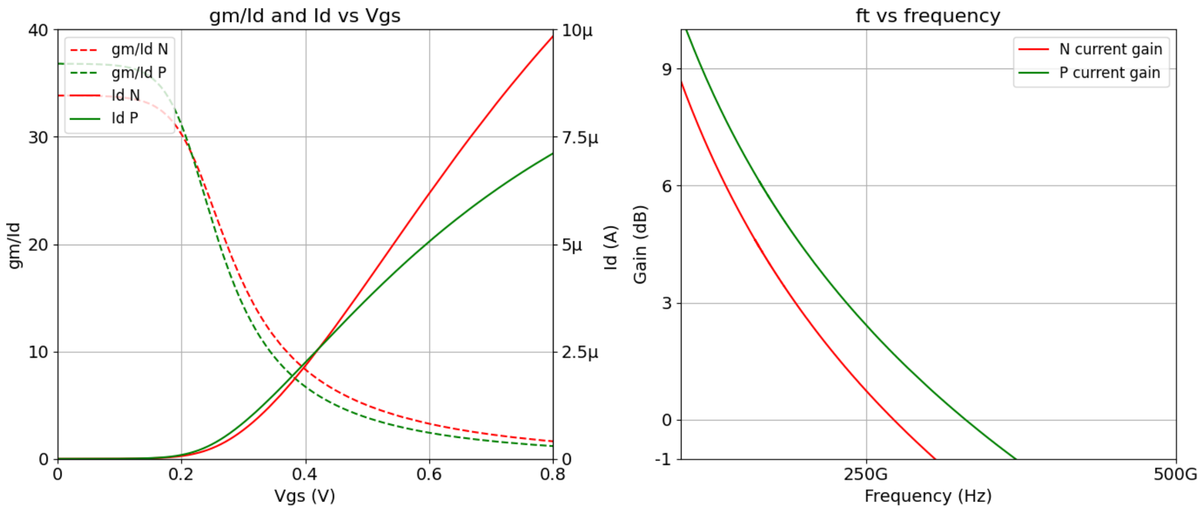
3 DESIGN

The Voltage-Controlled Oscillator (VCO) presented in this work was developed as part of an internal project at Chipus Microelectronics, utilizing a 12 nm FinFET technology. The VCO is intended for integration within a Phase-Locked Loop (PLL) block, serving as a clock reference generator for a digital system. As the project remains under active development, certain specifications were progressively defined and refined throughout the design process to meet evolving project requirements.

3.1 PARAMETER EXTRACTION

This section is dedicated to the early stages of the design, where the focus was on discovering the limitations and capabilities of the technology.

Figure 13 – Technology parameter extraction simulations



Source: Author

From the g_m/I_D and I_D vs V_{gs} graph, and using ACM methodology, it is possible to approximate the threshold voltage V_T and the characteristic current I_{SH} of the transistor, with I_{SH} serving as a reference value for the device operation. Additionally, the transition frequency f_t, defined as the frequency at which the current gain becomes unity, can be obtained from the graph f_t vs. frequency.

From the simulations, the following values were extracted.

Table 5 – Extracted parameters

Parameter	N type	P type	Unit
V_T	0.288	0.265	V
I_{SH}	171	148	nA
f_t	272.21	330.17	GHz

Source: Author

Table 5 show the values obtained through simulation for the defined parameters. The V_T and I_{SH} are approximations for the model, that still valid for the FinFET technology, and f_t values do not differ too much from the article (SINGH et al., 2017), being used as guidelines for the next steps.

3.2 DESIGN DESCRIPTION AND SPECIFICATIONS

The Voltage-Controlled Oscillator (VCO) presented in this work was developed as part of an internal project at Chipus Microelectronics, utilizing a 12 nm FinFET technology. The VCO is intended for integration within a Phase-Locked Loop (PLL) block, serving as a clock reference generator for a digital system. As the project remains under active development, certain specifications were progressively defined and refined throughout the design process to meet evolving project requirements.

The PLL is designed to deliver a stable 16 GHz clock output, maintaining this target frequency despite variations in supply voltage, ambient temperature, and fabrication process, thereby ensuring reliable operation for the subsequent system blocks.

In this technology, the selected family of transistors operates with a maximum drain-to-source voltage V_{DS} of 0.8 V. Although the process library includes devices capable of withstanding higher voltages, these are intended primarily for I/O applications. Transistors with shorter channel lengths, critical for achieving higher output frequencies, are designed to operate within this limit V_{DS}. The positive supply voltage V_{DD} is modeled using an ideal voltage source with a $\pm 10\%$ variation, resulting in a range from 0.72 V to 0.88 V.

Given the nature of the target application, the circuit must operate reliably across all intended environmental conditions. Consequently, the design is validated in a temperature range of -40 $^{\circ}$C to 125 $^{\circ}$C and in all main parts of the process, including slow-slow, slow-fast, typical-typical, fast-slow and fast-fast, ensuring robust performance under fabrication and environmental variability.

For clock generation circuits, an important performance metric is the duty cycle, which represents the proportion of the clock period during which the signal remains at the logic high level. The target is typically a 50% duty cycle, ensuring a symmetric waveform. Additionally, rise and fall times should remain below 5% of the clock period to maintain signal integrity and ensure proper timing behavior in subsequent digital stages.

Phase noise is one of the most critical metrics in oscillator design. Achieving low phase noise translates to a cleaner and more reliable signal for downstream applications. However, this often comes at the cost of increased circuit complexity and higher power consumption. The phase noise specification adopted in this work was defined based on references from the literature and internal design reviews to ensure alignment with the project's performance targets.

The output voltage of the VCO must remain close to V_{DD}, as it will directly interface with subsequent circuit blocks. Power consumption is also a key design constraint, with a target of less than 2 mW at all process corners and operating conditions, considering the complete set of blocks developed in this work.

Table 6 – Tests combinations

<table>
<tr><td colspan="5">Simple PVT</td></tr>
<tr><td>Parameter</td><td>Minimal</td><td>Typical</td><td>Maximum</td><td>Unit</td></tr>
<tr><td>Supply voltage</td><td>0.72, 0.88</td><td>0.80</td><td>0.72, 0.88</td><td>V</td></tr>
<tr><td>Temperature</td><td>-40, 125</td><td>25</td><td>-40, 125</td><td>$^\circ C$</td></tr>
<tr><td>MOSCAP</td><td>slow-slow</td><td>typical-typical</td><td>fast-fast</td><td></td></tr>
<tr><td>MOM</td><td>slow-slow</td><td>typical-typical</td><td>fast-fast</td><td></td></tr>
<tr><td>RES</td><td>slow-slow</td><td>typical-typical</td><td>fast-fast</td><td></td></tr>
<tr><td colspan="5">Possibilities = 9</td></tr>
<tr><td colspan="5">Medium PVT</td></tr>
<tr><td>Parameter</td><td colspan="3">Combinations</td><td>Unit</td></tr>
<tr><td>Supply voltage</td><td colspan="3">0.72, 0.88</td><td>V</td></tr>
<tr><td>Temperature</td><td colspan="3">-40, 125</td><td>$^\circ C$</td></tr>
<tr><td>MOSCAP</td><td colspan="3">slow-slow, typical-typical, fast-fast</td><td></td></tr>
<tr><td>MOM</td><td colspan="3">slow-slow, typical-typical, fast-fast</td><td></td></tr>
<tr><td>RES</td><td colspan="3">slow-slow, typical-typical, fast-fast</td><td></td></tr>
<tr><td colspan="5">Possibilities = 108</td></tr>
<tr><td colspan="5">Complete PVT</td></tr>
<tr><td>Parameter</td><td colspan="3">Combinations</td><td>Unit</td></tr>
<tr><td>Supply voltage</td><td colspan="3">0.72, 0.8, 0.88</td><td>V</td></tr>
<tr><td>Temperature</td><td colspan="3">-40, 25, 125</td><td>$^\circ C$</td></tr>
<tr><td>MOSCAP</td><td colspan="3">slow-slow, slow-fast, typical-typical,
fast-slow, fast-fast</td><td></td></tr>
<tr><td>MOM</td><td colspan="3">slow-slow, typical-typical, fast-fast</td><td></td></tr>
<tr><td>RES</td><td colspan="3">slow-slow, typical-typical, fast-fast</td><td></td></tr>
<tr><td colspan="5">Possibilities = 405</td></tr>
</table>

Source: Author

To optimize simulation time, Table 6 presents the structure of the different simulation sets. The Simple PVT set evaluates performance under three key operating conditions, focusing on typical and near-critical corners to provide a general overview of circuit behavior. The Medium PVT set expands coverage to include a broader range of conditions, capturing more edge-case variations. Finally, the Complete PVT set encompasses all possible combinations of process, voltage, and temperature, ensuring full validation across the entire design space.

Table 7 – VCO open-loop specifications

Parameter	Minimal	Typical	Maximum	Unit
VCO manageable frequency range	14	16	18	GHz
VCO output voltage		V_{DD}		V
Duty Cycle	47.5	50	52.5	%
Rise time			5	%
Fall time			5	%
Phase Noise @ 100 kHz			-60	dBc/Hz
Phase Noise @ 1 MHz			-80	dBc/Hz
Phase Noise @ 10 MHz			-100	dBc/Hz
Phase Noise @ 100 MHz			-120	dBc/Hz
Phase Noise @ 1 GHz			-140	dBc/Hz
Power consumption			2	mW
Measurement	Simulation			

Source: Author

Table 7 summarizes the design specifications defined for the VCO. The target output frequency is 16GHz under typical operating conditions, with an acceptable tuning range from 14GHz to 18GHz to provide sufficient margin for the PLL to lock at the desired frequency despite process, voltage, or temperature variations. The output voltage swing must reach V_{DD} to ensure compatibility with subsequent blocks, and the duty cycle is specified at 50 %. The maximum allowable phase noise for each frequency offset Δ_f is also listed in the table and follows the expected trend for this parameter. Additionally, a maximum power consumption of 2 mW was established to comply with future Power Management Unit (PMU) design constraints.

3.3 OSCILLATOR

3.3.1 Description

This block constitutes the core of the voltage-controlled Oscillator, as it receives the control voltage and generates the corresponding output signal at the specified frequency. It must provide a voltage swing sufficient to properly drive the subsequent buffer stage, while ensuring the output amplitude remains low enough to preventint transistor to work in saturation within the voltage-controlled current source.

The oscillator design specifications are defined as

Table 8 – Oscillator design specifications

Parameter	Minimal	Typical	Maximum	Unit
Oscillator swing	300	450	600	mV
Phase Noise @ 1 MHz			-80	dBc/Hz
Power			0.5	mW
Duty cycle	47.5	50.0	52.5	%

Source: Author

The minimal value of the voltage swing was defined so that it can excite the buffer stage, while the maximum value was defined because the transistors of the voltage controlled current source would not be saturated. The power consumption of the oscillator was limited, so it does not need more than $0.5mW$ to oscillate. Also, phase noise at $1MHz$ will be used as a metric to evaluate different oscillator performance over noise, as including other blocks before will increase this value.

3.3.2 Design

Crystal oscillators are unsuitable for the target application due to limited frequency range, narrow tunability, and lack of on-chip integration. While LC oscillators offer better phase noise and frequency stability, their performance is highly dependent on the tank circuit quality factor, requiring large passive components that increase area and limit tuning range. Given these constraints, alternative topologies such as ring oscillators are considered more appropriate for compact, high-frequency designs.

The ring oscillator topology was chosen due to its inherent advantages aligned with the design requirements of a PLL. Its wide frequency tuning range supports frequency locking across multiple bands, which is essential for flexible PLL operation. Additionally, the compact layout of the ring oscillators makes them highly suitable for integration in dense ASIC environments, avoiding the large area overhead associated with on-chip inductors used in LC-based designs. The topology also efficiently covers the target frequency range, like 16 GHz, without the need for bulky passive components.

Despite higher phase noise and power consumption compared to LC oscillators, these trade-offs are manageable through careful transistor sizing, supply regulation, and the inclusion of output buffering and current control circuits. Therefore, the ring oscillator offers a practical balance between performance, area efficiency, and frequency agility for the intended application.

As seen before, ring oscillators can be implemented using either single-ended or differential architectures. In the single-ended configuration, the oscillator and buffer consist of a single chain of inverters, which results in less transistors being utilized, leading to lower area and improved power efficiency. In contrast, the differential implementation employs cross-coupled inverter outputs, effectively forming a latch with two pairs of inverters. This configuration requires approximately four times more transistors, increasing both area and power consumption. However, it offers significant advantages in terms of duty cycle symmetry and frequency stability, making it a more robust option for applications requiring precise timing.

Due to the latching mechanism present in the differential circuit, as one output transitions low, the cross-coupled feedback ensures that the complementary output transitions high. This behavior promotes a duty cycle close to 50 %, improving signal symmetry. Additionally, since both signal paths are interconnected, any mismatch between transistors or variations across the silicon die is mitigated, with the slower path dictating the overall oscillation timing. An additional advantage of the differential topology is the availability of complementary outputs with a 180° phase shift, which can be used as reference signals elsewhere in the system.

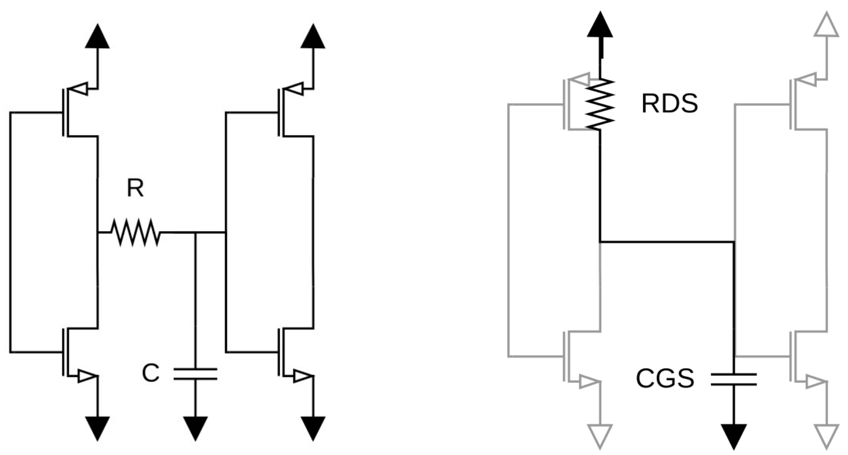
The delay cells are a critical component of the ring oscillator, as they provide the necessary phase shift to satisfy the Barkhausen criteria. One possible implementation involves adding resistors *R* and capacitors *C* to introduce the required delay. In the case of a three-stage ring oscillator, the phase shift needed is 60°per stage, with R = 1 kΩ requiring a capacitance in the order of approximately 10 fF, comparable to the intrinsic gate-source parasitic capacitance C_{gs} of the transistors in this technology node.

This observation enables an alternative design strategy that uses the intrinsic parasitic elements of the transistors to implement the delay cell, removing the need for specific passive components. Fine-tuning of the oscillation frequency is then achieved by modulating the inverter delay through control of the starving current, using a voltage-controlled current source.

Figure 14 – Different delay cell comparison

(a) Delay cell using *R* and *C* devices

(b) Delay cell using transistor R_{DS} and G_{GS}



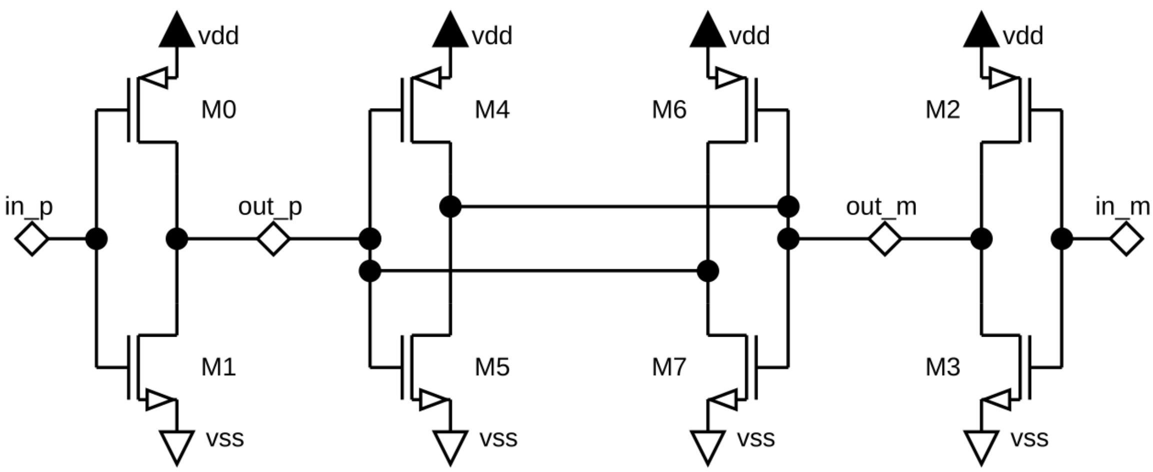
Source: Author

For a five-stage oscillator, using Equation (19) with bias current I = 500 μA and a supply voltage V_{DD} = 0.8 V, for an oscillation frequency of 16 GHz, it requires a capacitance of approximately C = 7.81 fF. This value is compatible with the intrinsic capacitance of the transistors in this technology. For the specific device model used in this work, operating near the minimum dimensions, the capacitance seen from the previous stage, including metalization effects and parasitic contributions from the layout, is approximately C = 6.98 fF. Therefore, it is possible to implement the oscillator without the need for external resistors or capacitors, relying only on the intrinsic characteristics of the transistors and the control of the current to achieve the target frequency.

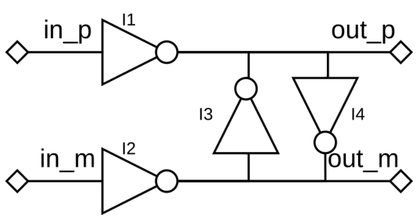
Figure 14(a) illustrates a delay cell implementation using integrated resistor R and capacitor C, and Figure 14(b) employs the intrinsic transistor parameters R_{ds} and C_{gs} to achieve the required delay. These parasitic components exhibit magnitudes comparable to those of discrete elements that would otherwise be introduced. The approach shown in (b) offers significant advantage, as it reduces the area required per stage, since the parasitic elements are inherent to the inverter structure, and mitigates additional parasitic effects introduced by discrete passive components in the substrate, such as unintended capacitances and increased series resistance. Otherwise, these factors would increase the current consumption of the circuit.

Figure 15 – Differential inverter circuit implemented

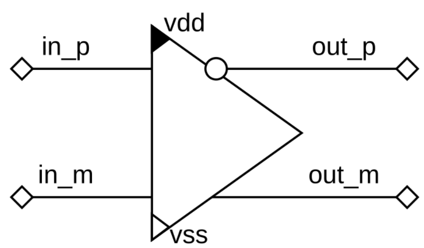
(a) Differential inverter transistors schematic



(b) Equivalent circuit



(c) Differential inverter block symbol



Source: Author

Figure 15 presents the schematic of the ring oscillator. Subfigure 15(a) illustrates the transistor-level implementation from M0 to M7, while 15(b) shows the system-level inverter diagram, and 15(c) depicts the symbolic representation of a single differential inverter stage. Transistors M0 and M1 form inverter I1, M2 and M3 form inverter I2, M4 and M5 form inverter I3, and M6 and M7 form inverter I4. In this configuration, I1 and I2 constitute the upper and lower differential paths, respectively, whereas I3 and I4 serve as cross-coupled latching inverters to ensure proper oscillation.

The cross-coupled topology is implemented to ensure strong feedback between the differential nodes, enabling synchronized operation of both transistor branches. This configuration promotes enhanced switching transitions and improves signal symmetry, effectively aiding in achieving a near 50% duty cycle. By regenerative reinforcing each transition, the topology enhances signal integrity and minimizes mismatch-induced imbalances, which is especially critical at high frequencies. In addition, it helps stabilize the differential swing and reduces phase noise by maintaining a tighter timing between complementary signals.

To improve the analysis by accounting for additional parasitic effects that will arise in a real circuit, a model containing device imperfections was added in the simulations. This model, provided by the foundry, includes parasitic effects from metal interconnections, introducing another level of non-ideal behavior to the actual silicon implementation. Furthermore, a net parasitic capacitance of p_{cap} = 1 fF was added in the nodes between the ring oscillator stages and the ground, to emulate the layout-induced capacitance that will be present after fabrication.

To determine the optimal number of stages for the ring oscillator, four different transistor sizing configurations were evaluated across two distinct transistor families. Although the latching inverters do not require a sizing identical to that of the line inverters, the channel length was kept consistent across all transistors to facilitate layout regularity.

In this configuration, inverters I1 and I2 drive the primary capacitive loads, while I3 and I4 form the cross-coupled latching feedback. Therefore, it is not necessary for both groups to share the same transistor widths. Since I1 and I2 must operate with higher switching speeds to charge and discharge the next stages, transistors in I3 and I4 can be dimensioned with smaller widths. Based on guidelines provided by an external consultant, a width ratio of 4:1 between line and latch inverters offers a favorable relation between power consumption and switching performance, as it minimizes current through the latches while maintaining high-speed operation in the main signal path. Table 9 summarizes the four transistor sizing configurations considered.

Table 9 – Ring oscillator stages sizing

Type	M0,M1,M2 and M3				M4, M5, M6 and M7			
	Effective Width (W_{eff}) and Length (L) in nm							
	Multiplier	Fins	W_{eff}	L	Multiplier	Fins	W_{eff}	L
A	1	6	250	16	1	2	58	16
B	1	6	250	36	1	2	58	36
C	1	10	442	16	1	3	106	16
D	4	4	154	16	1	4	154	16

Source: Author

The sizing of the oscillator stages was defined through empirical testing using the components available in the design library. The approach prioritized minimizing the channel lengths whenever possible, with the aim of increasing speed and reducing parasitic. However, careful attention was also given to maintaining the sizing ratio between inverters I1 and I2, the signal path, and I3 and I4, latching path, in alignment with the proportions recommended by the external consultant.

These width and length ratios were chosen to minimize both the number of fins and the effective width required for each transistor while still preserving the critical sizing relationship between the inverter pairs. This balance ensures proper regeneration in the cross-coupled inverters and consistent signal propagation in the differential path , contributing to the overall stability and symmetry of the oscillator.

Type A corresponds to the minimum allowable sizing configuration within the design rules of the chosen technology. Its associated parasitic components, particularly C_{gs} and R_{ds} serve as a baseline for comparison. Type B employs a longer channel length, allowing analysis of the impact of R_{ds} on the oscillator behavior. Type C, on the other hand, is designed to assess the influence of C_{gs} on the oscillation frequency and overall performance. Finally, Type D is proposed as a uniform sizing alternative, where all transistors in the oscillator share the same dimensions. This option supports layout regularity and may simplify the placement and routing process.

The initial test was carried out under simple PVT combinations, as its objective is to evaluate the magnitude of each parameter and enable direct comparison between configurations. To evaluate the performance of different oscillator configurations, an ideal DC current source can be connected to the oscillator V_{DD}, supplying a fixed current that enables oscillation at 16 GHz under typical conditions. By maintaining this constant current, variations in PVT conditions can be observed, allowing analysis of the oscillator behavior across different process, voltage, and temperature corners. This test demonstrates how the oscillator parameters vary when the starving current remains constant despite environmental and process variations.

Table 10 – Testbench for oscillator design

Testbench		
Simulations		
Type	Stimulus	Objective
Shooting Newton Periodic Steady State (PSS)	Force DC supply voltage to a DC bias current source biasing V_{DD} to oscillate with 16 GHz at typical	Evaluate the oscillator steady state behavior
Shotting Newton Noise	Made with the results of (PSS)	Evaluate the noise interference
Observed parameters		
Parameter	Objective	
Oscillator output swing	Measure the maximum and minimum voltage swing due PVT variation	
Oscillator frequency	Measure the maximum and minimum oscillator frequency due PVT variation	
Phase Noise	Measure the noise component at specified frequency delta	

Source: Author

Table 11 – Results for different number of stages and transistor sizing

PVT for different Ring oscillators metalization library and 1 fF parasitic capacitance						
Test	Frequency (GHz)		Swing (mV)		I_{meas}	Maximum Phase Noise @ 1MHz
	Min	Max	Min	Max	(μA)	(dBc/Hz)
Low threshold voltage						
3 Stages - A	15.46	16.43	509.91	628.59	172	-76.00
B	15.37	16.47	669.06	756.95	246	-79.89
C	15.48	16.37	505.07	628.99	238	-77.41
5 Stages - A	15.29	16.66	755.95	854.46	445	-81.20
B	14.71	16.79	1124.5	1264.7	825	-85.78
C	15.42	16.50	765.56	869.58	650	-83.04
7 Stages - A	14.93	16.91	1272.9	1433.8	1257	-85.30
B	11.07	12.91	1389.6	1592.5	1210	-90.56
C	13.68	15.00	1066.3	1166.8	1283	-87.29
Ultra-low threshold voltage transistors						
3 Stages - A	15.11	17.18	325.15	456.32	220	-75.07
B	15.55	16.43	519.44	608.47	193	-77.52
C	15.43	16.45	365.20	487.13	182	-74.23
5 Stages - A	15.39	16.53	583.34	680.24	347	-79.38
B	14.88	16.71	863.91	951.42	602	-83.92
C	15.45	16.39	575.39	680.10	509	-80.71
7 Stages - A	15.26	16.52	605.10	706.72	970	-85.33
B	12.25	14.29	1310.8	1499.8	1300	-89.02
C	15.09	16.72	1053.5	1153.4	1585	-86.18
Extra ultra-low threshold voltage transistors						
5 Stages - D	15.59	16.38	462.69	575.94	515	-81.12

Source: Author

The value of I_{meas} is obtained by sweeping the DC current source and evaluating the current needed for a stable oscillation near 16 GHz. As seen in Table 11, some combinations could not achieve all the specifications. As the bias current is imposed by an ideal current source, it is possible that the swing, a parameter that should not exceed V_{DD}, is achieving values much higher than possible, which means that the oscillator is not viable for the application. The use of a ideal DC current source is made to evaluate the oscillator isolated performance, with no dependency of other circuits.

As seen before, phase noise, oscillation frequency, and swing depend on the starving current, so increasing the current will directly increase the oscillation frequency and swing, while decreasing the phase noise value. As oscillators with fewer stages will need less current, it is expected that in comparison, it will have lower phase noise and lower swing than those of oscillators with more stages.

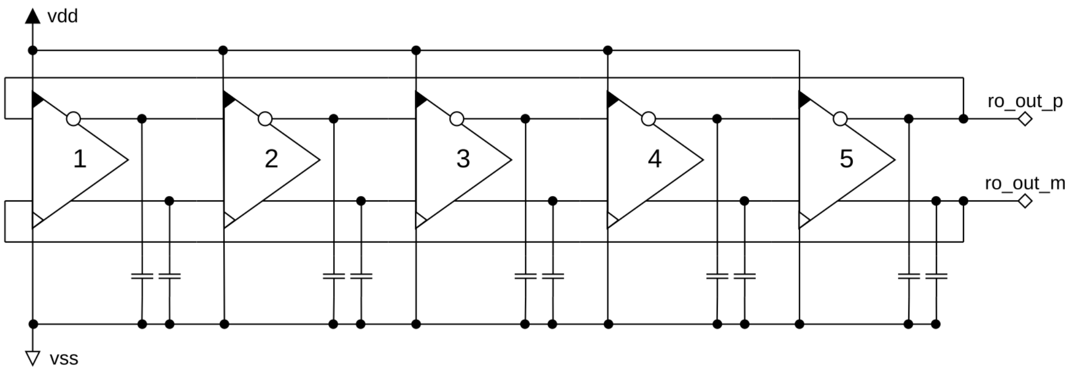
As seen in Table 11, certain configurations failed to meet all specified requirements. As the bias current is imposed by an ideal current source, it is possible that the swing, a parameter that should not exceed V_{DD}, achieves values much higher than possible, meaning that the oscillator combination is not suitable for the application. As discussed previously, phase noise, oscillation frequency, and output swing are directly influenced by the starving current, thus, increasing the current results in proportional increases in these parameters.

For the low threshold voltade model, three-stage oscillators exhibited difficulty in meeting the phase noise and output swing specifications. In the case of five-stage configurations, although the phase noise criteria were satisfied, the output swing exceeded the maximum allowed voltage, indicating a violation of physical constraints and resulting in inconsistent simulation results. Additionally, tests conducted with seven-stage oscillators failed to achieve the target oscillation frequency and simultaneously exceeded the limits for both output swing and current consumption, with these configurations unsuitable for the intended application.

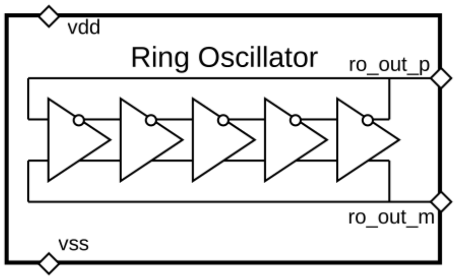
A similar behavior was observed for the ultra-low threshold voltage transistors, however, the type D sizing was evaluated in the five-stage oscillator, as it presented results closer to the desired specifications, with minimal deviations. This sizing alternative focused on the use of multiple identical transistors instead of a single device with varied dimensions, also aiming in layout implementation. A five-stage ring oscillator using type D sizing was determined to be the most suitable configuration for the oscillator block, since under PVT variations, all process corners achieved output swing and oscillation frequency within the specified margins, while maintaining relatively low current consumption. Additionally, the maximum phase noise at 1 MHz offset remained below the maximum defined acceptable threshold.

Figure 16 – Ring oscillator design

(a) Ring oscillator schematic



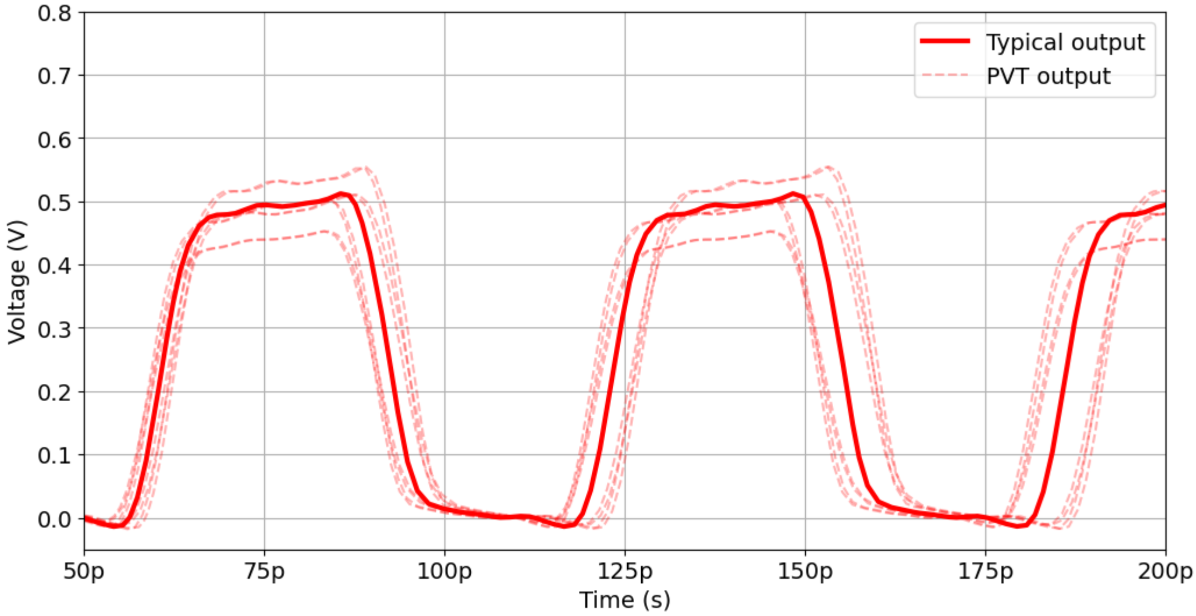
(b) Ring oscillator symbol



Source: Author

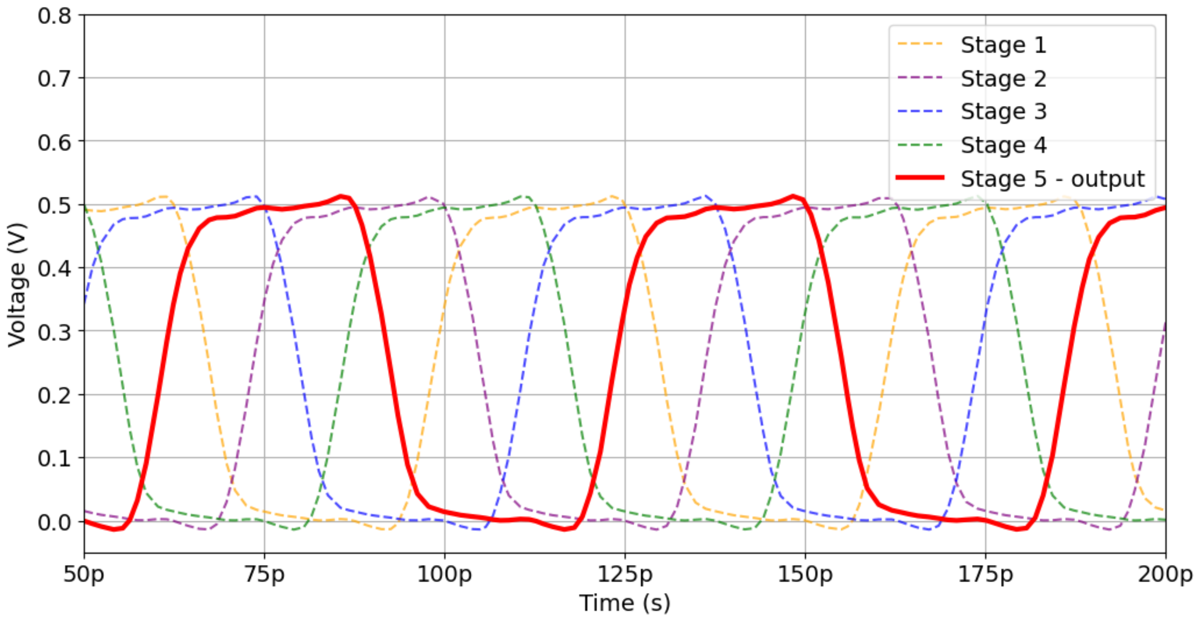
Figure 16 shows the design for the ring oscillator, using the type of ultra-low threshold voltage model and the size of the D type transistor, with parasitic capacitance between the nets and the substrate.

Figure 17 – Ring oscillator swing with PVT variation over time



Source: Author

Figure 18 – Ring oscillator internal stages swing over time



Source: Author

Figure 17 illustrates the output waveform over time under typical operating conditions and with PVT variations. As shown, the signal swing remains within the expected maximum and minimum limits, and the oscillation frequency exhibits only minor deviations from the target value. The waveform closely resembles a square wave, with a visually symmetric duty cycle around 50%, which is advantageous for subsequent circuit blocks, as it aligns well with the design specifications.

Figure 18 shows the swing over each stage for the typical operating condition. As each inverter has the same sizing of the others, the waveforms are similar, and each stage is adding a phase shift of 36° for the next stage, as intended.

Table 12 – Oscillator results for complete PVT simulation

Parameter	Minimal	Maximum	Mean	Unit	Match specification
Frequency	15.59	16.38	15.95	*GHz*	Yes
Swing	462.98	575.94	521.01	mV	Yes
PN @ 100 kHz	-66.93	-61.12	-64.22	dBc/Hz	Yes
PN @ 1 MHz	-86.93	-81.12	-84.22	dBc/Hz	Yes
PN @ 10 MHz	-106.94	-101.12	-104.22	dBc/Hz	Yes
PN @ 100 MHz	-126.95	-121.12	-124.23	dBc/Hz	Yes
PN @ 1 GHz	-147.05	-141.07	-144.24	dBc/Hz	Yes
Power	229.5	274.35	258.80	μW	Yes
Duty-cycle	50.24	51.24	50.73	%	Yes

Source: Author

The results presented in Table 12 were obtained under complete variation in PVT, which included all possible process, voltage, and temperature conditions. All oscillator design specifications were met, confirming the suitability of this block for integration into the subsequent buffer stage.

3.4 BUFFER

3.4.1 Description

The main motivation for adding a buffer in the VCO is to isolate it from subsequent stages that will utilize the generated signal, while also ensuring a voltage swing close to the V_{DD} level. However, since the buffer acts as an additional load to the oscillator, it increases the current required to charge the output stage capacitance, directly impacting the oscillator current consumption and performance.

As seen before, the voltage swing from the oscillator may vary due to the supply voltage, temperature, fabrication process, or even the biasing current. For sensitive circuits that receive this signal, this variation can interfere in the signal use, as it may not achieve a threshold value to define whether the signal is high or low for digital circuits, thus not activating posterior circuits. The buffer specifications are defined so it receives the signals between the minimum and maximum oscillator swing values, and amplify to a value closer to V_{DD}, maximizing the swing range. In addition, another function associated with the buffer is to isolate the oscillator from the circuits that will use the signal. As discussed before, connecting more circuits to the oscillator output pins will increase the load attached to the oscillator, interfere in the oscillation frequency, and increase the current consumption to achieve the desired oscillation.

As discussed previously, the oscillator voltage swing can vary as a result of fluctuations in supply voltage, temperature, fabrication process, or even bias current. For sensitive circuits receiving this signal, these variations may compromise signal integrity, particularly in digital applications where the swing may not reach the required threshold voltage to distinguish between logic high and low levels. To address this, the buffer is specified to accept input signals ranging between the minimum and maximum oscillator swing levels and to amplify them to a value closer to V_{DD}, maximizing the output swing, also, the combined performance of the oscillator designed previously and buffer must not exceed the output phase noise performance of the specified value. In addition, the buffer serves the critical function of isolating the oscillator from subsequent circuit stages. The buffer design specifications are shown in the next table.

Table 13 – Buffer design specifications

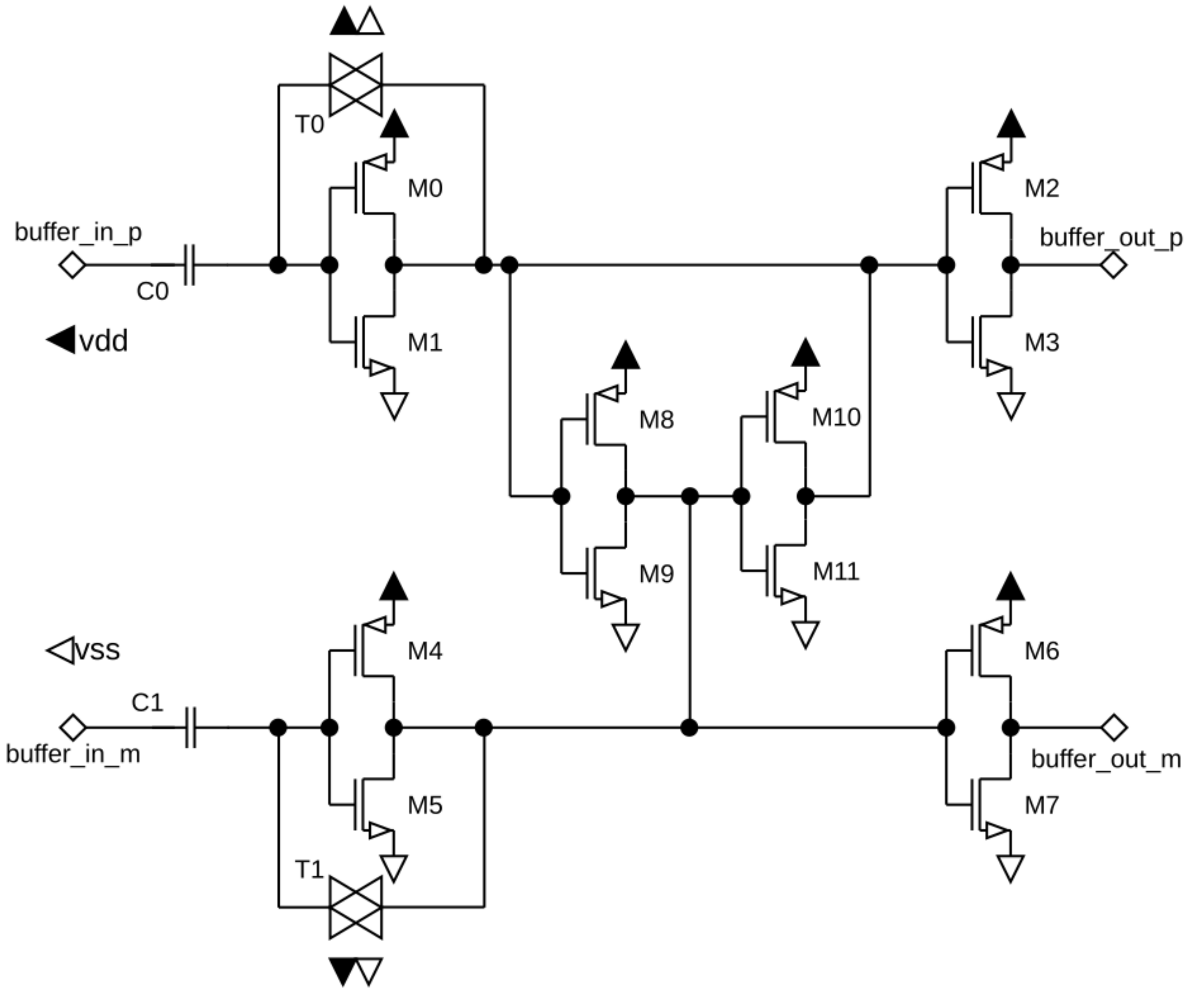
Parameter	Minimal	Typical	Maximum	Unit
Buffer swing		V_{DD}		mV
Phase Noise @ 1 MHz			-80	dBc/Hz
Power			0.5	mW
Duty cycle	47.5	50.0	52.5	%
Rise time			5	%
Fall time			5	%

Source: Author

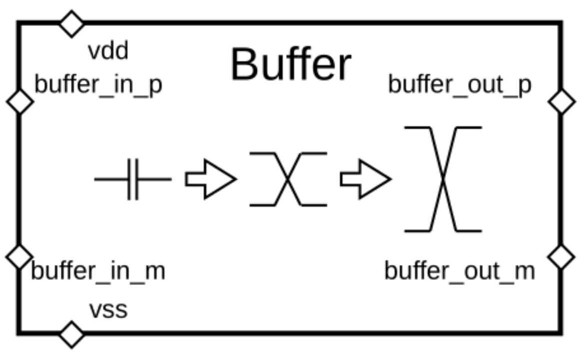
As the designed oscillator voltage swing ranges from almost 300 mV to 600 mV, it is expected that the buffer will output a typical value of V_{DD}. In addition, power consumption is defined so that the buffer does not exceed 0.5 mW, evaluating the phase noise at a specified frequency to ensure that the buffer does not add a significant amount of noise to the circuit.

Figure 19 – Buffer design

(a) Buffer Transistors schematic



(b) Buffer Block symbol



Source: Author

Table 14 – Buffer sizing

Buffer components sizing				
Transistors Effective Width (W_{eff}) and Length (L) in nm				
Name	Multiplier	Fins	W_{eff}	L
M0, M1, M4 and M5	6	4	154	16
M2, M3, M6 and M7	4	4	154	16
M8, M9, M10 and M11	1	4	154	16
Capacitors Width (W) and Length (L) in nm				
Name	W	L	Area	Capacitance
C0 and C1	2000	2000	$4pm^2$	$88.8fF$
Transmission Gate Effective Width (W_{eff}) and Length (L) in nm				
Name	Multiplier	Fins	W_{eff}	L
M0 and M1	1	2	58	100

Source: Author

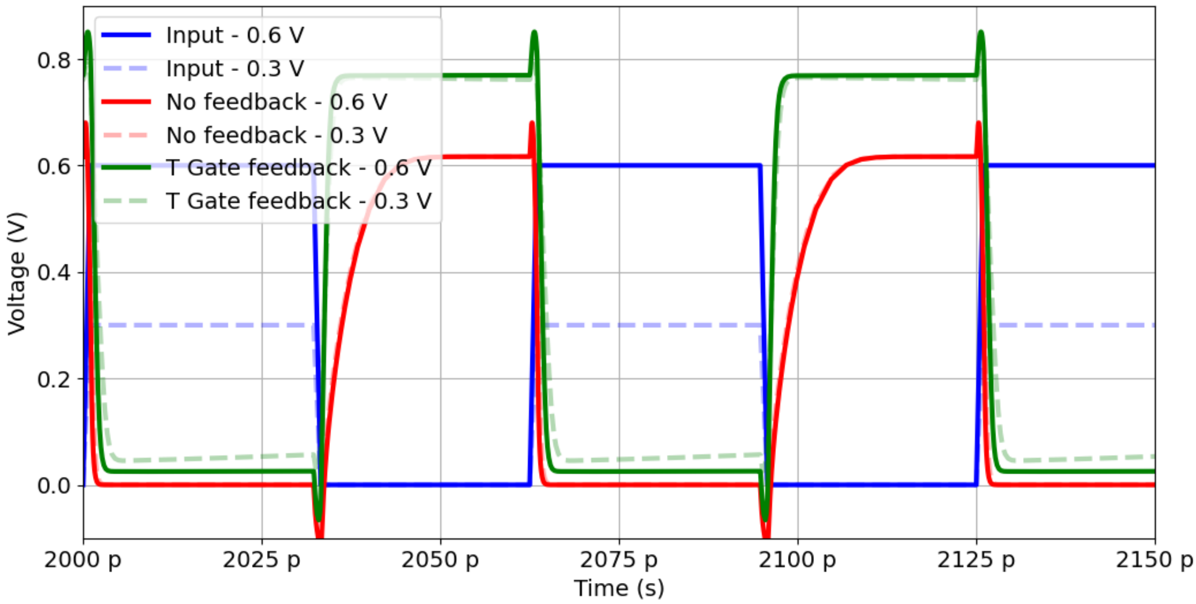
The device sizing in the buffer stage was defined to match that of the oscillator block, employing the same number of fins and channel lengths. This approach simplifies the layout process by maintaining uniform transistor dimensions across blocks, enforcing symmetry between both differential paths enhances signal balance and improves matching, which is critical for minimizing skew and ensuring consistent differential signal propagation.

The buffer design was made using capacitors C_0 and C_1 as a high-pass filter to remove the DC component of the input signal. The input impedance seen from the ring oscillator is associated with the size of the transistors M0, M1, M4, and M5. As the buffer introduces an additional load to the oscillator output, increase in the current needed so that the ring oscillator can sustain oscillation. According to Equation (37), an increase in P_{sig} leads to a reduction in phase noise, positively impacting the subsequent blocks, although increasing the oscillator starving current to compensate for the added load may compromise the functionality of the current source, as previously discussed in Table 11.

After passing through the filter, the signal is directed to a Trans-impedance Amplifier (TIA), composed of M0, M1 and T0 and by M4, M5 and T1. The desinged transmission gates operate as a resistor, always applying feedback between input and output. This configuration provides a large current gain while maintaining a voltage noise gain as unity, improving phase noise results, and, because of the self-biasing feedback, it is faster than a conventional inverter amplifier.

As the TIA is connected to V_{DD} and V_{SS} rails, it allows the output voltage to swing close to the supply rails, which would not be possible in the VCO inverter stages due to the presence of the voltage-controlled current source connected to the ring oscillator V_{DD} pin. M8 to M11 will form the latching inverters, as seen before, the latching circuit enforces the duty cycle to remain close to 50 %, while also maintaining both lines in synchronization.

Figure 20 – Comparison of simple inverter with no feedback and TIA (Inverter with transmission gate self-bias



Source: Author

Figure 20 presents the comparison between a simple inverter and a TIA with the filtering capacitor, emulating the buffer input circuit. The average power needed for the simple inverter is approximately 52 μW, while the TIA is approximately 44 μW, a reduction of almost 16%. Also, in scenarios where the magnitude vary from 0.3 V to 0.6V, the simple inverter with no load limits the output voltage to 0.6V, while the TIA can reach V_{DD} values. Also, the figure shows that the TIA response is faster than the simple inverter, reaching the peak value before.

Because both TIAs will invert the signal, additional inverters made with M2 and M3 on the upper line and other made with M6 and M7 on the lower line are included so the output signal has phase alignment with the input, accounting for time delays.

This design allows the buffer to do fast switch between low and high states, with minimal noise interference and an in-phase output signal. To evaluate the buffer performance, the following testbench applies Simple PVT variations to observe its behavior due the variations with the oscillator exciting the buffer.

Table 15 – Testbench for VCO

Testbench		
Simulations		
Type	Stimulus	Objective
Shotting Newton Periodic Steady State (PSS)	Force DC supply voltage and know differential input signal with specified frequency	Evaluate the buffer steady state behavior and hability to amplify input signal
Shotting Newton Noise	Made with the results of (PSS)	Evaluate the noise interference
PSS Ibias sweep	Force DC supply voltage and vary the oscillator bias current	Evaluate the current needed to oscillate at 16 GHz
Observed parameters		
Parameter	Objective	
Buffer output swing	Measure the maximum and minimum voltage swing due PVT variation	
Buffer output frequency	Measure the maximum and minimum oscillator due PVT variation	
Buffer current	Measure the operating current consumption	
Oscillator current	Measure the new operating current to oscillate at 16 GHz with buffer as load	
Phase Noise	Measure the noise component at specified frequency delta	
Duty cycle	Evaluate if duty cycle is close 50%	
Rise time	Evaluate time needed going from low to high	
Fall time	Evaluate time needed going from high to low	

Source: Author

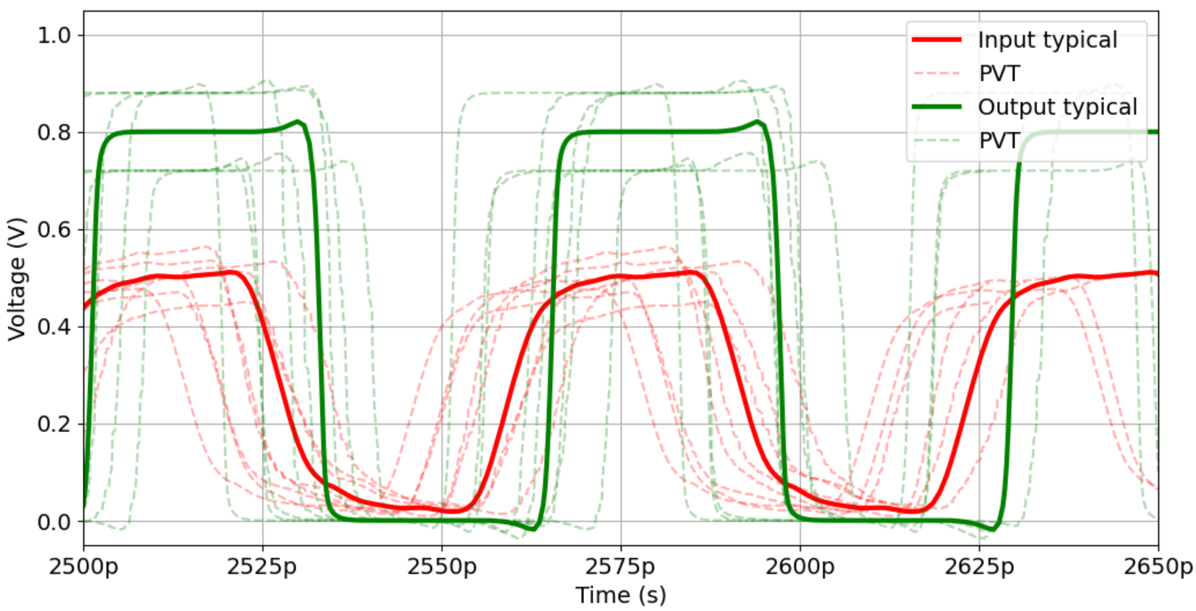
Similarly to the oscillator testbench, these tests aim to evaluate the buffer behavior with PVT variations, but now observe more parameters, such as the new current needed to oscillate with 16 GHz under the typical conditions and the buffer output performance.

Similarly to the oscillator testbench, these tests are designed to evaluate the buffer behavior with PVT variations, focus on additional parameters, such as the new current required to sustain a 16 GHz oscillation under typical conditions and the buffer output performance.

To perform the simulations, the buffer is connected in the input ports of the oscillator with a DC current source connected to the V_{DD} pin, but measuring the main parameters at the output pins of the buffer. The output frequency must be closer to the values obtained with the isolated buffer, expecting few variations, and the output swing must be near V_{DD} values. As the buffer is the interface between the VCO and other circuits, duty cycle, fall time, and rise time are parameters that focus in evaluating whether the buffer forces the circuit to have a square-wave behavior, with fast switching time between low and high values and duty cycle near half the period.

To perform the simulations, the buffer is connected to the output pins of the oscillator, with a DC current source applied to the V_{DD} oscillator pin. The main parameters measured at the buffer output terminals are the output frequency and if it remain close to the expected values obtained when the oscillator operates alone, with minimal variation. The output voltage swing must be close to V_{DD}. As the buffer is the interface between the VCO and subsequent circuits, parameters such as duty cycle, rise time, and fall time are evaluated to determine whether the buffer presents a square wave output, showing fast transitions between logic levels and a duty cycle close to 50%.

Figure 21 – Buffer input and output swing with PVT variation over time



Source: Author

Table 16 – Buffer results for complete PVT simulation

Parameter	Minimal	Maximum	Mean	Unit	Match specification
Frequency	15.413	16.445	15.912	GHz	Yes
Swing	736.90	927.55	834.83	mV	Yes
PN @ 100 kHz	-68.936	-60.726	-64.186	dBc/Hz	Yes
PN @ 1 MHz	-88.936	-80.726	-84.186	dBc/Hz	Yes
PN @ 10 MHz	-108.93	-100.72	-104.18	dBc/Hz	Yes
PN @ 100 MHz	-128.93	-120.71	-124.18	dBc/Hz	Yes
PN @ 1 GHz	-148.79	-140.59	-144.04	dBc/Hz	Yes
Power	150.80	781.46	337.583	μ W	Yes
Duty-cycle	49.173	49.698	49.466	%	Yes
Rise time	2.1321	4.4315	3.0611	%	Yes
Fall time	2.0231	4.4034	2.9118	%	Yes

Source: Author

Using the previously developed ring oscillator, with the buffer connected as a load, the starving current required increases to $I_{RO+BUFFER}$ = 660 μ A to sustain the oscillation at 16 GHz under typical conditions, instead of I_{RO} = 515 μ A, increasing the current consumption of the previous block by 28.15 %

Figure 21 shows the buffer input signal in red and the output signal in green. It can be observed that the buffer effectively amplifies the input signal, enforcing a duty cycle close to 50%, and improves the rise and fall time, as in the input signal slope value for the ascending and descending ramps are smaller than those of the buffer.

Also, Table 16 demonstrates that the combination of ring oscillator and buffer block match the design specifications. The output frequency has minimal deviation from previously obtained values, while the voltage swing approaches the supply voltage V_{DD} more closely.

It is important to note that the values of the minimum and maximum output voltage swing of the buffer are associated with V_{DD} = 0.72 V and V_{DD} = 0.88 V, respectively. As only buffer transistors are connected between V_{DD} and V_{SS}, the occurrence of output voltages exceeding V_{DD} is attributed to device non-idealities, causing them to resonate and occur higher voltages, resulting in voltage overshoots beyond the nominal supply voltage, unlike ideal components which would restrict the output strictly within the supply rails.

Table 17 – Oscillator bias current variation to sustain oscillation at 16 GHz for simple PVT variation

Parameter	Minimal	Maximum	Mean	Unit
Oscillator bias current	634.28	699.62	667.28	μA

Source: Author

Table 17 shows the values of I_{RO} required from an ideal DC current source to ensure oscillation at the target frequency for different PVT combinations. These results highlight the necessity for the Voltage-Controlled Current Source to cover a wide current tuning range, enabling the oscillator to compensate for variations from the typical condition by mirroring the required current as a function of the control input voltage.

The use of an ideal DC current source in the initial tests is a useful simplification to characterize the oscillator and buffer performance together. However, this approach introduces a limitation, as it neglects the impact of V_{DS} variations on the VCCS transistors and does not account for their intrinsic non-idealities and operational constraints.

An additional simulation, conducted using a previous version of the ring oscillator, was carried out to evaluate the impact of the current mirror mirroring effect on oscillator performance. In this setup, a current mirror with varying mirroring factors, biased by an ideal current source supplying a reference current I_{BIAS}, delivered current to the oscillator via the V_{DD} pin. The simulation results demonstrate that variations in the mirroring factor can significantly impact the oscillator's behavior.

Table 18 – Current mirror with 1:1 factor

$I_{BIAS}(\mu A)$	$I_{MIRROR}(\mu A)$	Frequency (GHz)	Real factor
615	468.46	12.888	0.7617
800	530.34	13.641	0.6629
1000	568.15	15.13	0.5681
1200	607.12	15.70	0.5059
1345	617.81	16.01	0.4593

Source: Author

Table 19 – Current mirror with different factors

Design factor	$I_{BIAS}(\mu A)$	$I_{MIRROR}(\mu A)$	Frequency (GHz)	Real factor
1:10	61.5	611.68	15.86	0.9942
1:100	6.15	632.89	16.00	1.029
1:1000	0.615	694.05	16.15	1.128
1:10000	0.0615	704.65	16.20	1.145

Source: Author

Mirroring I_{BIAS} by a factor X will also multiply the associated noise by the same factor. Table 18 shows that for a $1:1$ ratio, mutual interference between the oscillator and the current mirror causes a significant increase in the bias current required to sustain the desired mirrored current. This results in a reduction in overall efficiency as a considerable portion of power is dissipated to bias the VCCS rather than being effectively biasing the oscillator, despite the benefit of reduced additional noise.

However, Table 19 shows that reducing the bias current while increasing the mirroring factor, to maintain the output current near the target value, results in a slight increase in the effective mirroring ratio. This raises the actual starving current required for oscillation and introduces additional noise into the circuit.

These details must be carefully considered while in the VCCS design, aiming to determine the optimal trade-off between the bias current and the mirroring factor.

3.5 VOLTAGE CONTROLLED CURRENT SOURCE

3.5.1 Description

Voltage-controlled current sources are circuit blocks that receive an input control voltage, typically provided by a feedback loop or a frequency-selection mechanism, and convert it into a proportional output current. Since the selected ring oscillator topology is current-starved, a controllable current source is required to modulate the charging and discharging currents of the internal nodes, thereby enabling precise tuning of the oscillation frequency.

3.5.2 Concept

Initial tests showed that due to PVT variations, the ring oscillator with the buffer as a load requires different starving current levels when biased by an ideal DC current source, ranging approximately from $I_{RO+BUFFER_{min}}$ = 630 μA to $I_{RO+BUFFER_{max}}$ = 700 μA. As a result, the voltage-controlled current source must be capable of sourcing a range of current values, while incorporating a safety margin to account for unanticipated conditions. Additionally, since the current mirror mirroring factor can influence the final current delivered, this effect must be considered during design. Given the VCCS power budget constraints, the design must balance efficiency with the need to avoid excessive current levels that could lead to transistor saturation, potentially degrading the oscillator's performance.

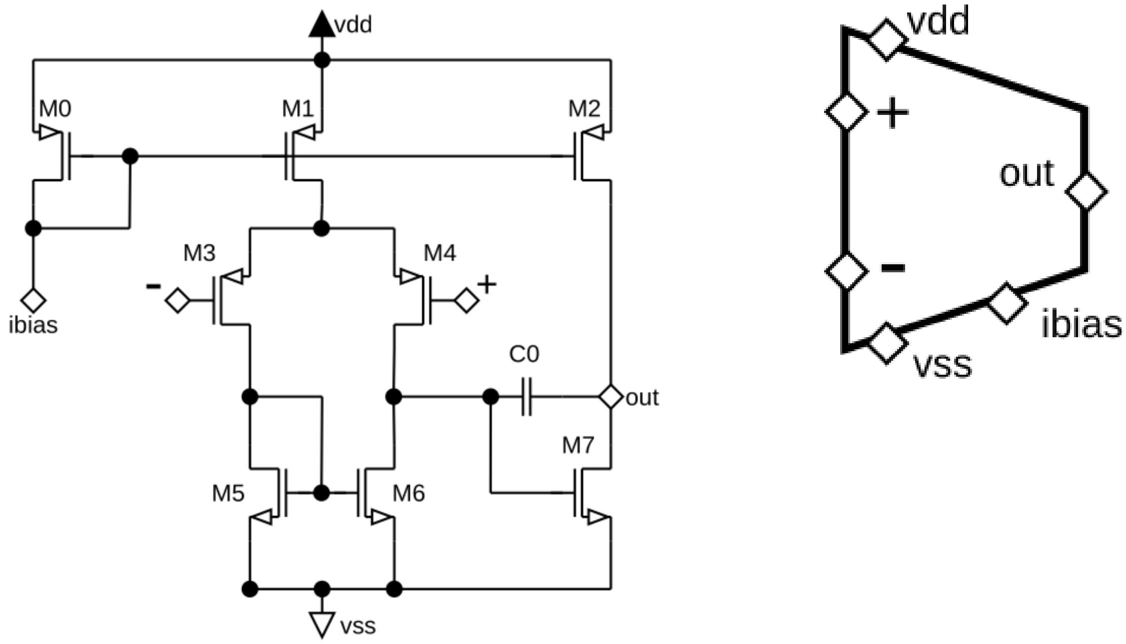
The control voltage V_{ctrl} is expected to vary between 0.2 V and 0.6 V, as the feedback and control circuitry to be designed later may require sufficient headroom to prevent transistor V_{DS} working out saturation. To ensure full coverage of the required current range, the VCCS must be designed such that V_{ctrl} = 0.4 V yields a current equal to $I_{RO+BUFFER}$, which ensures 16 GHz oscillation under typical conditions. Consequently, V_{ctrl} = 0.2 V should result in a current equal to $I_{RO+BUFFER_{min}}$ minus a safety margin, while V_{ctrl} = 0.6 V should correspond to $I_{RO+BUFFER_{max}}$ plus margin, thereby covering worst-case PVT scenarios.

The OTA schematic design was based on (HESHAM; HASANEEN; HAMED, 2019), for low voltage applications. The sizing was performed with the focus on a minimal viable application considering noise addition and power consumption.

The paper (AZCONA et al., 2013) presents a potential implementation of a VCCS using an operational transconductance amplifier (OTA) with current mirror feedback, as shown in the cited paper Figure 2(b), with a wide-swing topology. This design was selected due to its suitability for low-voltage applications, as alternative topologies previously tested failed to exhibit sufficient linearity. The chosen design aims to maximize the linear operating range of the control voltage V_{ctrl}, specifically between 0.2 V and 0.6 V.

Figure 22 – OTA design

(a) OTA Transistors schematic (b) OTA Block symbol



Source: Author

Table 20 – OTA sizing

OTA components sizing				
Transistors Effective Width (W_{eff}) and Length (L) in nm				
Name	Multiplier	Fins	W_{eff}	L
M0, M1 M5 and M6	1	4	154	16
M2 and M7	5	10	442	16
M3 and M4	1	16	730	16
Capacitor Width (W) and Length (L) in nm				
Name	W	L	Area	Capacitance
C0	5000	5000	$25pm^2$	$555.5fF$

Source: Author

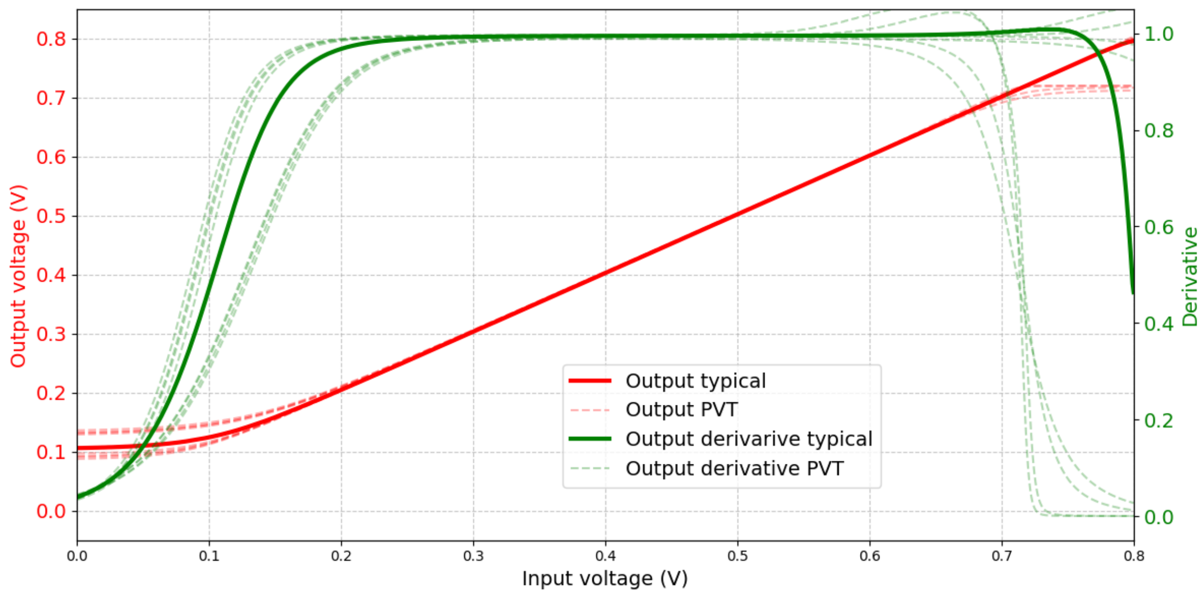
Since the OTA will function as a feedback circuit, the tests aim to evaluate the output linearity and virtual short-circuit capabilities across the full range of control voltages, from the minimum to the maximum defined values.

Table 21 – Testbench for OTA design

Testbench		
Simulations		
Type	Stimulus	Objective
DC	Force DC supply voltage and vary the input control voltage linearly	Evaluate OTA's buffer behavior and performance
Observed parameters		
Parameter	Objective	
Output voltage	Evaluate if the output voltage follows the input voltage	
Output voltage derivative	Measure the range where OTA's buffer behavior is linear	

Source: Author

Figure 23 – OTA output linearity DC simulation

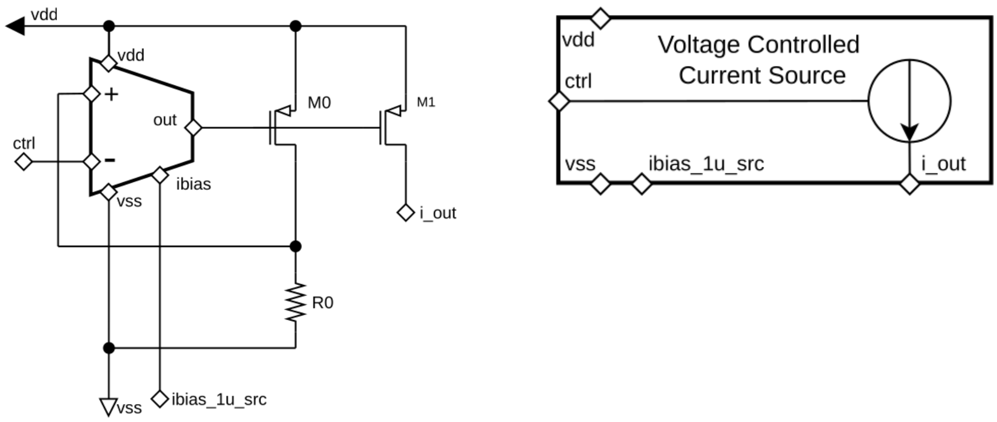


Source: Author

Figure 23 shows that the OTA behaves nearly linearly across most of the defined input voltage range, where the condition $\frac{dV_{OUT}}{dV_{IN}} \approx 1$ holds between V_{IN} = 0.2 V and V_{IN} = 0.6 V. Under certain PVT variations, particularly those involving higher V_{DD} values, the linear operating region tends to narrow, with linearity beginning only after V_{IN} = 0.3 V. However, this behavior is not critical for the design, as a higher V_{DD} results in a lower output frequency, which in turn requires a lower V_{CTRL}. Therefore, the results presented are satisfactory, confirming that the OTA is capable of operating effectively as a buffer over the desired control voltage range.

Figure 24 – VCCS design

(a) VCCS Transistors schematic (b) VCCS Block symbol



Source: Author

As the proposed circuit is defined using the paper as reference, part of the design consisted of testing different mirroring factors, adjusting the effective width (W_{eff}) for both M0 and M1, also adjusting R0 sizes to match the biasing current value.

Table 22 – Testbench for VCCS sizing

Testbench		
Simulations		
Type	Stimulus	Objective
Shotting Newton Periodic Steady State (PSS)	Force DC supply voltage and $V_{CTRL} = 0.4V$	Evaluate the buffer and oscillator steady state performance with VCCS
Observed parameters		
Parameter	Objective	
Buffer output swing	Measure the voltage swing for typical condition	
Buffer output frequency	Measure the frequency for typical condition	
Phase Noise	Measure the noise component at specified frequency delta	
Reference current	Measure the VCCS reference current	
Oscillator current	Measure the new operating current to oscillate at 16 GHz with buffer as load and VCCS as current source	
$M0$ and $M1$ sizes	Observe the area relation between transistors	

Source: Author

Table 23 – VCCS sizing

VCCS components sizing				
Transistors Effective Width (W_{eff}) and Length (L) in nm				
Name	Multiplier	Fins	W_{eff}	L
M0	1	3	106	240
M1	9	20	922	240
Resistor Width (W) and Length (L) in nm				
Name	W	L	Series	Resistance ($k\Omega$)
R0	200	11500	1	36.121

Source: Author

Considering an ideal OTA in a first-order analysis, if V_{CTRL} = 0.4 V, then due to the virtual short circuit condition between the input terminals + and –, the voltage across the resistor R_0 is $V_{R_0} = V_{CTRL}$ = 0.4 V. According to Kirchhoff current law (KCL), and assuming that no bias current flows into the OTA input terminals, the drain current of transistor M_0, denoted as $I_{D_{M0}}$, is given by:

$$I_{D_{M0}} = I_{RES} = \frac{V_{CTRL}}{R0} \tag{54}$$

For this scenario, $I_{D_{M0}} = 11.07\mu A$

Due to the feedback configuration, the OTA output terminal adjusts its voltage to establish a gate source voltage ($V_{GS_{M0}}$) that enables the desired drain current $I_{D_{M0}}$ to flow through the transistor M0. Since transistors M0 and M1 are configured with identical gate-source voltages, the drain current of M1 will mirror that of M0, scaled by the ratio of their effective channel areas. Thus, the mirrored current is defined by the expression:

$$I_{MIRROR} = \left(\frac{W}{L}\right)_{M1} \Bigg/ \left(\frac{W}{L}\right)_{M0} \cdot I_{D_{M0}} \tag{55}$$

Mirroring behavior tests for the VCCS were conducted using a resistor of R = 780 Ω. This resistor serves as a DC load emulating the VCO. The value was chosen based on the buffer tests, where the VCO voltage was approximately V_{VCO} = 512 mV and the current was I_{VCO} = 660 μA when driven by the current mirror.

Table 24 – VCCS calculation and simulation comparison

Parameter	I_{BIAS}	I_{MIRROR}
Calculated	11.07μA	866.59μA
Simulation with resistor as load	10.96μA	663.20μA
Simulation with oscillator and buffer as load	10.93μA	669.79μA

Although the bias current I_{BIAS} is very close to the calculated value in both simulation scenarios, it is evident that the VCCS requires a larger transistor sizing ratio than initially calculated. The theoretical mirror ratio was estimated as $K_{CALC} \approx 78$, whereas the simulated ratio is approximately $K_{SIM} \approx 61$. This discrepancy is due to simplifications in the current mirror model, which neglect factors such as inefficiencies, leakage currents, and parasitic effects that influence actual behavior. Additionally, VCCS output transistors may not be operating with sufficient saturation headroom, further affecting the accuracy of the mirroring performance.

This current results in an oscillation frequency slightly different from 16 GHz and undergoes a fine-tuning process by adjusting and combining different transistor sizes to match the exact resistance value needed for oscillation at the desired frequency. However, since a feedback correction loop will be implemented later, the current frequency is sufficiently close to continue the VCCS design.

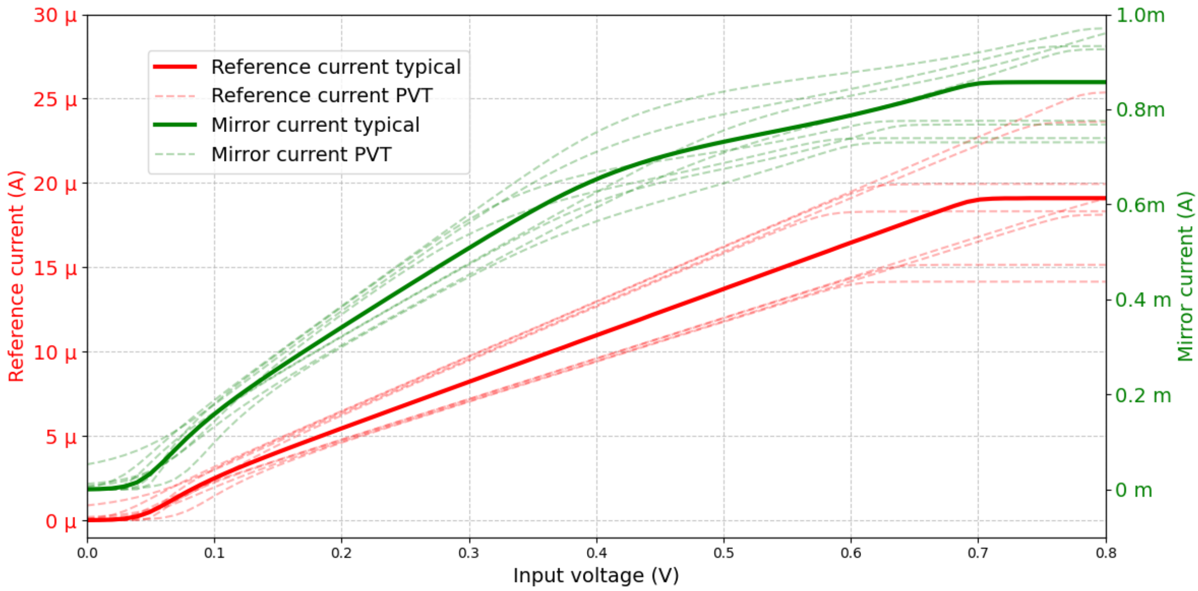
A margin of 200 μA was defined, considered a high margin value, so that the VCCS can cover a frequency range wider than originally designed for the future PLL. Although this reduces the effective V_{CTRL} usage for the current work, it is a deliberate design choice to accommodate future applications.

Table 25 – Testbench for VCCS design

Testbench		
Simulations		
Type	Stimulus	Objective
DC	Force DC supply voltage and vary the input control voltage linearly	Evaluate VCCS mirroring behavior and performance
Stability	Force a DC supply voltage and monitor a feedback loop probe	Evaluate loop behavior under disturbance
Observed parameters		
Parameter	Objective	
Reference current	Measure the reference current for different control voltages	
Mirror current	Measure the mirrored current for different control voltages	
Loop gain	Measure the loop gain	
Gain margin	Measure the gain margin	
Phase margin	Measure the phase margin	

Source: Author

Figure 25 – VCCS mirroring capabilities DC simulation



Source: Author

Figure 25 shows that PVT variations exhibit slopes differing from the typical scenario. This can be explained by the fact that process variations also affect the resistivity of the resistor, altering its total resistance and consequently impacting the bias current and the mirrored current. These variations also affect channel modulation, altering the effective channel length and, consequently, the drain current, especially in short-channel devices.

Despite these variations, the mirrored current maintains two almost nearly linear slopes within the defined input control voltage range. The difference in behavior between the mirrored current and the reference current arises because the mirror transistor may experience stress due to the magnitude of the current passing through it, and the available V_{DS} may be insufficient to meet the requirements. In such cases, channel length modulation becomes more prominent, as the effective channel length reduces with increasing V_{DS}, leading to a deviation from the ideal current mirroring.

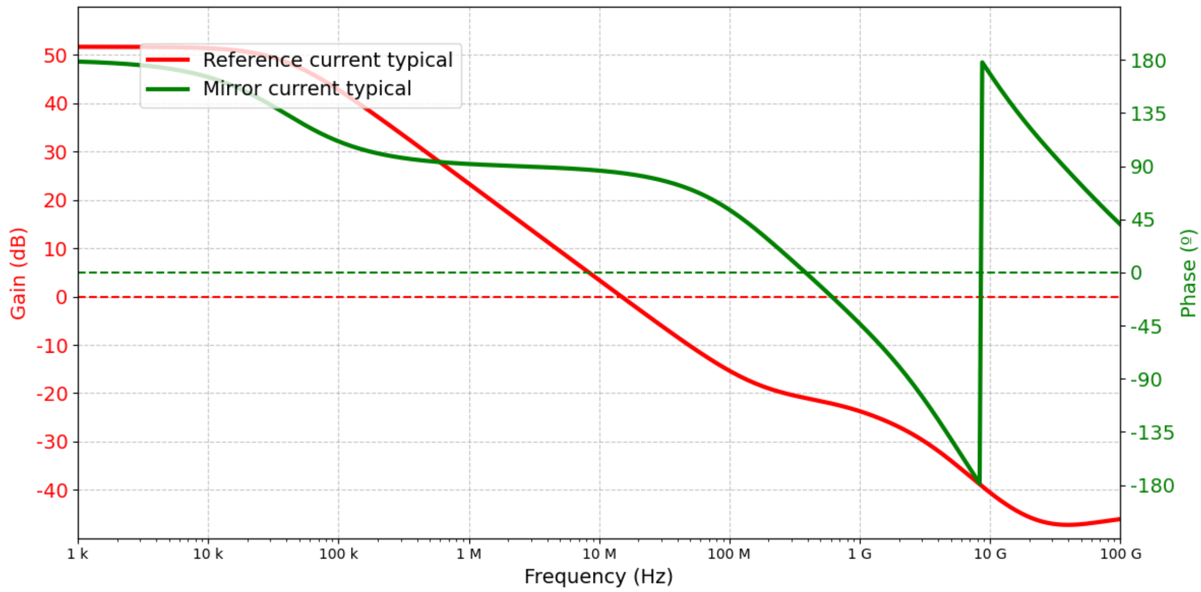
An alternative mirroring ratio was tested, involving more transistors on the mirror side with a smaller reference current, however, this led to an increase in phase noise in the oscillator. Therefore, the previously described configuration was retained.

Table 26 – VCCS results for complete PVT simulation

Parameter	Minimal	Maximum	Mean	Unit	Match specification
Mirror current for $V_{ctrl} = 200mV$	299.97	386.03	344.83	μA	Yes
Mirror current for $V_{ctrl} = 400mV$	576.91	761.96	657.19	μA	Yes
Mirror current for $V_{ctrl} = 600mV$	768.91	927.65	832.32	μA	Yes
Gain margin	16.007	19.387	17.680	dB	
Phase margin	78.145	82.395	80.501	$^\circ$	

Source: Author

Figure 26 – VCCS feedback loop gain and phase



Source: Author

Figure 26 shows the loop gain and phase over frequency of the voltage-controlled current source, evidencing the circuit gain and phase margin.

The VCCS is capable of providing the desired controlled current values as specified. Although gain margin and phase margin specifications were not defined in the project, it is evident that the circuit maintains a sufficient margin before the VCCS approaches instability.

This design allows the theoretical voltage-controlled oscillator gain, $k_{VCO_{Theoretical}}$, to be defined as follows:

$$k_{VCO_{Theoretical}} = \frac{\Delta f}{\Delta V_{CTRL}} = \frac{18G - 14G}{0.6 - 0.2} = 10\frac{GHz}{V} \tag{56}$$

3.6 EVALUATION FEEDBACK LOOP VERILOG-A CIRCUIT

3.6.1 Description

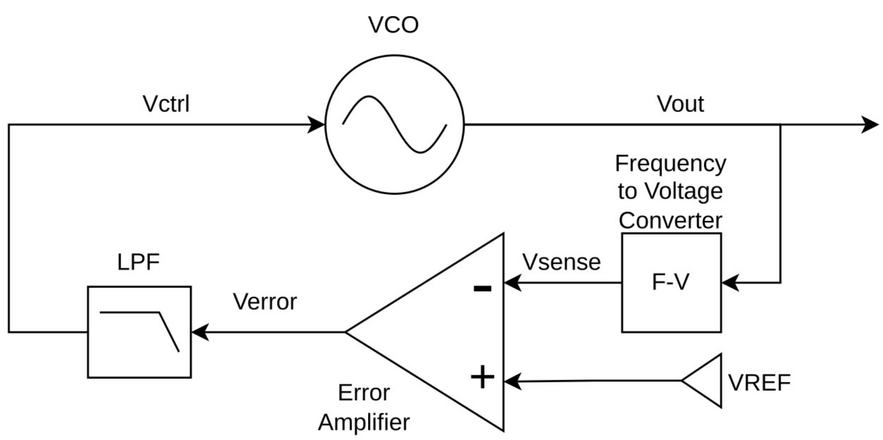
This block was developed for validation purposes emulating part of the PLL feedback path, commonly known as the error amplifier and correction circuit. However, since its full design exceeds the scope of this work, it was implemented using Verilog-A, a hardware description language specialized in analog signal modeling, to emulate the behavior of these blocks. To ensure that the VCO converges to the desired frequency regardless of variations, this block outputs a proportional control voltage connected to the VCCS, thus adjusting the bias current to achieve the target oscillation frequency.

3.6.2 Concept

To start the design, a feedback model was developed to understand the requirements of the feedback path. Similar to a phase-locked loop (PLL), an alternative approach is the frequency-locked loop (FLL), which is also a correction and control circuit. While the PLL monitors the phase of two signals and aims to synchronize both phase and frequency, the FLL focuses only on synchronizing the frequency. For this first-order analysis, the main circuit specification is the VCO output frequency, without influencing the signal phase.

Using the work of (DJEMOUAI; SAWAN; SLAMANI, 2001) as a reference and adapting it to current requirements, a block diagram of the feedback path was derived and analyzed.

Figure 27 – Feedback path block diagram



Source: Author

Assuming $V_{ctrl}(t = 0) = 0.4\,V$, the processes, voltage, and temperature variations will converge for different frequencies as shown. The objective of the FLL is to measure the frequency difference and adjust V_{ctrl} so that the frequency converges to 16 GHz, or another desired value in the future.

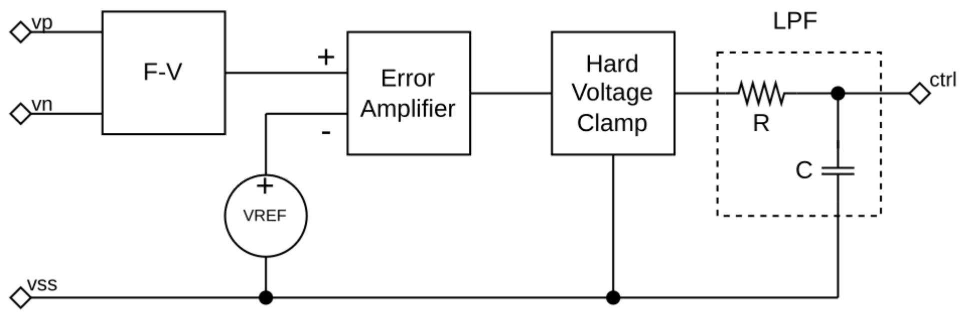
Assuming $V_{ctrl}(t = 0) = 0.4\,V$, variations in process, voltage, and temperature will cause the oscillator to initially operate at different frequencies, as shown. The objective of the frequency-locked loop (FLL) is to measure the frequency difference and adjust V_{ctrl} accordingly so that the frequency converges to 16 GHz, or to another desired value in future applications.

3.6.3 Block description

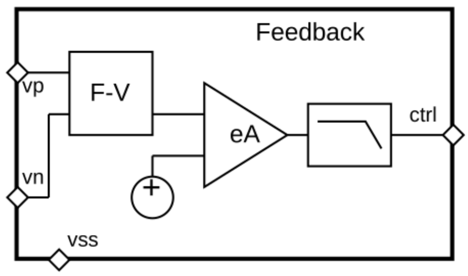
The simulation tools provide access to various libraries for circuit development, one of which is the *ahdlLib* library. This library contains multiple blocks implemented in Verilog-A. Part of the knowledge acquired came from studying the available documentation, while another part was gained by reading the descriptive comments and understanding the intended use of each function. Within the *ahdlLib* library, some pre-developed blocks could be adapted to suit the specific requirements of the project.

Figure 28 – Feedback loop design

(a) Feedback loop blocks schematic



(b) Feedback loop symbol



Source: Author

The frequency-to-voltage converter (F–V) is a block responsible for measuring the instantaneous frequency of the V_{out} signal and converting it into a voltage signal proportional to that frequency. The original *ahdlLib* implementation outputs the signal as a one-to-one current ratio, meaning the output has a gain of $K = 1\frac{A}{Hz}$. However, it can be adapted to output a voltage signal by modifying its internal routines. To align the converter output range with the other circuits, a scaling factor $k = 25 \cdot 10^{-12}$ is applied to the output, adjusting the gain to $K' = 25\frac{pV}{Hz}$. This means that an input frequency of 16 GHz corresponds to an output voltage $V_{sense} = 0.4$ V.

The error amplifier is also an *ahdlLib* block that was adapted to meet the design requirements. Its function is to compare and amplify the difference between two signals, V_{ref} and V_{sense}, and then add this amplified difference to the desired output value, following the relation below. Here, V_{ref} is modeled as a reference voltage. A gain factor G is included to enhance the conversion by increasing the open-loop gain.

$$EA(V) = 0.4 + (G \cdot (V_{ref} - V_{sense})) \tag{57}$$

Considering F as some function, let $F(t)$ be the instantaneous value at time t, and $F(t + 1)$ be the subsequent output value. Since the oscillation frequency is proportional to the starving current, and this current is proportional to the control voltage, it follows that if:

$$f_{osc}(t) > 16GHz \rightarrow V_{CTRL}(t+1) < V_{CTRL}(t) \rightarrow I_{RO}(t+1) < I_{RO}(t) \rightarrow f_{osc}(t+1) < f_{osc}(t)$$

$$\uparrow\downarrow$$

$$f_{osc}(t) = 16GHz \rightarrow V_{CTRL}(t+1) = V_{CTRL}(t) \rightarrow I_{RO}(t+1) = I_{RO}(t) \rightarrow f_{osc}(t+1) = f_{osc}(t)$$

$$\uparrow\downarrow$$

$$f_{osc}(t) < 16GHz \rightarrow V_{CTRL}(t+1) > V_{CTRL}(t) \rightarrow I_{RO}(t+1) > I_{RO}(t) \rightarrow f_{osc}(t+1) > f_{osc}(t)$$

A hard voltage clamp was implemented to restrict the error voltage values within the range of 0.2 V to 0.6V. These limits were defined to prevent the circuit from driving transistors in saturation, ensuring an adequate voltage margin for proper operation.

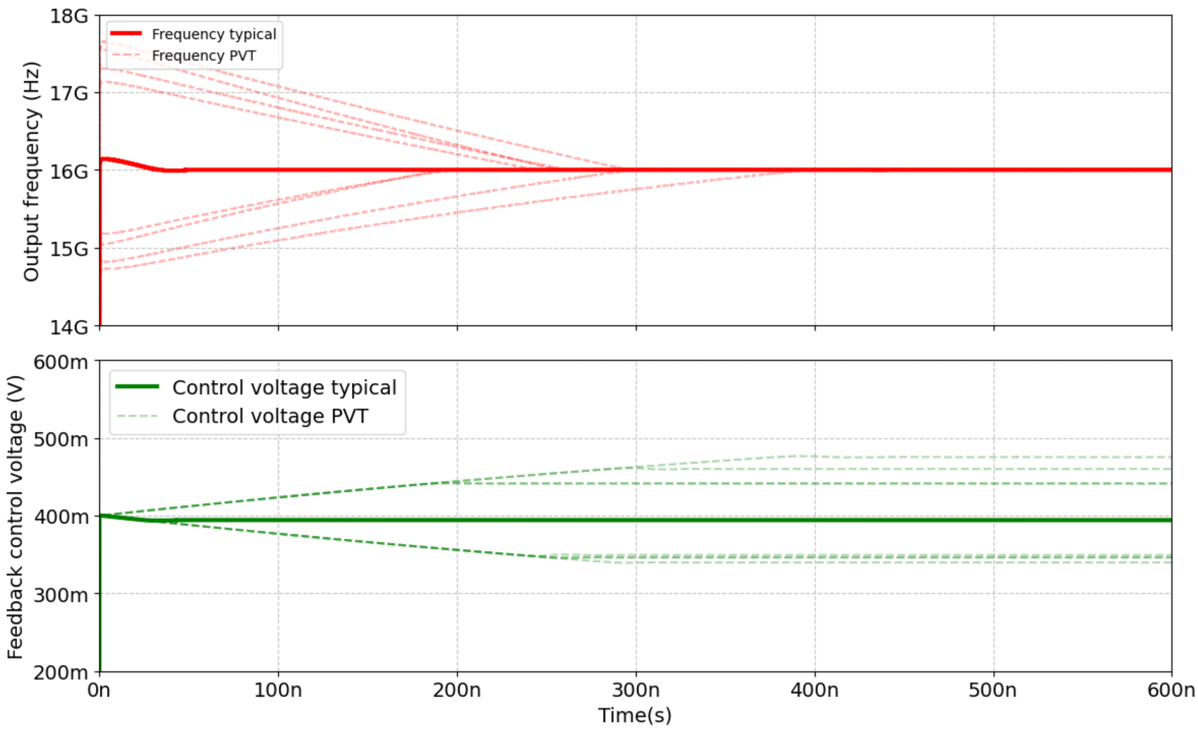
In addition, a low-pass RC filter was incorporated to extract the DC component proportional to the error correction signal while suppressing any high-frequency components that could cause unwanted VCO behavior due to transient spikes from the circuit's operation. Using a resistor $R = 1$ MΩ and a capacitor $C = 800$ fF, the cutoff frequency f_{cut} of this first-order RC low-pass filter can be calculated by:

$$f_{cut} = \frac{1}{2\pi \cdot R \cdot C} = \frac{1}{2\pi \cdot 1 \cdot 10^{6} \cdot 800 \cdot 10^{-15}} = 198.94kHz \approx 200kHz \tag{58}$$

This cutoff frequency was chosen because initial simulations without the low-pass filter showed oscillation frequency variations around 20 MHz. Thus, setting the cutoff approximately two decades below this frequency was a deliberate design decision to effectively filter the signal.

This creates a control scenario where if the oscillation frequency f_{osc} is higher than the target, the control voltage V_{ctrl} will decrease, reducing the current and consequently lowering the oscillation frequency. Conversely, if f_{osc} is higher, V_{ctrl} will increase, raising the current and the oscillation frequency. When f_{osc} equals the desired frequency, V_{ctrl} remains stable without change.

Figure 29 – Frequency and Control voltage over time



Source: Author

Figure 29 shows the frequency and control voltage evolution over time under a simple PVT variation. The graph demonstrates that, despite starting at different initial frequencies due to process, voltage, and temperature changes, the feedback circuit adapts the control voltage to bring the output frequency close to the target of 16 GHz. As observed, the feedback loop requires several hundreds of nanoseconds to converge. Since convergence time was not a primary design criterion, using alternative transistor configurations or design techniques could reduce this settling time. Overall, the feedback loop model is validated as an effective evaluation tool and can be used for further simulations.

4 RESULTS

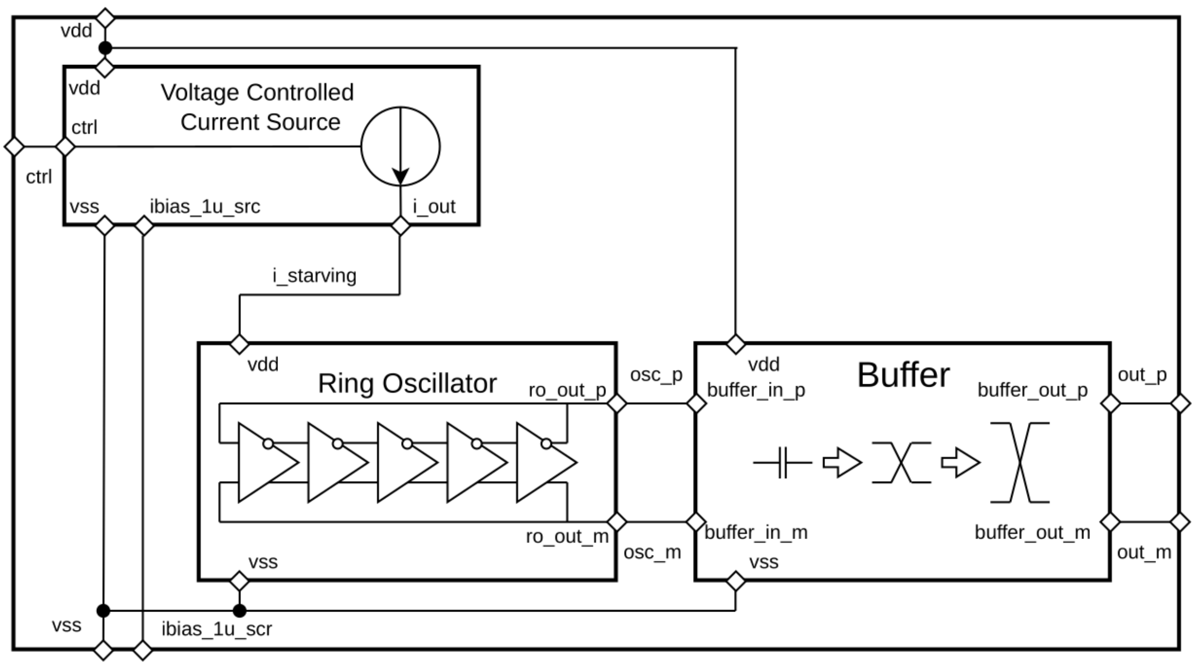
4.1 MOTIVATION

With all the required blocks, the oscillator core, the buffer stage, and the voltage-controlled current source designed and integrated, the next step is to evaluate the global performance of the complete VCO system. These final simulations aim to replicate a range of realistic operating conditions, including process, voltage, and temperature (PVT) variations, as well as different control voltage scenarios.

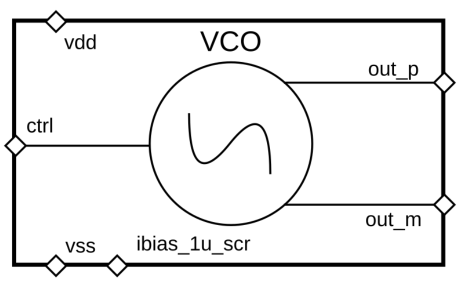
The objective is to assess the system ability to maintain the desired output specifications under non-ideal conditions. By analyzing how the assembled VCO responds as a whole, it becomes possible to validate the robustness of the design and ensure that the interactions between blocks do not degrade performance.

Figure 30 – Voltage controlled oscillator design

(a) VCO schematic



(b) VCO symbol



Source: Author

Figure 30 presents the schematic of the complete VCO. The block features six pins: two for the power supply, one for OTA biasing, one for the input control voltage, and two output pins, with all blocks referenced to $V_{SS} = 0\,V$.

The VCCS receives a bias current source with a DC value of 1 μA to bias the internal OTA. The control voltage is applied at the node ctrl, which sets a proportional current at the i_out pin. This current flows through node i_starving.

The ring oscillator receives the current flowing through i_starving to bias the oscillator relative to V_{DD}. The output signal from the oscillator is then routed to the buffer through the nodes osc_p and osc_m.

After receiving the signal from the oscillator, the buffer processes it and outputs the VCO differential signal through the nodes out_p and out_m, which can then be evaluated and used by subsequent circuits.

Table 27 – Testbench for VCO design

Testbench		
Simulations		
Type	Stimulus	Objective
Shotting Newton Periodic Steady State (PSS)	Force DC supply voltage, I_{BIAS} current and voltage at V_{CTRL}	Evaluate the VCO steady state behavior
Shotting Newton Noise	Made with the results of (PSS)	Evaluate the noise interference
Observed parameters		
Parameter	Objective	
VCO output swing	Measure the maximum and minimum voltage swing due PVT variation	
VCO output frequency	Measure the maximum and minimum oscillator due PVT variation	
VCO power	Measure the average power consumption	
Phase Noise	Measure the noise component at specified frequency delta	
Duty cycle	Evaluate if duty cycle is close 50%	
Rise time	Evaluate time needed going from low to high	
Fall time	Evaluate time needed going from high to low	

Source: Author

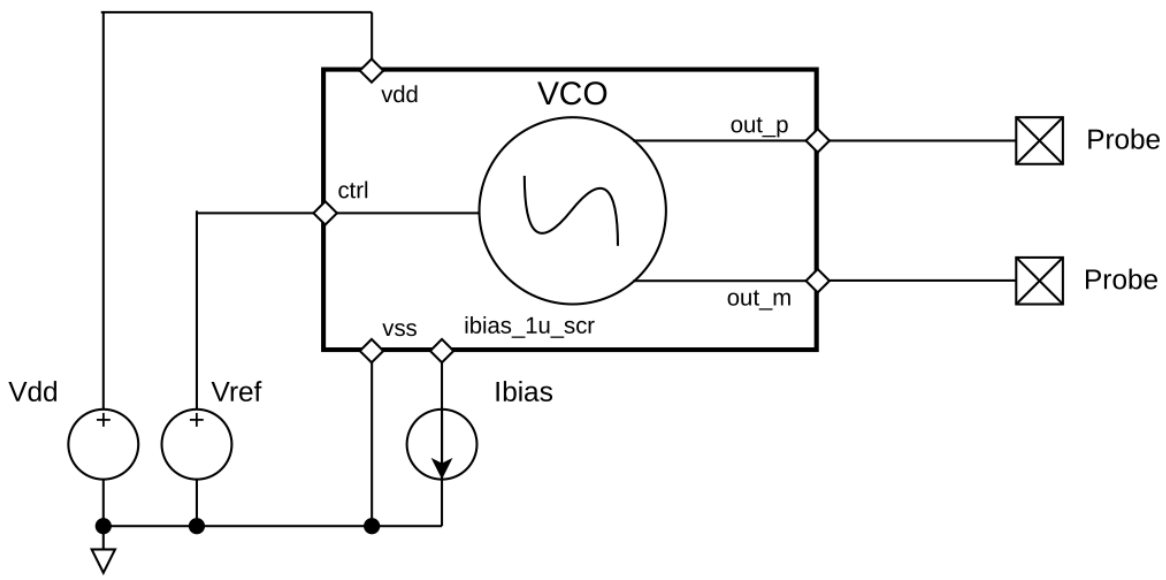
Table 27 presents the testbench developed to evaluate the VCO. This setup is intended to assess the performance and verify whether the design meets the defined specifications, serving as the basis for the subsequent tests.

4.1.1 Open-loop test

Open-loop tests are performed to evaluate the free-running performance of the VCO, with no feedback loop or additional circuitry connected. These results are intended to characterize the VCO in isolation, without the influence of other circuit blocks that could affect its behavior.

Under these conditions, the VCO is the only active block in the testbench, and all other components are considered ideal. Consequently, the control voltage, typically provided by a feedback or channel selection circuit, is also modeled as an ideal source, set to the nominal design value of V_{CTRL} = 0.4 V.

Figure 31 – Open-loop testbench diagram



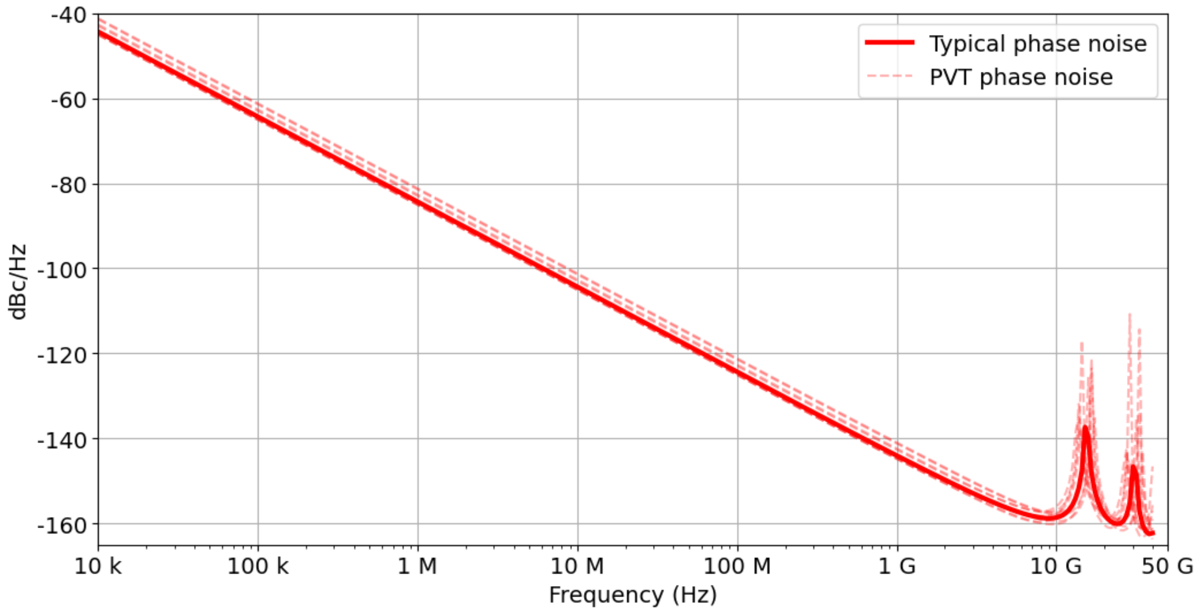
Source: Author

Table 28 – VCO open-loop results with Complete PVT variation

Parameter	Minimal	Maximum	Mean	Unit	Match specification
Frequency	14.150	17.858	15.824	*GHz*	Yes
Swing	732.83	932.65	833.94	mV	Yes
PN @ 100 kHz	-67.803	-60.410	-63.413	dBc/Hz	Yes
PN @ 1 MHz	-87.803	-80.410	-83.413	dBc/Hz	Yes
PN @ 10 MHz	-107.80	-100.41	-103.41	dBc/Hz	Yes
PN @ 100 MHz	-127.82	-120.38	-123.41	dBc/Hz	Yes
PN @ 1 GHz	-147.48	-140.13	-143.12	dBc/Hz	Yes
Power	609.48	1458.6	919.27	μW	Yes
Duty-cycle	49.262	49.795	49.547	%	Yes
Rise time	2.3675	4.1546	3.0311	%	Yes
Fall time	2.2733	4.2057	2.9764	%	Yes

Source: Author

Figure 32 – Phase noise over frequency offset for open-loop simulations for V_{REF} = 0.4 V



Source: Author

Figure 32 shows the phase noise graph over the frequency offset for the open-loop simulations for a simple PVT variation, showing that all corners stay below the specifications.

Table 28 presents the results obtained for all possible combinations that can occur. All design specifications were successfully met under these conditions. The simulations were performed using a periodic steady-state (PSS) analysis, which captures the circuit behavior under stable operating conditions, after all transient effects have settled. This provides a reliable representation of the VCO's steady-state output performance.

Although the deviation of the oscillation frequency increased, driven by a broader range of achievable maximum and minimum values, the phase noise performance remained within acceptable limits. The rise in current required for the oscillator to operate at 16 GHz contributed positively to the phase noise characteristics. Additionally, the buffer and VCCS blocks introduced negligible noise into the system. The average power consumption remained well below the specified maximum threshold and, even under the worst-case scenario, the design still complies with the defined specifications.

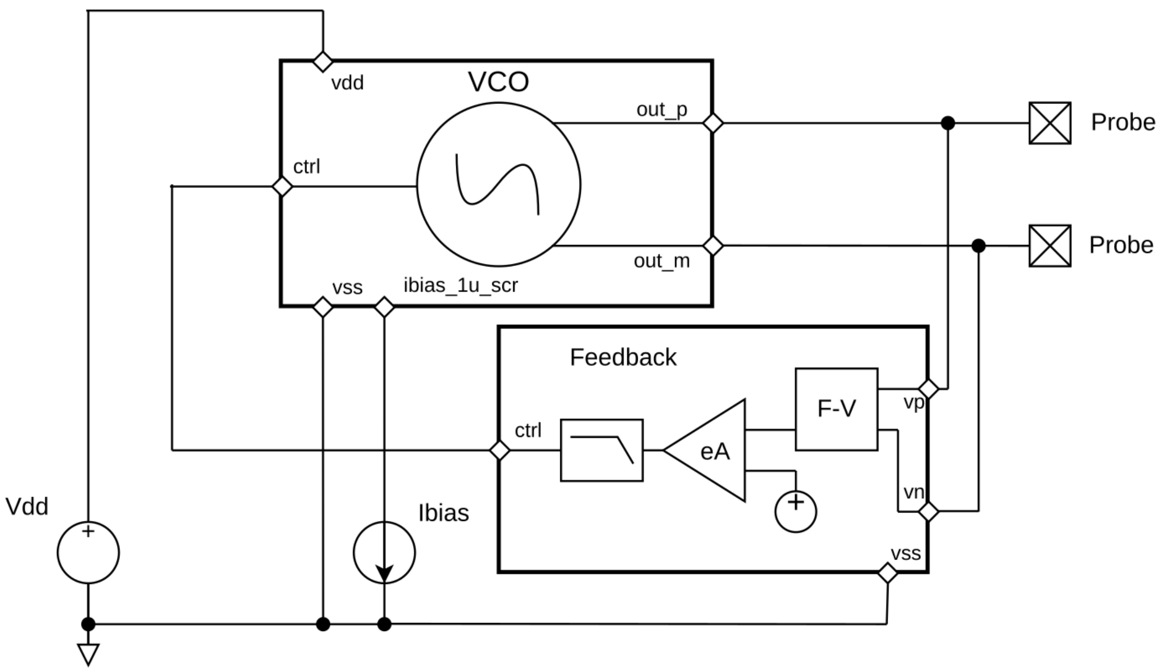
The output swing follows the variations in V_{DD}, with the minimum, maximum, and mean values directly reflecting the corresponding voltage corners. These results indicate that the buffer is capable of delivering a signal with a full voltage excursion from V_{SS} to V_{DD}, rather than a reduced fraction of the supply range. Consequently, for digital circuits that operate within the same voltage reference levels, the amplitude of the buffered signal will not compromise edge detection, ensuring a reliable interpretation of rising and falling transitions.

Additionally, the results for duty cycle, rise time, and fall time demonstrate that the VCO output closely resembles an ideal square wave. The duty cycle remains near 50 %, and the rising and falling transitions occupy a minimal portion of the signal period.

These findings confirm that the designed VCO, even when operating in open loop mode without a feedback path, satisfies all specified design requirements in the evaluated scenarios. This validates the architectural and circuit-level design choices and confirms the feasibility and robustness of the proposed VCO implementation.

4.1.2 Close-loop tests

Figure 33 – Close-loop testbench diagram



Source: Author

The feedback circuit was designed as an auxiliary tool for evaluation and validation purposes. While it is not an essential component of the VCO architecture, it enables the assessment of the VCO dynamic behavior when integrated with a control system that enforces convergence to a target frequency. In this context, the results presented in this section do not focus on the absolute performance metrics of the VCO, but rather on its ability to achieve frequency convergence when subject to closed-loop control. Although the open-loop specifications are used as reference values, they will not serve as criteria for evaluating VCO performance in this configuration.

Table 29 – VCO close-loop results with Medium PVT variation

Parameter	Minimal	Maximum	Mean	Unit	Match open-loop specification
Frequency	15.839	16.126	15.992	*GHz*	Yes
PN @ 100 kHz	-75.004	-40.886	-63.211	dBc/Hz	No
PN @ 1 MHz	-95.231	-60.887	-83.284	dBc/Hz	No
PN @ 10 MHz	-115.25	-80.891	-103.33	dBc/Hz	No
PN @ 100 MHz	-135.53	-100.87	-123.36	dBc/Hz	No
PN @ 1 GHz	-159.42	-120.77	-143.10	dBc/Hz	No
Power	648.80	1403.3	947.08	μW	Yes
Duty-cycle	49.396	49.623	49.521	%	Yes
Rise time	2.2219	4.0858	3.1413	%	Yes
Fall time	2.3372	4.1612	3.0819	%	Yes
V_{CTRL}	335.43	516.51	418.03	V	Yes

Source: Author

Table 29 presents the results obtained under closed-loop conditions. It can be observed that the phase noise performance does not meet the same specifications established for the open-loop scenario. The primary cause appears to be the additional noise introduced by the feedback circuit itself. Tests revealed that even when the feedback circuit is connected to the output nodes but disconnected from the control input, the phase noise performance deteriorates compared to when the feedback circuit is completely disconnected. This behavior may be related to the interaction between the Verilog-A model and the simulator, as the code is not fully optimized for the entire system, being primarily designed to enforce frequency convergence via control voltage adjustment.

From the 108 simulation scenarios, 4 failed completely due to convergence issues with the simulator. Additionally, 22 cases were unable to complete the periodic steady-state (PSS) simulations, though these cases still produced V_{CTRL} values within the maximum allotted simulation time. Further investigation and model refinement could help mitigate these convergence problems. Nonetheless, the V_{CTRL} values obtained from these simulations can be applied in open-loop simulations to verify whether the VCO output, under virtual feedback, continues to meet the design specifications.

Apart from phase noise degradation, all other performance specifications were met, demonstrating that the feedback circuit allows the system to converge reliably to the desired output frequency.

4.1.3 Open-loop test with defined control voltage

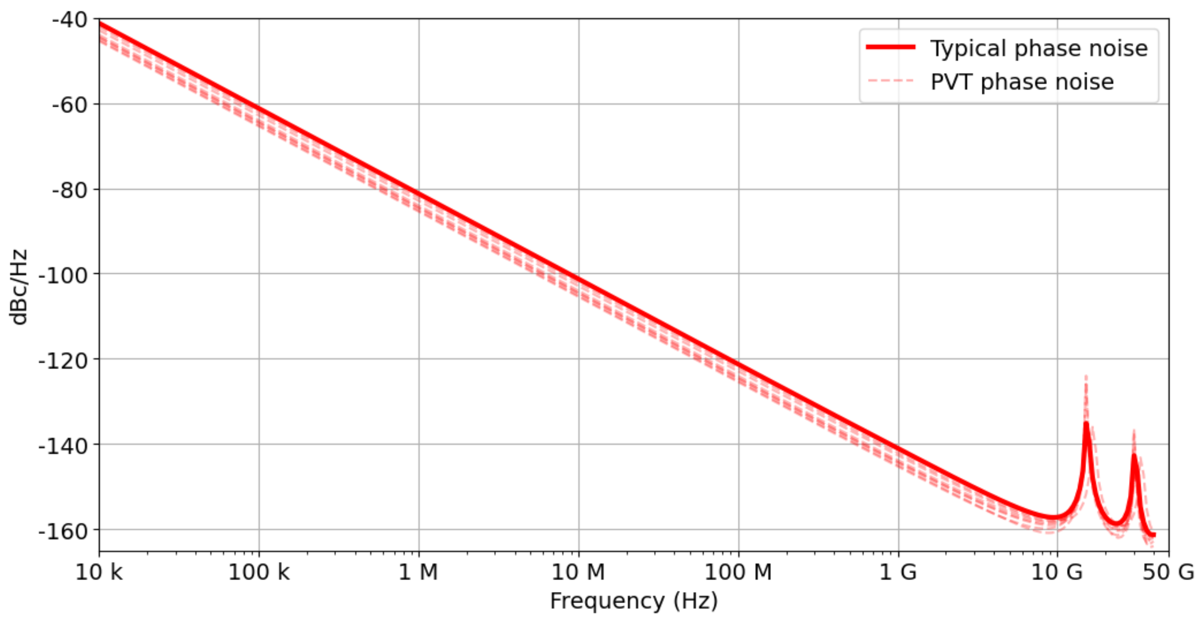
Using the same circuit setup as shown in Figure 33, the current test applies the V_{CTRL} values obtained from the closed-loop simulations for specific PVT corners. This approach aims to validate the VCO performance under feedback conditions without the feedback loop itself interfering with the measurements. The four corners that failed to converge in the previous closed-loop tests were excluded from this validation.

Table 30 – VCO open-loop results with defined V_{CTRL} and Medium PVT variation

Parameter	Minimal	Maximum	Mean	Unit	Match open-loop specification
Frequency	15.987	16.031	16.007	*GHz*	Yes
Swing	732.83	932.65	833.94	mV	Yes
PN @ 100 kHz	-70.267	-60.641	-63.498	dBc/Hz	Yes
PN @ 1 MHz	-90.267	-80.641	-83.498	dBc/Hz	Yes
PN @ 10 MHz	-110.27	-100.64	-103.50	dBc/Hz	Yes
PN @ 100 MHz	-130.28	-120.62	-123.50	dBc/Hz	Yes
PN @ 1 GHz	-149.95	-140.38	-143.23	dBc/Hz	Yes
Power	687.75	1403.1	950.55	μW	Yes
Duty-cycle	49.231	49.788	49.555	%	Yes
Rise time	2.4948	4.0911	3.1497	%	Yes
Fall time	2.3706	4.1611	3.0943	%	Yes

Source: Author

Figure 34 – Phase noise over frequency offset for open-loop simulations for V_{REF} = V_{CTRL} of close-loop tests



Source: Author

Figure 32 shows the phase noise graph over the frequency offset for the open-loop simulations with the control voltage set as the close-loop final result for a simple

PVT variation, showing that all corners stay below the specifications, evaluating phase noise behavior with a virtual feedback loop .

Table 30 presents the results of the VCO operating with an ideal feedback circuit, using the control voltages previously determined to achieve the desired oscillation frequency. These results demonstrate that the VCO can converge to the target frequency while meeting the design specifications established in the open-loop simulations.

This confirms that suitable input control voltages exist to enable proper frequency convergence, suggesting that with a well-designed feedback loop, the VCO will maintain the expected performance. Although the feedback circuit implemented here serves primarily as a proof-of-concept, the parameters and blocks developed provide valuable guidelines for the final design.

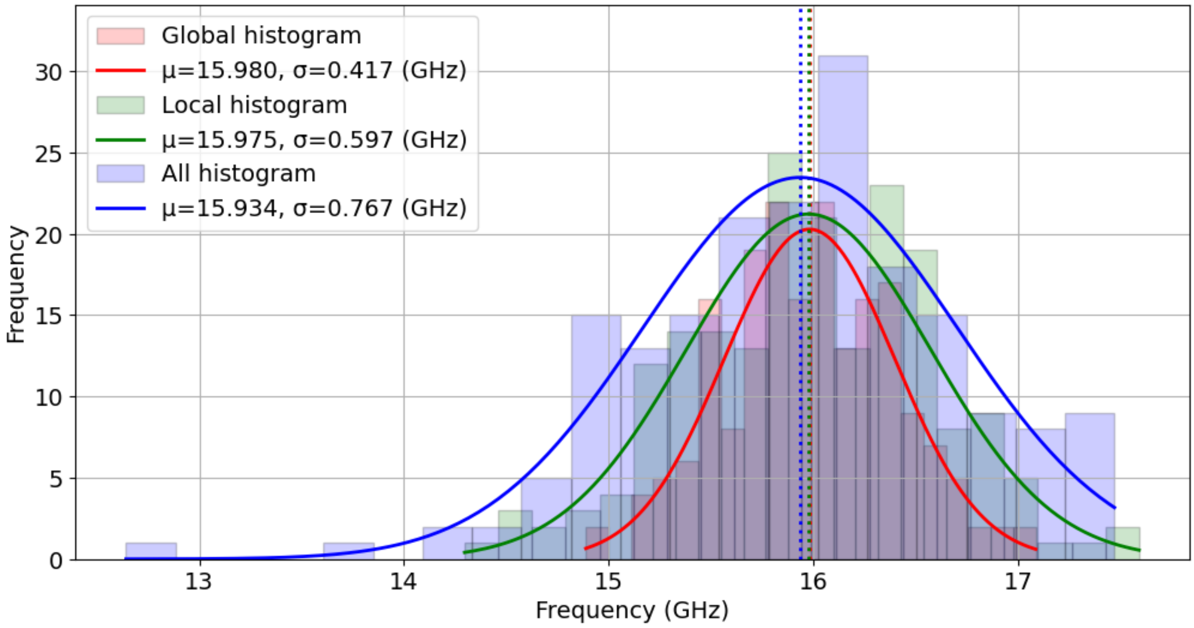
4.1.4 Monte Carlo open-loop simulations

Monte Carlo simulations are performed to model uncertainties in the design. While previous simulations assume ideal transistor parameters as specified in the models, the actual fabrication process can introduce variations. These variations affect parameters such as threshold voltage (V_T), effective channel width (W_{eff}), and channel length (L), thereby influencing the circuit behavior and performance.

Monte Carlo simulations address this by running numerous iterations with randomly varied parameters, simulating the impact of process variations. These variations can be classified as Global, affecting all devices uniformly, Local, affecting each device independently, or a combination of both, all.

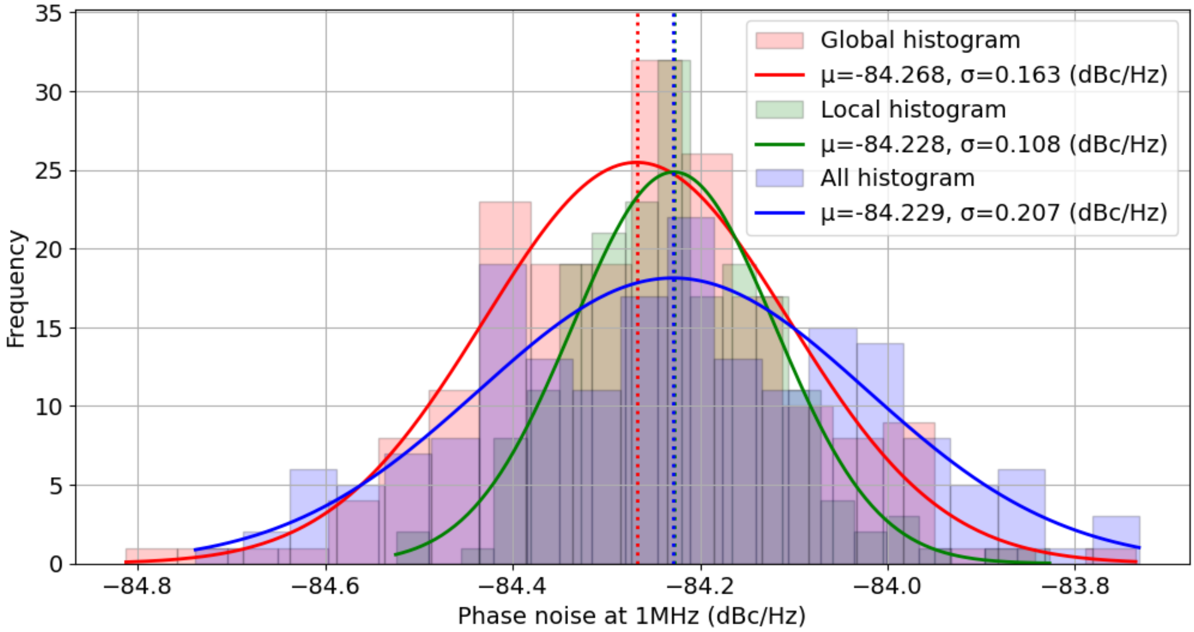
For these tests, 200 iterations will be performed for each variation type, Global, Local, and All, using random seeds to evaluate the open-loop oscillator performance under these randomized fabrication variations.

Figure 35 – Monte Carlo results for Frequency



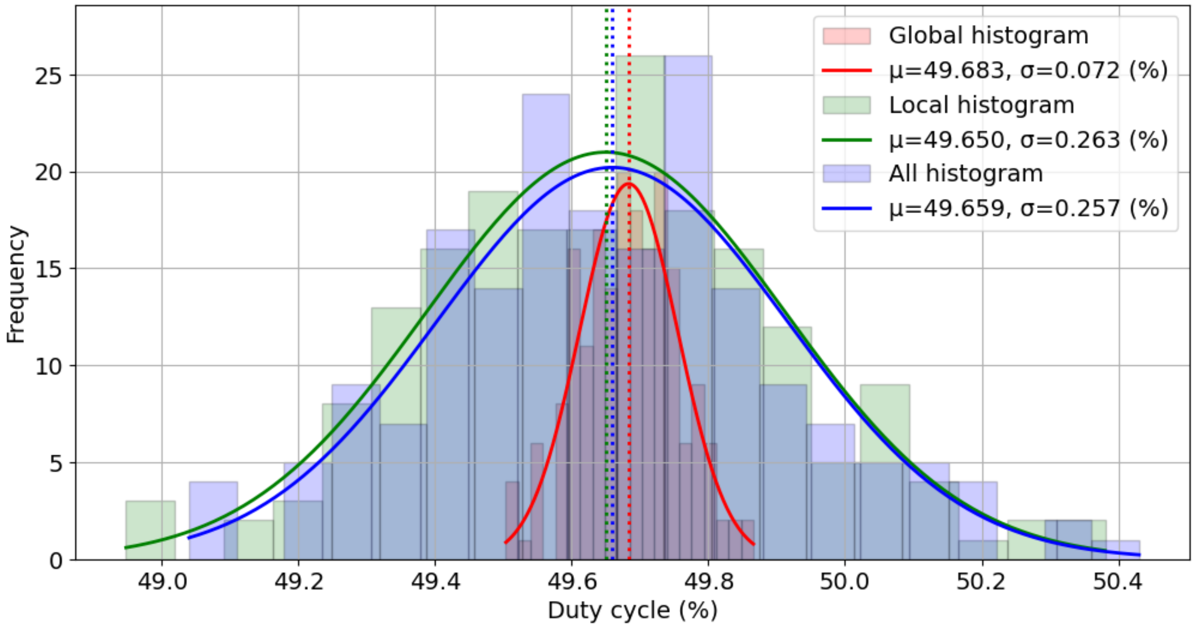
Source: Author

Figure 36 – Monte Carlo results for Phase noise



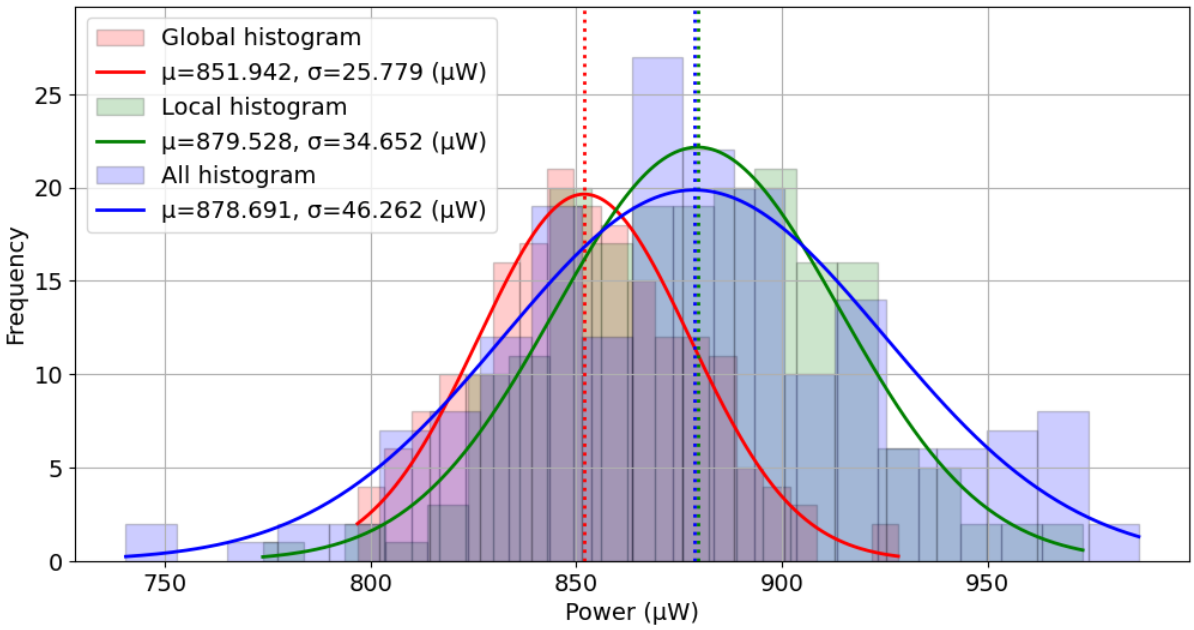
Source: Author

Figure 37 – Monte Carlo results for Duty cycle



Source: Author

Figure 38 – Monte Carlo results for Power



Source: Author

As expected, the Global Monte Carlo simulations exhibited fewer deviations because the same variation is applied uniformly to all devices, causing them to behave proportionally to the baseline circuit. In contrast, the Local and All variation simulations showed greater deviations, which is also expected since devices can vary independently. This can lead to imbalance in the circuit, for example, different stages charging and discharging with varying slopes.

All simulations and iterations met the specifications except for two iterations in the All variation case, which failed to meet the frequency requirements. This behavior likely resulted from mismatch in the VCCS current mirror transistors. Since the design relies on both the *p* and *m* lines oscillating in synchrony, severe mismatch in these transistors caused the mirrored current to be too low. Consequently, the ring oscillator loaded with the buffer could not achieve the expected oscillation frequency at $V_{CTRL} = 0.4\,V$.

This finding highlights a potential risk in the design. Further investigation may be needed to mitigate such mismatches, or alternatively, the feedback loop could be designed to suppress these issues in future implementations.

5 CONCLUSION

This work presented the design of a 16 GHz voltage-controlled oscillator (VCO) intended for digital PLL clock generation, implemented using 12 nm FinFET technology. During the design process, various oscillator topologies were evaluated, highlighting their advantages, limitations, and the impact of each design decision on the overall architecture. The analysis emphasized the trade-offs involved and the dependency of key performance parameters on schematic choices, circuit adaptations, and simulation results.

Key design specifications, including output frequency, voltage swing, and duty cycle, were comprehensively addressed, with particular emphasis on optimizing phase noise and power consumption. The final architecture employs a ring oscillator topology, selected for its advantageous frequency tunability and compact footprint relative to alternative approaches. This is complemented by a buffer stage that isolates the oscillator from downstream circuit loads while maximizing the output voltage swing. A voltage-controlled current source (VCCS) governs the oscillator bias current, allowing precise frequency control. Collectively, these components constitute a robust VCO design optimized for integration within advanced PLL systems.

To meet the specifications, each block was developed independently and then integrated sequentially for testing and evaluation. Selecting an appropriate oscillator topology was crucial not only to satisfy the performance requirements but also to ensure manufacturability, with considerations for power consumption, area efficiency, future scalability, and noise impact. The ring oscillator topology proved to be the most suitable choice. Furthermore, the necessity of including a buffer was confirmed to prevent loading effects from subsequent circuits and to enable a full signal swing. The voltage-controlled current source (VCCS) design incorporated an operational transconductance amplifier (OTA) to internally fulfill the buffering function, ensuring proper operation while minimizing noise contribution. The design process highlighted the critical role of transistor sizing, as it directly affects parasitic effects and overall circuit behavior. Additionally, it emphasized how each transistor and block influences the global VCO performance and their respective importance within the design.

The results showed that the circuit can match the design specifications. The voltage swing with the typical voltage supply value allows for maximum excursion. For specific frequencies, phase noise had a maximum value of -80.41 dBc/Hz at 1 MHz from the carrier, a great performance over noise for ring oscillators, but also having a margin from the specification. Comparing this result with the same specification for only the oscillator, the VCO circuit is 0.71 dB noisier than the oscillator alone, showing that the complete design did not add much noise to the main block. The duty cycle, rise time, and fall time also show that it can produce a very coherent digital clock signal for other circuits, validating the design concept of the VCO as part of a future PLL. The frequency output is close to 16 GHz for all variations, showing that even though the circuit is not in typical conditions, it still is close to the original design, also the developed feedback line makes it possible for the circuit to converge to the desired frequency. This results shows that the VCO is capable of performing the actions that are intended to it, but also it matches the design specifications made for the project.

The results demonstrate that the circuit meets the design specifications. The voltage swing, under typical supply voltage conditions, achieves maximum excursion. For specific frequencies, the phase noise reaches a maximum value of –80.41 dBc/Hz at 1 MHz offset from the carrier, representing excellent noise performance for a ring oscillator and providing a comfortable margin relative to the specification. Comparing this to the oscillator alone, the full VCO design introduces only 0.71 dB additional noise, indicating that the integrated circuit adds minimal noise beyond the core oscillator block. The duty cycle, rise time, and fall time results confirm that the VCO can produce a highly stable and coherent digital clock signal suitable for downstream circuits, thereby validating the VCO design concept for integration within a future PLL. The output frequency remains close to the target 16 GHz across process, voltage, and temperature variations, confirming robust performance even under non-ideal conditions. Furthermore, the implemented feedback loop ensures frequency convergence to the desired value. These results collectively demonstrate that the VCO not only fulfills its intended function but also aligns well with the project's design specifications.

In comparison to state-of-the-art designs, the performance of this VCO is comparable to results reported in recent literature. Since the referenced works do not share identical specifications with this project, an individual analysis provides clearer insight. For instance, (XIA; WU; TIAN, 2024) employs a more advanced FinFET technology node than this work and discusses a complete PLL implementation. While meeting the frequency specifications, their design exhibits higher power consumption. The work by (LI et al., 2024) also utilizes 12 nm FinFET technology, enabling a more direct comparison. It achieves a phase noise of -81.45 dBc/Hz at 1 MHz offset under typical conditions, whereas this work attains an average phase noise of -83.41 dBc/Hz at 1 MHz across tested corners, with a slightly higher power consumption but operating at a higher center frequency. On the other hand, (SUN et al., 2024) presents a dual LC-based oscillator optimized for different frequency bands, enhancing tunability at the cost of increased area due to the technology node and higher power consumption. Similarly, (TURKER et al., 2018) reports an LC oscillator with improved phase noise performance but with a notable increase in power consumption. Collectively, these comparisons indicate that the proposed VCO design is competitive in terms of phase noise, frequency range, and power efficiency.

Future work could focus on implementing a complete PLL using this VCO as the core oscillation source. This would involve designing and integrating a transistor-level feedback loop and error amplifier to evaluate circuit performance with real components, enabling further testing and optimization of the VCO. Although layout design was considered within the scope of this work, it was deprioritized due to time constraints. Completing the layout would allow more accurate extraction of parasitic effects, enhancing design precision and supporting the circuit's feasibility for fabrication, testing, and eventual production.

Table 31 – State of art comparison with this work

Work	Power supply (V)	Power consumption (mW)	Frequency (GHz)	Phase Noise @ 1 MHz (dBc/Hz)	Tech. (nm)	Topology
LI et al., 2024 ◦	0.8	1.08	0.7 - 12.5	-81.45	12	RO
SUN et at., 2024	1.2	30.07	0.05 - 17.8	-109.9	65	Dual LC
XIA; WU; TIAN; 2024	0.75	4.95	4-16	-	6	RO
TURKER et al.,2018	-	45	7.4 - 14	-123.2	16	LC
LIU; GOH; SIEK, 2005	1.8	50	8.4 - 10.1	-99.9	180	RO
This work *: Typical	0.8	0.91927	16	-83.41	12	RO

Source: Author

*Simulated results only
◦ VCO only

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APPENDIX A – VERILOG-A

As described in the work body, some Verilog-A codes were adapted to compose the feedback circuit line. Some adaptations, as the documentation is scarce, and the first contact with this hardware description language was while developing the work, to fix and understand errors Gemini Pro Artificial Intelligence was used. In sequence, there are the codes adapted from *ahdlLib*:

A.0.1 Frequency to voltage converter

```
`include "discipline.h"
`include "constants.h"


`define PI  3.14159265358979323846264338327950288419716939937511

nature Frequency
   abstol = 1m;
   access = FF;
   units = "Hz";
endnature

module freq_meter(vp,vn,fout);
electrical vp, vn;
electrical fout;
parameter integer log_to_file = 0;

   integer out_file;

   real tlast_cross = -1.0;
   real t_prev_cross = -1.0;
   real fout_freq_val = 0.0;

    parameter real voltage_scaling_factor = 25e-12;

   analog begin

      @ ( initial_step ) begin
         if (log_to_file ) begin
            out_file = $fopen( "%C:r.dat" );
            $fstrobe(out_file,"# Generated by Spectre from module `%M'");
         end
```

```
          V(fout) <+ 0.4;
      end

      @ ( cross (V(vp,vn),0,1.0, vp.potential.abstol) ) begin
          if (tlast_cross >= 0) begin
              t_prev_cross = tlast_cross;
          end
          tlast_cross = $abstime;

          if (t_prev_cross >= 0 && (tlast_cross - t_prev_cross) > 0) begin
           fout_freq_val = 1/(2*(tlast_cross - t_prev_cross));
          end else begin
              fout_freq_val = 0.0;
          end
      end

      if (log_to_file) begin
         $fstrobe(out_file, "%-.10g\t%-.10g", $abstime, V(fout));
      end

      V(fout) <+ fout_freq_val * voltage_scaling_factor;

      @ ( final_step ) begin
         if (log_to_file) $fclose(out_file);
      end
   end
endmodule
```

A.0.2 Error amplifier

```
`include "discipline.h"
`include "constants.h"


module error_calc(sigset, sigact, sigerr);
input sigset, sigact;
output sigerr;
electrical sigset, sigerr;
rotational sigact;
parameter real tdel = 0;
parameter real trise = 10f from (0:inf);
```

```
parameter real tfall = 10f from (0:inf);
parameter real gain = 400;

   analog begin

      V(sigerr) <+ transition(V(sigset) + (gain * (V(sigset) - Theta(sigact))),
          tdel, trise, tfall);

   end

endmodule
```