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Matheus Schramm Dall'Asta

AC-AC Hybrid Boost Switched-Capacitor Converter

Florianópolis

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Matheus Schramm Dall'Asta

AC-AC Hybrid Boost Switched-Capacitor Converter

O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Prof. André Luís Kirsten, Dr.
Universidade Federal de Santa Catarina

Prof. Clóvis Antônio Petry, Dr.
Instituto Federal de Santa Catarina

Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

Bartolomeu Ferreira Uchoa Filho:47636211491
Digitally signed by Bartolomeu Ferreira Uchoa Filho:47636211491
Date: 2019.09.17 16:34:06 -03'00'

Prof. Bartolomeu Uchôa-Filho, Dr.
Coordenador do Programa

Assinado de forma digital por Telles Brunelli Lazzarin:02340071925
Dados: 2019.09.17 09:34:50 -03'00'

Prof. Telles Brunelli Lazzarin, Dr.
Orientador

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Este trabalho é dedicado aos meus pais, Nilda e Paulo.

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"Life is a struggle and the potential for failure is ever present, but those who live in fear of failure, or hardship, or embarrassment will never achieve their potential. Without pushing your limits, without occasionally sliding down the rope headfirst, without daring greatly, you will never know what is truly possible in your life."

William H. McRaven

RESUMO

Esta dissertação apresenta a análise e o projeto de um conversor *boost* híbrido a capacitor chaveado operando como um transformador CA-CA de estado sólido não isolado. A topologia é um resultado da integração de uma célula de comutação indutiva básica com uma célula a capacitor chaveado do tipo *ladder* e realiza a conversão direta de energia com elevado ganho de tensão. A análise teórica apresenta as principais características operacionais do conversor híbrido, incluindo o modelo médio do circuito elétrico equivalente e o cálculo de esforços de corrente nos componentes, considerando o modo de carga parcial dos capacitores. Uma metodologia de projeto é apresentada, detalhando a modulação utilizada e os critérios de escolha dos capacitores, interruptores, do indutor e da frequência de comutação. O estudo é validado através de simulações e experimentação de um protótipo monofásico em dois pontos de operação na frequência da rede elétrica: conversão 55/220 V e 110/400 V com potências nominais de 1 kVA e 2 kVA, respectivamente. A máxima eficiência obtida é 93,9% para cargas resistivas. Os testes experimentais comprovam a operação com diferentes frequências de rede, cargas indutivas e cargas não lineares. Testes adicionais confirmam o funcionamento da estrutura em outros 14 diferentes pontos de conexão de entrada e saída.

Palavras-chave: Conversor Boost Híbrido CA-CA, Capacitor Chaveado, Autotransformador Monofásico de Estado Sólido.

RESUMO EXPANDIDO

Introdução

Autotransformadores de baixa tensão têm sido utilizados por décadas como forma de adequação de níveis de tensão entre fonte e carga, principalmente em aplicações que não exigem o isolamento galvânico. No entanto, estes dispositivos geralmente são volumosos, pesados, geram ruídos audíveis e utilizam grande quantidade de ferro e cobre. Recentemente, conversores estáticos operando com frequências de comutação na faixa de dezenas e centenas de kHz foram sugeridos como alternativas aos autotransformadores, com principais vantagens sendo a redução do peso e do volume e também a possibilidade de controlar o valor da tensão de saída. Nessa classe de conversores estão aqueles originados a partir de topologias clássicas CC-CC, como os conversores *buck*, *boost* e *buck-boost*. No entanto, estas estruturas não são adequadas para aplicações onde elevada relação de transformação é necessária. Outras topologias emergentes têm como base o conceito de capacitores chaveados. Elas permitem a obtenção de elevadas relações de transformação empregando apenas capacitores e semicondutores de potência, porém são dificilmente controláveis devido ao ganho de tensão praticamente fixo. Assim, sugere-se a utilização de conversores híbridos a capacitor chaveado, que integram uma célula de comutação indutiva (por exemplo o conversor *boost*), para obter a controlabilidade, com células a capacitor chaveado (por exemplo a célula *ladder*), para obter maiores ganhos de tensão.

Objetivos

Esta dissertação tem como objetivo principal realizar o estudo de uma topologia híbrida de conversor CA-CA empregando célula de comutação indutiva com uma célula a capacitor chaveado. Os objetivos secundários são: (i) analisar os conversores *ladder*, *boost* e híbrido; (ii) calcular os esforços de corrente nos componentes a partir da variação de quantidade de carga e considerando o modo de carga parcial dos capacitores; (iii) representar os conversores com um modelo médio equivalente; (iv) projetar um controlador para regular a tensão de saída; (v) propor novas topologias híbridas; (vi) validar experimentalmente o conversor híbrido.

Metodologia

Inicialmente é apresentada uma revisão dos conversores a capacitor chaveado e suas aplicações na eletrônica de potência. A célula unitária é analisada considerando ambos os modos de operação de carga parcial e sem carga dos capacitores. O modelo médio equivalente e os valores máximos e eficazes das correntes e das tensões nos componentes são obtidos. Na sequência, a célula *ladder* CA-CA é analisada e suas características são comparadas com a célula unitária. O modelo médio equivalente também é encontrado e a partir dele uma análise de potências ativa e reativa é realizada.

Em seguida, o conversor *boost* CA-CA é apresentado juntamente com a análise estática da topologia. As expressões dos valores de tensões e correntes considerando a operação CA são determinadas, destacando-se as diferenças em relação ao modo CC-CC. O modelo médio equivalente é obtido e uma análise de potências é efetuada. Devido à operação com tensões e correntes alternadas, o funcionamento do conversor empregando interruptores de quatro quadrantes é detalhado, com destaque à técnica de modulação utilizada. Além disto, é verificada a necessidade de adicionar um circuito de grampeamento para evitar sobretensões sobre os interruptores. Nota-se a possibilidade de controlar o valor de pico/eficaz da tensão

de saída a partir da variação da razão cíclica.

Seguindo a proposta do trabalho, o conversor híbrido resultante da integração do conversor *boost* com a célula a capacitor chaveado do tipo *ladder* CA-CA é analisado. As etapas de operação são descritas e o equacionamento é realizado considerando os modos de operação com carga parcial ou sem carga. As características estáticas e dinâmicas são obtidas e a estrutura é comparada com as suas partes integrantes. Detalhes de projeto são apresentados e exemplificados, incluindo a escolha do indutor, dos capacitores, dos interruptores e da frequência de comutação. O projeto de um compensador para controlar o valor de pico da tensão de saída é mostrado.

A partir da topologia híbrida CA-CA proposta, outras 14 derivações foram obtidas, sendo estas todas bidirecionais. Outras variações topológicas são sugeridas, como o acréscimo de mais estágios a capacitor chaveado, a inserção de um indutor para a operação como conversor ressonante, a redução do número de interruptores e a aplicação do conceito em conversores trifásicos.

Resultados e discussão

Os testes foram efetuados para duas condições de operação: conversão de 55/220 V e 110/400 V, com potências nominais de 1 kVA e 2 kVA, respectivamente, na frequência da rede de 60 Hz. Na operação em 55/220 V, o conversor operou com baixas taxas de distorção harmônica nas variáveis de entrada e saída, com o valor do fator de potência medido igual a 0,97 capacitivo e eficiência de 89% nas condições nominais e carga resistiva. Verificou-se que, em baixos níveis de carga, a eficiência e o fator de potência são bastante reduzidos, devido à grande parcela de corrente reativa que circula internamente no conversor devido à presença dos capacitores. O funcionamento do conversor foi verificado com cargas indutivas e não-lineares e, além disto, observou-se a possibilidade de operação em outras frequências de entrada: 16,67 Hz, 50 Hz, 100 Hz e 400 Hz. Adicionalmente, verificou-se o funcionamento com cargas individuais resistivas de 250 W, com uma conectada na saída de 110 V e a outra na saída de 220 V. Por fim, foram analisadas outras 14 possíveis conexões de entrada/saída do conversor para potências em torno de 400 W.

Para a operação em 110/400 V, não foi possível utilizar uma fonte de tensão estabilizada como tensão de entrada. Assim, quando conectado à rede elétrica através de um transformador, é verificada uma distorção na forma de onda da tensão de entrada, que é refletida para a saída do conversor. No entanto, os resultados dos testes mostraram valores de eficiência e fator de potência de 93% e 0,91 capacitivo, respectivamente, nas condições nominais com carga resistiva. Um teste adicional verificou a operação com uma carga indutiva de 1950 VA e fator de potência 0,916, resultando em valores de eficiência e de fator de potência de entrada iguais a $94,6\%$ e 0,99, respectivamente.

A experimentação também ocorreu com o conversor operando em malha fechada, validando uma de suas vantagens em relação às estruturas puramente a capacitor chaveado, que é a controlabilidade da tensão de saída. O conversor se comportou de maneira estável durante transitórios de degrau de carga e variações na tensão de entrada.

Considerações finais

Esta dissertação apresenta a análise de um conversor *boost* híbrido a capacitor chaveado operando como um autotransformador monofásico CA-CA. A análise estática é efetuada considerando a operação no modo de carga parcial e os resultados teóricos e de simulação estão de acordo com aqueles obtidos experimentalmente.

O conversor apresentou funcionamento adequado para as condições de operação propostas. O dobro do ganho de tensão de um conversor *boost* convencional pode ser obtido, além de permitir a controlabilidade da tensão de saída a partir de uma malha de controle simples, o que é difícil de se obter em conversores puramente a capacitor chaveado. Além disto, os esforços de tensão sobre os capacitores e interruptores são reduzidos à metade em relação ao conversor *boost* e as tensões sobre os capacitores são equilibradas naturalmente. O funcionamento em tensões ou frequências mais elevadas resulta em um aumento da energia reativa consumida, reduzindo os seus valores de eficiência e fator de potência. Por apresentar inerentemente fator de potência capacitivo, seu melhor ponto de operação ocorre para cargas indutivas, em que a energia reativa da carga é compensada pelo conversor.

Como trabalhos futuros, as sugestões incluem o estudo da topologia monofásica com duas células *ladder* conectadas de forma diferencial, a adição do número de células a capacitor chaveado, a inserção de um indutor em série com o capacitor chaveado para a operação como conversor ressonante e consequente redução das perdas de comutação, o estudo de outras conexões de entrada e saída nesta mesma topologia e a aplicação do conceito em conversores trifásicos CA-CA híbridos controlados.

Palavras-chave: Conversor Boost Híbrido CA-CA, Capacitor Chaveado, Autotransformador Monofásico de Estado Sólido.

ABSTRACT

This master thesis presents the analysis and design of a hybrid boost switched capacitor converter operating as an AC-AC solid-state non-isolated transformer. The topology is a result of the integration between a basic inductive switching cell with a switched capacitor ladder cell and performs the direct energy conversion with a high gain output voltage. The theoretical analysis presents the main operational characteristics of the hybrid converter, including the equivalent average electric circuit model and the current stresses calculation considering the partial charge operating mode of the capacitors. A design methodology is presented, focusing on the modulation technique and criteria for determining capacitors, semiconductor devices, inductor and switching frequency. Simulation and experimental results validate the study with a single phase prototype in two different operation points at the grid frequency: 55/220 V and 110/400 V voltage conversion with 1 kVA and 2 kVA rated power, respectively. The maximum measured efficiency is 93.9% for a resistive load. Additional tests prove the operation at different grid frequencies and loads (inductive and non-linear). Tests also confirm the operation of this structure in another 14 different input and output connections.

Keywords: AC-AC Hybrid Boost Converter, Switched Capacitor, Single-Phase Solid-State Autotransformer.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
CC	Complete Charge
CCM	Continuous Conduction Mode
CMC	Conventional Matrix Converter
C-BBC	Current DC-Link Back-to-Back Converter
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DL	Double Ladder
HBSCC	Hybrid Boost Switched Capacitor Converter
IMC	Indirect Matrix Converter
NC	No charge
PC	Partial charge
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SCC	Switched-Capacitor Converter
SL	Single Ladder
THD	Total Harmonic Distortion
V-BBC	Voltage DC-Link Back-to-Back Converter

LIST OF SYMBOLS

$v_i(t)$	Input voltage
$v_o(t)$	Output voltage
L	Input inductance
S_k	Switch k (k=1,2,...)
C_k	Capacitor k (k=1,2,...)
Z_o	Impedance load
$s_k(t)$	Switching function k (k=1,2,...)
R_o	Output resistance
X_o	Output reactance
C_o	Output capacitor
C_{sc}	Switched-capacitor
$i_o(t)$	Output current
i_{C_o}	Current through the output capacitor
$i_{C_{sc}}$	Current through the switched capacitor
v_{S_k}	Voltage over the switch k (k=1,2,...)
i_{S_k}	Current through the switch k (k=1,2,...)
d	Duty cycle
T_s	Switching period
r_s	Conduction resistance of a switch
r_k	Conduction resistance of the switch k (k = 1,2,...)
V_{ip}	Input voltage peak value
t	Time
I_{op}	Output current peak value
i_i	Input current
$v_{C_{sc}}$	Voltage over the switched-capacitor
ωt	Grid angle
ω_g	Angular grid frequency
ϕ_{io}	Output current phase angle
f_s	Switching frequency
f_g	Grid frequency
x	Generic variable
i_c	Current through a generic capacitor
v_c	Voltage over a generic capacitor
C	Generic capacitance
q_c	Net capacitor charge during a switching period
$q_{C_{sc}}$	Net charge in the switched capacitor during a switching period
q_{C_o}	Net charge in the output capacitor during a switching period
q_o	Net load charge during a switching period
T_c	Charging time of a capacitor
I_{nc}	Current through a capacitor for no-charge mode
I_{ipc}	Initial current in a capacitor during partial charge mode

I_{fpc}	Final current in a capacitor during partial charge mode
I_{cc}	Initial current in a capacitor for complete charge mode
q_{charge}	Generic net charge in a capacitor
I_{C_{sc},nc_1}	Switched capacitor current during first operating stage in no charge mode
I_{C_{sc},nc_2}	Switched capacitor current during second operating stage in no charge mode
X_{ef}	Effective value of a generic variable x
θ	Grid angle
$i_{S_k,nc}$	Current through switch k for no-charge mode. (k = 1,2,...)
$i_{C_{sc},nc}$	Switched capacitor current for no-charge mode.
$i_{C_{sc},nc}$	Current through the output capacitor for no-charge mode.
τ_1	Time constant in the first operating stage
$i_{C_{sc},1}$	Switched capacitor current during the first operating stage
τ_2	Time constant in the second operating stage
$i_{C_{sc},2}$	Switched capacitor current during the second operating stage
$i_{C_o,2}$	Output capacitor current during the second operating stage.
τ	Time constant
$I_{S_k,ef}$	Effective value of current through the switch k (k=1,2,...)
$I_{C,ef}$	Effective value of current through a capacitor
k_r	Resistance factor
k_{r_m}	Resistance factor of the switch m (m = 1, 2, ...)
$I_{S,pc,ef}$	Effective value of the current through a switch during partial-charge mode
$I_{S,nc,ef}$	Effective value of the current through a switch during no-charge mode
X	Amplitude of a generic phasor $\boldsymbol{x}$
ϕ	Angle of a generic phasor $\boldsymbol{x}$
$\boldsymbol{x}$	Generic phasor
j	Imaginary unit $j = \sqrt{-1}$
R_{out}	Output series equivalent resistance
$v_{o,avg1}$	Output voltage for the no-charge average model
$v_{o,avg2}$	Output voltage for the partial charge average model
$v_{o,sw}$	Output voltage for the switched model
r'_k	Equivalent resistance of switch k (k = 1, 2, ...)
PF_o	Output power factor
PF_i	Input power factor
ϕ_o	Output phase angle between current and voltage
I_o	Output current effective value
V_i	Input voltage effective value
G	Ideal voltage gain
v_L	Voltage over the input inductor
i_L	Current through the input inductor
L	Inductance

I_{ip}	Input current peak value
g_v	Voltage gain
f_{ress}	Resonant frequency
y_i	Input admittance
Q_i	Input reactive power
Q_o	Output reactive power
I_L	Inductor current effective value
T_D	Dead time
S_{ka}	Lower MOSFET of switch k
S_{kb}	Upper MOSFET of switch k
V_{lim}	Limit voltage of conventional modulation
δ	Ratio between total dead time and switching period
R_{cl}	Clamping resistor
C_{cl}	Clamping capacitor
D_{cl}	Clamping diode
v_{cl}	Clamping voltage
V_{clp}	Peak clamping voltage
V_{cli}	Initial clamping voltage
Δv_{cl}	Clamping voltage ripple
t_α	Modulation-changing time
α	Angle when modulation changes
C_k	Capacitance k ($k = 1, 2, ...$)
i_{C_k}	Current through a capacitor k ($k = 1, 2, ...$)
v_{C_k}	Voltage over a capacitor k ($k = 1, 2, ...$)
C_{eq}	Equivalent capacitance
S_i	Input apparent power
$Q_{o,opt}$	Optimum output load reactive power
$i_{C_k,nc}$	Current through capacitor k for no-charge mode (k = 1,2,...)
$i_{C_k,1}$	Current through capacitor k in first operating stage (k = 1,2,...)
$i_{C_k,2}$	Current through capacitor k in second operating stage (k = 1,2,...)
r_L	Inductor parasitic resistance
$\overline{R_{out}}$	Parameterized output resistance
X	Steady-state value of a generic variable x
$\tilde{x}$	Small-signal variation of a generic variable x
S_o	Output apparent power
ΔI_L	Input current ripple
ΔV_o	Output voltage ripple
Q_L	Reactive power in the inductor
Q_C	Reactive power in the capacitors
ϕ_i	Phase displacement between input voltage and current
P_d	Total power losses
$v_{o,ref}$	Reference voltage
$v_{o,meas}$	Measured voltage

e	Error signal
$C(s)$	Controller transfer function
$G(s)$	Converter transfer function
$H(s)$	Measurement transfer function
k_v	PI-Controller gain
w_z	Zero of the PI-controller
PM	Phase Margin
f_c	Cross frequency
ω_c	Angular cross frequency
k_c	Total loop gain
k_{vs}	Voltage sensor gain
k_{sig}	Signal conditioning circuit gain
k_{adc}	Analog-Digital Converter gain
k_{pwm}	Modulator gain
T_i	Controller time constant
N	Number of cells
N_p	Number of cells in the positive side
N_n	Number of cells in the negative side
$V_{S,max}$	Maximum voltage stress over a switch
$V_{C,max}$	Maximum voltage stress over a capacitor
$V_{o,alternative}$	Alternative output voltages
V_{km}	Differential voltage between points k and m
N	Number of connection points
N_{diff}	Number of possible differential voltages
N_g	Number of possible voltage ratios

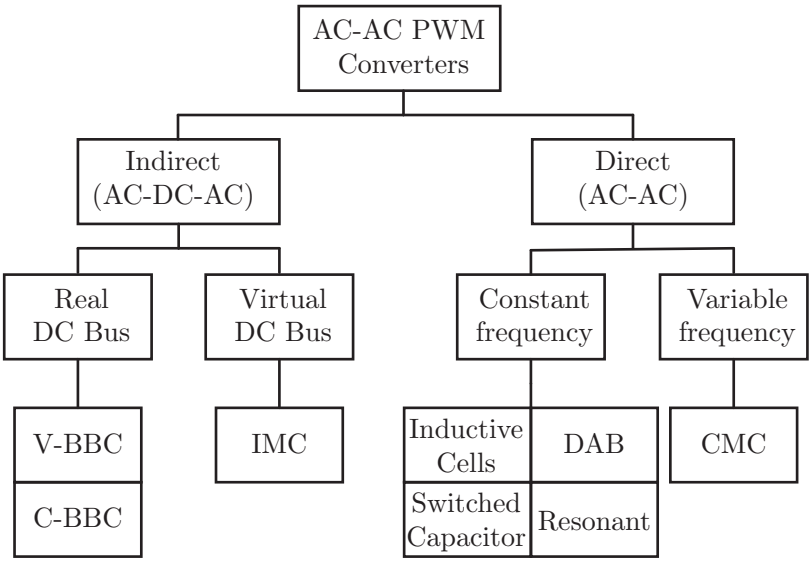
CONTENTS

1 INTRODUCTION

Autotransformers have been employed for decades in residential and industrial applications as devices that adjust the voltage levels between the electric grid and equipment when isolation is not a requirement. These devices are usually bulky and provide a fixed voltage gain, not being able to supply all loads maintaining the energy quality. Then, power converters employing solid state devices have been developed to fill this gap, whose characteristics may include the regulation of output voltage/current, power factor correction, harmonic elimination, among others. Some thyristor-based converters were developed to perform the AC-AC conversion, such as the cycloconverters. High level of harmonic components at low frequencies, bulky filters and the limitation of voltage/frequency conversion range are some of their characteristics.

During the last decades, the PWM AC-AC converters have been explored. Figure 1.1 shows a simplified diagram of most researched topologies. The indirect converters perform the AC-AC conversion by creating a DC-bus, which can be either assured by a capacitor/inductor or be virtual. They are usually able to change the output frequency, as one AC-port is dynamically decoupled from the other. In direct converters, all the currents and voltages are alternating. Most topologies grant a regulated output voltage and some of them might also convert the grid frequency (KOLAR et al., 2011).

Figure 1.1 – PWM AC-AC Converters.

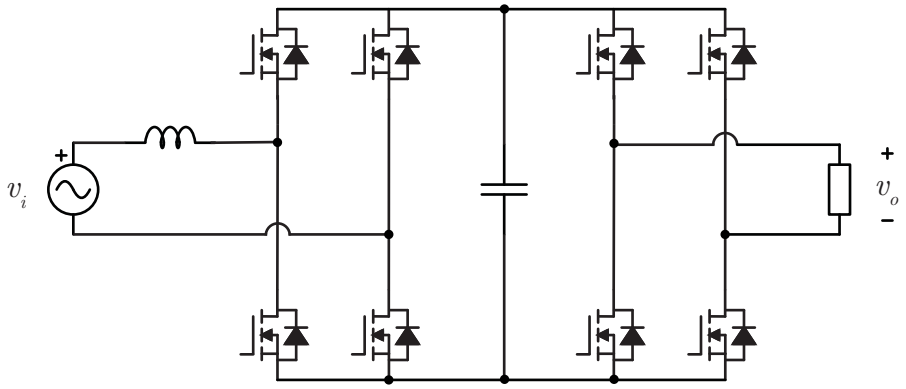


Source – Author.

Among the AC-AC topologies, the indirect converter with a decoupling capacitor in DC bus, referred as Voltage dc-link Back-to-Back Converter (V-BBC) and shown in Figure 1.2, is the most researched and developed in academy and industry (FRIEDLI et al., 2012). While it is bulky because of the electrolytic capacitor in the DC voltage bus,

the decoupling of input and output dynamics increases its reliability and facilitates the control strategy. The main frequency and voltage values can be modified and the operation with input power factor correction is possible. Only two-quadrant switches are employed, which also increases the reliability. The main drawbacks of this converter are the bulky DC energy storage element and the DC-voltage level, which must be always higher than the output voltage. Also, the input and output grounds are not connected, which may lead to common current mode issues.

Figure 1.2 – Single-phase Voltage DC-link Back-to-Back Converter (V-BBC).



Source – Author.

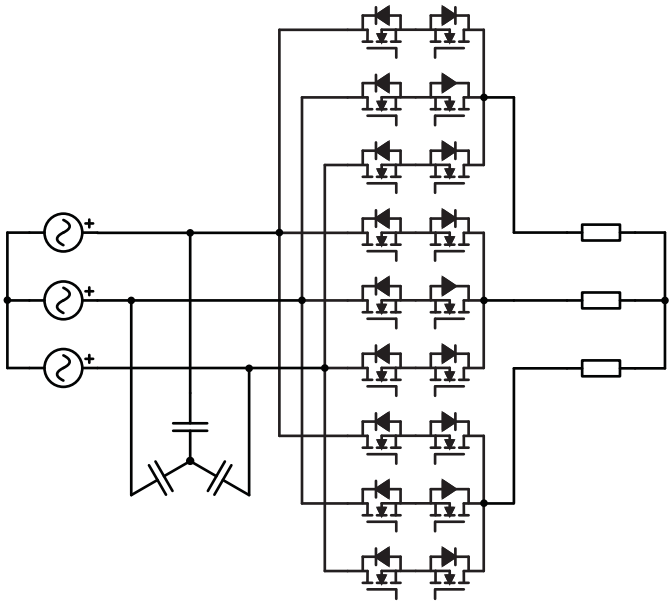
In order to reduce size/weight and increase the power density, other AC-AC topologies were developed to eliminate the DC-link devices. The Indirect Matrix Converter (IMC) (WEI; LIPO, 2001) presents a similar structure to the three-phase V-BBC, however it does not contain a DC-link capacitor. The converter employs four-quadrant switches in the input stage and generate a virtual voltage DC-link, resulting in a high power density. The drawback of this topology is the increased complexity of the modulation and the reduced reliability.

A direct version of this topology is the three-phase conventional matrix converter (CMC), shown in Figure 1.3. It also achieves high levels of power density at the cost of an increased complexity in modulation schema, even when compared to the IMC. Alongside its characteristics, there are the voltage and frequency regulation and the absence of magnetic elements (besides input/output EMI filters) (KOLAR et al., 2011).

Regarding isolated topologies, there is the Dual Active Bridge converter (DAB) (KANG; ENJETI; PITEL, 1999), depicted in Figure 1.4. It is composed of two active bridges connected via a high-frequency transformer and the power flow is usually controlled by phase shift modulation between the input and output bridges, while the grid frequency is unchanged. This topology employs four-quadrant switches, whose maximum voltage stresses are the grid voltage levels.

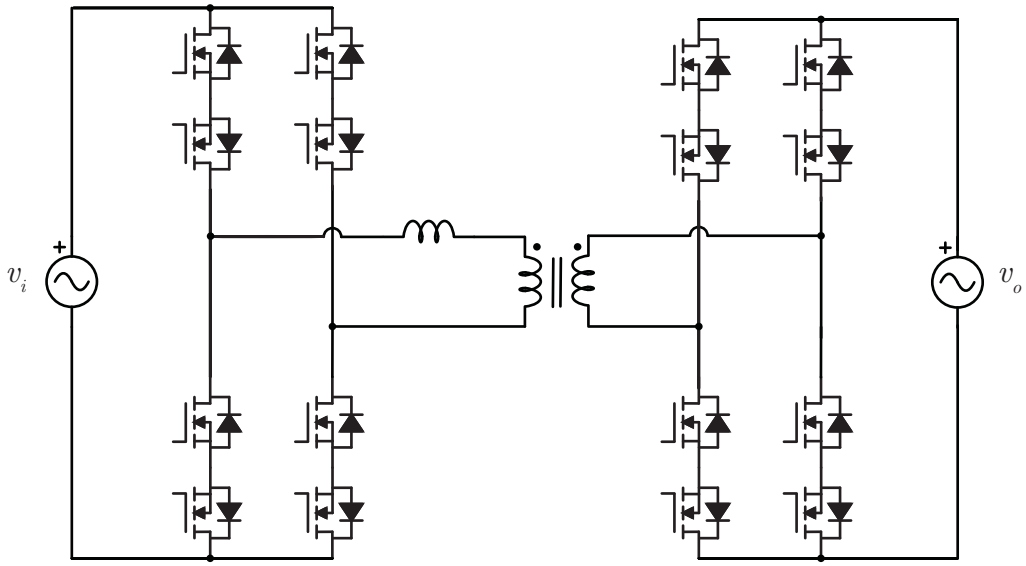
Other family of direct AC-AC converters comes from widely known topologies. By modifying the switching realization, both isolated as non-isolated inductive DC-DC

Figure 1.3 – Three-phase direct conventional matrix converter (CMC).



Source – Adapted from (FRIEDLI et al., 2012).

Figure 1.4 – Single-phase Dual Active Bridge (DAB) converter.

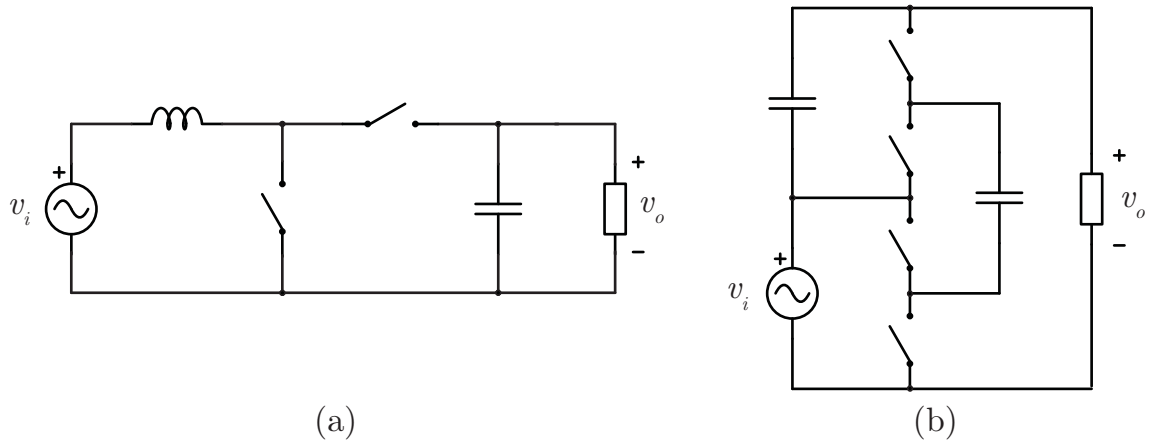


Source – Adapted from (KANG; ENJETI; PITEL, 1999).

converters can be employed in AC-AC systems (ROSAS-CARO et al., 2010) (SRINIVASAN; VENKATARAMANAN, 1995). Figure 1.5(a) shows the AC-AC boost converter, whose main advantages are the common input and output grounds, the low device count and the constant duty cycle. Its output voltage can be only higher than the input voltage. Moreover, it employs four-quadrant switches, that are submitted to the output voltage levels and input current levels, reducing its efficiency for high voltage gains. Regarding the frequency, it is not variable.

During the last decade some switched-capacitor converters have been proposed

Figure 1.5 – (a) AC-AC boost converter; (b) AC-AC Ladder Switched-Capacitor converter.



Source – Author.

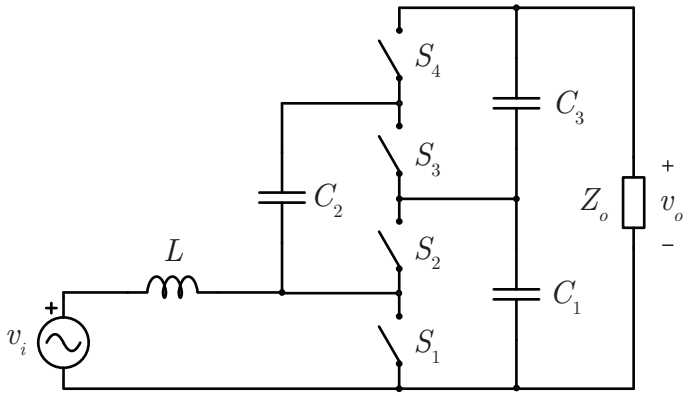
as alternatives for the AC-AC fixed frequency conversion. A basic converter is shown in Figure 1.5(b) (ANDERSEN; LAZZARIN; BARBI, 2013). It provides a fixed voltage gain of 2 and operates without any closed-loop control. The switches operate in four quadrants and their voltage stresses are from the low-voltage side, which is a great advantage in comparison to most topologies. The absence of magnetic elements leads to a high power density. Its major drawback is the difficulty to control the output voltage. Furthermore, the parallelism of capacitors during one part of the switching period leads to current spikes, that depend on the capacitances and the conduction resistances of the switches.

1.1 MOTIVATION

Switched capacitor converters are well known in the field of low-voltage electronics, given their simplicity and the absence of magnetic elements. Recently, these converters have been researched for operations in higher voltage and power levels, mainly for DC-DC conversion. Thus, hybrid switched capacitor converters were presented, aggregating the characteristics of high voltage gain and sharing of voltage stresses in traditional topologies. The presence of a magnetic element means that the converter can be controlled via duty cycle variation, which complements the issue from which pure Switched Capacitor Converters (SCCs) suffer.

Aiming a controllable and high gain non-isolated direct AC-AC converter, this works presents the study of the integration of a basic AC-AC inductive cell with a switched-capacitor ladder cell, as shown in Figure 1.6. This converter could be employed as an solid state autotransformer with an output RMS voltage control, in which the desirable voltage ratio is greater than 2.

Figure 1.6 – AC-AC Hybrid Boost Switched-Capacitor Converter.



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1.2 GOALS AND CONTRIBUTIONS

The general purpose of this Thesis is to perform the analysis and experimental validation of the boost converter integrated with a switched capacitor cell operating as an AC-AC converter. The goals of this work regarding the study of the topology are listed as:

- Analysis of the operating stages;
- Mathematical analysis employing phasors theory;
- Calculation of current efforts based on charge flow quantity and simplified solutions of differential equations;
- Representation of a hybrid converter as an average equivalent circuit model;
- Dynamic analysis and control design;
- Simulation and experimental validation;
- Proposal of new topologies of AC-AC converters;

Some contributions of this Thesis are:

- Simplified methodology to obtain current equations in AC-AC switched capacitor converters;
- Design methodology to obtain an accurate average model of hybrid switched-capacitor converters;
- Validation of an AC-AC hybrid boost switched-capacitor topology.

1.3 GENERAL OUTLINE

The document outline is hereafter described:

Chapter 2: A brief history of switched-capacitor converters and a literature review are presented. The study of an unitary cell is performed to analyze the main

characteristics of a switched-capacitor converter. The ladder cell is analyzed as an AC-AC converter, introducing the currents analyses via differential equations.

Chapter 3: This chapter focuses on the basic AC-AC boost converter. The analogy to the DC-DC converter is made, highlighting their differences. A study regarding the commutation problem is performed, leading to an alternative modulation schema combined with a passive voltage clamping circuit.

Chapter 4: An AC-AC hybrid boost switched capacitor converter is proposed and analyzed. The steady-state and dynamic analyses are performed and an equivalent average circuit model is obtained. Control methods are discussed and design equations are analyzed to obtain the best operating points.

Chapter 5: This chapter discusses the experimental results. Details of the prototype are mentioned and results for 55/220 V and 110/400 V operating conditions are shown. The converter is also validated experimentally for different input frequencies, duty cycles, loads and input/output connections. Efficiency and power factor curves are presented.

Chapter 6: Topological variations of the converter are proposed: insertion of a higher number of switched capacitor cells, different input/output connections, three-phase versions, resonant switched-capacitor converter and two-bridge structure. Simulated and some experimental results are presented.

Chapter 7: A final discussion concludes this Thesis followed by suggestions of future studies.

2 SWITCHED CAPACITOR CONVERTERS

Switched capacitor converters are mainly characterized by employing only capacitors and semiconductor devices in order to provide voltage conversion. They have been developed since the beginning of the 20^{th} century (TANZAWA, 2016). In 1914, Greinacher published experimental validation of a voltage doubler operating at the grid frequency. Cockcroft-Walton expanded the concept to several voltage multiplier stages, making an 1 MV prototype (COCKCROFT; WALTON, 1932), which is currently known as the ladder cell. Later on, other SCCs were developed, such as the series-parallel (BRUGLER, 1971), the parallel connection (FALKNER, 1973), (DICKSON, 1976), the Fibonacci (UENO et al., 1991) and the exponential (CERNEA, 1995).

In the early of 1990s, the development of high frequency switching devices allowed the manufacture of SCCs operating as active switching converters. The first ones operated with a DC-DC conversion, expanding later for AC-DC, DC-AC and AC-AC applications (IOINOVICI,). The main difference between switched-capacitor converters and inductive switching converters is the absence of magnetic elements, because SCCs are composed mainly by capacitors and semiconductor devices.

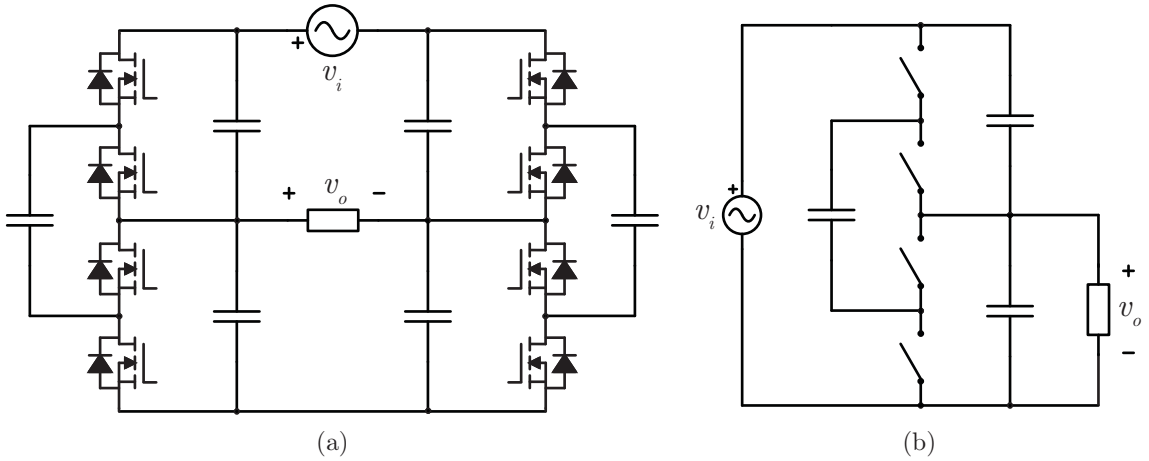
2.1 AC-AC SWITCHED CAPACITOR CONVERTERS

AC-AC switched capacitors converters were firstly introduced in 2012 by (LAZZARIN et al., 2012), in which two ladder cells were connected to provide a voltage gain of 2. The proposed converter is depicted in Figure 2.1(a) and consists of the differential connection of two ladder cells, named in this master thesis as Double Ladder (DL) configuration. Eight MOSFETs and six capacitors are employed, whose block voltages are rated to half the high-side peak voltage value. An experimentation was performed with a prototype rated to 600 W and a voltage conversion from 220 V to 110 V at the grid frequency, obtaining a maximum efficiency of 95.6% at 180 W and 90.6% at rated power. The provided voltage gain is fixed and a common ground is not shared between input and output (MARTINS, 2013).

One year later a new version of this topology was presented, as shown in Figure 2.1(b), which contains just one ladder cell and is named in this master thesis as Single Ladder (SL) configuration. Four switches composed of two reverse-series connected MOSFETs are employed (ANDERSEN; LAZZARIN; BARBI, 2013) and, comparing to the first converter, the capacitor count is reduced from 6 to 3. A prototype was developed for a rated power of 1 kW and a voltage conversion from 220 V to 110 V, obtaining a maximum efficiency of 98% and reached 96% at rated power.

The addition of a inductance connected in series with the switched capacitor is

Figure 2.1 – First AC-AC switched-capacitor converters. (a) Double-Ladder converter; (b) Single-Ladder converter.

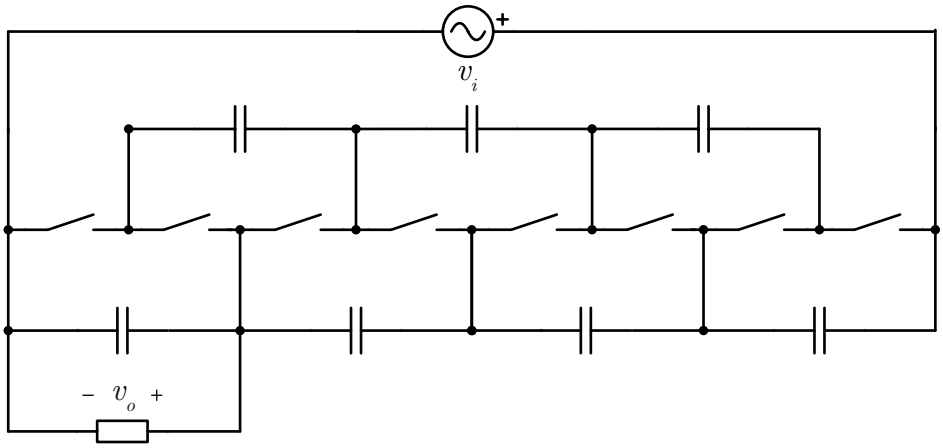


Source – Adapted from (LAZZARIN et al., 2012).

known as an alternative to reduce the switching losses in DC-DC switched-capacitor converters, which operate as resonant converters. This concept was employed for AC-AC operation in (MU et al., 2016).

The concept of AC-AC SCCs was further developed by (YOU; HUI, 2015), in which a ladder cell with multiple stages provides some fixed voltage gain ratios, as depicted in Figure 2.2. The lower possible gain is 1/4, at the cost of eight bidirectional switches (16 MOSFETs) and seven capacitors.

Figure 2.2 – AC-AC converter with multiple ladder cells.

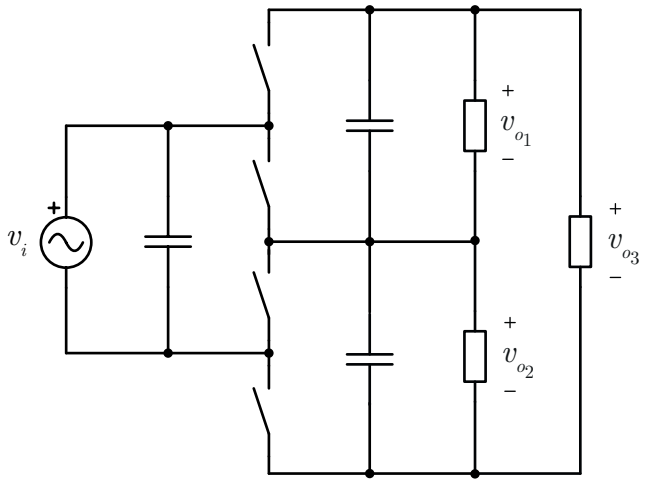


Source – Adapted from (YOU; HUI, 2015).

Later on, the AC-AC ladder cell was proposed as a split-phase autotransformer with and input voltage of 110 V and 110 V/110 V/220 V output voltages, as shown in Figure 2.3 (BARBI; MOCCELINI; LAZZARIN, 2015). A prototype was developed for a rated power of 1 kW and operated in a range from 16.67 Hz to 400 Hz at grid frequency. This topology was also employed in an intermediate stage of an single-phase inverter (Dal

Pont et al., 2015).

Figure 2.3 – Ladder cell used as split-phase autotransformer.



Source – Adapted from (BARBI; MOCCELINI; LAZZARIN, 2015).

In order to improve efficiency for higher gains, some AC-AC converters have been proposed . One example, from (DO; OOTA; EGUCHI, 2017), shows a switched capacitor AC-AC converter using nested voltage equalizers. Compared to the traditional topology, there is an increase in the efficiency and a reduction in the component count for the same voltage gain. On the other hand, the voltage stresses are not equal shared among the capacitors and switches. In (HE; NAI; ZHANG, 2018), a Bridge Modular Switched Capacitor AC-AC bidirectional converter was presented. It provides a $4N$ gain for N series-connected modules, at the cost of higher voltage stresses and no common-ground between input and output ports. Another example is found in (EGUCHI et al., 2018). In general, the main characteristics of AC-AC SCCs are:

- Almost entirely absent of magnetic elements (EMI filters are needed);
- Lower size and weight when compared to autotransformers;
- Scalable voltage gain by adding more cells;
- Operation in open-loop with a good voltage regulation;
- Capacitive power factor for resistive loads;
- May allow multiple output voltage levels;
- A high number of semiconductor devices and capacitors is necessary;
- Duty cycle variation is not able to control the output voltage;
- May have high peak current values in semiconductor devices and capacitors.

These topologies can also be performed as three-phase solid-state transformers. In (LAZZARIN; ANDERSEN; BARBI, 2015), a 6 kW 220/380 V prototype was developed and compared to a comercial autotransformer.

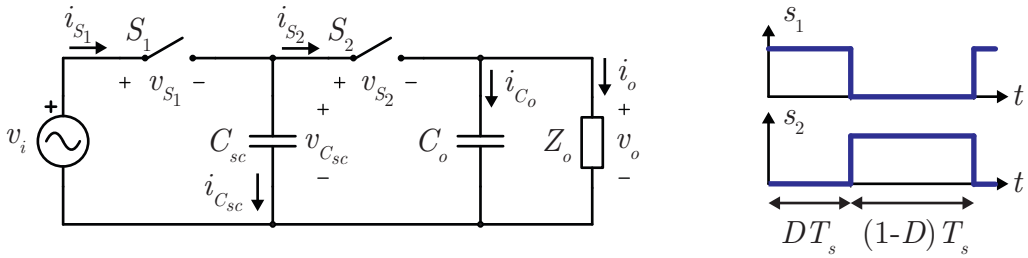
One drawback from pure switched capacitor converters operating at high power levels is the high peak current values in semiconductor devices and capacitors, which might reduce the device's lifespan, increase the conduction and switching losses and cause EMI problems. Aiming to diminish this problem, some authors prefer to add a small inductance connected in series with the switching capacitor. This results in sinusoidal-shaped current waveforms, reducing the switching losses and the EMI effects. However, for pure AC-AC converters, the addition of a small inductance may cause overvoltages during the commutation, because if the value of the current in the inductor is not zero during the dead-time, there is no path where it can flow through. Thus, the modulation schema must be modified or an additional current path should be provided.

Next section focuses on the study of a basic switched capacitor cell, which explains the principle of operation of a pure switched capacitor converter.

2.2 BASIC SWITCHED CAPACITOR CELL

The switched capacitor analysis is performed initially for a basic SC cell, shown in Figure 2.4. It is composed of two bidirectional switches S_1 and S_2, one switched capacitor C_{sc} and one output capacitor C_o. The switches conduct complementary and their conduction times are given respectively by the switching functions s_1 and s_2, which are also shown in Figure 2.4. The input sinusoidal voltage source v_i is considered ideal and the load is a linear impedance $Z_o = R_o + jX_o$.

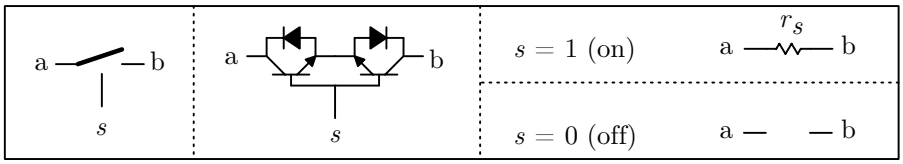
Figure 2.4 – Basic AC-AC switched-capacitor cell.



Source – Author.

Since both the input voltage and the output current are sinusoidal, switches S_1 and S_2 must be able to operate in the four quadrants (positive and negative current and voltage). By empolying MOSFETs in series-reversed connection, a simple switch realization and its simplified equivalent model are shown in Figure 2.5 . In some analysis, switches conduction resistances r_s are employed. This analysis consider that both MOSFETs that compose a switch receive the same drive signal, meaning that their body diode would never conduct. Thus, the conduction resistance r_s is given by the sum of drain-source resistances of two MOSFETs.

Figure 2.5 – Four quadrant switch realization.



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The input voltage source v_i is defined as

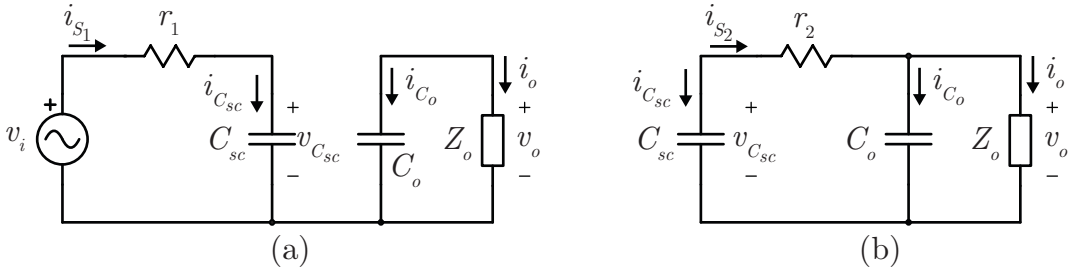
$$v_i(t) = V_{ip} cos(\omega_g t), \tag{2.1}$$

where V_{ip} is the input voltage peak value and ω_g the angular frequency. The analysis of operating stages consider that the load is resistive and the grid frequency is much higher than the switching frequency, then the input voltage source can be considered constant during a switching period. Operating stages are hereafter described for a positive input voltage and illustrated in Figure 2.6.

First stage ($0 < t < DT_s$): The capacitor C_{sc} is charged by the input voltage source v_i and the output capacitor C_o supplies energy to the load. The voltage $v_{C_{sc}}$ is approximately equal to input voltage v_i.

Second stage ($DT_s < t < T_s$): The capacitor C_{sc} delivers energy to the output capacitor C_o and to the load. The voltage v_o is approximately equal to the voltage $v_{C_{sc}}$.

Figure 2.6 – Equivalent electric circuit for the basic cell. (a) First operating stage ($0 < t < DT_s$). (b) Second operating stage ($DT_s < t < T_s$).



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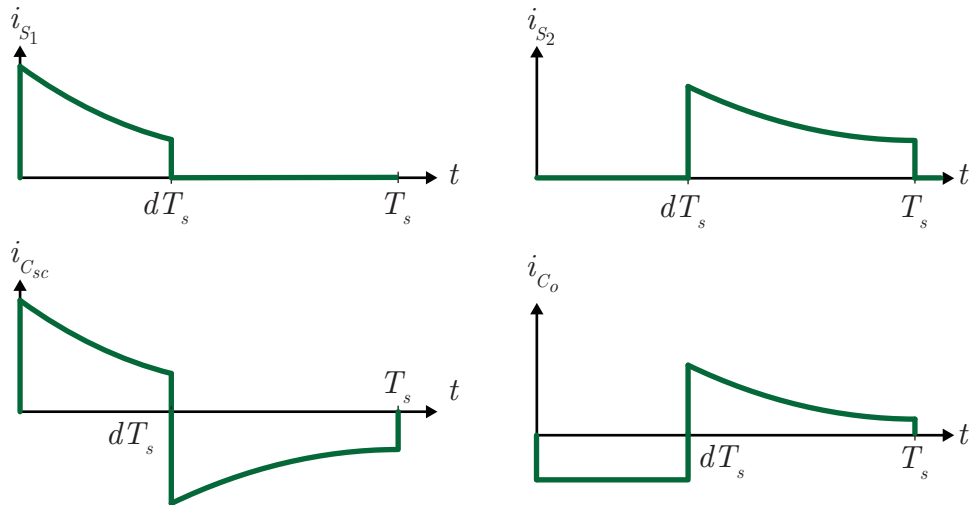
Currents waveforms for a switching period during the positive half-cycle are depicted in Figure 2.7. It should be noted that the currents present an exponential waveform, given that the switched capacitor is either connected in parallel to a voltage source or to the output capacitor. Thus, the currents on the switched capacitor are limited only by the parasitic resistances (in fact, the parasitic inductances also limit the currents, but their influences are neglected in this analysis).

Considering a grid period, the main waveforms are displayed in Figure 2.8. It is

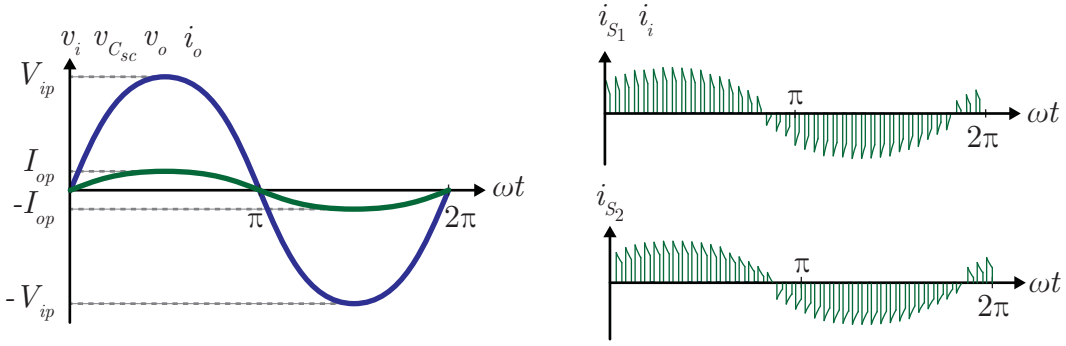
Figure 2.7 – Current waveforms during a switching period.



Source – Author.

observed that, ideally, the voltages over both capacitors are sinusoidal and equal to the input voltage. The currents over the switches present sinusoidal envelopes, which represent the need of four-quadrant switches. Another characteristic to note is that the input current leads the input voltage, resulting in a capacitive input power factor, a consequence of the reactive energy related to the capacitors.

Figure 2.8 – Theoretical waveforms for the unitary cell during a grid period.



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After the basic concepts of the converter operating stages, next section focuses on the analysis of charge flows during each operating stage.

2.2.1 Charge transfer and ideal voltage levels

Initially, an ideal analysis of the converter is performed in order to obtain a simplified mathematical representation of the structure. The following assumptions are made for this analysis:

- The conduction resistances r_1 and r_2 are negligible;

- The switching frequency f_s is much higher than the grid frequency f_g;
- The capacitances C_{sc} and C_o are large enough that the high frequency voltage ripples of $v_{C_{sc}}$ and v_{C_o} are small and can be neglected.

As the analysis takes into account both switching and grid frequencies, some definitions are necessary to avoid misunderstanding. The average value of a variable x during a switching period is defined as

$$x(\omega t) = \langle x \rangle = \frac{1}{T_s} \int_0^{T_s} x(t)dt, \tag{2.2}$$

in which the variable $\langle x \rangle$ is constant during a switching period, however variable during a grid period.

From the equivalent circuit for the first operating stage, depicted in Figure 2.6, it is observed that the voltage $v_{C_{sc}}$ is equal to the input voltage v_i, because the resistance r_1 is neglected. During the second operating stage, the output voltage v_o equals the voltage $v_{C_{sc}}$. Thus, for a sinusoidal steady state, the output voltage average value in a switching period is ideally given by

$$\langle v_o \rangle = \langle v_{C_{sc}} \rangle = \langle v_i \rangle = V_{ip} cos(\omega_g t). \tag{2.3}$$

This result shows that, ideally, the voltages over the capacitors are equal to the input voltage in the unitary switched-capacitor cell. Applying the capacitor current-voltage relation, the current average value in one capacitor during a switching period is obtained as:

$$\langle i_c \rangle = C \frac{dv_c(t)}{dt} = -\omega_g C V_{ip} sin(\omega_g t). \tag{2.4}$$

It should be observed that this current depends proportionally on the grid frequency, capacitance and voltage values. Moreover, it leads the voltage in one quarter of the grid period. As the averaged current of a capacitor during a switching period is not null, the net charge after one switching period is given by

$$q_c = \int_0^{T_s} i_c(t)dt = \langle i_c \rangle T_s = -\omega_g C V_{ip} T_s sin(\omega_g t). \tag{2.5}$$

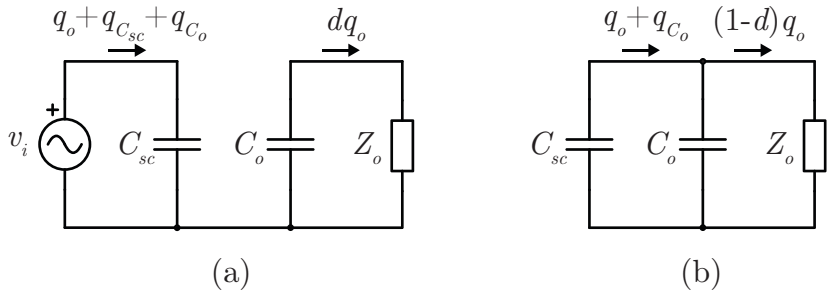
In a similar way, the total charge transferred to the output load is defined as

$$q_o = \int_0^{T_s} i_o(t)dt = \langle i_o \rangle T_s. \tag{2.6}$$

By analyzing both operation stages using the Kirchhoff's current law, it is possible to determine the charge variations in each capacitor during each stage, as illustrated in

Figure 2.9. It can be noticed that, differently from the analysis of DC-DC converters, the capacitor average charge during a switching period is not null. This analysis helps to determine in a simplified way the equation for capacitors currents during a switching period, which is the topic of the next section.

Figure 2.9 – Charge flow during the (a) first and (b) second operating stages.



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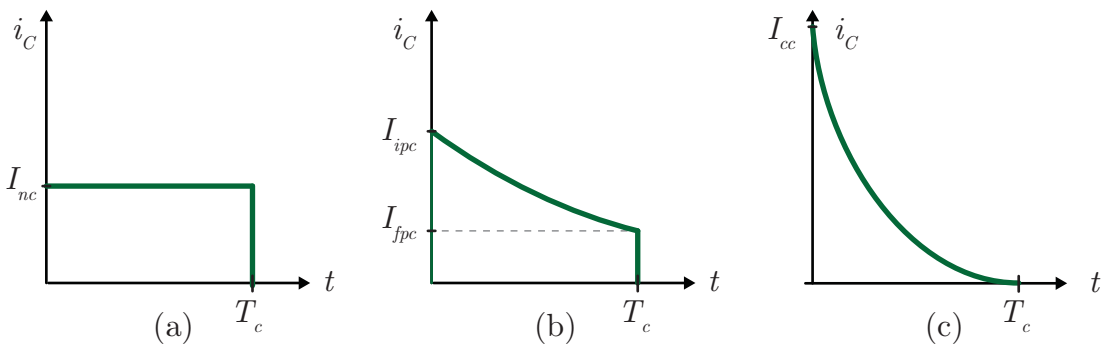
2.2.2 Currents analysis and charging modes

In switched capacitor converters, when two capacitors are connected in parallel via a switch, their voltages may be slightly different. Given the small voltage difference between capacitors and the small conduction resistance from the switch, the charging current may fluctuate significantly during an operation stage, which occurs in cases that the circuit time constants are smaller than the switching period. The charge of a capacitor is classified in three different modes, which are depicted in Figure 2.10(a) for no-charge (nc), Figure 2.10(b) for partial charge (pc) and Figure 2.10(c) for complete charge (cc) modes (BEN-YAAKOV, 2012). It is assumed that, in all modes, the charge that the capacitor receives is the same. The difference among these modes is the equivalent time constants of the charging circuits.

Figure 2.10 – Operating mode based on the currents waveforms. (a) No-charge; (b) Partial charge; (c) Complete charge.



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Independently of the operating mode, the total charge quantity should be the same. Thus, (2.7) must be always satisfied, where $i_c(t)$ is the charging current, q_{charge} the total charge variation and T_c the charging time.

$$\int_0^{T_c} i_c(t)dt = q_{charge} \tag{2.7}$$

Firstly the no-charge operating mode is considered, in which time constants RC from the charging circuit are sufficiently high that the current is approximately a constant during the charging time T_c and is written as $i(t) = I_{nc}$. From the waveform shown in Figure 2.10(a) and solving (2.7) yields

$$I_{nc} = \frac{q_{charge}}{T_c}. \tag{2.8}$$

On analyzing the first operating stage of the unitary cell (Figure 2.9(a)) and using (2.8), the current that flows through the capacitor C_{sc} during the first operation stage is given by

$$I_{C_{sc},nc1} = \frac{q_o + q_{C_{sc}} + q_{C_o}}{dT_s}, \tag{2.9}$$

that depends on the output current, grid frequency, capacitance and input voltage values. A similar analysis can be performed for the capacitor discharge. During the second operation stage, the current in the capacitor C_{sc} is

$$I_{C_{sc},nc2} = -\frac{q_o + q_{C_o}}{(1-d)T_s}. \tag{2.10}$$

These results show that the charging and discharging currents depend on the operating grid frequency. That means, for an DC input voltage, the variables q_{C_o} and $q_{C_{sc}}$ would vanish. As the current in the switched-capacitor is equal to the current in switches S_1 and S_2 during the first and second operating stages, respectively, all the currents can be obtained by a simple circuit analysis. The results are displayed in Table 2.1, whose values are valid for a switching period. Considering that the variables q_o, $q_{C_{sc}}$ and q_{C_o} are time-varying, an effective current value should be calculated for a grid period, following the equation

$$X_{ef} = \sqrt{\frac{1}{2\pi T_s}\int_0^{2\pi}\int_0^{T_s} x^2 dt d\theta}, \tag{2.11}$$

which defines the effective value of a generic variable x and $\theta = \omega_g t$ corresponds to the grid angle.

In general, high power switched-capacitor converters tend to operate in partial-charge mode, given that for no-charge mode it is necessary a high value of switching frequency or capacitances. Thus, a simplified analysis via differential equations is performed

Table 2.1 – Currents of the unitary cell in no-charge mode in a switching period.

	$0 < t < DT_s$	$DT_s < t < T_s$	Average value
$i_{S_1,nc}$	$\frac{q_o + q_{C_{sc}} + q_{C_o}}{DT_s}$	0	$\frac{q_o + q_{C_{sc}} + q_{C_o}}{T_s}$
$i_{S_2,nc}$	0	$\frac{q_o + q_{C_o}}{(1-D)T_s}$	$\frac{q_o + q_{C_o}}{T_s}$
$i_{C_{sc},nc}$	$\frac{q_o + q_{C_{sc}} + q_{C_o}}{DT_s}$	$-\frac{q_o + q_{C_o}}{(1-D)T_s}$	$\frac{q_{C_{sc}}}{T_s}$
$i_{C_o,nc}$	$-\frac{q_o}{T_s}$	$\frac{dq_o + q_{C_o}}{(1-d)T_s}$	$\frac{q_{C_o}}{T_s}$

Source – Author.

to calculate with more precision the effective current values. This methodology can be applied for any kind of operation, given that the no-charge and complete-charge modes are just special cases of the partial-charge mode. Thus, considering the partial charge mode and the Figure 2.6, the differential equations for the currents in the capacitors during the first operating stage are described by:

$$\begin{aligned} \frac{d}{dt} i_{C_{sc}} + \frac{i_{C_{sc}}}{r_1 C_{sc}} &= 0 \\ i_{C_o} &= -\langle i_o \rangle. \end{aligned} \tag{2.12}$$

The total charge flow in the capacitor C_{sc} during the interval DT_s is given in Figure 2.9(a) and employed as a boundary condition. Then, solving (2.12) yields in the current i_{S_1}, which is also the current $i_{C_{sc}}$ in the first operating stage:

$$i_{C_{sc},1}(t) = \frac{T_s e^{-\frac{t}{\tau_1}}}{\tau_1 \left(1 - e^{-\frac{DT_s}{\tau_1}}\right)} \left[\langle i_o \rangle - (C_{sc} + C_o) V_{ip} \omega_g sin(\omega_g t)\right]. \tag{2.13}$$

where τ_1 is the time constant in the first operating stage, defined as $\tau_1 = r_1 C_{sc}$. It is observed that the current in the switched capacitor during the first operating stage depends not only on the output current and duty cycle, but also on the grid frequency, capacitances, input voltage, switch resistance and switching frequency. For the second operating stage, the differential equations are described by

$$\begin{aligned} \frac{d}{dt} i_{C_{sc}} + i_{C_{sc}} \left(\frac{C_o + C_{sc}}{r_2 C_o C_{sc}}\right) &= -\frac{\langle i_o \rangle}{r_2 C_o} \\ \frac{d}{dt} i_{C_o} + i_{C_o} \left(\frac{C_o + C_{sc}}{r_2 C_o C_{sc}}\right) &= -\frac{\langle i_o \rangle}{r_2 C_{sc}}. \end{aligned} \tag{2.14}$$

Using the same idea of boundary condition as it was used for the first operating stage, (2.14) can be solved and leads to the current in the switch S_2, which is equal to the negative current through the capacitor C_{sc} during the second operating stage, given by

$$i_{C_{sc},2}(t) = -\frac{T_s}{\tau_2\left(1-e^{-\frac{(1-D)T_s}{\tau_2}}\right)}\left[\langle i_o\rangle\frac{C_o+DC_{sc}}{C_o+C_{sc}} - C_oV_{ip}\omega_g sin(\omega_g t)\right]e^{-\frac{t}{\tau_2}} - \frac{C_{sc}}{C_o+C_{sc}}\langle i_o\rangle, \tag{2.15}$$

where the time constant τ_2 is defined as $\tau_2 = r_2C_{sc}C_o/(C_{sc}+C_o)$. The current in capacitor C_o is obtained as

$$i_{C_o,2}(t) = \frac{T_s}{\tau_2\left(1-e^{-\frac{(1-D)T_s}{\tau_2}}\right)}\left[\langle i_o\rangle\frac{C_o+DC_{sc}}{C_o+C_{sc}} - C_oV_{ip}\omega_g sin(\omega_g t)\right]e^{-\frac{t}{\tau_2}} - \frac{C_o}{C_o+C_{sc}}\langle i_o\rangle. \tag{2.16}$$

Knowing the current in capacitors during each operating stage, the current in switches S_1 and S_2 can be determined. The obtained current equations depend on several parameters, such as: conduction resistances, capacitances, duty cycle, switching frequency, grid frequency and output current. A major advantage of this method is the simplicity compared to the solution of a system of differential equations and the accuracy if compared to the no-charge consideration.

A comparison of simulated results between the two presented methods is described in Table 2.2 for an unitary cell operating with $d = 0.45$ and an output current effective value equal to 5 A. These results show that, when the time constant is small comparing to the switching period (small values of $f_s\tau$), the consideration of no-charge mode leads to high accuracy error when computing the effective values of the currents. On the other hand, the analysis considering a partial-charge operation is accurate with the simulation results for all values of time constants.

A more accurate analysis could be performed, in which no simplifications would be made. However, it would result in two differential systems composed of two equations each, and the boundary conditions of one system depends on the other. This could be solvable for a two-order converter, however the solution would be difficult for higher order converters. In the presented analysis, the differential equations of one operating stage do not depend on the other stage, which has lead to an accurate and relatively easy approach to compute current stresses in switched capacitor converters.

The difference between the no-charge and partial charge is visible in the simulation results. Thus, it is quantified as an equivalent resistance factor k_r, which computes the

Table 2.2 – Comparison among methods for computing current stresses in an unitary switched-capacitor cell.

	Variable	Simulation (A)	PC-method (A)	Error (%)	NC-method (A)	Error (%)
$f_s\tau$=0.01	$I_{S_1,ef}$	36.66	37.25	1.61	7.853	78.58
	$I_{S_2,ef}$	26.81	26.70	0.41	6.834	74.51
	$I_{C_{sc},ef}$	45.42	45.83	0.90	10.41	77.08
	$I_{C_o,ef}$	26.34	26.23	0.42	4.659	82.31
$f_s\tau$=0.1	$I_{S_1,ef}$	11.87	11.91	0.31	7.853	33.86
	$I_{S_2,ef}$	9.643	9.554	0.92	6.834	29.13
	$I_{C_{sc},ef}$	15.30	15.27	0.2	10.41	31.96
	$I_{C_o,ef}$	8.213	8.141	0.88	4.659	43.27
$f_s\tau$=1	$I_{S_1,ef}$	7.978	7.919	0.74	7.853	1.57
	$I_{S_2,ef}$	6.952	6.880	1.04	6.834	1.70
	$I_{C_{sc},ef}$	10.58	10.49	0.85	10.41	1.61
	$I_{C_o,ef}$	4.763	4.726	0.78	4.659	2.18

Source – Author.

square of the ratio between no-charge and partial charge effective current values:

$$k_r = \left(\frac{I_{S,pc,ef}}{I_{S,nc,ef}}\right)^2. \tag{2.17}$$

The equivalent resistance factor computes how much the switch conduction losses are increased in the partial charge mode when compared to the no-charge mode. Calculating the resistance factor for the switch S_1 results, for any parameters, in

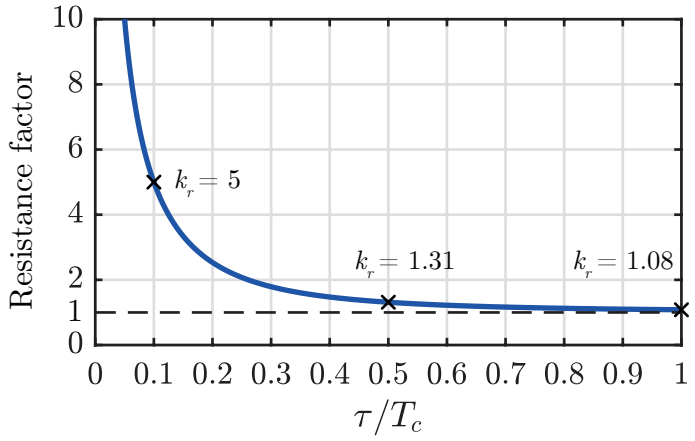
$$k_{r_1} = \frac{dT_s}{2\tau_1}\left(\frac{e^{\frac{dT_s}{\tau_1}}+1}{e^{\frac{dT_s}{\tau_1}}-1}\right), \tag{2.18}$$

where it can be seen that the factor depends on the switching period, duty cycle, and time constant. The complete analytical result for the factor regarding S_2 is more complex, because it also depends on the output current. However, a simplification can be made for partial charging mode and low output currents, and it is given by

$$k_{r_2} = \frac{(1-d)T_s}{2\tau_2}\left(\frac{e^{\frac{(1-d)T_s}{\tau_2}}+1}{e^{\frac{(1-d)T_s}{\tau_2}}-1}\right). \tag{2.19}$$

It should be noted that both equations are similar. Thus, Figure 2.11 shows the resistance factor as a function of the switching frequency and conducting time ($T_c = dT_s$ or $T_c = (1-d)T_s$) for a generic time constant τ. It is observed that values smaller than 0.1 lead to an increase in the effective resistance by 5 times. For an unitary ratio between time constant and conduction time, there is an increase of 8% in conduction losses.

Figure 2.11 – Resistance factor as function of time constant and conduction time.



Source – Author.

This increase of equivalent resistances is a design specification when sizing an AC-AC switched-capacitor converter, because it might lead to an efficiency drop. Thus, the best operating case would be with a high value of the product RCf_s, which could be achieved by: (i) increasing the conduction resistances, by adding an external resistance or choosing other semiconductors, which would lead to even more losses; (ii) employing higher capacitances, which would increase the reactive circulating current, that diminishes the input power factor and the efficiency; and (iii) increasing the switching frequency, that would lead to higher switching losses and has practical limitations. In case of DC-DC converters, the reactive power is not a restriction, thus this resistance factor is usually reduced by raising the capacitance values. In AC-AC applications, there is no perfect operating point. Thus, an optimization analysis must be performed to choose the switches, the capacitance values and the switching frequency.

2.2.3 Analysis via state equations

Obtaining the equations of the converter using the charge flow concept requires a more detailed analysis and verification of equivalent circuits. Moreover, it is complicated to obtain a converter average equivalent model. Thus, this section presents the analysis of a switched-capacitor unitary cell based on state equations, which allows to obtain the converter average circuit model. For this analysis, conduction resistances should be considered, because without a decoupling between two states $v_{C_{sc}}$ and v_o, the solution of the obtained circuit is more complex because of the interdependence of two state variables. Moreover, this analysis is accurate only if the converter time constants (τ_1 and τ_2) values are high compared to the switching period, because the no-charge operating mode is considered. For this study, the same conditions from the ideal analysis are assumed, except that in this case the conduction resistances are not neglected. This analysis considers as states the voltages over the capacitors $v_{C_{sc}}$ and v_{C_o}. Based on Figure 2.6, the differential

equations that represent the first operating stage are

$$\begin{aligned} C_{sc}\frac{dv_{C_{sc}}}{dt} &= \frac{v_i - v_{C_{sc}}}{r_1} \\ C_o\frac{dv_{C_o}}{dt} &= -i_o, \end{aligned} \tag{2.20}$$

and for the second operating stage,

$$\begin{aligned} C_{sc}\frac{dv_{C_{sc}}}{dt} &= \frac{v_{C_o} - v_{C_{sc}}}{r_2} \\ C_o\frac{dv_{C_o}}{dt} &= \frac{v_{C_{sc}} - v_{C_o}}{r_2} - i_o. \end{aligned} \tag{2.21}$$

Considering that the total time of the first operating stage is dT_s and the second operating stage is $(1-d)T_s$, the resulting average system within a switching period is obtained as

$$\begin{aligned} \left\langle C_{sc}\frac{dv_{C_{sc}}}{dt}\right\rangle &= \langle v_i\rangle\frac{d}{r_1} - \langle v_{C_{sc}}\rangle\left(\frac{d}{r_1}+\frac{1-d}{r_2}\right) + \langle v_{C_o}\rangle\frac{1-d}{r_2} \\ \left\langle C_o\frac{dv_o}{dt}\right\rangle &= \langle v_{C_{sc}}\rangle\frac{1-d}{r_2} - \langle v_o\rangle\frac{1-d}{r_2} - \langle i_o\rangle. \end{aligned} \tag{2.22}$$

When the converter operates in steady state, voltages and currents are time-varying in the grid frequency. Thus, it is not possible to assume that their derivatives are equal to zero. Thus, the concept of phasors is employed in order to solve the state equations. Then, the phasor of a generic variable x is defined as

$$x(t) \longleftrightarrow Re\{Xe^{j(\omega t+\phi)}\} = Re\{\boldsymbol{x}e^{j\omega t}\}, \tag{2.23}$$

where the variable $\boldsymbol{x}$ is the phasor of x and, in general, time-dependent both in magnitude as well as in phase (MAKSIMOVIC et al., 2001). The derivative average value of a dynamic phasor is written as

$$\left\langle \frac{d}{dt}\boldsymbol{x}\right\rangle = \frac{d}{dt}\langle\boldsymbol{x}\rangle + j\omega\langle\boldsymbol{x}\rangle. \tag{2.24}$$

Applying the phasor transform to (2.22) results in

$$\begin{aligned} C_{sc}\frac{d\langle\boldsymbol{v_{C_{sc}}}\rangle}{dt} &= -j\omega_g C_{sc}\langle\boldsymbol{v_{C_{sc}}}\rangle + \langle\boldsymbol{v_i}\rangle\frac{d}{r_1} - \langle\boldsymbol{v_{C_{sc}}}\rangle\left(\frac{d}{r_1}+\frac{1-d}{r_2}\right) + \langle\boldsymbol{v_o}\rangle\frac{1-d}{r_2} \\ C_o\frac{d\langle\boldsymbol{v_o}\rangle}{dt} &= -j\omega_g C_o\langle\boldsymbol{v_o}\rangle + \langle\boldsymbol{v_{C_{sc}}}\rangle\frac{1-d}{r_2} - \langle\boldsymbol{v_o}\rangle\frac{1-d}{r_2} - \langle\boldsymbol{i_o}\rangle. \end{aligned} \tag{2.25}$$

Now it is possible to obtain the steady state solution, given that in steady state the

phasors are constant. Thus, the left side of (2.25) is equal to zero and the system solution can be obtained. The complete result is quite large to be displayed, therefore only the dc solution is presented and given as

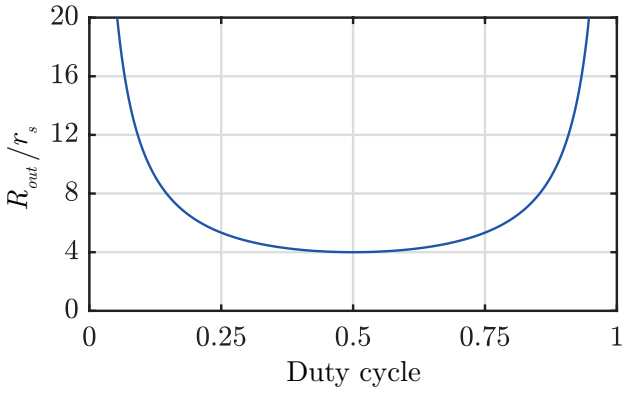
$$\boldsymbol{v_o} = \boldsymbol{v_i}\left(\frac{R_o}{R_o + \frac{r_1}{d} + \frac{r_2}{1-d}}\right), \tag{2.26}$$

where R_o is the load resistance. From this result, the converter series output resistance for DC-input is obtained, considering the operation in no-charge mode:

$$R_{out} = \frac{r_1}{d} + \frac{r_2}{1-d} = \frac{r_s}{d(1-d)}, \tag{2.27}$$

where the right side of the equation considers that the value of both conducting resistances are $r_1 = r_2 = r_s$. Figure 2.12 presents the equivalent output resistance for this case as function of duty cycle. The minimum point is located at $d = 0.5$ and corresponds to an equivalent resistance of $4r_s$. As conclusion, the converter operation with extreme values of duty cycle should be avoided, because the equivalent resistance is much higher in these operating points.

Figure 2.12 – Equivalent output series resistance as function of the duty cycle and switch resistances.

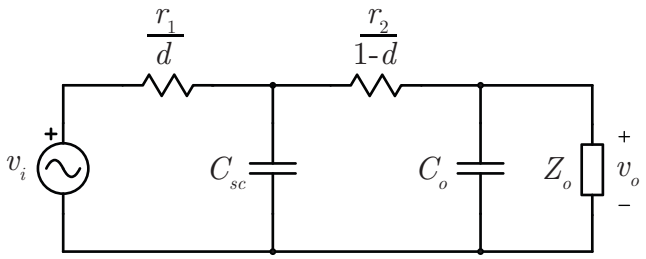


Source – Author.

By analyzing (2.25), the equivalent low frequency model shown in Figure 2.13 is obtained. The model is useful for simulations, given that the exponential characteristic of switched capacitor currents requires a small simulation step size. Furthermore, it simplifies the analysis for low-frequency parameters, such as the input and output voltages.

The equivalent model is not accurate enough when the time constants of the converter are low, because it considers the charging current as approximately constant during an operating stage. Thus, one alternative is to multiply the resistances r_1 and r_2 by their respective resistance factors, and the obtained averaged model is suitable for all charging modes. A comparison among the switched averaged models is presented in

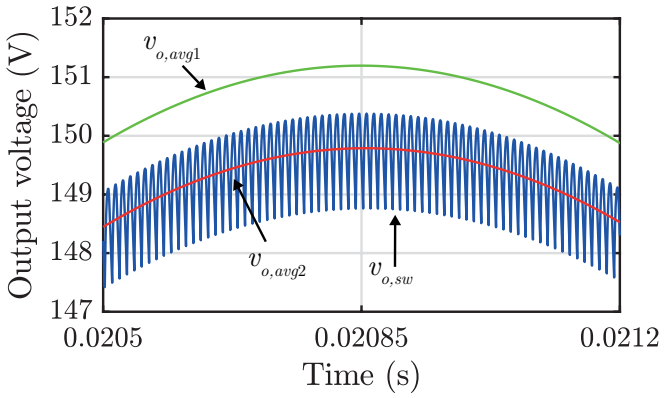
Figure 2.13 – Averaged circuit model for the unitary switched-capacitor cell.



Source – Author.

Figure 2.14 for a detail in the output voltage for a simulation of an unitary cell with time constants equal to 0.2. It should be noted that the averaged model without correction factor usually presents less voltage drop than the simulations or the corrected averaged model.

Figure 2.14 – Comparison among simulation results for the switching ($v_{o,sw}$), averaged ($v_{o,avg1}$) and (c) averaged with correction factor ($v_{o,avg2}$) models.



Source – Author.

From the obtained low frequency equivalent model, it is possible to determine the output characteristics of the converter, as shown in (2.28) for the output voltage as function of the input voltage and output current. The resistances r'_1 and r'_2 are equal to r_1/d and $r_2/(1-d)$, respectively.

$$\boldsymbol{v_o} = \frac{\boldsymbol{v_i} - \boldsymbol{i_o}\left(r'_1 + r'_2 + j r'_1 r'_2 \omega_g C_{sc}\right)}{1 - \omega_g^2 r'_1 r'_2 C_{sc} C_o + j\left(\omega_g r'_1 (C_{sc} + C_o) + r'_2 \omega_g C_o\right)} \tag{2.28}$$

By neglecting the parasitic resistances, it is obtained that the output voltage is equal to the input voltage. In this case, the average input current can be estimated as

$$\boldsymbol{i_i} = \boldsymbol{i_o} + j\omega_g\left(C_o + C_{sc}\right)\boldsymbol{v_o}, \tag{2.29}$$

which means that, even with an unitary voltage gain, the current gain is not equal to 1. It

also depends on the output voltage. Setting the angular grid frequency to null in (2.29) shows that the input and output current are equal in DC-DC conversion. Also, because of the capacitive nature of the converter, the input current will always lead the output current for any frequency. By considering an output current equal to $I_o\sqrt{2}cos(\omega_g t + \phi_o)$, the input power factor is

$$PF_i = \frac{I_o cos(\phi_o)}{\sqrt{I_o^2 + 2I_o V_i \omega_g (C_o + C_{sc}) sin(\phi_o) + (V_i \omega_g (C_o + C_{sc}))^2}}. \tag{2.30}$$

It is noted that the input power factor does not depend only on the output power factor, but also on the grid frequency, capacitance values, input voltage and output current.

The analysis of the unitary cell allowed to understand following points related to this topology, which are listed as:

- The best operating point regarding efficiency is at duty cycle equal to 0.5;
- Low time constants lead to higher current effective and peak values, which decrease the converter efficiency;
- Higher grid frequency, capacitances and output voltage result in increased input current and lower input power factor;
- The analysis must consider the partial-charge mode to obtain accurate results when the converter presents low time constants;
- Output voltage gain is fixed and approximately equal to 1, therefore it is not controllable.

2.3 LADDER CELL

The previous analysis of a basic unitary switching capacitor cell was important to understand some phenomena, such as the high peak charging current, the low frequency influence and the equivalent resistance. This section is focused on studying the ladder cell, depicted in Figure 2.15, which is also a switching capacitor cell. It consists of four switches S_1, S_2, S_3, S_4, a switched-capacitor C_{sc} and an output capacitor C_o.

During a switching period T_s, the converter operates in two different topological states, as shown in Figure 2.16. The operating stages are hereafter described for the positive half-cycle of the input voltage.

First operating stage: Switches S_1 and S_3 are turned-on, while switches S_2 and S_4 are turned-off. The capacitor C_{sc} is charged by the input voltage source. The load current is supplied by the output capacitor C_o and the input voltage source.

Figure 2.15 – Equivalent electric model of a switched-capacitor AC-AC ladder cell.

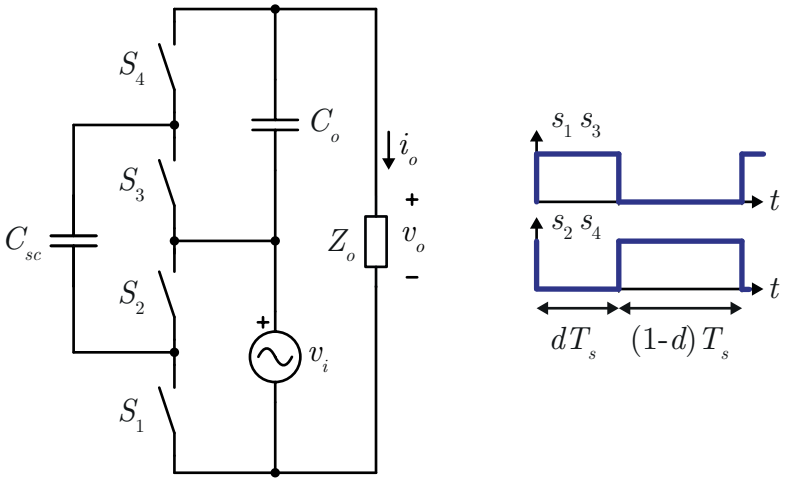


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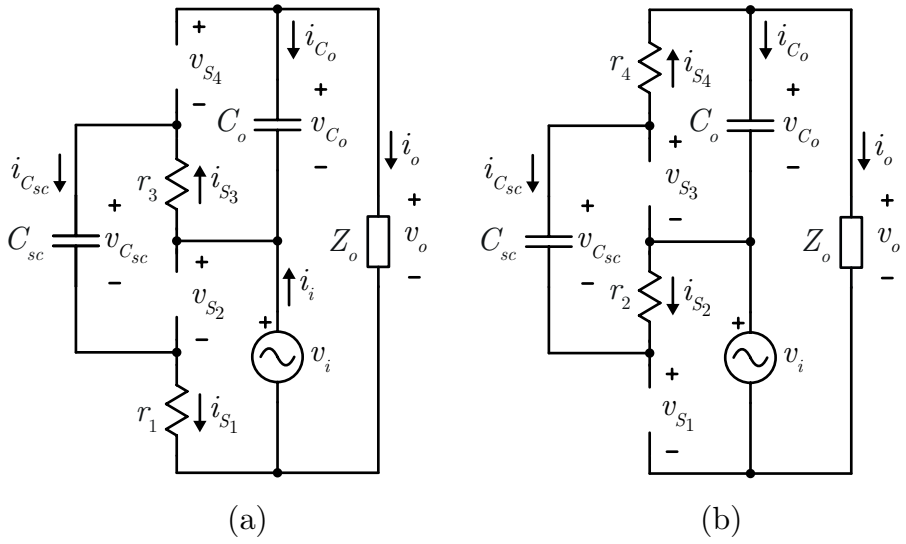
Figure 2.16 – (a) First and (b) second operating stages of the ladder cell.



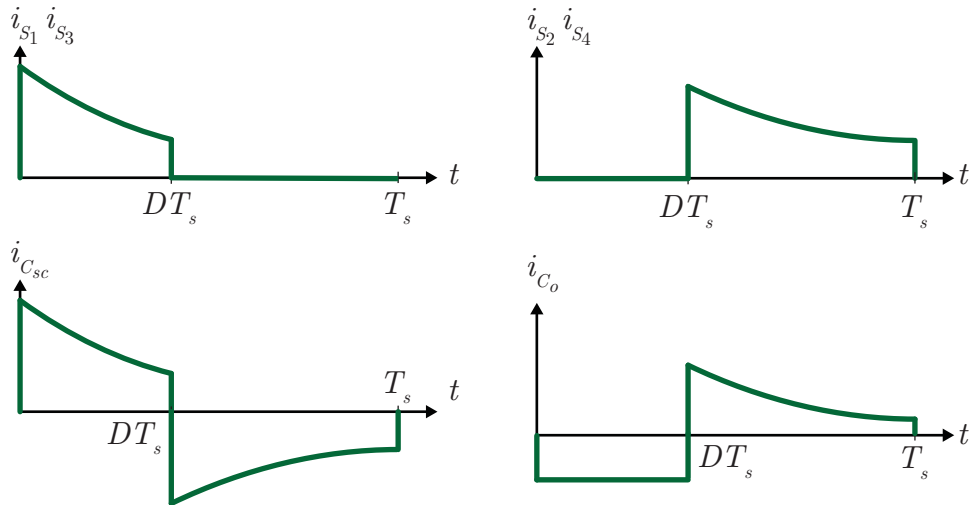
Source – Author.

Second operating stage: Switches S_2 and S_4 are turned-on, while S_3 and S_4 are turned-off. The capacitor C_{sc} provides energy to the output capacitor C_o. The load receives energy from the switched capacitor C_{sc} and the input voltage source.

The main current waveforms of the ladder cell during a switching period in the positive grid half-cycle are displayed in Figure 2.17. It is noticed that these waveforms are very similar to those of the unitary cell and are described with exponential equations.

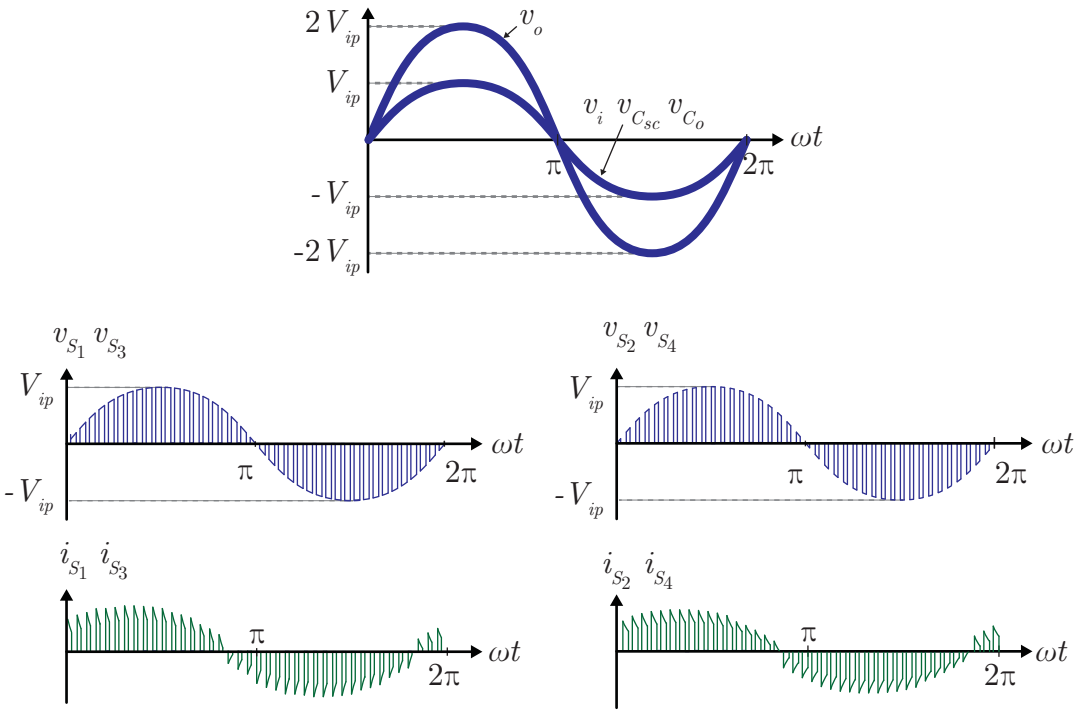
Graphics depicting the main waveforms during a grid period are displayed in Figure 2.18. It is observed that the voltage stresses over all the components are equal to the input voltage peak value. The output voltage is given as the double of the input voltage, therefore it is difficult to be controlled. The currents in switches also lead the voltage,

Figure 2.17 – Theoretical current waveforms for the ladder cell during a switching period.



Source – Author.

Figure 2.18 – Theoretical waveforms for the ladder cell during a grid period.



Source – Author.

indicating a capacitive input power factor.

From Figure 2.18 it should be noted that all switches conduct and block positive and negative currents and voltages, respectively. Therefore, for this topology it is also necessary to employ four-quadrant switches.

2.3.1 Ideal analysis

A similar analysis from the unitary cell is performed for the ladder cell, highlighting the similarities and differences between the converters. The considerations made for the ideal analysis are:

- Switches conduction resistances are neglected;
- Voltage ripples over the capacitors are null during a switching period.

From Figure 2.16, it is noted that the switched capacitor C_{sc} is connected in parallel with the input voltage source v_i during the first operating stage, sharing the same voltage. In the second operating stage, the output capacitor C_o is connected in parallel with the switched capacitor C_{sc}, also sharing the same voltage. As there is the consideration of low voltage ripples, the average voltage values over the capacitors are equal to

$$\langle v_{C_o} \rangle = \langle v_{C_{sc}} \rangle = \langle v_i \rangle = V_{ip} cos(\omega_g t), \tag{2.31}$$

which means that the capacitors rated voltage should be greater than the input voltage peak value. As the output voltage is equal to the sum of the input voltage v_i and v_{C_o}, the following relation is obtained:

$$\langle v_o \rangle = \langle v_{C_o} \rangle + \langle v_i \rangle = 2\langle v_i \rangle. \tag{2.32}$$

Thus, the ideal static voltage gain for the ladder cell, which corresponds to the ratio between input and output voltage, is ideally given by

$$G = \frac{\langle v_o \rangle}{\langle v_i \rangle} = 2. \tag{2.33}$$

It is observed that, ideally, the voltage gain is not a function of the duty cycle. Thus, the control of output voltage is not possible by duty cycle variations. Furthermore, from the operating stages analysis it should be noted that the peak voltage over the switches are equal to the input voltage peak value.

2.3.2 Low-frequency equivalent model

The equivalent low-frequency model helps the analysis and simulation of the converter when there is interest only in the low-frequency parameters, such as the input and output voltages and currents. Based on Figure 2.16, the state equations for the first

operating stage are written as

$$\begin{aligned} C_{sc}\frac{d}{dt}v_{C_{sc}} &= \frac{v_i - v_{C_{sc}}}{r_1 + r_3} \\ C_o\frac{d}{dt}v_{C_o} &= -\langle i_o \rangle, \end{aligned} \tag{2.34}$$

and, comparing to the unitary cell equations, the only difference is that there is a sum of resistances $r_1 + r_3$ instead of only r_1. For the second operating stage, the state equations are:

$$\begin{aligned} C_{sc}\frac{d}{dt}v_{C_{sc}} &= \frac{v_{C_o} - v_{C_{sc}}}{r_2 + r_4} \\ C_o\frac{d}{dt}v_{C_o} &= \frac{v_{C_{sc}} - v_{C_o}}{r_2 + r_4} - \langle i_o \rangle. \end{aligned} \tag{2.35}$$

Once more, the only difference between ladder and unitary cell is at the resistances, which are $r_2 + r_4$ instead of r_2. Moreover, the charge analysis for the capacitors is exactly the same as the unitary cell. Therefore all obtained results of the currents in the unitary cell can be applied for the ladder cell, only substituting the conducting resistance r_1 for $r_1 + r_3$ and r_2 for $r_2 + r_4$.

Following the analysis, after determining the state equations for both operating stage, the averaged operator for both operating stages can be applied and the equations result in

$$\begin{aligned} \left\langle C_{sc}\frac{d}{dt}v_{C_{sc}} \right\rangle &= d\frac{v_i - v_{C_{sc}}}{r_1 + r_3} + (1-d)\frac{v_{C_o} - v_{C_{sc}}}{r_2 + r_4} \\ \left\langle C_o\frac{d}{dt}v_{C_o} \right\rangle &= (1-d)\frac{v_{C_{sc}} - v_{C_o}}{r_2 + r_4} - \langle i_o \rangle. \end{aligned} \tag{2.36}$$

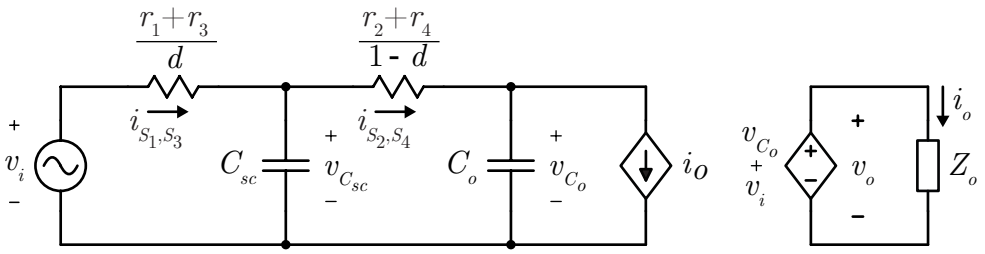
Writting the system of equations with phasor variables, (2.36) results in

$$\begin{aligned} C_{sc}\frac{d}{dt}\langle \boldsymbol{v_{C_{sc}}} \rangle &= -j\omega_g C_{sc}\langle \boldsymbol{v_{C_{sc}}} \rangle + d\frac{\langle \boldsymbol{v_i} \rangle - \langle \boldsymbol{v_{C_{sc}}} \rangle}{r_1 + r_3} + (1-d)\frac{\langle \boldsymbol{v_{C_o}} \rangle - \langle \boldsymbol{v_{C_{sc}}} \rangle}{r_2 + r_4} \\ C_o\frac{d}{dt}\langle \boldsymbol{v_{C_o}} \rangle &= -j\omega_g C_o\langle \boldsymbol{v_{C_o}} \rangle + (1-d)\frac{\langle \boldsymbol{v_{C_{sc}}} \rangle - \langle \boldsymbol{v_{C_o}} \rangle}{r_2 + r_4} - \langle \boldsymbol{i_o} \rangle. \end{aligned} \tag{2.37}$$

From (2.37) and knowing that $v_o = v_i + v_{C_o}$ the equivalent converter, shown in Figure 2.19, is obtained. It should be noted that it is also very similar to the ladder cell, despite the doubled output voltage gain.

Comparing the equivalent circuits from the ladder and the unitary cell, it can be concluded that they are analogous, with the odd and even switches from ladder cell corresponding to the switches S_1 and S_2 from the unitary cell, respectively. The only difference on the equivalent low-frequency circuit is the output voltage, which is the sum of

Figure 2.19 – Low-frequency equivalent circuit for the Ladder cell.



Source – Author.

the output capacitor voltage v_{C_o} and the input voltage v_i. That said, all the low-frequencies characteristics, besides the output voltage, are equal for both converter, only substituting r_1 for $r_1 + r_3$ and r_2 for $r_2 + r_4$ when the Ladder cell is considered. This similarity is also applied to the analysis of the currents via differential equations. For a same output current for both converters and same time constants, the currents stresses are equal. Thus, the conclusions obtained for the unitary cell are also applied to the ladder cell.

2.4 CONCLUSIONS

This chapter presented a brief review of switched capacitor converters. The AC-AC unitary cell was analyzed via two methods: the first considered the converter ideal to determine the voltage over the capacitors, while the effective values of the currents were computed through the analysis of charge flow during each operating stage. The second method is applied by determining and solving the state equations, which allows to calculate the voltage levels considering the non-idealities of the switches (such as the conduction resistances). This method is useful to obtain the average circuit model.

A comparison among the switched-capacitor charging modes was performed. It was observed that the "no-charge" mode leads to the minimum equivalent resistance and, as consequence, higher efficiency. The equivalent resistance was also quantified for partial-charge operating mode.

Finally, the ladder cell was analyzed and a comparison with the unitary cell was performed. It is concluded that both operate similarly, being the biggest difference the fact that the output voltage of the ladder cell is the double from the unitary cell. Furthermore, the output voltage control is hardly achieved for both structures, given the fact that, ideally, the output voltage does not depend on the duty cycle.

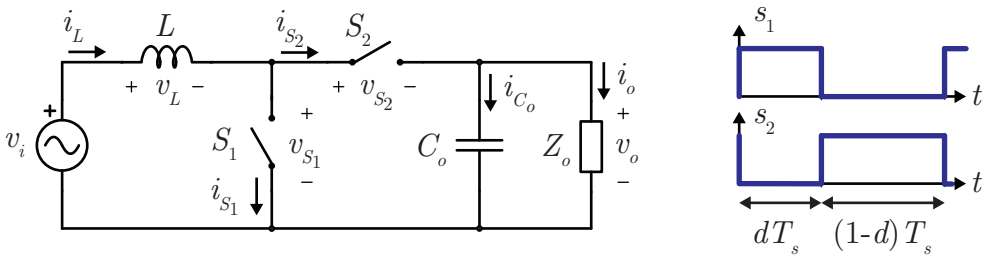
3 INDUCTIVE SWITCHING AC-AC CONVERTERS

AC-AC converters which are derived from DC-DC topologies are known in the literature as "AC-AC Choppers". They are considered as an special case of matrix converters (KOLAR et al., 2011). The operating principle of these structures are simpler than the conventional matrix converters, moreover, they operate with a constant duty cycle. Whereas the output voltage can be controlled, these topologies are not able to change the main frequency. These converters can be used as solid state autotransformers, serial voltage regulator or controllable reactance (FEDYCZAK; STRZELECKI; BENYSEK, 2002). In addition, they can be used in three-phase systems (SRINIVASAN; VENKATARAMANAN, 1995) (ROSAS-CARO et al., 2010). This chapter focuses on studying a basic inductive switching cell (boost) operating as an AC-AC converter. The main equations are obtained and the modulation schema is explained.

3.1 SINGLE-PHASE AC-AC BOOST CONVERTER

An ideal equivalent circuit of an AC-AC single-phase boost converter is represented in Figure 3.1. It consists of an input inductor L, an output capacitor C_o and two four-quadrant switches S_1 and S_2 (Figure 2.5) . The drive signals for both switches are complementary to each other.

Figure 3.1 – Equivalent switched model of an AC-AC boost converter.



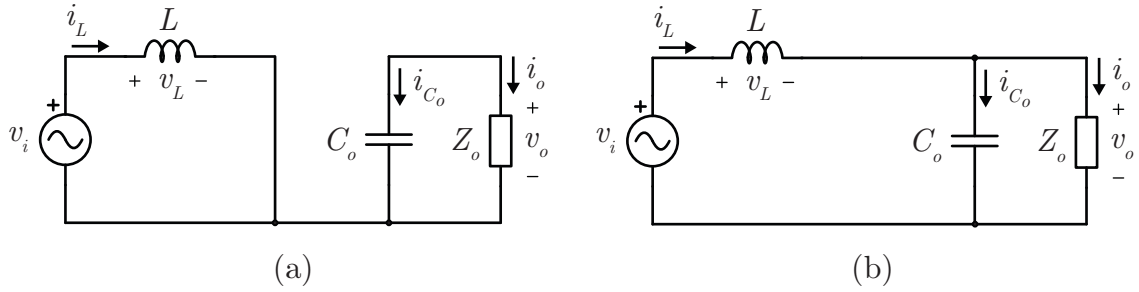
Source – Author.

Considering the modulation signals, the converter operates in two different topological stages, which are depicted in Figure 3.2 and hereafter described.

First operating stage: The switch S_1 is turned-on while S_2 is turned-off. The current i_L increases and the inductor stores energy. The output capacitor C_o supplies the load current.

Second operating stage: The switch S_2 is turned-on while S_1 is turned-off. The inductor L and the input source provide energy to the output capacitor C_o and to the load Z_o.

Figure 3.2 – Topological stages of AC-AC boost converter. (a) First stage ($0 < t < DT_s$). (b) Second stage ($DT_s < t < T_s$).



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The main waveforms within a switching period during the grid positive half-cycle are shown in Figure 3.3. In a boost converter, the voltage stresses over the switches are equal to the output voltage peak value. Furthermore, the currents through the switches are approximately constants during an operation stage, which differs from the switched-capacitor ladder converter, as seen in 2.3.

Figure 3.3 – Main waveforms of a boost converter during a switching period.

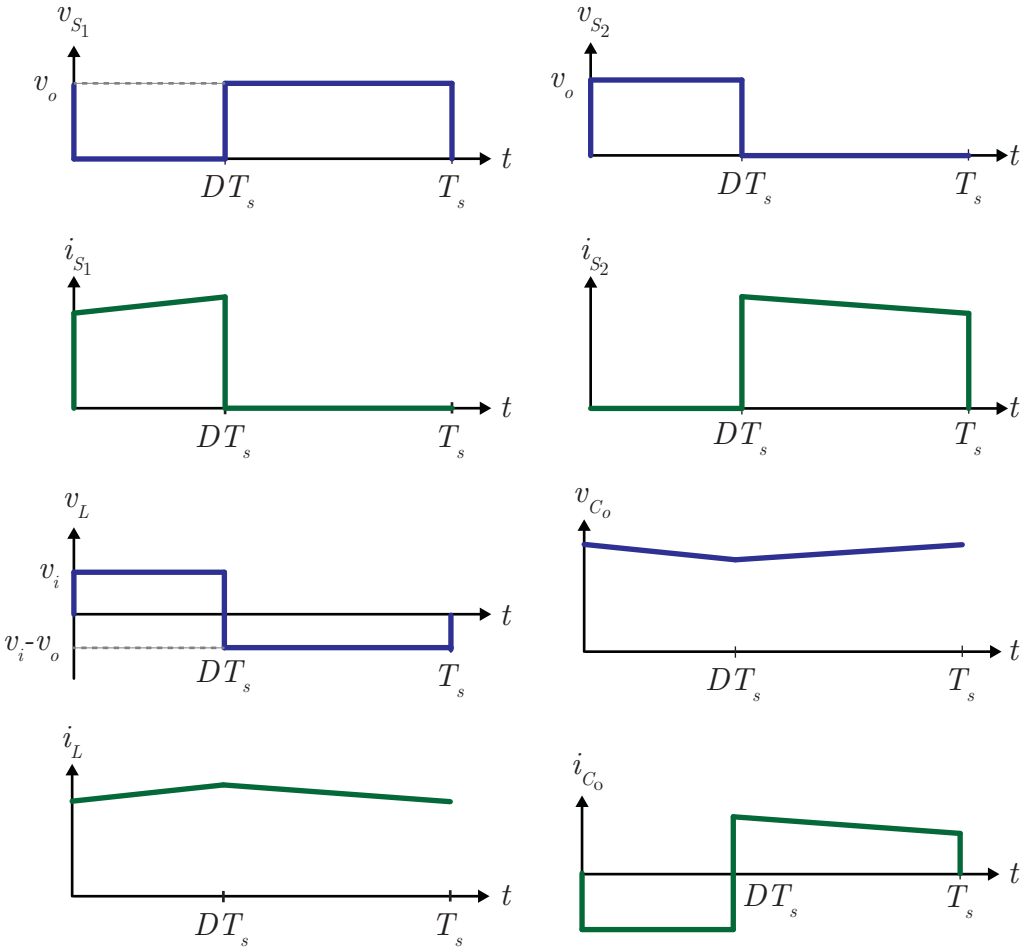

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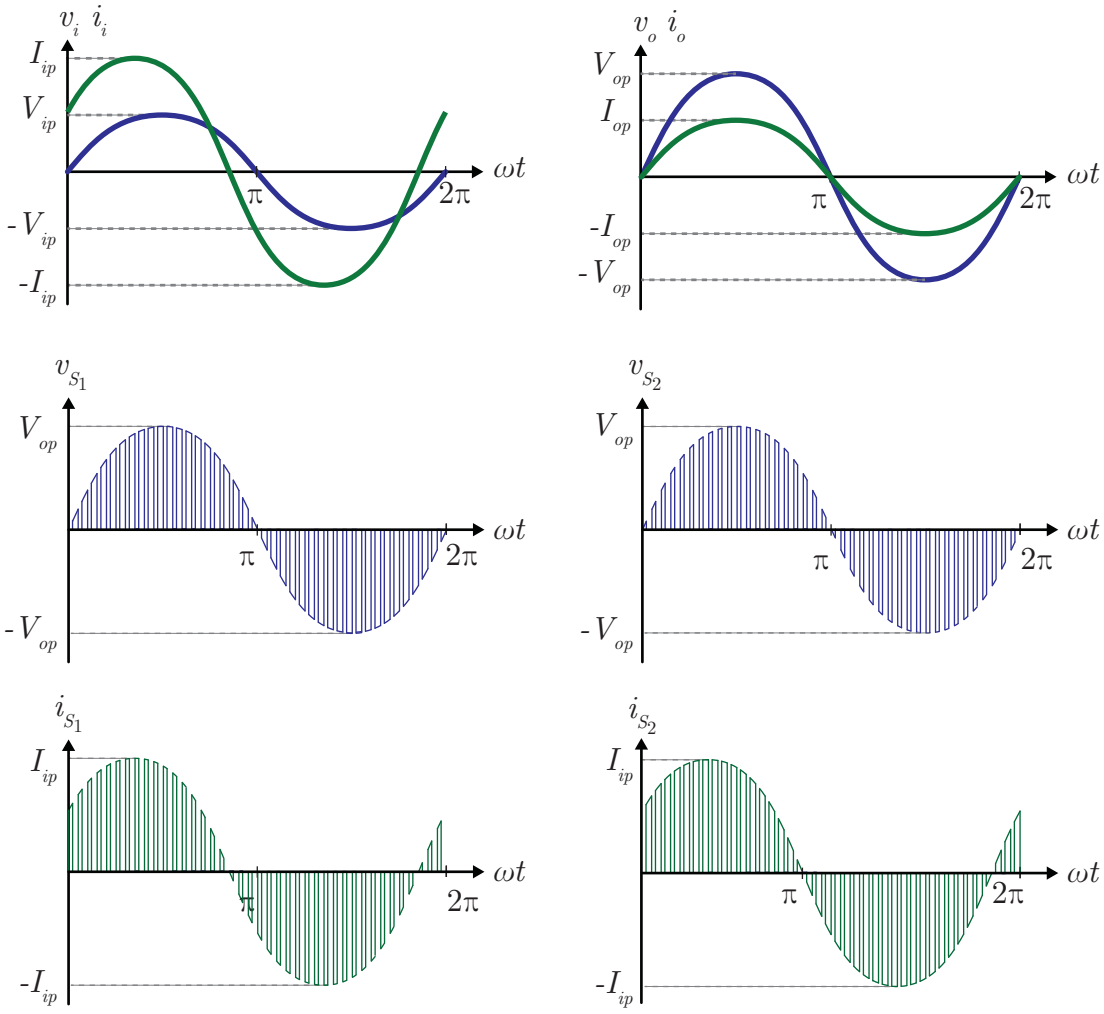
Figure 3.4 shows the main waveforms during a grid period for a resistive load. It is observed that the output voltage is higher than the input voltage and in phase. One interesting factor is regarding the input current, which leads the voltage, characterizing a capacitive input power factor, that occurs because of the reactive power related to the output capacitor. The voltages over the switches S_1 and S_2 present sinusoidal envelopes with maximum values equal to the output voltage peak value. Similarly, the currents envelopes in switches are equal to the inductor current. It should be noted that switches have to block and conduct voltages and currents with both polarities, which shows the necessity of four-quadrant switches for this topology.

Figure 3.4 – Main waveforms of an AC-AC boost converter during a grid period.



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After an inital qualitative analysis of the converter, the equations for the steady-state operation are obtained. From Figure 3.2, the equations that describe the equivalent

circuit in the first operating stage are:

$$\begin{aligned} v_L &= L\frac{di_L}{dt} = v_i \\ i_{Co} &= C_o\frac{dv_{Co}}{dt} = -i_o, \end{aligned} \tag{3.1}$$

and, for the second operating stage, they are given by:

$$\begin{aligned} v_L &= L\frac{di_L}{dt} = v_i - v_{Co} \\ i_{Co} &= C_o\frac{dv_{Co}}{dt} = i_L - i_o. \end{aligned} \tag{3.2}$$

The average equations for a switching period can be written as:

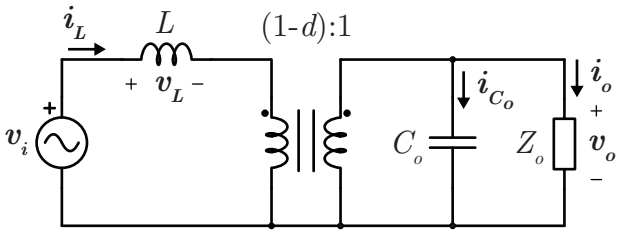
$$\begin{aligned} \langle v_L \rangle &= \left\langle L\frac{d}{dt}i_L \right\rangle = \langle v_i \rangle - (1-d)\langle v_{Co} \rangle \\ \langle i_{Co} \rangle &= \left\langle C_o\frac{d}{dt}v_{C_o} \right\rangle = (1-d)\langle i_L \rangle - \langle i_o \rangle . \end{aligned} \tag{3.3}$$

Considering that the variables are phasors, (3.3) is given by

$$\begin{aligned} L\frac{d}{dt}\langle \boldsymbol{i_L} \rangle &= -j\omega_g L\langle \boldsymbol{i_L} \rangle + \langle \boldsymbol{v_i} \rangle - (1-d)\langle \boldsymbol{v_{Co}} \rangle \\ C_o\frac{d}{dt}\langle \boldsymbol{v_{C_o}} \rangle &= -j\omega_g C\langle \boldsymbol{v_{C_o}} \rangle (1-d)\langle \boldsymbol{i_L} \rangle - \langle \boldsymbol{i_o} \rangle . \end{aligned} \tag{3.4}$$

An equivalent average circuit is obtained from (3.4) and depicted in Figure 3.5. It reminds of the equivalent circuit of an transformer, and allows performing theoretical analysis and simulations when only input and output characteristics are considered. In addition, control methods can be tested using this model, given that the pass bands of control meshes are usually lower than the switching frequency.

Figure 3.5 – Equivalent average circuit of an AC-AC boost converter.



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In steady state, the derivative of the phasors $\langle \boldsymbol{i_L} \rangle$ and $\langle \boldsymbol{v_{C_o}} \rangle$ are equal to zero. Thus, the left side of (3.4) vanishes and the solution of this system of equations leads to

an expression for the output voltage as function of the input voltage and output current:

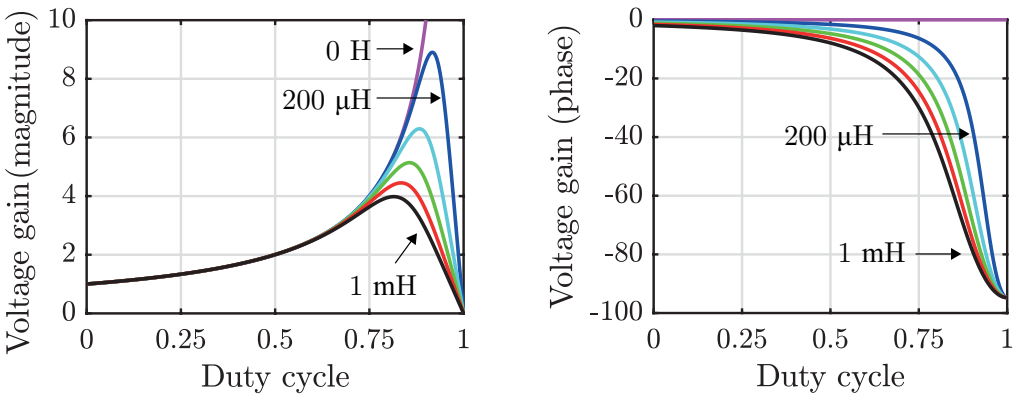
$$\boldsymbol{v_o} = \frac{1}{\left(1 - \frac{w_g^2 LC_o}{(1-d)^2}\right)} \left(\frac{\boldsymbol{v_i}}{(1-d)} - j\frac{\omega_g L}{(1-d)^2}\boldsymbol{i_o} \right). \tag{3.5}$$

If the load is linear and described by $Z_o = R_o + jX_o$, then the output voltage is given by

$$\boldsymbol{v_o} = \frac{\frac{\boldsymbol{v_i}}{1-d}}{\left(1 - \frac{w_g^2 LC_o}{(1-d)^2} + \frac{\omega_g L X_o}{(1-d)^2|Z_o|^2} + j\frac{\omega_g L R_o}{(1-d)^2|Z_o|^2}\right)}. \tag{3.6}$$

The voltage gain, defined as $\boldsymbol{g_v} = \boldsymbol{v_o}/\boldsymbol{v_i}$ is shown in Figure 3.6 as a function of the duty cycle for different input inductances $L = 0, 200, ..., 1000\ \mu$H. It is observed that an increment in the inductance results in a reduced voltage gain for duty cycles higher than 0.75. Furthermore, the phase-shift between input and output voltages becomes significant for duty cycles above 0.5 and is increased for higher inductance values.

Figure 3.6 – Voltage gain as a function of duty cycle for different input inductances.



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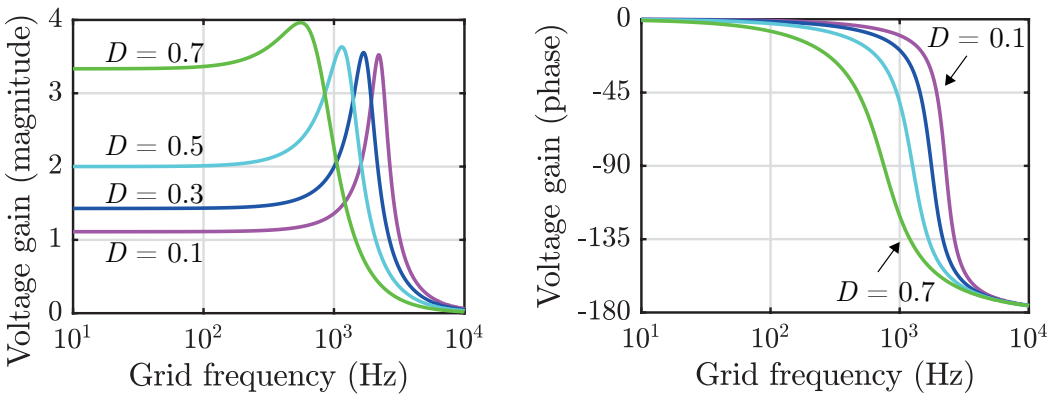
A comparison of the voltage gain based on the grid frequency is depicted in Figure 3.7. When operating with frequencies below 100 Hz, the voltage gain is approximately the same as a DC-DC converter. However, it is observed a resonant frequency, which decreases for higher duty cycles. Also, after the resonant frequency, the output phase is 180 degrees shifted from the input voltage and the voltage gain magnitude tends to zero.

Differently from a DC-DC boost converter, when operating with an AC input, the inductor and capacitor also influence on the voltage gain. Moreover, from (3.5) it is observed that the denominator may be zero for a certain parametric combination. This leads to a resonant frequency, given by

$$f_{ress} = \frac{1-d}{2\pi\sqrt{LC_o}}. \tag{3.7}$$

Figure 3.7 – Voltage gain for different grid frequencies and duty cycles.



Source – Author.

The existence of a resonant frequency also restricts the converter operation, in which the passive elements L and C_o must be chosen so that the resonant frequency is sufficiently higher than the grid frequency, so that it does not modify the converter performance. Now, focusing on the input variables, the obtained input current is calculated as

$$\boldsymbol{i_L} = \frac{1}{\left(1 - \frac{w_g^2 L C_o}{(1-d)^2}\right)} \left(\frac{\boldsymbol{i_o}}{(1-d)} + j \frac{\omega_g C_o}{(1-d)^2} \boldsymbol{v_i} \right), \tag{3.8}$$

and, for a linear load, it is computed as:

$$\boldsymbol{i_L} = \boldsymbol{v_i} \frac{R_o + j(\omega_g C_o Z_o^2 - X_o)}{(1-d)^2 Z_o^2 - \omega^2 L C_o Z_o^2 + \omega_g L X_o + j\omega_g L R_o}. \tag{3.9}$$

The next graphic, shown in Figure 3.8, plots the input admittance as a function of the grid frequency and output capacitance, given a constant output resistance load. It is observed that the input admittance increases with the output capacitance. That means, for the same load, the input current increases. This corresponds to a higher circulating reactive current, that results in a lower input power factor. Moreover, the reactive power reduces significantly the efficiency, specially for high grid frequencies.

The admittance as a function of the output resistance is shown in Figure 3.9. It can be seen that, for light loads (high value resistances), the input admittance remains constant. This value is proportional to the output capacitance. It means that, even for a light load (or even no load), there will be a minimum circulating reactive current in the converter. The phase graphic shows the phase shift between input current and voltage. For light loads, the angle tends to increase until 90 degrees. For heavy loads (low resistances), the phase shift becomes negative, meaning that the reactive power associated to the input inductance becomes more significant than the capacitive reactive power.

Figure 3.8 – Input admittance for different grid frequencies and output capacitances.

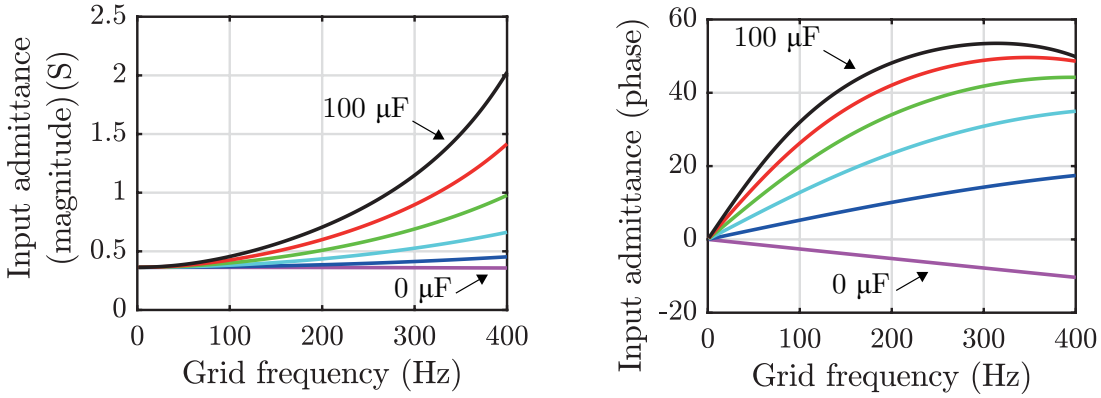


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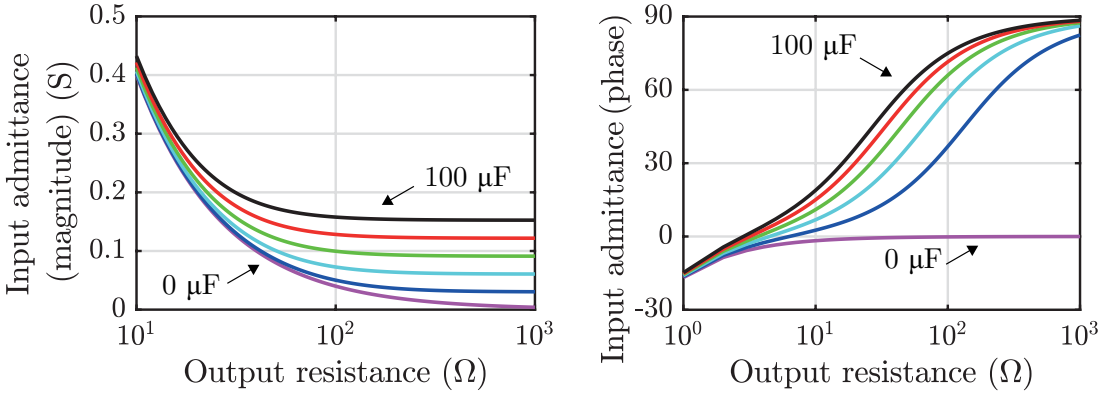
Figure 3.9 – Input admittance as function of output resistance and output capacitance.



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Regarding the input reactive power, it is computed by

$$Q_i = Q_o + I_L^2 \omega_g L - V_o^2 \omega_g C_o. \tag{3.10}$$

Thus, neglecting the power losses, the input power factor is determined by (3.11). It shows that, for a constant output voltage and a resistive load, the power factor only approaches the unity when the output power is much higher than the reactive power.

$$PF_i = \frac{P_o}{\sqrt{P_o^2 + (Q_o + I_L^2 \omega_g L - V_o^2 \omega_g C_o)^2}} \tag{3.11}$$

After the analysis of the ideal AC-AC boost converter, it is concluded that:

- The topology can operate as an AC-AC converter by employing four-quadrant switches as S_1 and S_2;
- In sinusoidal steady state, the duty cycle is constant;

- An average circuit model can be obtained and used when only the input/output characteristics are analyzed;
- At grid frequency (60 Hz), the inductance values almost do not affect the voltage gain for duty cycles lower than 0.75, whereas the phase is slightly changed;
- The maximum voltage gain of the ideal AC-AC boost converter is limited by the input inductance, which does not affect in the DC-DC converter;
- The main frequency should be below the resonant frequency, which depends on the inductance, capacitance and duty cycle values;
- Higher capacitance values decrease the input power factor and increase the input reactive current;
- Operation in higher main frequencies require lower output capacitance values.

3.2 COMMUTATION ANALYSIS

The topologies derived directly from DC-DC converters usually suffer from commutation problem, which will be explained in this section. Thus, the focus of many researches is to improve the commutation. For example, in (SHARIFI; JAHANI; MONFARED, 2018) a converter with buck-boost characteristic is proposed, where an impedance network is employed in order to avoid the use of snubber circuits. A similar idea is applied in (HE; NAI; ZHANG, 2018), where a trans-Z-source converter is presented and it operates either as in-phase boost or out-of-phase buck-boost converter. In (ZHANG; RUAN; MEMBER, 2014), an AC-AC buck-boost converter is cascaded with a third-harmonic trap in order to control both the amplitude and the phase of the output voltage.

Initially, the commutation of a DC-DC converter is studied. Figure 3.10 shows the current's path during a switching period, considering the dead time T_D. During the first operating stage (Figure 3.10(a)), S_1 conducts the current. When the transition occurs and none of the switches is turned on (Figure 3.10(b)), the body diode of S_2 is directly biased and conducts. After that, S_2 is turned on an the current flows through both channel and body diode of S_2 (Figure 3.10(c)). When dead time occurs again, only the body diode of S_2 conducts again (Figure 3.10(d)). If the input current was negative, a similar behavior would occur. In this case, the body diode of switch S_1 would conduct instead of S_2. Given that the switches do not receive positive gate signal simultaneously, there is always one diode preventing a short-circuit in the output voltage source.

Considering the same DC-DC converter, but employing two anti-series connected MOSFETs as switches S_1 and S_2, the resultant switching path of the current is shown in Figure 3.11. During the first operating stage, the current flows through the channel of S_{1b} and is divided between the channel and body diode of S_{1a}. The body diode of S_{2b} prevents a short-circuit. During the transition between stages, none of the switches is turned-on. Thus, the current I_L has no available path, given that in this case the body diodes are

Figure 3.10 – Current path in each operation stage for single MOSFETs used as switches S_1 and S_2.

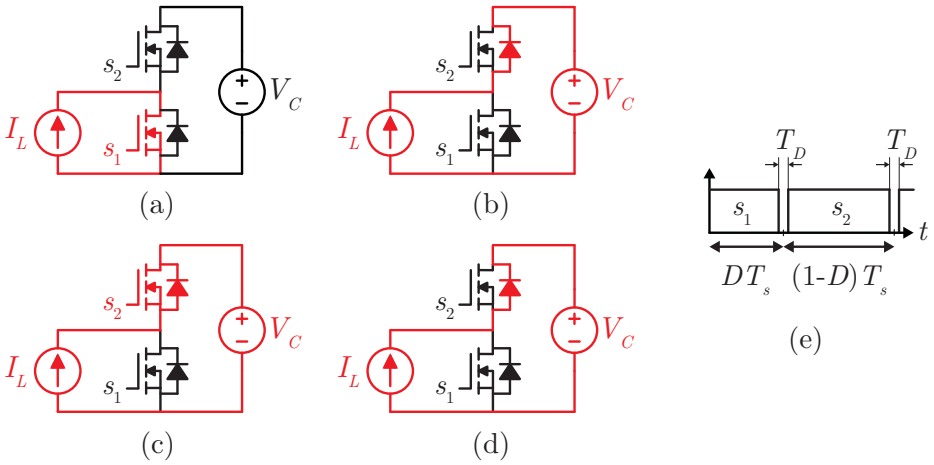

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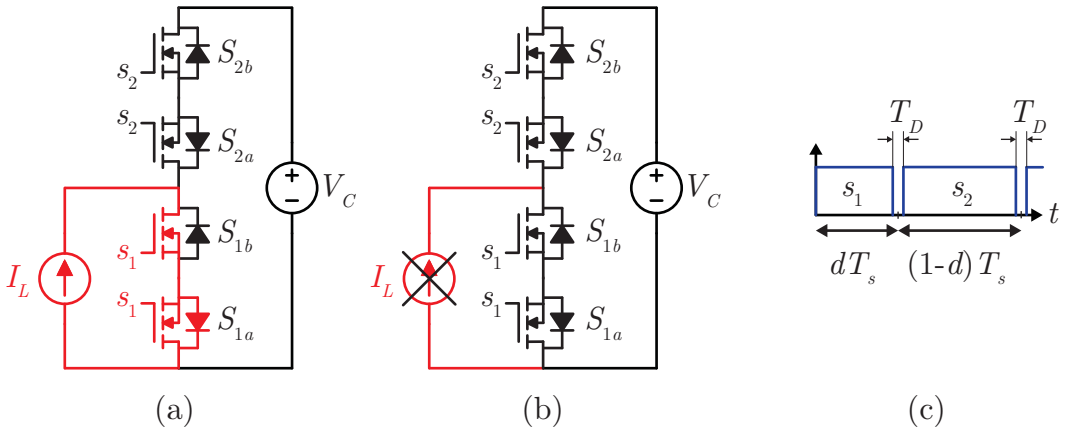
Figure 3.11 – Current path in each operation stage for anti-series connected MOSFETs used as switches.



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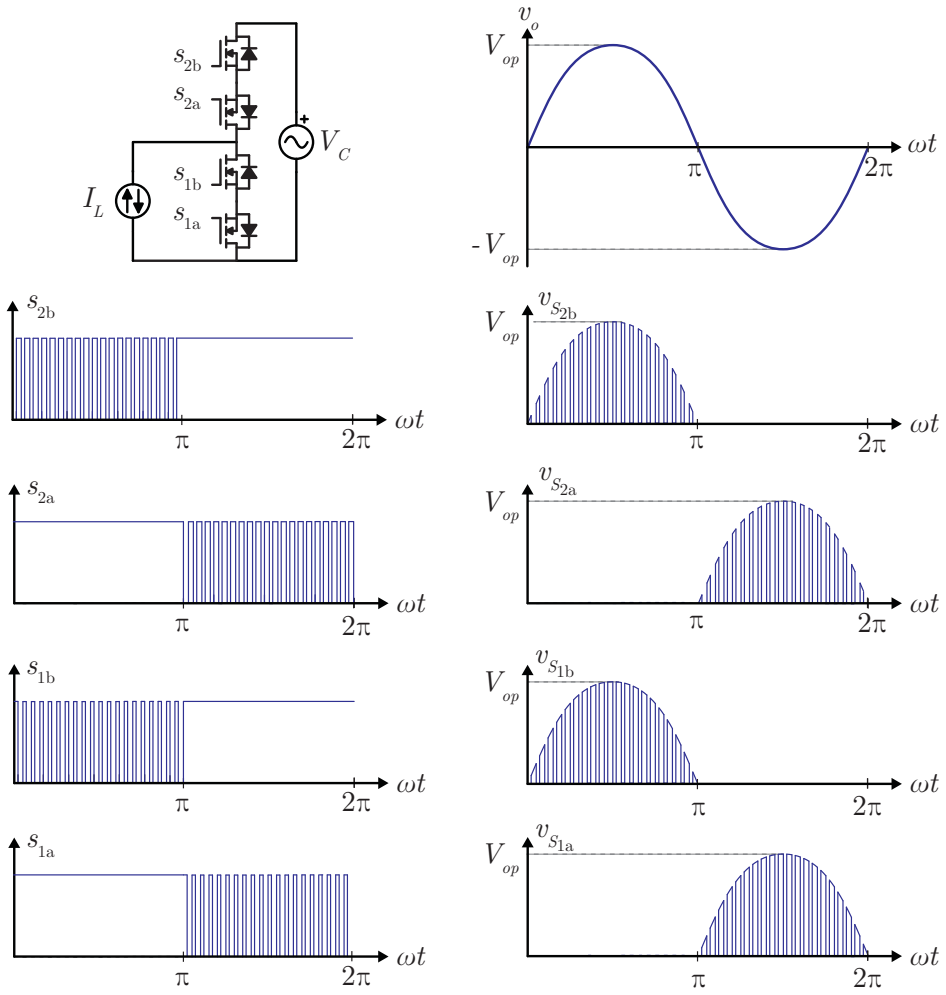
connected in anti-series and prevent the current flow. Consequently, there would be a high voltage spike over the inductor, which could damage some devices. In conclusion, this modulation schema is not suitable for this structure. One alternative for the modulation schema is presented in Figure 3.12 (PETRY; FAGUNDES; BARBI, 2006).

In this case, each of the four switches receives a different gate signal, and it is necessary the output voltage measurement. When the output voltage is positive, the lower switches S_{1a} and S_{2a} receive always a high gate signal, while PWM signals are applied to switches S_{1b} and S_{2b}. In other words, S_{1a} and S_{2a} are turned-on during all positive grid half-cycle. The opposite occurs during the negative half cycle of the output voltage. Then, during each half cycle the converter operates as a bidirectional DC-DC converter.

An analysis step-by-step of the commutation using the alternative modulation is shown in Figure 3.13. It considers the positive output voltage half-cycle. Figures 3.13(a) to

Figure 3.12 – Drive signals and drain-source voltages during a grid period using the enhanced modulation.



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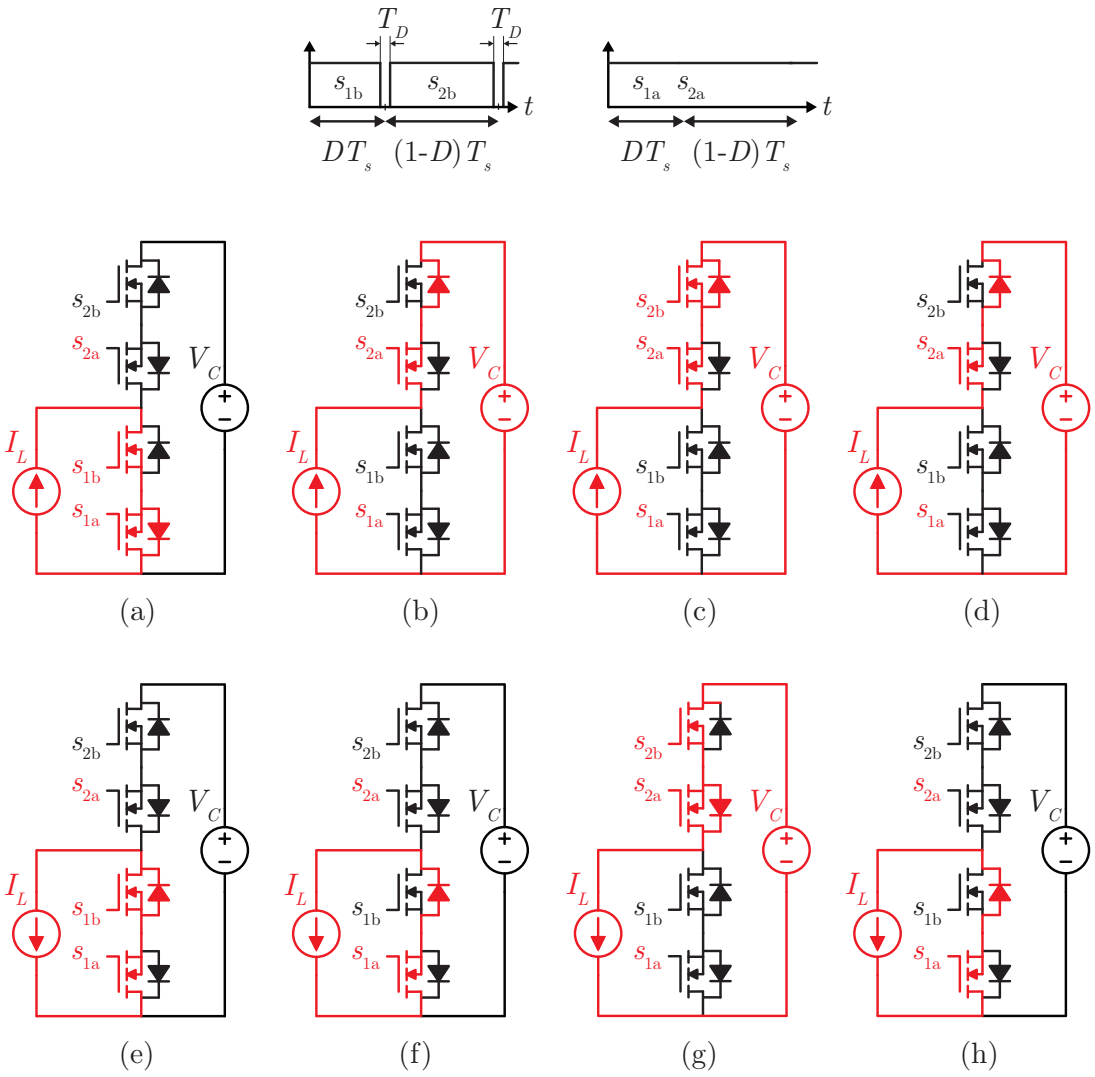
3.13(d) show the commutation for a positive current, while from Figure 3.13(e) to Figure 3.13(h) the representation is performed for a negative current. It is observed that there is always a path where the current can flow through. Furthermore, either body diode of S_{1b} or S_{2b} blocks the output voltage, avoiding a short circuit on the output voltage source. When the output voltage is negative, a similar analysis can be performed.

This modulation seems to work properly, however, when the value of the output voltage approximate zero, its measurement may not be accurate. This is because of the measure range of the voltage sensor, which has a lower limit value, and the voltage ripple, which may adds noise to the measurement. That said, if the output signal is wrongly determined, a short-circuit will occur and may damage the components. In order to avoid wrong signal measurements, the enhanced modulation is not used in a determined range of output voltage. A simplified block diagram is presented in Figure 3.14. First, the output voltage is read by the Analog Digital Converter (ADC) of a microcontroller. If the module is smaller than a previously defined value, the conventional modulation is used. On the

Figure 3.13 – Current path during each operation stage when the enhanced modulation is employed.



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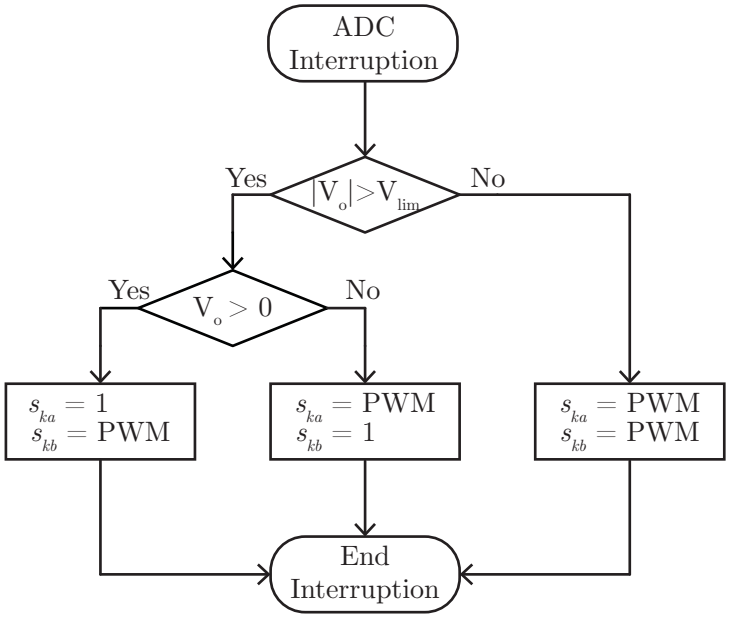
other hand, it is verified the signal of the output voltage. If it is positive, the lower MOSFETs S_{1a} and S_{2a} are always turned on. In the case of negative output voltage, the upper MOSFETs S_{1b} and S_{2b} receive a high level gate signal.

The following conclusions are made about this commutation analysis:

- It is not possible to employ the traditional modulation of DC-DC Boost converter when operating as an AC-AC converter with four-quadrant switches;
- A dead-time is required to avoid short circuit in the capacitors;
- The modified modulation provides a current path during dead-time;
- In order to implement the modified modulation, the output voltage should be measured.

Figure 3.14 – Simplified block diagramm of the employed modulation.



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Even though the enhanced modulation is not used during a short period, the voltage spikes may damage the components. Thus, dissipative voltage clamping circuits are inserted in each four-quadrant switch. A voltage clamping circuit composed by two diodes, one capacitor and one resistor is studied. Its representation is shown in Figure 3.15, in which the diodes work as a rectifier, then the voltage over the capacitor C_{cl} is always positive. The resistor R_{cl} is used to dissipate the excess of energy stored in the capacitor.

The voltage clamping circuit receives energy from the inductor during the dead-time when the conventional modulation is employed. An equivalent representation is depicted on Fig 3.16(a).

The variable δ is computed by (3.12). It represents the fraction between the total dead time and the switching period.

$$\delta = \frac{2T_D}{T_s} \tag{3.12}$$

An averaged circuit can be derived, as shown in Figure 3.16(b). Due to the clamping diodes, the polarity of the voltage v_{cl} is always positive. For the mathematical analysis, it is considered that the inductor is large enough, so that its current is approximately constant during the dead time. The differential equation that describes the averaged circuit is given by:

$$\delta|I_L(\omega_g t)|R_{cl} - C_{cl}R_{cl}\frac{dv_{C_{cl}}(t)}{dt} - v_{Ccl}(t) = 0 \tag{3.13}$$

Figure 3.15 – (a) Representation for the voltage clamping circuit; (b) Current path for positive current and voltage; (c) Current path for negative current and positive voltage.

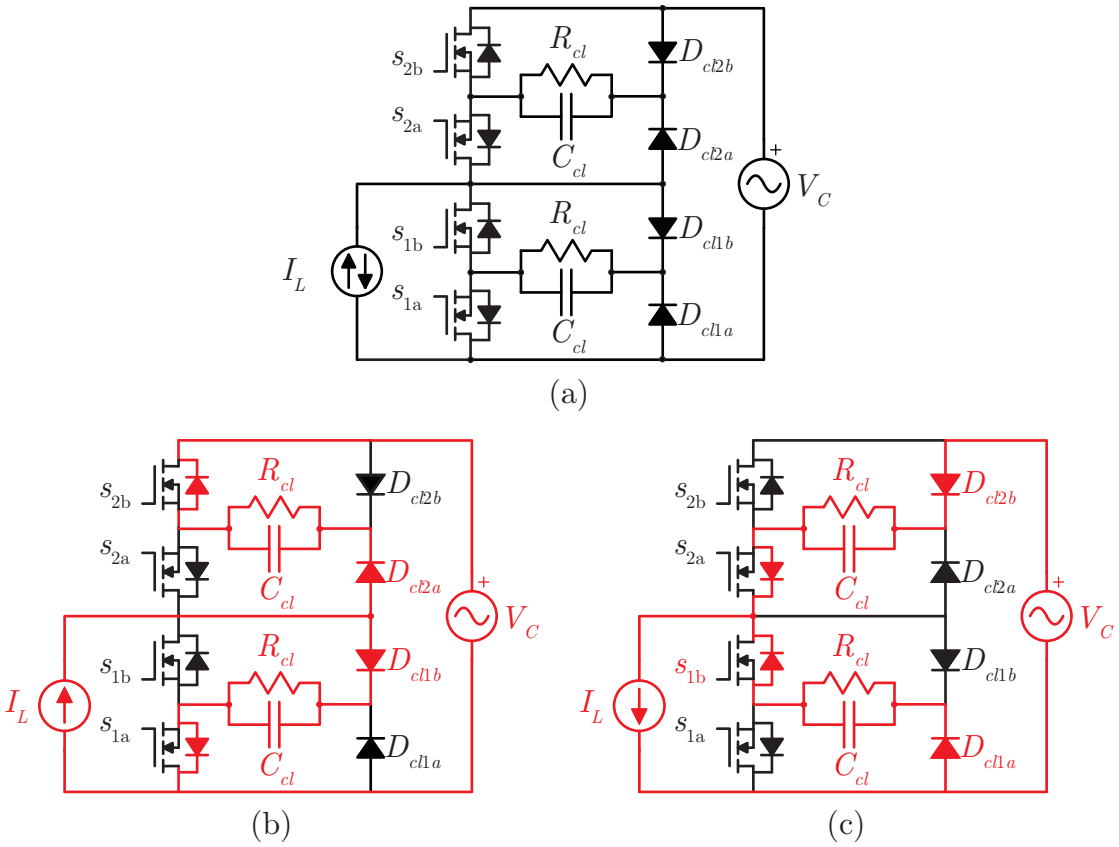

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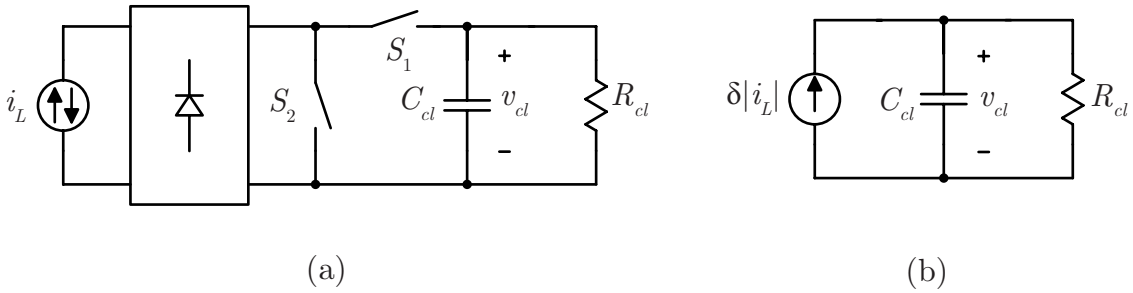
Figure 3.16 – Equivalent representation for the voltage clamping circuit. (a) Switched model (b) Averaged model.



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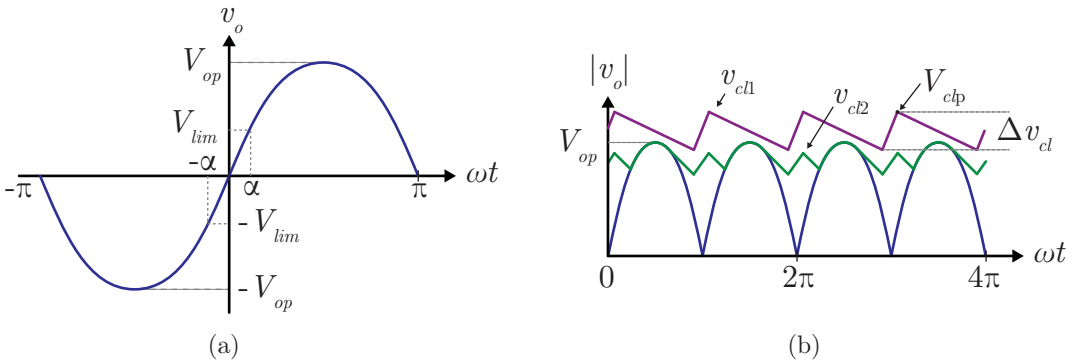
The angle in which the voltage clamping circuit operates is defined as α. It is calculated for a predefined output voltage value V_{lim} (Figure 3.17(a)). Thus,

$$\alpha = sin^{-1}\left(\frac{V_{lim}}{V_{op}}\right). \tag{3.14}$$

Given the condition that the time constant $R_{cl}C_{cl}$ is much higher than the conduc-

Figure 3.17 – (a) Output voltage representation and limits of modulation. (b) Simplified possible voltage waveforms over a clamping capacitor.



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tion time $t_\alpha = \alpha\omega_z$, the clamping voltage variation obtained is

$$\Delta V_{cl} = \frac{\delta}{\omega_g C_{cl}} \int_{-\alpha}^{\alpha} |i_L|(\omega t) d(\omega t). \tag{3.15}$$

This variation occurs when the output voltage is near zero. Thus, the initial clamping voltage is approximated by

$$V_{cl,i} = \frac{V_{op}}{2}\left(1 - \frac{1}{4 f_g R_{cl} C_{cl}}\right), \tag{3.16}$$

and the peak voltage equal to

$$V_{cl,p} = V_{cl,i} + \Delta V_{cl}. \tag{3.17}$$

In the case that the voltage variation is high enough, that the clamping voltage do not cross the output voltage (v_{cl1}), then

$$V_{cl,p} = 4 f_g R_{cl} C_{cl} \Delta V_{cl}. \tag{3.18}$$

Thus, it is possible to design a voltage clamping circuit that allows the operation of the converter during the dead-time, when the modified modulation is disabled.

3.3 CONCLUSION

This chapter presented the analysis of an AC-AC boost converter. The basic operation concepts were introduced, followed by a simple steady-state analysis. An equivalent average model was obtained, which simplifies the input-output analysis and simulations of the converter. The main equations were derived and the influence of parametric variations

were studied. A commutation problem in typical AC-AC PWM converters was presented, followed by a modulation strategy and an analysis of the voltage clamping circuit, which operates when the traditional modulation is on. The main conclusions of this chapter are listed as:

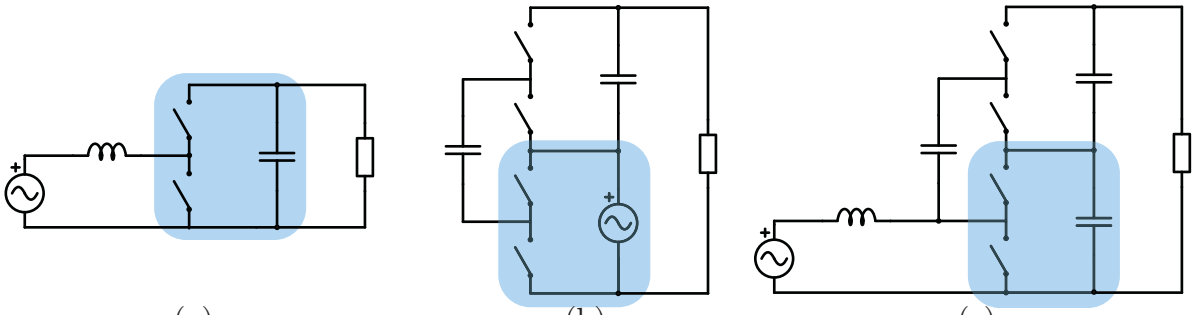
- The boost converter can operare as an AC-AC converter with fixed duty cycle;
- Inductance and capacitance influence on the input/output characteristics in low frequency, specially when either the duty cycle or the grid frequency are high;
- It is possible to control the output voltage via duty cycle variation;
- For low power levels and common grid voltages the input power factor is usually capacitive for resistive loads;
- AC-AC converters present commutation problems when conventional modulations are applied;
- By using a modified modulation it is possible to almost eliminate the commutation problem, at the cost of output-voltage measuring;
- The voltage stresses over the components are equal to the output peak voltage.

4 AC-AC HYBRID BOOST SWITCHED CAPACITOR CONVERTER

Switched capacitor converters have the advantage of voltage efforts sharing and achieve high voltage gains. However, the difficulty of controlling the output voltage outside low voltage and low power applications has lead to the development of hybrid DC-DC converters, which combine one or more switched-capacitor cells with other converters. These resultant topologies have the same characteristics of switched-capacitor converters, although they can be easily controlled by duty cycle variation. The integration can be applied to both non-isolated (VECCHIA; LAZZARIN, 2016) and isolated converters (DALL'ASTA; FUERBACK; LAZZARIN, 2018).

The previous chapters were focused on two direct AC-AC constant frequency topologies: the switched capacitor ladder converter and the inductive commutated cell. The fixed voltage gain from the ladder topology and the practical limited gain and high voltage stresses of boost converter are some drawbacks of these topologies. However, it is possible to combine both topologies to obtain a boost hybrid switching-capacitor converter (ROSAS-CARO; RAMÍREZ; GARCÍA-VITE, 2008). Figures 4.1(a) and 4.1(b) show respectively the AC-AC boost and the AC-AC ladder converters. It should be noted that both converters present a similar part, in which two switches are connected to a capacitor. Thus, the input voltage source of the ladder converter can be exchanged by the output capacitor of a boost converter, integrating the two lower switches. It results in an AC-AC hybrid structure, as shown in Figure 4.1(c). This hybrid topology was already employed in other applications, such as high gain PWM rectifiers (DIAS et al., 2017).

Figure 4.1 – Common elements in (a) boost and (b) ladder converters and their integration to the (c) hybrid structure.



Source – Author.

A hybrid structure usually combines the characteristics from composing structures. A comparison among the boost, ladder and hybrid topologies is presented in Table 4.1. The main advantage of this combination is the high controllable gain, the low voltage stresses and the low input current THD.

The hybrid boost switched-capacitor converter was already studied as part of

Table 4.1 – Comparison among boost, ladder and hybrid topologies.

Converter	Ladder	Boost	Ladder + Boost
Gain	Fixed 2	Variable $\frac{1}{1-D}$	Variable $\frac{2}{1-D}$
Modulation complexity	Low	Medium	Medium
Voltage stresses	$\frac{V_o}{2}$	V_o	$\frac{V_o}{2}$
Input current THD	High	Low	Low
Number of switches	4	2	4
Number of capacitors	3	1	3
Number of inductors	0	1	1

Source – Author.

rectifiers (DIAS; MUSSA; LAZZARIN, 2016) and inverters (SILVA; COELHO; LAZZARIN, 2016), highlighting its advantages of voltage sharing without an additional control strategy. The following sections will explore the operation of the hybrid boost switched-capacitor cell as an AC-AC converter.

4.1 HYBRID CONVERTER

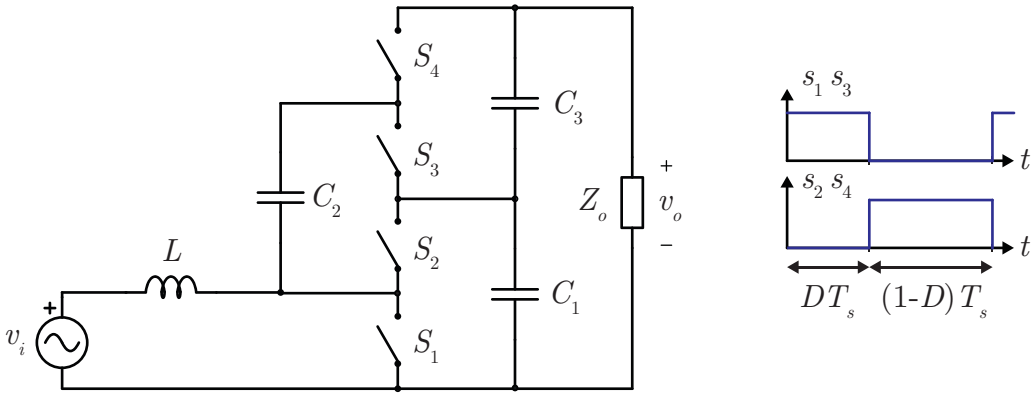
This section focuses on the steady state and dynamic analyses of the Hybrid Boost Switched-Capacitor Converter (HBSCC). The equivalent electric circuit is shown in Figure 4.2 and is composed of an input inductor L, two output capacitors C_1 and C_3, a switched capacitor C_2 and four-quadrant switches S_1, S_2, S_3 and S_4. The input and output are represented as an alternating voltage source and an impedance load, respectively. The modulation consists in switches S_1 and S_3 commuting concurrently between each other and complementary to S_2 and S_4. The modulation schema leads to two different operating stages, which are depicted in Figure 4.3(a) and Figure 4.3(b).

The analysis of the operating stages considers that the switching frequency is much higher than the grid frequency. Moreover, the operation stages are described considering a positive input voltage and output current. For a negative input voltage, the analysis would be similar.

First operating stage: Switches S_1 and S_3 are turned-on, while S_2 and S_4 are turned-off. The input current increases and the inductor stores energy from the voltage source; capacitors C_1 and C_3 supply the output current and capacitor C_2 is charged by capacitor C_1.

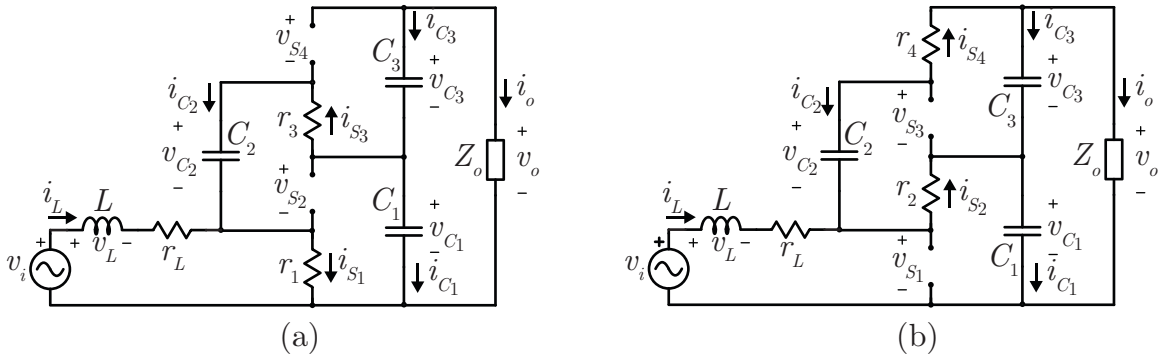
Second operating stage: Switches S_2 and S_4 are turned-on, while S_1 and S_3 are turned-off. The input current decreases and the inductor transfers energy to the output

Figure 4.2 – Equivalent electric circuit for the hybrid boost switched capacitor converter.



Source – Author.

Figure 4.3 – Equivalent electric circuit of the HBSCC in the first and second operating stages.



Source – Author.

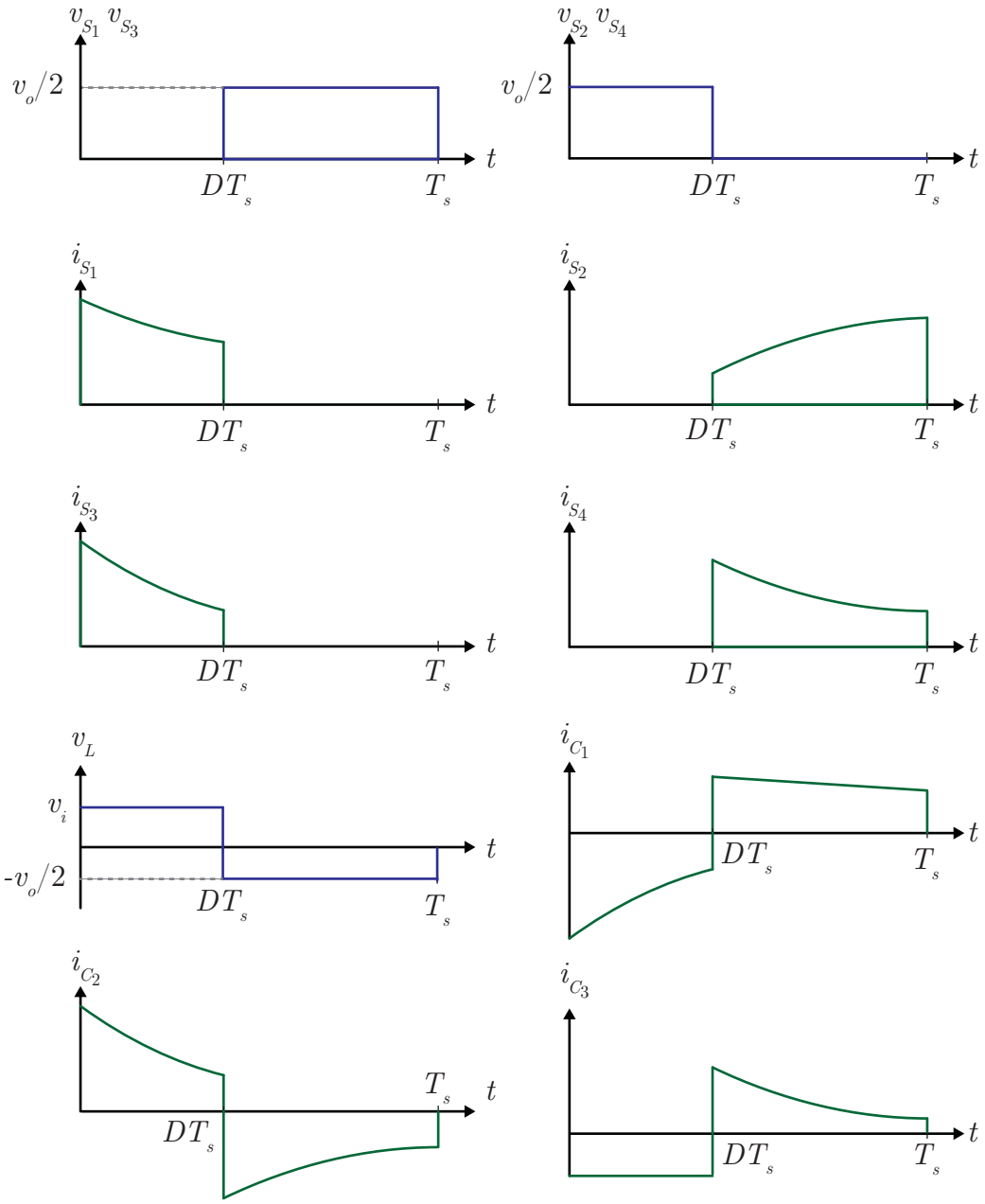
capacitor C_1. The switching capacitor C_2 charges capacitor C_3 and supplies the output current.

The theoretical waveforms considering a switching period in the positive half cycle are illustrated in Figure 4.4. It is apparent that the voltage over the switches is limited to half of the output voltage peak value. Furthermore, all currents in the switches and capacitors present partially an exponential shape, due to the switched capacitor cell operating in partial-charging mode.

A comparison among input and output voltages and currents for a resistive load is presented in Figure 4.5. One interesting characteristic to be noted is that even if the output power factor is unitary, the input power factor is capacitive, due to the reactive power related to the capacitors. Therefore, the ratio between input and output currents is higher than the ratio between output and input voltages. Furthermore, there is almost no phase-shift from input to output voltages, given that the voltage drop in input inductance is usually negligible for low grid frequencies.

Regarding the components, the main waveforms for a grid period are presented in Figure 4.6. The capacitors are designed in order to maintain a small voltage ripple and

Figure 4.4 – Main waveforms of the HBSCC during a switching period in the positive half-cycle and operating in partial charging mode.

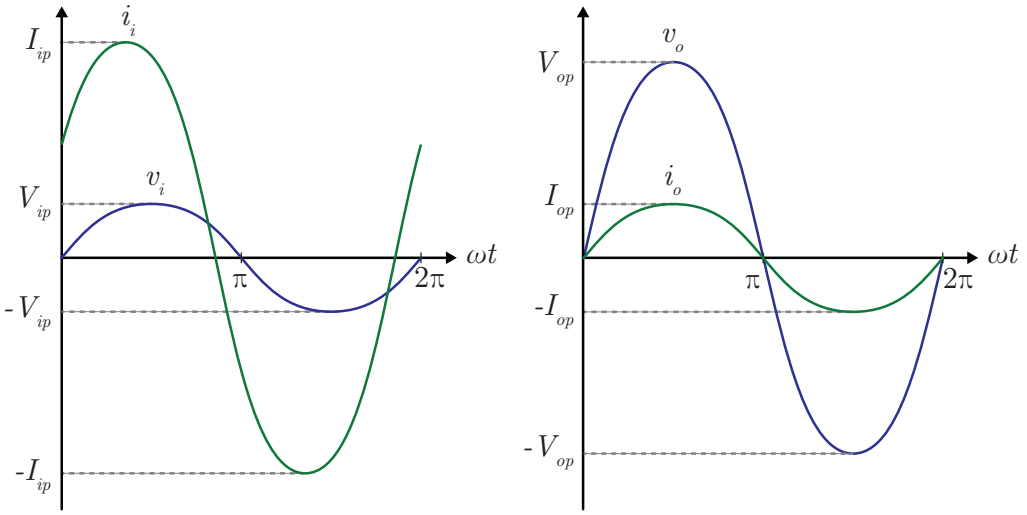


Source – Author.

the peak value of the voltages over them are equal to half of output peak value. This maximum value is also applied to all switches, whose envelopes follow the voltages over the capacitors. The currents through the switches also present a sinusoidal envelope, however, they lead the voltages, given an input capacitive power factor. One fact to be considered is that the voltages and currents on switches alternate between positive and negative values. This shows the necessity of employing four-quadrant switches.

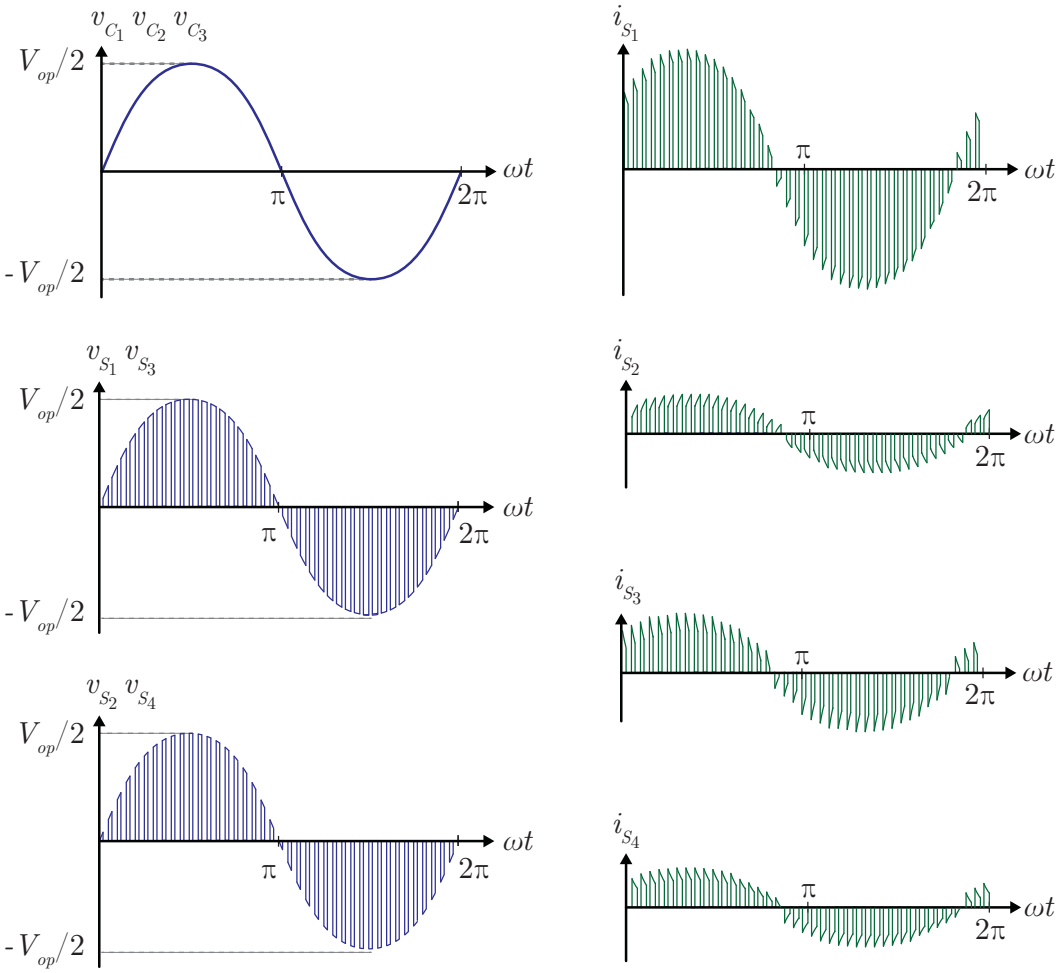
This section has analyzed qualitatively the operating stages and the main waveforms in high and low frequencies. Next sections will approach quantitatively the converter.

Figure 4.5 – Input and output voltages and currents during a grid period.



Source – Author.

Figure 4.6 – Main waveforms of voltages over devices and currents through switches.



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4.2 IDEAL ANALYSIS

Initially an ideal analysis of the converter is performed. It helps to understand the basics characteristics of the converter and a small error is expected, because all the non-idealities are negleted. From Figure 4.3 and considering the conduction resistances equal to zero, the relations (4.1) are obtained for the first operation stage. It should be noted that, as there is a switching capacitor cell, the capacitors C_1 and C_2 are connected in parallel, resulting ideally in the same voltage over them.

$$\begin{aligned} v_L &= v_i \\ v_{c_1} &= v_{c_2} \\ i_{c_1} + i_{c_2} &= -i_o \\ i_{c_3} &= -i_o \end{aligned} \tag{4.1}$$

During the second operation stage, capacitors C_2 and C_3 are connected in parallel. Thus, the obtained equations are:

$$\begin{aligned} v_L &= v_i - v_{c_1} \\ v_{c_3} &= v_{c_2} \\ i_{c_1} &= i_L - i_o \\ i_{c_2} + i_{c_3} &= -i_o. \end{aligned} \tag{4.2}$$

Supposing that the capacitances are large enough, so that the voltage ripples over the capacitors are small, it is concluded that the averaged voltages over the three capacitors are approximately the same:

$$\langle v_{C_1} \rangle = \langle v_{C_2} \rangle = \langle v_{C_3} \rangle. \tag{4.3}$$

The output voltage is equal to the sum of the voltages over capacitors C_1 and C_3. As their voltages are equal, the following relation can be written:

$$\langle v_{C_1} \rangle = \langle v_{C_2} \rangle = \langle v_{C_3} \rangle = \frac{\langle v_o \rangle}{2}. \tag{4.4}$$

Now, writing the averaged voltage over the inductor during a switching period results in

$$\langle v_L \rangle = \left\langle L \frac{d}{dt} i_L \right\rangle = \langle v_i \rangle - (1-d) \langle v_{C_1} \rangle. \tag{4.5}$$

As the current in the inductor is sinusoidal, the variables i_L, v_{C_1}, v_{C_2} and v_{C_3} are expressed as phasors and the following relation is obtained:

$$\left\langle L \frac{d}{dt} \boldsymbol{i_L} \right\rangle = L \frac{d}{dt} \langle \boldsymbol{i_L} \rangle + j\omega_g L \langle \boldsymbol{i_L} \rangle. \tag{4.6}$$

Considering the operation in steady state, the derivative of the input current is zero. Then, applying (4.4) in (4.5) and solving for the output voltage results in

$$\langle \boldsymbol{v_o} \rangle = \frac{2}{1-d} \left(\langle \boldsymbol{v_i} \rangle - j\omega_g L \langle \boldsymbol{i_L} \rangle \right). \tag{4.7}$$

From (4.7) it can be noticed that the input inductance value influences the voltage gain, even in an ideal analysis, because AC components are considered. To determine the input current value, firstly it is considered the averaged current value in the three capacitors, given that they share the same voltage.

$$\langle \boldsymbol{i_c} \rangle = \left\langle (C_1 + C_2 + C_3) \frac{d}{dt} \boldsymbol{v_c} \right\rangle = (1-d) \langle \boldsymbol{i_L} \rangle - 2 \langle \boldsymbol{i_o} \rangle \tag{4.8}$$

Thus, the input current in sinusoidal steady state operation is determined as

$$\langle \boldsymbol{i_L} \rangle = \frac{2}{1-d} \langle \boldsymbol{i_o} \rangle + j \frac{\omega_g (C_1 + C_2 + C_3)}{2(1-d)} \langle \boldsymbol{v_o} \rangle, \tag{4.9}$$

noting that it contains a imaginary part that depends on the output voltage, duty cycle, grid frequency and capacitances. It should be also observed that the this reactive part does not depend on the output power or output current, then for light loads its value is proportionally high in relation to the active component. The output voltage as function of input voltage and load current is obtained by applying (4.9) in (4.7) and is given by

$$\langle \boldsymbol{v_o} \rangle = \frac{1}{\left(1 - \frac{\omega_g^2 L (C_1+C_2+C_3)}{(1-d)^2} \right)} \left(\frac{2}{1-d} \langle \boldsymbol{v_i} \rangle - j \frac{4}{(1-d)^2} \omega_g L \langle \boldsymbol{i_o} \rangle \right). \tag{4.10}$$

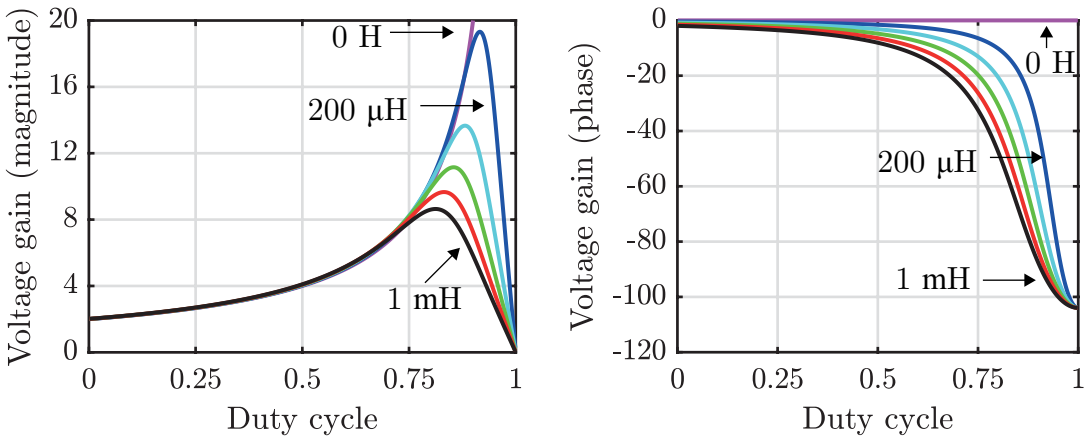
If the output load is linear and described as $Z_o = R_o + jX_o$, the output voltage is written as

$$\langle \boldsymbol{v_o} \rangle = \frac{\frac{2}{1-d} \langle \boldsymbol{v_i} \rangle}{1 - \frac{w_g^2 L (C_1+C_2+C_3)}{(1-d)^2} + \frac{4\omega_g L X_o}{(1-d)^2 |Z_o|^2} + j \frac{4\omega_g L R_o}{(1-d)^2 |Z_o|^2}}. \tag{4.11}$$

The voltage gain as function of duty cycle and input inductance for output capacitors $C_1 = C_2 = C_3 = 20\ \mu$F, 60 Hz grid frequency and resistive output load is presented in Figure 4.7. It is noted that, until a duty cycle of 0.75, there is almost no influence from the input inductance. However, for high values of duty cycles, the voltage gain is limited. It should be observed the similarities between Figures 3.6 and 4.7, which means that the voltage gain magnitude is multiplied by two and there is more phase shift when the switched capacitor cell is integrated to the boost converter.

By analyzing (4.10), it is noticed that the denominator may be zero for some

Figure 4.7 – Voltage gain for different duty cycles and input inductances.



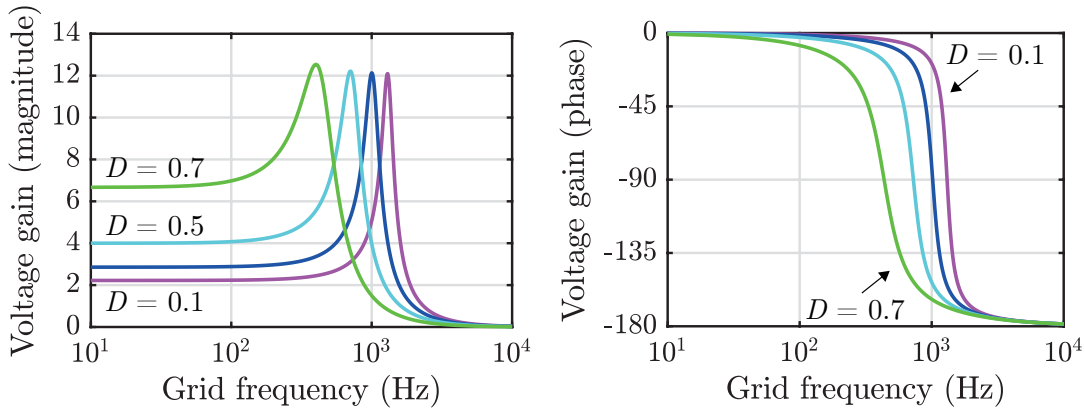
Source – Author.

parametric combination. Then, a resonant frequency is calculated as

$$f_{ress} = \frac{(1-d)}{2\pi}\sqrt{\frac{1}{L(C_1+C_2+C_3)}}. \tag{4.12}$$

A relation between the voltage gain and the grid frequency is illustrated in Figure 4.8. It is noted that there is a resonant frequency that decreases when there is an increase in the duty cycle. Thus, the operating point of the converter should be for main frequencies smaller than the resonant frequency. In addition, if there are harmonic components in the input voltage source, they might be amplified.

Figure 4.8 – Voltage gain as function of the grid frequency for different duty cycle values.



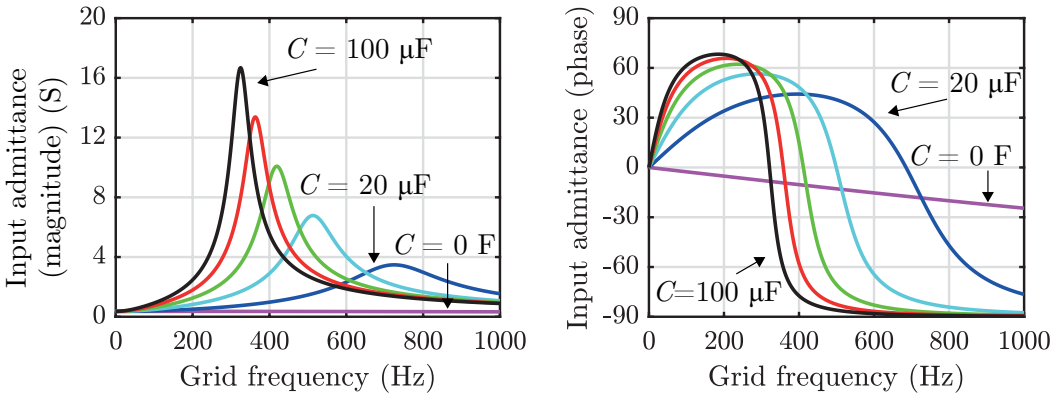
Source – Author.

If the load is linear and described as $Z_o = R_o + jX_o$, the input current is determined by

$$\langle \boldsymbol{i_i} \rangle = \langle \boldsymbol{v_i} \rangle \frac{4R_o + j(\omega_g(C_1+C_2+C_3)Z_o^2 - 4Xo)}{(1-d)^2 Z_o^2 - \omega_g^2 L(C_1+C_2+C_3)Z_o^2 + 4\omega_g L X_o + j4\omega_g L R_o}. \tag{4.13}$$

Defining the input admittance as $\boldsymbol{y_i} = \boldsymbol{i_i}/\boldsymbol{v_i}$, it is displayed in Figure 4.9 for different grid frequencies and capacitance values. In this case, all the capacitances are considered equal. It is observed that higher values of capacitances lead to lower resonant frequencies. Thus, the magnitude of the input admittance increases significantly, considering it a short-circuit at resonant frequency. Another interesting graphic is on the right, in which the phase is displayed. The admittance phase is equal to the phase shift between input current and voltage. Thus, it is concluded that the input power factor is highly dependent on the output capacitance values and grid frequency.

Figure 4.9 – Input admittance as function of grid frequency and output capacitance.



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An analysis of the admittance as function of the output resistance can be seen in Figure 4.10. This figure is interesting because for high load impedance values, the input admittance is different from zero except when the output capacitance is zero. That means, even for light loads there are reactive currents, which increase with the output capacitance. For example, considering capacitances equal to 100 μF, the input admittance for light loads is 0.5 S. Therefore, for an 100 V input voltage, the reactive input current would be 50 A. In conclusion, capacitance values should be limited to avoid high reactive current values.

The right graphic in Figure 4.10 shows that, for lower output loads, the input power factor decreases, because the admittance phase increases (higher phase shift between input current and voltage). Furthermore, there is a load value in which the reactive component of the input inductance overweights the reactive capacitive power.

The ideal averaged circuit model, that represents the ideal steady state equations, is presented in Figure 4.11. It summarizes the input and output characteristics of the converter and may be compared to the equivalent circuit of a conventional transformer. Furthermore, it allows faster simulations when only the input and output variables are necessary.

The capacitance C_{eq} is the sum of all capacitances reflected to the high voltage

Figure 4.10 – Input admittance as function of the output load and output capacitance values.

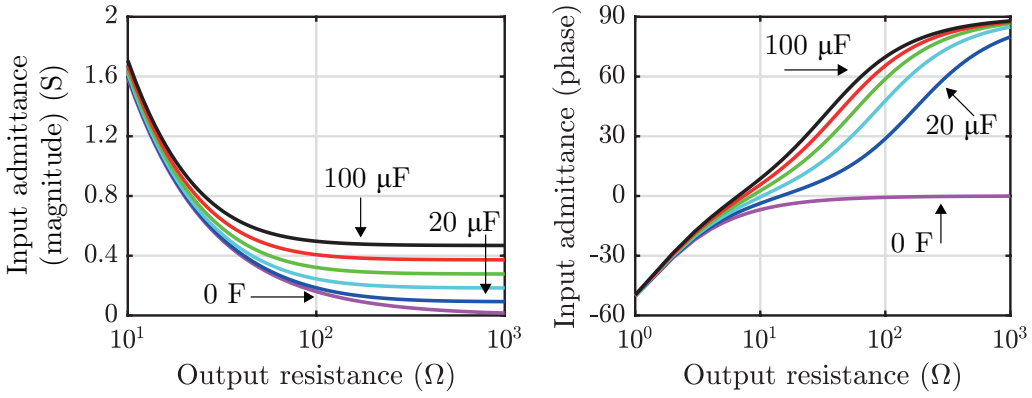

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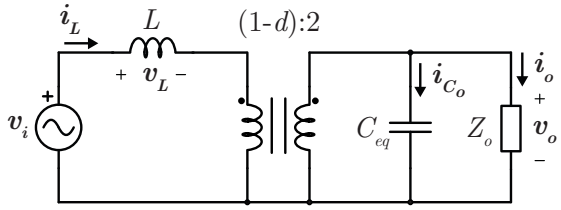
Figure 4.11 – Equivalent electric circuit for hybrid converter



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side:

$$C_{eq} = \frac{C_1 + C_2 + C_3}{4}. \tag{4.14}$$

By defining an inductive and capacitive reactive power as positive and negative, respectively, the relation between input and output reactive power is given by:

$$Q_i = Q_o + |I_L|^2 \omega_g L_b - |V_o|^2 \omega_g C_{eq} \tag{4.15}$$

Ideally, the input power is the same as the output power ($P_i = P_o$). Thus, the input apparent power is computed by

$$S_i = \sqrt{P_i^2 + Q_i^2} = \sqrt{P_o^2 + (Q_o + |I_L|^2 \omega_g L_b - |V_o|^2 \omega_g C_{eq})^2}, \tag{4.16}$$

and the input power factor by

$$PF_i = \frac{P_i}{S_i} = \frac{P_o}{\sqrt{P_o^2 + (Q_o + |I_L|^2 \omega_g L_b - |V_o|^2 \omega_g C_{eq})^2}}. \tag{4.17}$$

From (4.17) and knowing that for high output voltage levels and low/medium

rated power the reactive power related to the input inductance is much smaller than the one related to the capacitances. Thus, an optimum load is obtained, in order to grant an unitary input power factor:

$$Q_{o,opt} = +|V_o|^2 \omega_g C_{eq}. \tag{4.18}$$

Some conclusions that are made from this ideal analysis:

- Input and output characteristics are similar to the AC-AC boost converter;
- The output voltage gain is doubled in comparison to the boost converter;
- It is possible to control the output voltage by duty cycle variation;
- The equivalent average circuit model is also similar to the boost converter, with modifications in the equivalent transformer turns ratio and in the output capacitance;
- The increased equivalent output capacitance implies in higher rective current values;
- The resonant frequency value is smaller when compared to the boost converter, given the fact that there are three capacitors;

4.3 CURRENT'S ANALYSIS VIA DIFFERENTIAL EQUATIONS

The analysis of the converter via state-space modeling is not suitable for obtaining current waveforms and effective values for switched capacitor converters with low $f_s\tau$ factor, because the exponential waveform is simplified by a constant value with equal average value. Then, this section focuses on obtaining a more accurate description of the currents in the semiconductors. Initially, the averaged charge transferred to the output load during a switching period is defined as

$$q_o = \int_0^{T_s} i_o dt = \langle i_o \rangle T_s. \tag{4.19}$$

There is an average charge in the capacitors in each switching period for non-constant output voltages. In this analysis, it is assumed that the voltages over the capacitors are equal to half of the output voltage. Thus, the net charge flow in a capacitor C after one switching period is

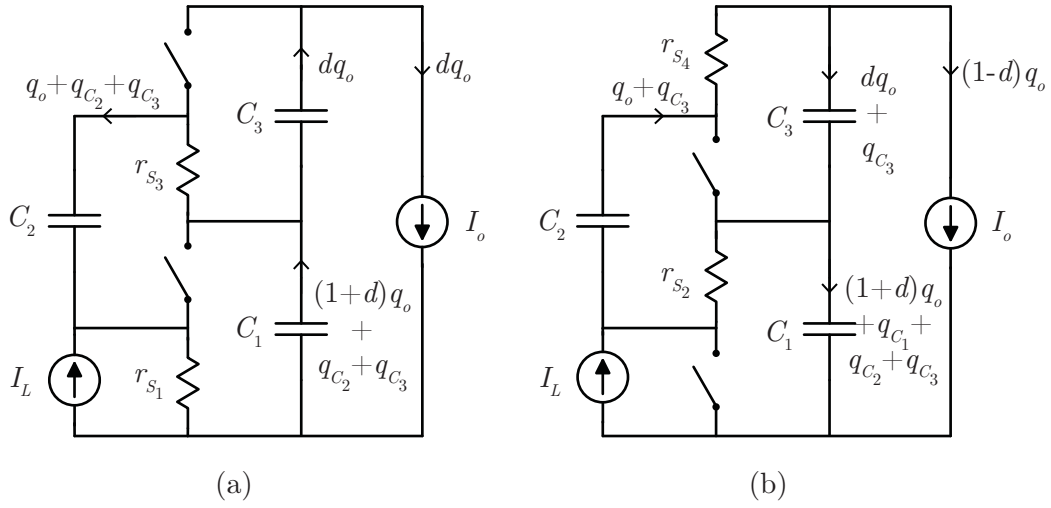
$$q_c = \int_0^{T_s} i_c dt = -\frac{V_{op}}{2} \omega_g C T_s sin(\omega_g t). \tag{4.20}$$

By analyzing both operating stages for all components, the charge variations in each stage were determined an depicted in Figure 4.12(a) and 4.12(b). It should be noted that the charge flow over the capacitors are higher for those located near the boost cell.

The total input charge during a switching period is

$$q_i = \frac{2q_o}{1-d} + \frac{q_{C_1} + q_{C_2} + q_{C_3}}{1-d}, \tag{4.21}$$

Figure 4.12 – Equivalent electric circuit of the HBSCC considering conduction resistances.



Source – Author.

therefore, the input current is obtained as

$$\langle i_i \rangle = \frac{2}{1-d}\langle i_o \rangle - \frac{\omega_g V_{op}}{2(1-d)}(C_1+C_2+C_3)sin(\omega_g t). \tag{4.22}$$

The expression for the input current is equal to the one demonstrated in (4.9) when $\langle v_o \rangle = V_{op}cos(\omega_g t)$. It is observed that the input current is a function not only of the output current and duty cycle, but also a function of the grid frequency, output voltage and capacitances. That said, even if the converter operates in a condition of no output load, there is still a reactive circulating current, which cause significant losses at light load operations.

4.3.1 Current analysis for no-charge mode

This section presents the simplified currents analysis, in which the no-charge operating mode (2.10) is considered. This method is usually accurate for converters whose time constants are higher than the switching period, then the charging and discharging capacitor are considered as constants during each operating stage.

Considerations made in section 2.2.2 are applied to this analysis. From Figure 4.12, the charge quantities in each element for both operating stages are obtained. Thus, applying (2.7) and (2.8), the ideal currents are obtained. The results are shown in Table 4.2, and represent the instantaneous currents values in each operating stage. In order to calculate the effective values, the definition in (2.11) should be applied.

Table 4.2 – Currents of the HBSCC in no-charge mode in a switching period.

	$0 < t < DT_s$	$DT_s < t < T_s$	Average value
$i_{S_1,nc}$	$\frac{(1+d)q_o + dq_{C_1} + q_{C_2} + q_{C_3}}{d(1-d)T_s}$	0	$\frac{(1+d)q_o + dq_{C_1} + q_{C_2} + q_{C_3}}{(1-d)T_s}$
$i_{S_2,nc}$	0	$\frac{q_o + q_{C_1} + q_{C_2}}{(1-d)T_s}$	$\frac{q_o + q_{C_1} + q_{C_2}}{T_s}$
$i_{S_3,nc}$	$\frac{q_o + q_{C_2} + q_{C_3}}{dT_s}$	0	$\frac{q_o + q_{C_2} + q_{C_3}}{T_s}$
$i_{S_4,nc}$	0	$\frac{q_o + q_{C_3}}{(1-d)T_s}$	$\frac{q_o + q_{C_3}}{T_s}$
$i_{C_1,nc}$	$-\frac{(1-d)q_o + q_{C_2} + q_{C_3}}{dT_s}$	$\frac{(1-d)q_o + q_{C_1} + q_{C_2} + q_{C_3}}{(1-d)T_s}$	$\frac{q_{C_1}}{T_s}$
$i_{C_2,nc}$	$\frac{q_o + q_{C_2} + q_{C_3}}{dT_s}$	$-\frac{q_o + q_{C_3}}{(1-d)T_s}$	$\frac{q_{C_2}}{T_s}$
$i_{C_3,nc}$	$-\frac{q_o}{T_s}$	$\frac{dq_o + q_{C_3}}{(1-d)T_s}$	$\frac{q_{C_3}}{T_s}$

4.3.2 Current analysis for partial-charge mode

The analysis of the no-charge mode considers that the capacitors currents are constants during one operation stage, which is not a suitable approximation for most real cases. Then, the effective current values are in fact higher than those obtained via this analysis. A similar method to the one used for the basic cell is described, in order to obtain one approximation of the current waveforms and their effective values. In this case, the current in the inductor is considered constant during a switching period, therefore represented by a current source, as well as the output current.

From Figure 4.12(a), three differential equations relating the currents in the capacitors are obtained:

$$\begin{aligned} \frac{di_{C_2}}{dt} + i_{C_2}\left(\frac{C_2 + C_1}{C_1 C_2 (r_1 + r_3)}\right) &= -\langle i_o \rangle \frac{1}{C_1(r_1 + r_3)} \\ i_{C_1} &= -i_{C_2} - \langle i_o \rangle \\ i_{C_3} &= -\langle i_o \rangle \end{aligned} \tag{4.23}$$

There is only one unknown variable in the first equation of (4.23). Solving it for the current i_{C_2} leads to

$$i_{C_2}(t) = I_{C_2,p_1} e^{-\frac{t}{\tau_1}} - \frac{C_2}{C_1 + C_2}\langle i_o \rangle, \tag{4.24}$$

in which the constant I_{C_2,p_1} is still unknown and the time constant τ_1 is defined as

$$\tau_1 = (r_1 + r_3)\frac{C_1 C_2}{(C_1 + C_2)}. \tag{4.25}$$

The boundary condition that can be used is to find I_{C_2,p_1} is the total electric charge flow in C_2 during the first operating stage, given by $q_o + q_{C_2} + q_{C_3}$. Thus, the following relation is written:

$$\int_0^{DT_s} i_{C_2}(t)dt = q_o + q_{C_2} + q_{C_3}. \tag{4.26}$$

The equation that describes the current i_{C_2} during the first operation stage is determined by applying (4.24) in (4.26) and results in

$$\begin{aligned} i_{C_2,1}(t) = &\frac{T_s}{\tau_1\left(1 - e^{-\frac{DT_s}{\tau_1}}\right)}\left[\langle i_o\rangle\frac{C_1 + C_2(1+d)}{C_1 + C_2} - \frac{V_{op}}{2}sin(\omega_g t)\omega_g(C_2 + C_3)\right]e^{-\frac{t}{\tau_1}} + \\ &- \frac{C_2}{C_1 + C_2}\langle i_o\rangle. \end{aligned} \tag{4.27}$$

It is noted that the current in the capacitor C_2 presents an exponential characteristic, which depends on the non-idealities of the components, such as the conduction resistances of the switches. In addition, there is a steady state term which depends only on the capacitance values and on the output current. Continuing the analysis, as given by (4.23), the current in capacitor C_1 is obtained from the negative of $i_{C_2,1}(t)$ minus the output current, resulting in

$$\begin{aligned} i_{C_1,1}(t) = &-\frac{T_s}{\tau_1\left(1 - e^{-\frac{DT_s}{\tau_1}}\right)}\left[\langle i_o\rangle\frac{C_1 + C_2(1+D)}{C_1 + C_2} - V_{op}sin(\omega_g t)\omega_g(C_2 + C_3)\right]e^{-\frac{t}{\tau_1}} + \\ &- \frac{C_1}{C_1 + C_2}\langle i_o\rangle. \end{aligned} \tag{4.28}$$

The current in C_3 is given directly as the negative of output current, thus $i_{C_3,1} = -\langle i_o\rangle$. Now, considering the second operating stage, the differential equations are written as:

$$\begin{aligned} \frac{di_{C_2}}{dt} + i_{C_2}\left(\frac{C_2 + C_3}{C_2 C_3(r_2 + r_4)}\right) &= -\langle i_o\rangle\frac{1}{C_3(r_2 + r_4)} \\ i_{C_1} &= \langle i_L\rangle - \langle i_o\rangle \\ i_{C_3} &= -i_{C_2} - \langle i_o\rangle. \end{aligned} \tag{4.29}$$

There is only one unknown variable in the first equation of (4.29). Solving it for

the current i_{C_2} results in

$$i_{C2,2}(t) = I_{C_2,p_2} e^{-\frac{t}{\tau_2}} - \frac{C_2}{C_2+C_3}\langle i_o \rangle, \tag{4.30}$$

in which the value of I_{C_2,p_2} is unknown and the time constant τ_2 is defined as

$$\tau_2 = (r_2 + r_4)\frac{C_2 C_3}{(C_2+C_3)}. \tag{4.31}$$

The charge flow in capacitor C_2 during the second operation stage is $-(q_o + q_{C_3})$. Using this information as boundary condition results in

$$\int_0^{(1-D)T_s} i_{C2,2}(t)dt = -(q_o + q_{C_3}). \tag{4.32}$$

An expression for the current in capacitor C_2 in the second operating stage is obtained by solving (4.32):

$$i_{C2,2}(t) = -\frac{T_s}{\tau_2\left(1-e^{-\frac{(1-D)T_s}{\tau_2}}\right)}\left[\frac{C_3+DC_2}{C_2+C_3}\langle i_o\rangle - \frac{C_3}{2}\omega_g V_{op} sin(\omega_g t)\right] e^{-\frac{t}{\tau_2}} - \frac{C_2}{C_2+C_3}\langle i_o\rangle \tag{4.33}$$

The current in capacitor C_2 was defined for both operating stages. Thus, the complete function that describes it during a switching period is given by (4.34).

$$i_{C_2}(t) = \begin{cases} i_{C_2,1}(t), & if \quad 0 \le t \le DT_s \\ i_{C_2,2}(t-DT_s), & if \quad DT_s \le t \le T_s \end{cases} \tag{4.34}$$

From (4.29) and (4.22) the current in capacitor C_1 is obtained for the second operating stage:

$$i_{C_1,2}(t) = \frac{1+D}{1-D}\langle i_o\rangle - \frac{\omega_g V_{op}}{2(1-D)}(C_1+C_2+C_3)sin(\omega_g t) \tag{4.35}$$

Applying the obtained result of (4.33) in the third equation of (4.29) leads to the current in capacitor C_3 during the second operating stage:

$$i_{C_3,2}(t) = \frac{T_s e^{-\frac{t}{\tau_2}}}{\tau_2\left(1-e^{-\frac{(1-D)T_s}{\tau_2}}\right)}\left[\frac{C_3+DC_2}{C_3+C_2}\langle i_o\rangle - \frac{\omega_g C_3}{2}V_{op} sin(\omega_g t)\right] - \frac{C_3}{C_2+C_3}\langle i_o\rangle. \tag{4.36}$$

One interesting characteristic to notice is that only the capacitor C_2 operates as a switching capacitor during the whole switching period. The equations show that for

both stages the current expression depends on the time constant. On the other hand, for capacitors C_1 and C_3, the current during one operation stage does not depend on the time constant and switching frequency. By possessing the expressions for the currents through the capacitors it is possible to compute the effective values during a grid period. Table 4.3 shows the comparison among simulated and theoretical results when considering no-charge and partial-charge operating modes.

Table 4.3 – Comparison between charging modes for computing current stresses.

	Variable	Simulation (A)	NC - Method (A)	Error (%)	PC - Method (A)	Error (%)
$f_s\tau$=0.01	$I_{S_1,ef}$	51.86	22.05	57.47	52.09	0.44
	$I_{S_2,ef}$	28.20	7.87	72.08	28.37	0.59
	$I_{S_3,ef}$	47.96	8.70	81.85	47.99	0.06
	$I_{S_4,ef}$	28.19	7.04	75.02	28.15	0.15
	$I_{C_1,ef}$	49.96	16.42	67.12	49.97	0.02
	$I_{C_2,ef}$	55.63	11.20	79.87	55.63	0.01
	$I_{C_3,ef}$	27.74	4.96	82.12	27.7	0.14
$f_s\tau$=0.1	$I_{S_1,ef}$	24.86	22.05	11.50	24.92	0.25
	$I_{S_2,ef}$	10.41	7.87	25.49	10.57	1.49
	$I_{S_3,ef}$	14.78	8.70	40.00	14.51	1.87
	$I_{S_4,ef}$	10.22	7.042	29.32	9.96	2.58
	$I_{C_1,ef}$	20.36	16.42	18.33	20.11	1.23
	$I_{C_2,ef}$	17.97	11.20	36.39	17.6	2.10
	$I_{C_3,ef}$	8.897	4.96	42.46	8.62	3.24
$f_s\tau$=1	$I_{S_1,ef}$	22.08	22.05	0.11	22.09	0.06
	$I_{S_2,ef}$	7.866	7.87	0.10	7.92	0.66
	$I_{S_3,ef}$	8.80	8.70	1.08	8.80	0.05
	$I_{S_4,ef}$	7.20	7.042	2.19	7.09	1.50
	$I_{C_1,ef}$	16.52	16.42	0.58	16.48	0.25
	$I_{C_2,ef}$	11.37	11.20	1.53	11.30	0.57
	$I_{C_3,ef}$	5.06	4.96	2.00	5.03	0.61

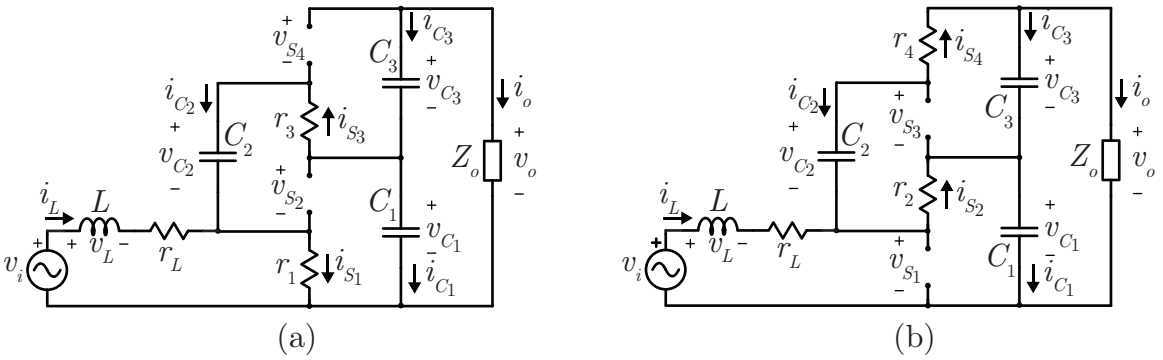
Source – Author.

From Table 4.3, it should be noted that, for low $f_s\tau$ factors, the theoretical results when considering no-charge mode are not accurate with the simulation. Therefore, the analysis considering the partial-charge mode should be applied. For high $f_s\tau$ values, the errors between theory and simulation are low for both charging modes.

4.4 ANALYSIS CONSIDERING NON-IDEALITIES

A simplified analysis is useful to understand the main characteristics of the converter. However, as the converter employs a switched-capacitor cell, the determination of current stresses on the components becomes difficult, prejudicing the converter design. Thus, an analysis considering non-idealities is performed. The equivalent circuit for both operation stages is shown again in Figure 4.13.

Figure 4.13 – (a) First and (b) second operation stages of the HBSSC.



Source – Author.

From Figure 4.13, the state equations are obtained for the first operating stage, as shown in (4.37).

$$\begin{aligned}
L\frac{di_L}{dt} &= v_i - \left(r_L + \frac{r_1 r_3}{r_1+r_3}\right) i_L - v_{C_1}\frac{r_1}{r_1+r_3} + v_{C_2}\frac{r_1}{r_1+r_3} \\
C_1\frac{dv_{C1}}{dt} &= i_L\frac{r_1}{r_1+r_3} - v_{C_1}\frac{1}{r_1+r_3} + v_{C_2}\frac{1}{r_1+r_3} - (v_{C_1}+v_{C_3})\frac{1}{Z_o} \\
C_2\frac{dv_{C2}}{dt} &= -i_L\frac{r_1}{r_1+r_3} + v_{C_1}\frac{1}{r_1+r_3} - v_{C_2}\frac{1}{r_1+r_3} \\
C_3\frac{dv_{C3}}{dt} &= -(v_{C_1}+v_{C_3})\frac{1}{Z_o}
\end{aligned} \tag{4.37}$$

A similar analysis is performed for the second operating stage. The resulting equations are given by (4.38).

$$\begin{aligned}
L\frac{di_L}{dt} &= v_i - i_L\left(r_L + \frac{r_2 r_4}{r_2+r_4}\right) - v_{C_1} + v_{C_2}\frac{r_2}{r_2+r_4} - v_{C_3}\frac{r_2}{r_2+r_4} \\
C_1\frac{dv_{C1}}{dt} &= i_L - (v_{C_1}+v_{C_3})\frac{1}{Z_o} \\
C_2\frac{dv_{C2}}{dt} &= -i_L\frac{r_2}{r_2+r_4} - v_{C_2}\frac{1}{r_2+r_4} + v_{C_3}\frac{1}{r_2+r_4} \\
C_3\frac{dv_{C3}}{dt} &= i_L\frac{r_2}{r_2+r_4} + v_{C_2}\frac{1}{r_2+r_4} - v_{C_3}\frac{1}{r_2+r_4} - (v_{C_1}+v_{C_3})\frac{1}{Z_o}
\end{aligned} \tag{4.38}$$

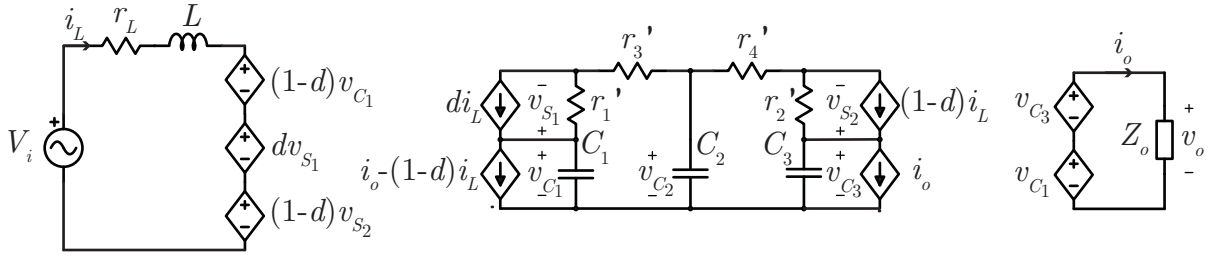
All the state variables and input voltage are time-varying. Thus, an conventional DC analysis would neglect the effect of the inductance and capacitances in steady state operation. Thus, the variables v_i, i_L, v_{C_1}, v_{C_2} and v_{C_3} are represented as dynamic phasors.

Thus, computing the averaged value of (4.37) and (4.38) leads to the averaging equations:

$$
\begin{aligned}
L\frac{d}{dt}\langle \boldsymbol{i_L}\rangle &= -j\omega_g L\langle \boldsymbol{i_L}\rangle + \langle \boldsymbol{v_i}\rangle - \langle \boldsymbol{i_L}\rangle\left(r_L + d\frac{r_1 r_3}{r_1+r_3} + (1-d)\frac{r_2 r_4}{r_2+r_4}\right) + \\
&\quad - \langle \boldsymbol{v_{C_1}}\rangle\left(1-d+d\frac{r_1}{r_1+r_3}\right) + \langle \boldsymbol{v_{C_2}}\rangle\left(d\frac{r_1}{r_1+r_3} + (1-d)\frac{r_2}{r_2+r_4}\right) + \\
&\quad - \langle \boldsymbol{v_{C_3}}\rangle(1-d)\frac{r_2}{r_2+r_4} \\
C_1\frac{d}{dt}\langle \boldsymbol{v_{C_1}}\rangle &= -j\omega_g C_1\langle \boldsymbol{v_{C_1}}\rangle + \langle \boldsymbol{i_L}\rangle\left(1-d+d\frac{r_1}{r_1+r_3}\right) - \langle \boldsymbol{v_{C_1}}\rangle d\frac{1}{r_1+r_3} + \langle \boldsymbol{v_{C_2}}\rangle d\frac{1}{r_1+r_3} + \\
&\quad - (\langle \boldsymbol{v_{C_1}}\rangle + \langle \boldsymbol{v_{C_3}}\rangle)\frac{1}{R_o+jX_o} \\
C_2\frac{d}{dt}\langle \boldsymbol{v_{C_2}}\rangle &= -j\omega_g C_2\langle \boldsymbol{v_{C_2}}\rangle - \langle \boldsymbol{i_L}\rangle\left(d\frac{r_1}{r_1+r_3} + (1-d)\frac{r_2}{r_2+r_4}\right) + \langle \boldsymbol{v_{C_1}}\rangle\frac{d}{r_1+r_3} + \\
&\quad - \langle \boldsymbol{v_{C_2}}\rangle\left(\frac{d}{r_1+r_3} + \frac{1-d}{r_2+r_4}\right) + \langle \boldsymbol{v_{C_3}}\rangle\frac{1-d}{r_2+r_4} \\
C_3\frac{d}{dt}\langle \boldsymbol{v_{C_3}}\rangle &= -j\omega_g C_3\langle \boldsymbol{v_{C_3}}\rangle + \langle \boldsymbol{i_L}\rangle(1-d)\frac{r_2}{r_2+r_4} + \langle \boldsymbol{v_{C_2}}\rangle\frac{1-d}{r_2+r_4} - \langle \boldsymbol{v_{C_3}}\rangle\frac{1-d}{r_2+r_4} + \\
&\quad - (\langle \boldsymbol{v_{C_1}}\rangle + \langle \boldsymbol{v_{C_3}}\rangle)\frac{1}{R_o+jX_o}.
\end{aligned}
\tag{4.39}
$$

From (4.39), it is possible to obtain an equivalent averaged model for the converter, as shown in Figure 4.14. As this model considers the conduction resistances, the representation of the converter is closer to the reality, giving a more accurate analysis of resonances, voltage gain and efficiency. Furthermore, it is also possible to obtain via simulation the voltage over each capacitor, that were considered to be equal in the ideal analysis.

Figure 4.14 – Averaged circuit model for the hybrid boost considering conduction resistances.



Source – Author.

The steady state response for the state variables are obtained from (4.39) when it is considered that all the variables are constant. Thus, the left side of the equations are null. As the response is quite large to be displayed, some simplifications are made. The capacitances C_1, C_2 and C_3 are considered equal to C. If the grid angular frequency is

zero (dc input), the solution for the output voltage is

$$\boldsymbol{v_o} = V_o = V_i \left(\frac{2}{1-D}\right) \left(\frac{R_o}{R_o + r_1 \frac{(1+D)^2}{D(1-D)^2} + r_2 \frac{1}{1-D} + r_3 \frac{1}{D} + r_4 \frac{1}{1-D} + r_L \frac{4}{(1-D)^2}} \right) \tag{4.40}$$

Thus, the equivalent series output resistance for the DC-DC converter is

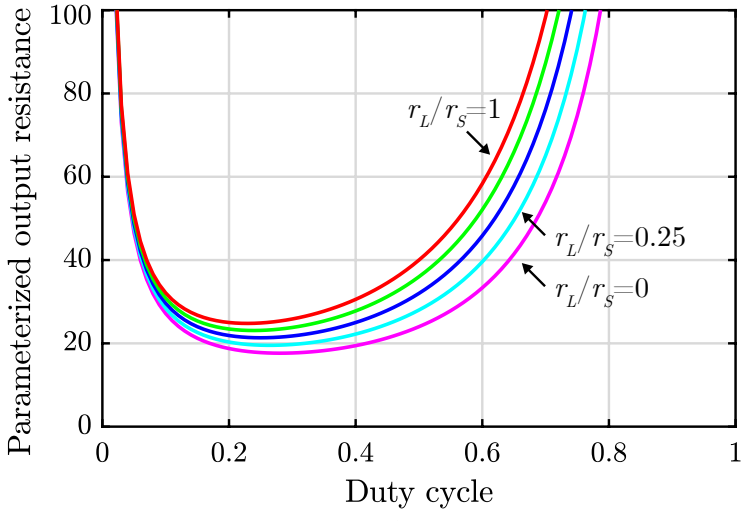
$$R_{out} = r_1 \frac{(1+D)^2}{D(1-D)^2} + r_2 \frac{1}{1-D} + r_3 \frac{1}{D} + r_4 \frac{1}{1-D} + r_L \frac{4}{(1-D)^2}. \tag{4.41}$$

If all the switches resistances are equal to r_s, then a parameterized output series resistance is obtained from 4.41:

$$\overline{R_o} = \frac{R_{out}}{r_s} = \frac{2(1+D)}{D(1-D)^2} + \frac{4}{(1-D)^2} \frac{r_L}{r_s}. \tag{4.42}$$

Figure 4.15 shows the output resistance variation for a duty cycle range from 0 to 1 and a variation on the relation of r_L/r_s from 0 to 1. It is observed that the minimum output resistance occurs at $d = 0.28$ when r_L is neglected. When r_L increases, the lowest output resistance point is at lower duty cycles.

Figure 4.15 – Parameterized output resistance.



Source – Author.

It should be noted that the output equivalent output resistance from the hybrid converter (Figure 4.15) is significantly different from the ladder (or also from the unitary) cell (Figure 2.12). As the ladder cell operates in open loop with a fixed gain, the duty cycle can be fixed in 0.5, which results in the smaller output resistance. In the case of the hybrid converter, the voltage gain depends on the duty cycle, thus it is not always possible

to adjust the duty cycle value in order to obtain the smaller output resistance. It means that the design should consider this topology for applications in which the duty cycle is limited between 0.1 and 0.6. Outside this operating range, the conduction losses would sharply increase.

4.5 DYNAMIC MODELING

An additional feature of the hybrid converters in relation to pure switched capacitor cells is the controllability via duty cycle. This section shows the control-oriented dynamic analysis of the hybrid boost AC-AC converter.

The state equations were obtained in (4.39) for the Hybrid Boost Switched Capacitor Converter. In order to determine the dynamics of the converter based on input and output variations, a small signal analysis will be performed. Then, consider that a variable x is composed by a steady-state value X plus a small variation $\tilde{x}$:

$$x = X + \tilde{x} \tag{4.43}$$

Applying (4.43) in (4.39), neglecting the steady-state components and multiplication of two small variations, a linear system is obtained. Thus, applying Laplace transform it is possible to obtain the transfer functions that relate the output voltage with the duty cycle. The result is very extensive when the grid frequency and conduction resistances are considered. For a simple analysis, the transfer function, neglecting the conduction resistances and for a DC input voltage is:

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_i\left(-\frac{8L}{(1-D)^2}s + 2R_o\right)}{3R_oLCs^2 + 4Ls + (1-D)^2R_o}. \tag{4.44}$$

It is observed a second-order transfer function and there is a zero in the right half-plane. The bode diagrams of the transfer function (4.44) and of the obtained transfer function considering the non-idealities are presented in Figure 4.16. It should be noted that the resonant frequency value is between 900 Hz and 1 kHz, and the model which considers the non-idealities shows a smaller peak value in the resonant area when compared to the ideal model. For low frequencies, the magnitude and phase of the transfer function are approximately constant.

The validation was performed via simulation for three cases: neglecting resistances (4.44), considering resistances in no-charge mode and considering resistances in partial-charge mode. The results are shown in Figure 4.17. It can be seen that the ideal model present a more oscillatory response and a DC error. The models which consider the resistances have shown similar results compared to the switched model.

Figure 4.16 – Bode diagram of the transfer function between output voltage and duty cycle.

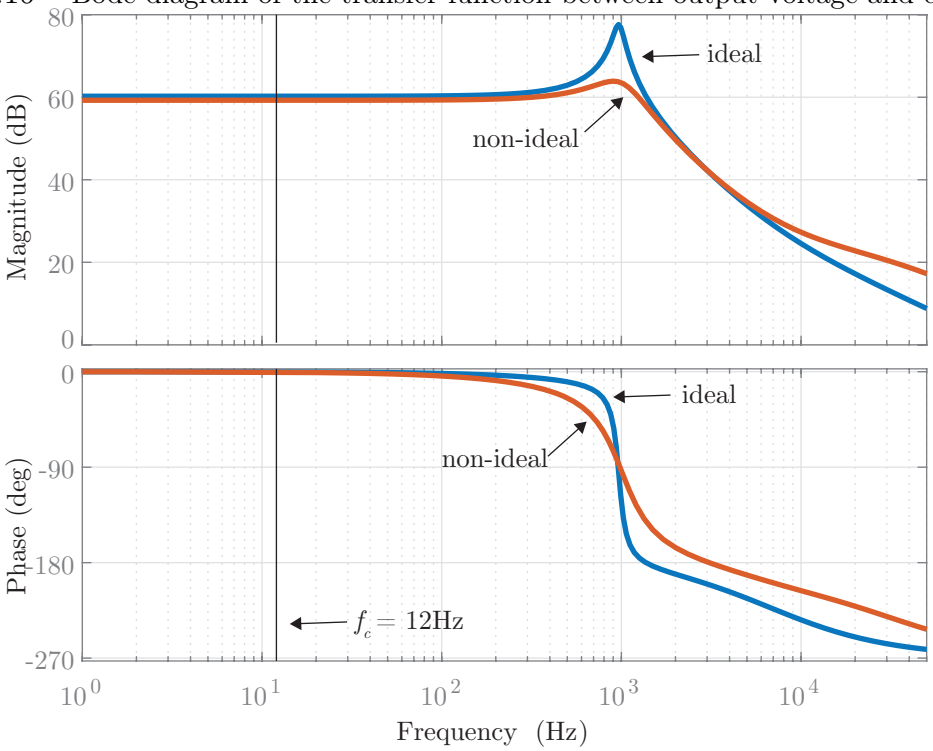


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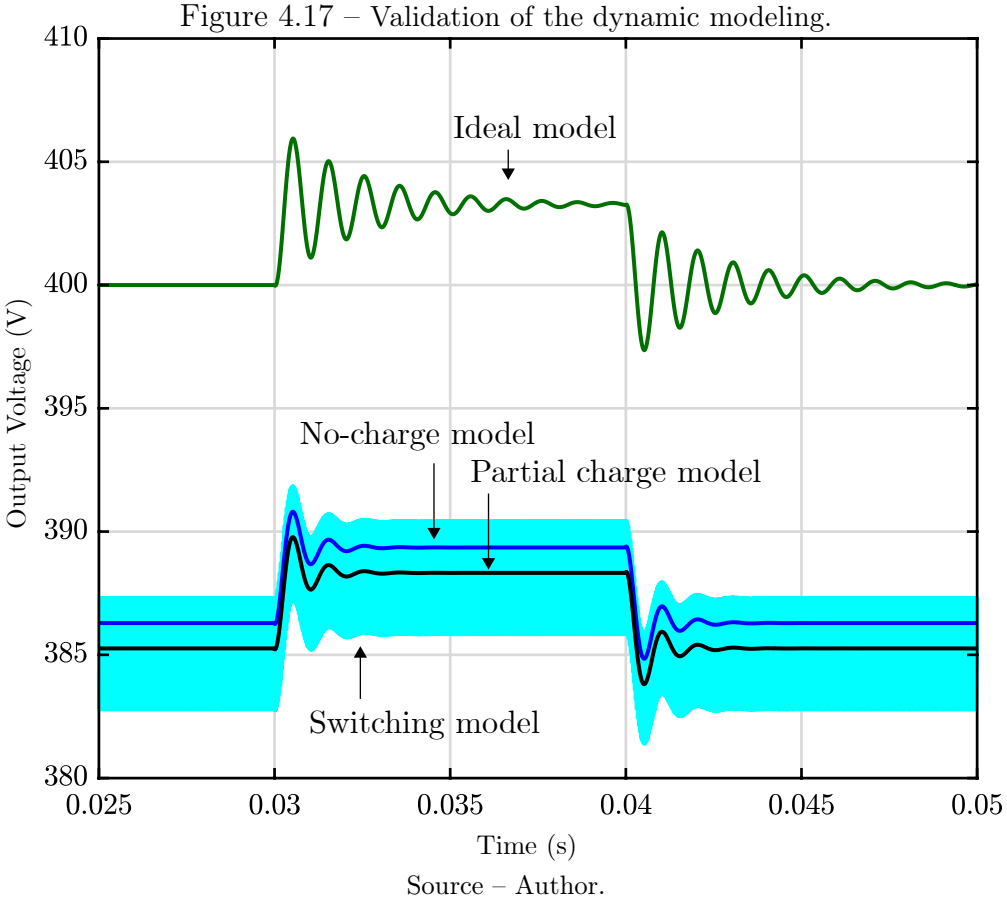
Figure 4.17 – Validation of the dynamic modeling.



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4.6 DESIGN METHODOLOGY

In order to validate the theoretical analysis, a single-phase prototype of the AC-AC hybrid boost switched capacitor was built. This sections presents a design methodology of this structure. The specifications are described in Table 4.4, in which two possibilities are considered: 55/220 V and 110/400 V voltage conversion. This values were chosen based on the most common grid voltages and, in addition, 127 V could be used instead of 110 V and 440 V instead of 400 V. Considering that the resonant frequency is much higher than the grid frequency, the output voltage gain for an input frequency of 60 Hz can be approximated to the DC gain. Thus, the equation for determining the duty cycle is

$$d = 1 - 2\frac{V_i}{V_o}, \tag{4.45}$$

which results in 0.45 and 0.5 for 110/400 V and 55/220 V operating points, respectively. The start-up of this converter could be achieved by measuring the input voltage and starting the converter during the voltage zero crossing.

Table 4.4 – Project specifications.

Parameter	Symbol	Value
Input voltage	V_i	55/110 V
Output voltage	V_o	220/400 V
Rated power	S_o	1/2 kVA
Minimum input power factor	$PF_{i.min}$	0.92
Grid frequency	f_g	60 Hz
Switching frequency	f_s	100 kHz
Input current ripple	$\Delta I_{L\%}$	20%
Output voltage ripple	$\Delta V_{o\%}$	2%

Source – Author.

4.6.1 Inductance

The input inductance is designed in order to maintain a low input current ripple. During the first operation stage, at the peak grid voltage value, the current ripple is computed by:

$$\Delta I_L = \frac{V_{ip} D}{L f_s}. \tag{4.46}$$

Isolating the inductance L and writing the equation in terms of output active power, input power factor and voltages yields

$$L = \frac{D V_i^2 PF_i}{f_s P_o \Delta I_{L\%}}. \tag{4.47}$$

The inductance value is then determined for the worst case, when the input power factor is unitary, and its value resulted in 136 μH. Some important facts to note from (4.47): the input inductance increases with the square of the input voltage, while it diminishes for higher switching frequencies and processed power. A parameter that is defined is the current ripple, which leads to a trade-off between the size of the inductor and the current's ripple, which increases inductor losses and the THD of the input current.

4.6.2 Capacitors

The design of capacitor values must satisfy some conditions, which are hereafter described:

Input power factor: The converter operates with a low frequency input voltage. This results in reactive currents because of the three capacitors. Then, given a minimum input power factor requirement, there is a maximum value of capacitance that is suitable.

The input active and reactive power are defined as

$$\begin{aligned} P_i &= P_o + P_d \\ Q_i &= Q_L + Q_o - Q_C, \end{aligned} \tag{4.48}$$

where P_i is the input active power, P_o the output active power and P_d the converter losses. Q_i, Q_L, Q_C and Q_o represent the input, the inductor, the capacitors and the output reactive powers, respectively. The input power factor is described as:

$$FP_i = cos(\phi_i) = cos\left(atan\left(\frac{|Q_L + Q_o - Q_C|}{P_o + P_d}\right)\right). \tag{4.49}$$

Substituting the input current in terms of input active power, power factor and input voltage, as well as writing Q_o in terms of output active power and power factor leads to the maximum value of capacitance for a minimum input power factor:

$$C_{eq} = \frac{1}{\omega_g V_o^2}\left[\frac{P_i}{FP_i V_i}^2 \omega_g L + P_o\frac{\sqrt{1-FP_o^2}}{FP_o} \pm (P_o + P_d)\frac{\sqrt{1-FP_i^2}}{FP_i}\right]. \tag{4.50}$$

Then, the sum of capacitances must be lower than the calculated value of C_{eq}:

$$C_1 + C_2 + C_3 \leq 4C_{eq}. \tag{4.51}$$

Interesting facts are that the capacitances are limited to a maximum value, because an increase in the capacitances leads to high reactive power flow in the converter and consequently increased losses.

Charging mode: The capacitance values must be chosen, along with the frequency,

in order that the converter operates in the partial or no charge mode, granting low effective and peak current values. Assuming an operation in the partial-charge mode, in which neither the value of capacitances nor the peak currents are high, the time constants should respect the following relation:

$$\tau \geq \frac{dT_s}{2}. \tag{4.52}$$

Looking at the two time constants, the following relations must be satisfied:

$$\begin{aligned} \frac{C_1 C_2}{C_1 + C_2} &\geq \frac{d}{2(r_1 + r_3) f_s} \\ \frac{C_2 C_3}{C_2 + C_3} &\geq \frac{(1-d)}{2(r_2 + r_4) f_s}. \end{aligned} \tag{4.53}$$

Output voltage ripple: Capacitors that are connected to the load must have a capacitance value that ensures a low output voltage ripple. It can be described by

$$\Delta V_o = \frac{q_{C1}}{C_1} + \frac{q_{C3}}{C_3}. \tag{4.54}$$

For equal capacitances, the minimum value of capacitance that satisfy the output voltage ripple condition is:

$$C_{1,min} = C_{3,min} = \frac{(1+2d)P_o}{\Delta V_{o\%} f_s P F_o V_{oef}^2} \tag{4.55}$$

If they are set to be different, but presenting the same voltage ripple, the following equations are obtained:

$$C_{1,min} = \frac{2P_o(1+d)}{\Delta V_{o\%} f_s P F_o V_o^2} \tag{4.56}$$

$$C_{3,min} = \frac{2dP_o}{\Delta V_{o\%} f_s P F_o V_o^2}. \tag{4.57}$$

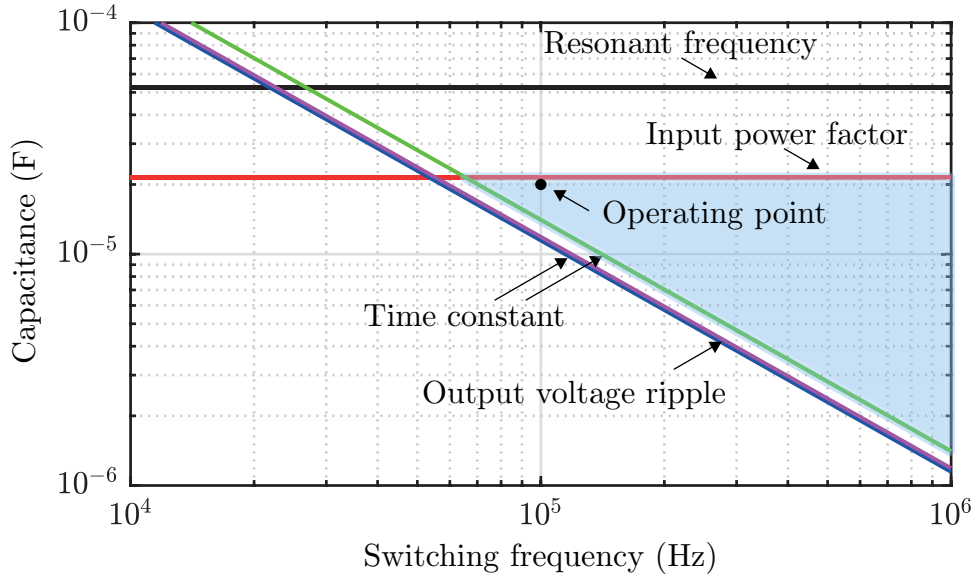
Resonant frequency: An obtained result from the ideal analysis is the existence of a resonant frequency, given by (4.12). In order to guarantee an operation without influence of the resonant frequency, the capacitance is limited to

$$C \leq \frac{(1-d)^2}{4\pi^2 f_{ress}^2 3L}, \tag{4.58}$$

where the resonant frequency f_{ress} can be chosen at least ten times the grid frequency. Figure 4.18 shows the five conditions for the capacitances. The resonant frequency and input power factor restrictions limit the upper values for a grid frequency equal to 60 Hz, while the time constant and output voltage ripple limit the minimum capacitance values. For operation at 60 Hz, the coloured area is the one which satisfies all the conditions.

Regarding capacitance values, a high switching frequency would be the best choice. For this project, three 20 μF capacitors and an 100 kHz switching frequency were employed.

Figure 4.18 – Capacitor design based on the grid and switching frequencies.

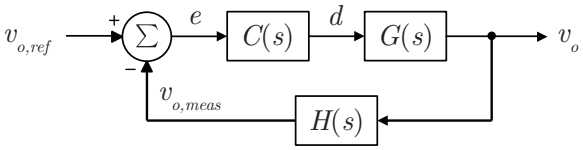


Source – Author.

4.7 OUTPUT VOLTAGE CONTROL

The voltage control diagram is shown in Figure 4.19, where the transfer funcions $C(s)$, $G(s)$ and $H(s)$ are related to the controller, system and measurement dynamics, respectively.

Figure 4.19 – Closed-loop control diagram.



Source – Author.

As the converter operates with a constant duty cycle and in continuous conduction mode, it presents a good output voltage regulation. Because of this, it is was chosen to perform only the control of the output voltage peak value, given that the waveform automatically follows the input voltage. Thus, as the controlled variable (peak voltage) changes only twice during a grid period, its equivalent frequency is 120 Hz. Thus, the chosen cross frequency is at one tenth of the equivalent frequency, resulting in $f_c = 12$ Hz. As the peak value is a constant value, a PI controller can be employed, because it guarantees zero error in steady state operation. The transfer function of a PI controller is

given by

$$C(s) = k_v \left(\frac{s + \omega_z}{s} \right). \tag{4.59}$$

This control project does not consider the dynamic interference from the voltage sensor, signal conditioning circuit, analog-digital converter and signal processing, because the frequencies related to these dynamics are much higher than the control band. In order to achieve a desirable phase margin PM and cross frequency f_c ($\omega_c = 2\pi f_c$), the parameters ω_z and k_c can be computed respectively as

$$\omega_z = \frac{\omega_c}{tan\left(PM - \frac{\pi}{2} - arg(G_{vd}(\omega_C))\right)} \tag{4.60}$$

and

$$k_c = \frac{\omega_c}{\sqrt{\omega_z^2 + \omega_c^2}|G_{vd}(\omega_c)|}, \tag{4.61}$$

where k_c is the product of the gains related to the controller k_v, voltage sensor k_{vs}, signal conditioning circuit k_{sig}, analog-digital converter k_{adc} and modulator k_{pwm}. Thus the controller gain k_v is obtained by

$$k_v = \frac{k_c}{k_{vs} k_{sig} k_{adc} k_{pwm}}, \tag{4.62}$$

and the results are shown in Table 4.5.

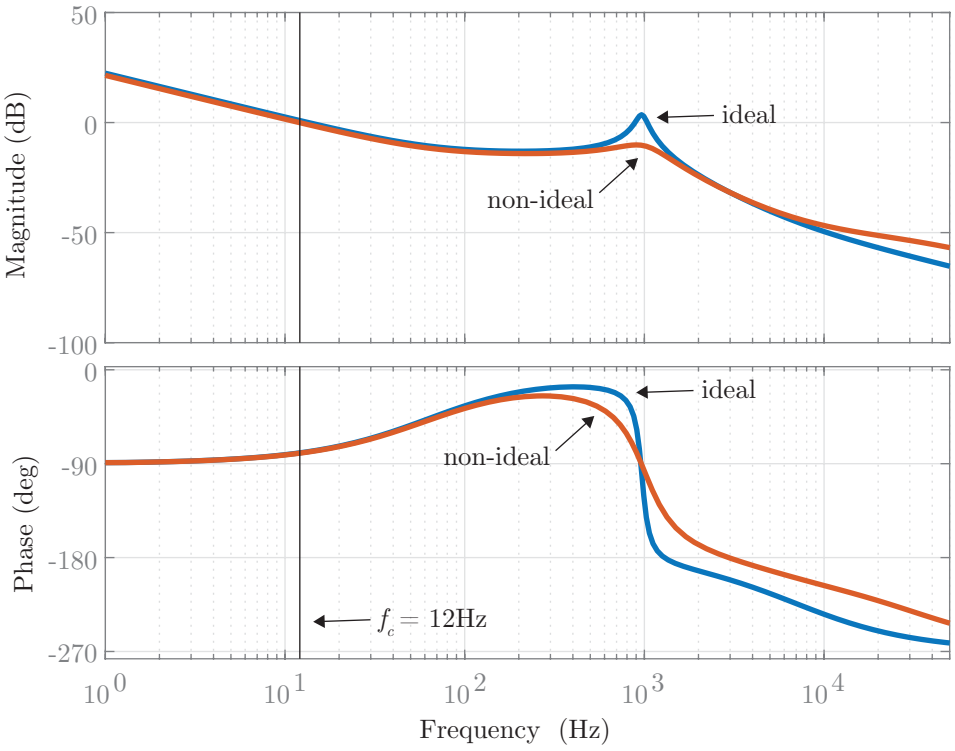
Table 4.5 – Control parameters

Parameter	Symbol	Value
Phase margin	PM	100°
Cross frequency	f_c	12 Hz
Total loop gain	k_l	$2{\cdot}10^{-4}$
Voltage sensor gain	k_{vs}	$3.68{\cdot}10^{-5}$
Analog gain	k_{sig}	130
ADC gain	k_{adc}	1241
Modulator gain	k_{pwm}	$3.33{\cdot}10^{-3}$
Controller gain	k_c	0.00982
Time constant	T_i	2.45 ms

Source – Author.

The bode diagram of the compensated open loop transfer function $G(s)H(s)C(s)$ is depicted in Figure 4.20. It is observed that the cross frequency in 0 dB is at 12 Hz and the respective phase is -100°, which corresponds to a phase margin of 80°. Then, the controller project is validated.

Figure 4.20 – Bode diagram of the compensated open loop transfer function.



Source – Author.

4.8 VOLTAGE AND CURRENT STRESSES

In order to choose semiconductors and capacitors some specifications must be considered: (i) maximum voltage, (ii) effective current values and (iii) switching frequency. A conclusion of the previous analysis is that the maximum voltage over the semiconductors and capacitor is equal to half of output voltage peak value, which corresponds to 283 V. Based on the previous studies and on the availability, the chosen components for the prototype are listed in Table 4.6. In order to reduce the conduction losses, two four-quadrant switches connected in parallel were employed as switch S_1, resulting in the use of 4 MOSFETs. Switches S_2, S_3 and S_4 employ only one four-quadrant switch.

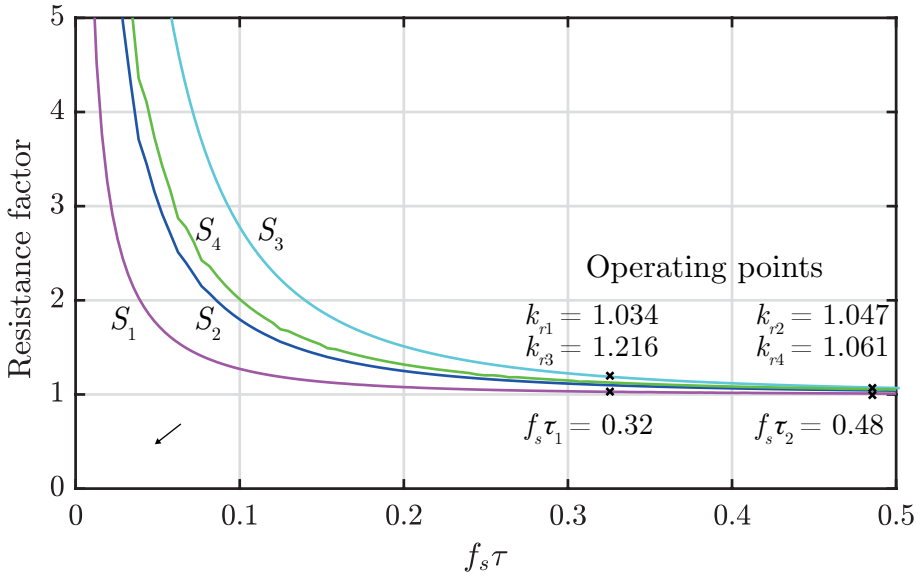
Table 4.6 – Component list.

Device	Description	Quantity
Input inductor	APH46P60 - 136 μH	1
Switches S_1	SCT3080AL - 650 V / 80 mΩ	4
Switches S_2, S_3, S_4	SCT2120AF - 650 V / 120 mΩ	6
Capacitors	600 V / 20 μF	4
Voltage sensor	LV25P	1
Diode (Clamping)	MUR160	8
Capacitor (Clamping)	630 V / 1 μF	4
Resistor (Clamping)	48 kΩ	4

Source – Author.

The conduction resistances of the MOSFETs are equal to 80 mΩ in S_1. Thus, the resistance of each four-quadrant switch is equal to 160 mΩ. As there are two switches connected in parallel, the resultant resistance for S_1 is 80 mΩ. In case of S_2, S_3 and S_4, the MOSFETs conduction resistances are equal to 120 mΩ. Then, the resistance of these four-quadrant switches are equal to 240 mΩ. Figure 4.21 presents the resistance factors for all four switches and the operating points considering a switching frequency of 100 kHz and capacitance values of 20 μF. From this graphic it is observed that the losses in switch S_3 are more sensible to the switching frequency, increasing in 21.6% in comparison with the ideal operating mode (no-charge). The conduction losses in S_1 increase only 3.4%, because most part of its current is from the input inductor, which presents a small ripple.

Figure 4.21 – Resistance factor as a function of $f_s\tau$ for switches S_1, S_2, S_3 and S_4.



Source – Author.

After determining the capacitance values, the current stresses can be calculated. Table 4.7 shows the theoretical and simulated values for current stresses considering the prototype parameters. The comparison with simulated results validate the theoretical analysis of effective current values. As it can be seen, the currents in switches S_1 are higher than the other switches, which justifies the use of MOSFETs parallel connections.

4.9 EFFICIENCY

The efficiency of switched capacitor converters usually differ from conventional topologies, specially regarding the switching frequency. Thus, considering the chosen components, theoretical efficiency curves were obtained for 55/110 V, 1 kW and 110/400 V, 2 kW operating points for different frequencies. The curves are depicted in Figure 4.22. The lower efficiencies for low frequencies are due the exponential characteristic of the currents, whose effective and peak values increase at lower switching frequencies. Also, the

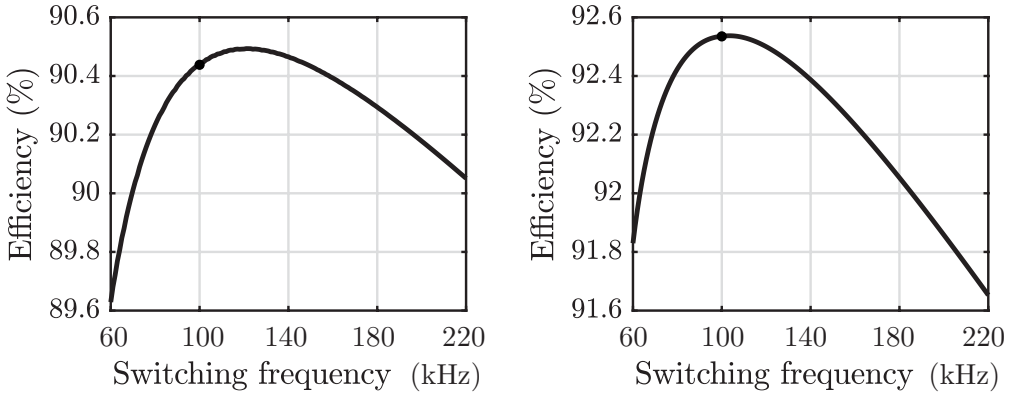
Table 4.7 – Theoretical and simulated values of current stresses.

Variable	Theoretical (A)	Simulated (A)	Error (%)
$I_{L,ef}$	19.96	19.90	-0.30
$I_{S_1,ef}$	22.43	22.60	0.76
$I_{S_2,ef}$	8.026	7.99	-0.45
$I_{S_3,ef}$	9.607	10.21	6.28
$I_{S_4,ef}$	7.252	7.38	1.77
$I_{C_1,ef}$	16.92	17.22	1.77
$I_{C_2,ef}$	12.04	12.63	4.90
$I_{C_3,ef}$	5.253	5.54	5.46

Source – Author.

efficiency is diminished for higher frequencies because of the increased switching losses. For operation as 55/220 V converter the highest efficiency is around 120 kHz, whereas for 110/400 V the maximum point is at 105 kHz. It should be noted that these results would be different if other devices were employed, for example MOSFETs with faster turn-on and turn-off dynamics or lower conduction resistances.

Figure 4.22 – Theoretical efficiency of hybrid converter for different frequencies. (a) 55/220 V 1kW and (b) 110/400 V 2kW operating points.

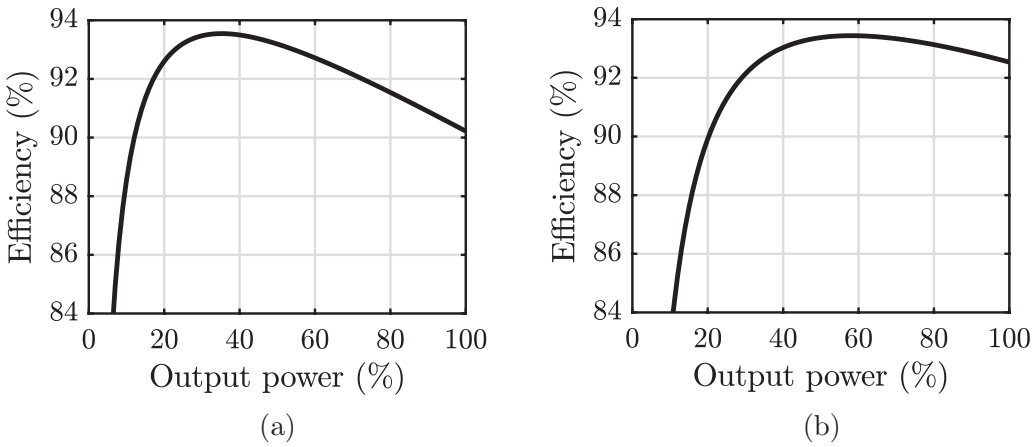


Source – Author.

Efficiency curves for different output power levels are displayed in Figure 4.23(a) for 55/220 V and in Figure 4.23(b) for 110/400 V voltage conversions. The efficiencies are attenuated for light loads, mainly because the reactive currents overweight the active components, as well as the voltage-dependent switching losses. For 55/220 V operation, the current levels are higher compared to the processed power. Thus, its efficiency tends to be lower than the converter in 110/400 V operation.

Theoretical losses distributions are shown in Figure 4.24(a) for 55/220 V and in Figure 4.24(b) for 110/400 V operating points. It is noticed that almost the half of losses are due the switch S_1, which is the integrating component from the boost and the ladder

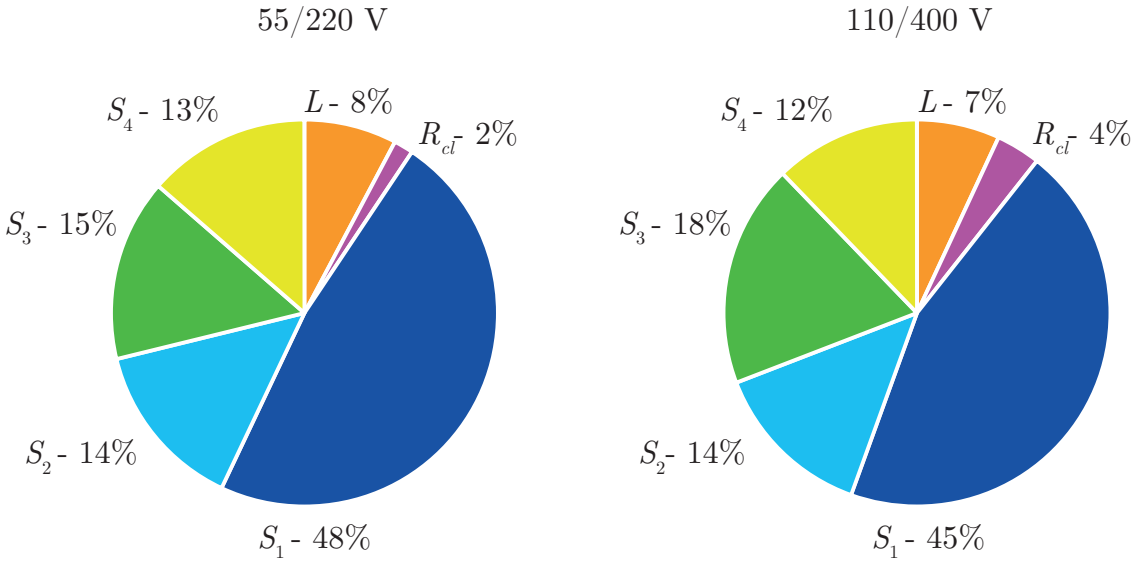
Figure 4.23 – Theoretical efficiency of hybrid converter for different output power levels. (a) 55/220 V and (b) 110/400 V operating points.



Source – Author.

converters. Comparing the operating points, it is observed that the voltage clamping increases its losses participation at higher voltage levels.

Figure 4.24 – Theoretical losses distributions in AC-AC hybrid boost switched capacitor converter.



Source – Author.

4.10 CONCLUSION

This chapter adressed the proposed topology and its operating modes. An ideal analysis was performed, in order to obtain a simple mathematical description of the converter and an equivalent averaged model. The analysis considering the non-idealities was also accomplished, obtaining a more accurate and complex model. The dynamic modeling

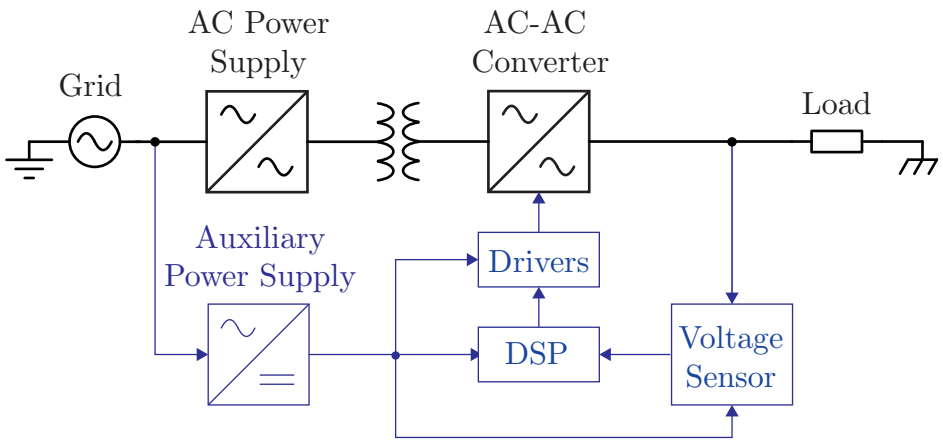
was presented, and the main equation projects have been explained. The conclusions of the analysis and design of the HBSCC are:

- The voltage gain characteristics are similar to the boost converter, with a magnitude multiplied by two;
- The voltage stresses over the semiconductor devices and capacitors are equal to half of the output voltage peak value;
- The voltage over the capacitors are balanced without any external control;
- An integration with a laddel cell increases the reactive power of the converter when compared to the conventional boost converter;
- The equivalent output resistance characteristic differs from the ladder cell, with a minimum point at lower values of duty cycle;
- As a pure switched capacitor converter, the partial charge operating mode leads to higher effective current values through the switches and capacitors;
- The output voltage peak value control has a slow dynamic and can be regulated by using a PI controller;
- Specifications regarding grid and switching frequencies limit the possible values of switching frequency and capacitances;
- Differently to conventional converters, a decrease in the switching frequency results in lower values of efficiency.

5 RESULTS

Experimental tests were performed in order to validate the theoretical analysis of the single phase hybrid boost switched-capacitor AC-AC converter. The tests were carried out mainly for a 60 Hz grid frequency at two different voltage conversion ratios: 55/220 V and 110/400 V for 1 kW and 2 kW rated output power (unitary power factor), respectively. Additional operating points were verified at lower power levels regarding grid and switching frequencies, output loads and input/output connections. The modified modulation schema (from chapter 3) was employed in all tests, with a voltage limit equal to 20 V, which corresponds to $\alpha = 3.68°$ and $\alpha = 2.03°$ for 220 V and 400 V output voltages, respectively. The diagram of the experimental setup is shown in Figure 5.1.

Figure 5.1 – Simplified diagram of the experimental setup.



Source – Author.

Table 5.1 lists the main devices which were employed during the tests. Some tests were limited because of the AC voltage source, which has a rated apparent power of 1750 VA and a maximum output current of 13 A. Thus, an isolating transformer was employed to double the output current of the voltage source. The output voltage control is performed using a microcontroller.

Table 5.1 – Device specifications.

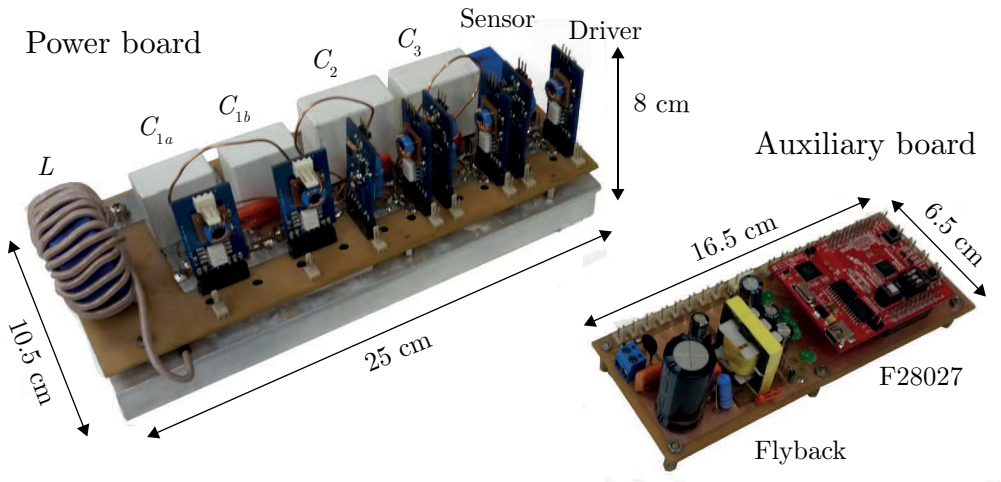
Device	Description
AC power supply	Agilent 6813B
Isolating transformer	220/110 V 5 kVA
Wattmeter	Yokogawa WT500
Oscilloscope	Tektronix DPO 5034/5054
Microcontroller	Texas Instruments TMS320F28027

Source – Author.

A photograph of the prototype is displayed in Figure 5.2 and it is composed by two circuit boards. The power board, on the left, contains the power components (inductor,

MOSFETs and capacitors), the driver boards and the voltage sensor. The calculated power densities for this board are 1.48 kW/kg and 0.95 kW/L. An auxiliary board, on the right, consists of: (i) an auxiliary isolated power supply (flyback converter), which provides energy to the drivers, signal conditioning circuit, voltage sensor and microcontroller; (ii) the signal conditioning circuit, which converts the output signal from the voltage sensor into an input signal for the analog-digital converter in microcontroller and (iii) the connections for the microcontroller, including the power supply, input and output ports and an output buffer for the signal commands, which are sent to the drivers. The schematics and PCB layout are presented in appendix C.

Figure 5.2 – Photograph of the prototype.



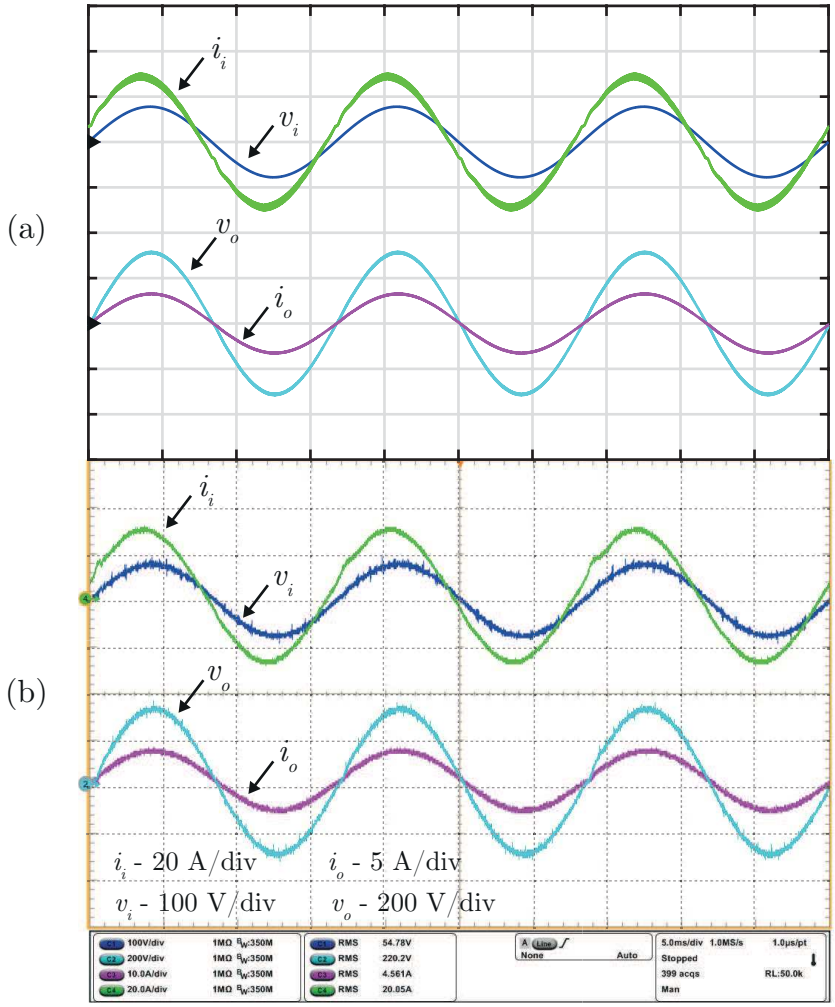
Source – Author.

5.1 55/220 V OPERATING POINT

Figure 5.3 shows the input and output currents and voltages for a 55 V/ 60 Hz input and an 1 kW, unitary power factor load. It can be noticed that all the currents and voltages waveforms are sinusoidal. Even though the output power factor is unitary, the input power factor is slightly capacitive, because the capacitors process higher reactive power levels than the input inductor.

It is observed a small distortion in the input current when the voltages cross the zero. That is possibly a result from the change of modulation, when the traditional modulation schema is employed and the voltage clamping circuits conduct the input current during the dead time. The voltage limit set for this test was 20 V. For smaller voltages, it was noticed that sometimes a short circuit occurred, activating the protection of the input voltage source. It was also observed that, for smaller processed power, the distortions are proportionally higher, leading to an increase in the input current THD. However, other variables appear to suffer lower influence from the voltage clamping circuit.

Figure 5.3 – Simulation (a) and experimental (b) results for input and output voltages and currents. Time scale: 5 ms/div.

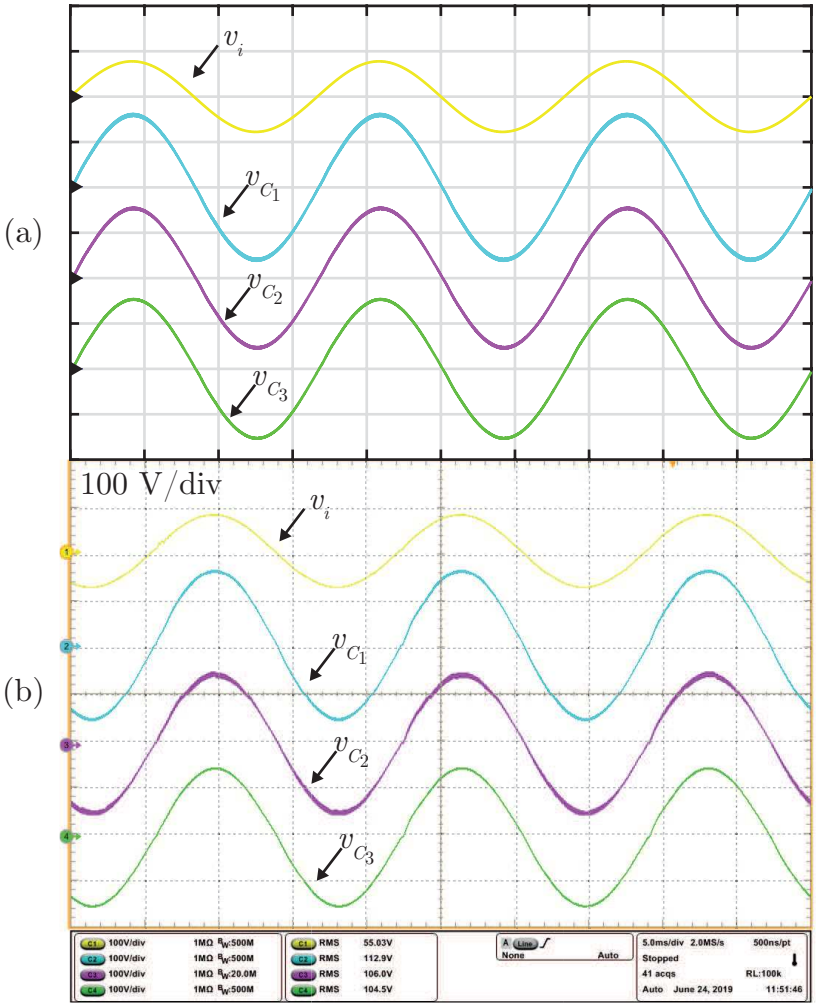


Source – Author.

The voltage balance among capacitors on the ladder cell is shown in Fig 5.4. The effective value of the voltage over each capacitor is about 110 V with peak values of 160 V, which confirms the consideration that the voltage stresses over the capacitors are equal to half of output voltage. This balance is obtained without using any control strategy. Moreover, it allows the connection of different loads at different output ports, resulting in a multi-port system. An addition of more switched-capacitor cells would lead to even higher output voltages with the same voltage stresses over the devices, being the conduction losses a practical limitation.

Waveforms for currents through the switches S_1 and S_2 are depicted in Figure 5.5. In Figure 5.5(a), the low-frequency components are displayed. It is noted that the currents present a sinusoidal envelope. Even though there are two parallel connected switches in S_1, the current through one of them is still higher than the currents over switch S_2. Details of the waveforms during some switching periods are shown in Figure 5.5(b). The current through S_1 was measured only for one of the parallel connected MOSFET. It

Figure 5.4 – Simulation (a) and experimental (b) results for voltages over the capacitors C_{in}, C_1, C_2 and C_3. Time scale: 5 ms/div.



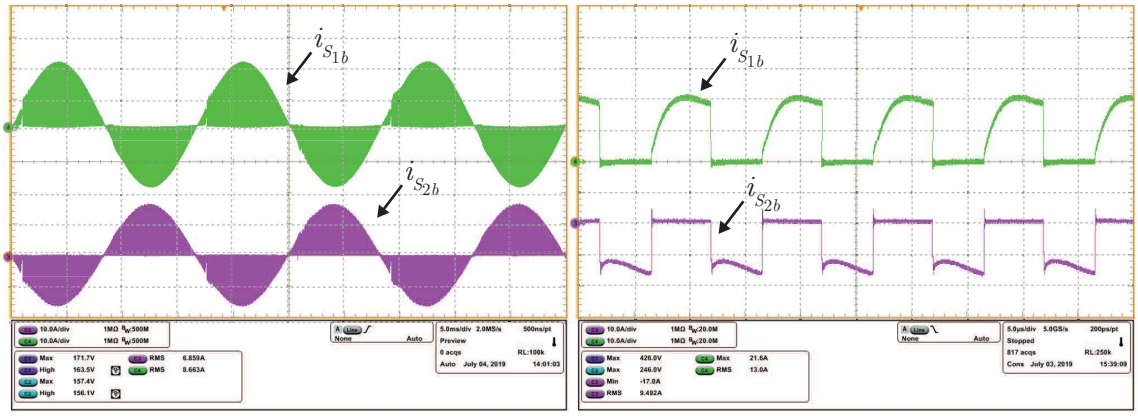
Source – Author.

might explain the slow turn-on transition, because a measurement loop was introduced in the path of only one MOSFET. Thus, its leakage inductance increased in comparison to the parallel connected switch. Also, the influence of the additional loop might have lead to smaller measured peak values of the currents. The reason for this is that the switched capacitor is now composed of a RLC loop instead of only RC, which results in a second order transitory response. It is noted that the switches conduct complementary with a duty cycle value of 0.55, which was increased in comparison with the theoretical value (0.5) due the non-idealities.

The voltages over the switches S_{1a} and S_{1b} are displayed in Figure 5.6. It is observed that either S_{1a} or S_{1b} blocks the voltage over the capacitor C_1 during the first operating stage, depending on the output voltage polarity. It is also noticed a voltage spike during the zero-crossing, because the voltage clamping circuit operates and limits the voltage.

The voltages over the switches S_{1b} and S_{2b} are displayed in Figure 5.7. Both switches

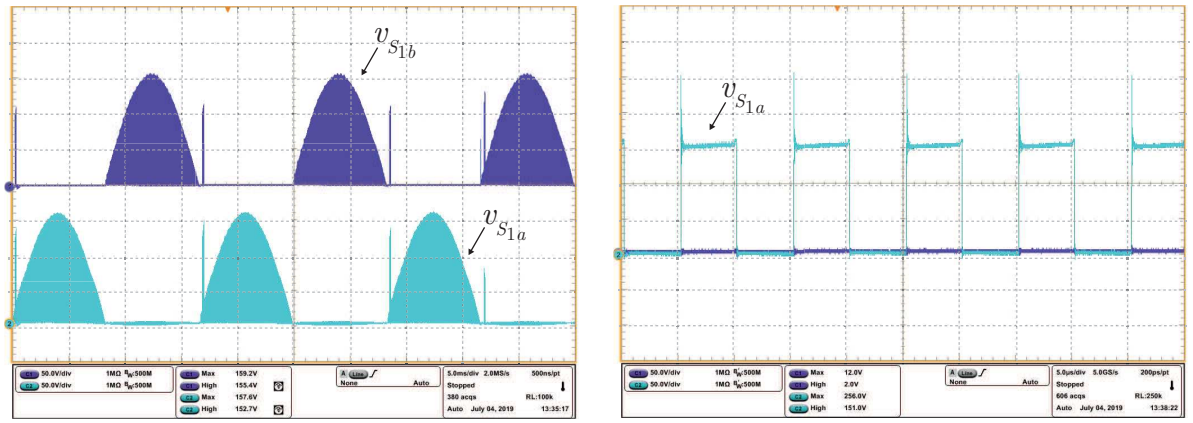
Figure 5.5 – Experimental results for currents through switches (green - S_1, purple - S_2) during three grid (a) and five switching periods (b). Scale = 10 A/div. Time scales: 5 ms/div (a) and 5 μs/div (b).



(a) (b)

Source – Author.

Figure 5.6 – Experimental results for voltages over switches S_{1a} and S_{1b} during three grid (a) and five switching periods (b). Scale = 50 V/div. Time scales: 5 ms/div (a) and 5 μs/div (b).



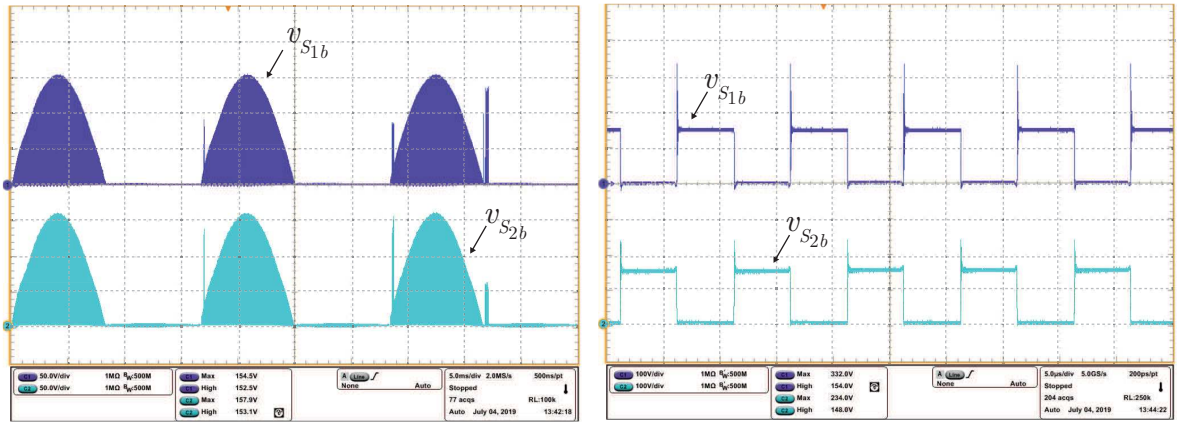
(a) (b)

Source – Author.

are blocked during the same half cycle, but in a complementary way in a switching period. The maximum blocked voltage is equal to half of the peak output voltage. Moreover, when the output voltage is negative, the switches still receive command signal and conduct both through the channel and the intrinsic diode. This leads to conduction losses, whereas the switching losses are zero (given that at the negative half cycle the blocked voltage is null). Some voltage spikes were measured during each switching period, but they are results of the measurement loops, and they were significantly reduced when these loops were removed.

Another important current to be measured was through the switched capacitor C_2.

Figure 5.7 – Experimental results for voltages over switches S_{1b} and S_{2b} during (a) three grid (Scale = 50 V/div) and (b) five switching periods. Scale = 100 V/div. Time scales: 5 ms/div (a) and 5 μs/div (b).

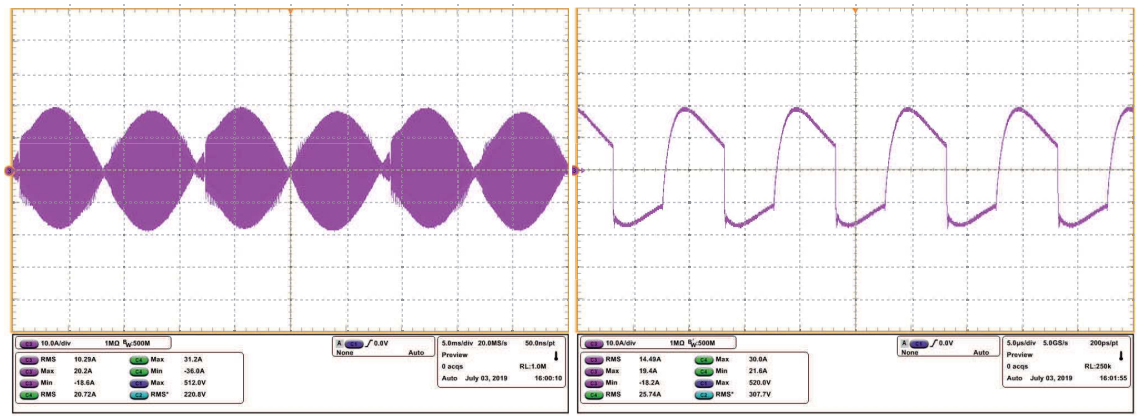


(a) (b)

Source – Author.

It also gives an idea of the currents through switches S_3 and S_4. The collected data for this current in a low-frequency scale is depicted in Figure 5.8(a). It can be noted that is shape is sinusoidal an its peak value is about 19 A, with an effective value of 10.1 A. A detail on the current during a switching period is shown in Figure 5.8(b) An special attention is given for the waveform, which appears to be a second-order response. This is possibly due to the increased loop inductance caused by the insertion of a measurement wire.

Figure 5.8 – Experimental results for the current through the switched capacitor C_2 during (a) three grid periods and (b) five switching periods. Scale = 10 A/div. Time scales: 5 ms/div (a) and 5 μs/div (b).



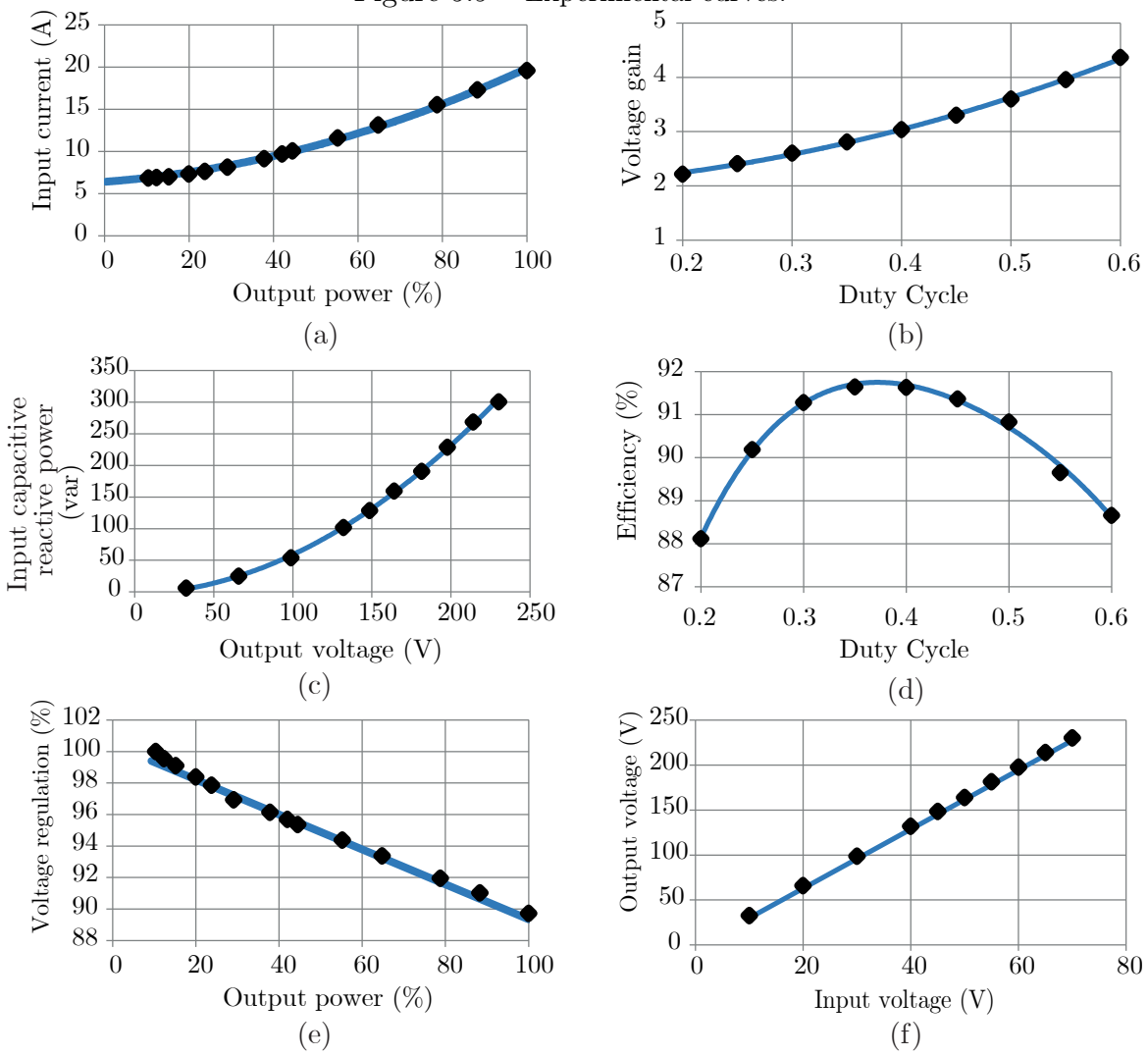
(a) (b)

Source – Author.

The experimental measurements of the input current are shown in Figure 5.9(a). It can be divided in two areas: for low power, it reaches a fixed value, related to the no-load

reactive power. At high power levels, the active power is much higher than the reactive, thus the input current value increases linearly with the output power.

Figure 5.9 – Experimental curves.



Source – Author.

Figure 5.9(b) provides the experimental results of the correlation between voltage gain and the duty cycle. As expected, the voltage gain increases in a non-linear tendency with the duty cycle. An important operation point is at D = 0.56, which implies in a voltage gain of 4, allowing the operation as a 55 V/220 V voltage converter.

Another result obtained was the input reactive power when operating with a resistive load equal to 52 Ω. The collected data is displayed in a graphic from Figure 5.9(c). It is observed a quadratic variation of the reactive capacitive input power with the output voltage. The result was also expected, given the reactive power on the capacitors overweights the reactive power related to the input inductor.

Efficiencyiy tests were performed by duty cycle variations. Figure 5.9(d) presents the results for a 1 kW/ 220 V output characteristic. It can be observed that extreme values

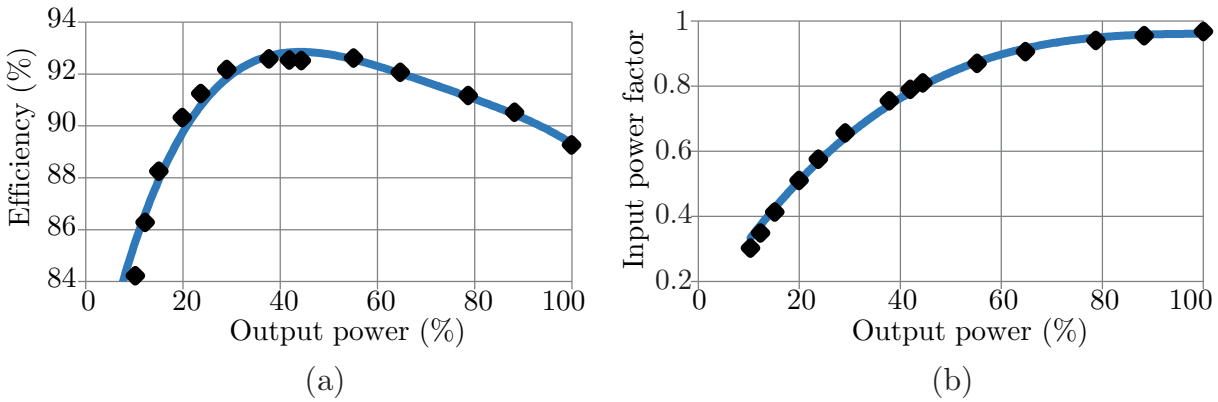
of duty cycle decreases the efficiency. In fact, an increase on the duty cycle leads to a higher voltage gain and input current. Thus, the losses on the input devices (inductor and switch S_1) are more significant, decreasing the overall efficiency. On the other side, the ladder cell operates with maximum efficiency at a value of 0.5 for the duty cycle. When this value approach the extremes (0 and 1), the effective values of the currents through the capacitors and switches sharply increase, as well as their peak values, implying in more losses. The best operation area regarding efficiency is a composition of the boost and ladder characteristics, which is between 0.35 and 0.4, as shown in Figure 5.9(d).

The results obtained for the regulation based on the output power are presented in Figure 5.9(e). The linear voltage drop characteristic that is observed reminds the equivalent circuit, which contains an output resistance. At rated power, the measured output voltage was about 90% compared to the test under light output load. This characteristic may be compensated through the operation with closed-loop control, which is a feature of this topology.

The linearity of the voltage gain regarding input voltage was verified. Figure 5.9(f) shows the output voltage values related to the input voltage for a constant duty cycle equal to 0.43 and a constant resistive load of 52 Ω. The graphic shows that, as expected, the ratio between output and input voltages is constant in a wide operation range.

Setting the duty cycle to 0.56, efficiency and regulation tests were carried out for different resistive loads and a constant input voltage of 55 V. The results obtained from the efficiency test for the power board are set out in Figure 5.10(a). It can be seen that the highest efficiency values are in the range of 92% - 93% at 40% - 50% power. For higher output power levels, there is a steadily decrease in efficiency, caused by the increase of conduction losses. The measured value at rated power is 89.3%. The graphic also shows a sharp drop in efficiency for light loads. This may be caused by two factors: high switching losses and high input reactive power compared to the processed active power.

Figure 5.10 – Experimental result for efficiency for 55/220 V 60 Hz operation.



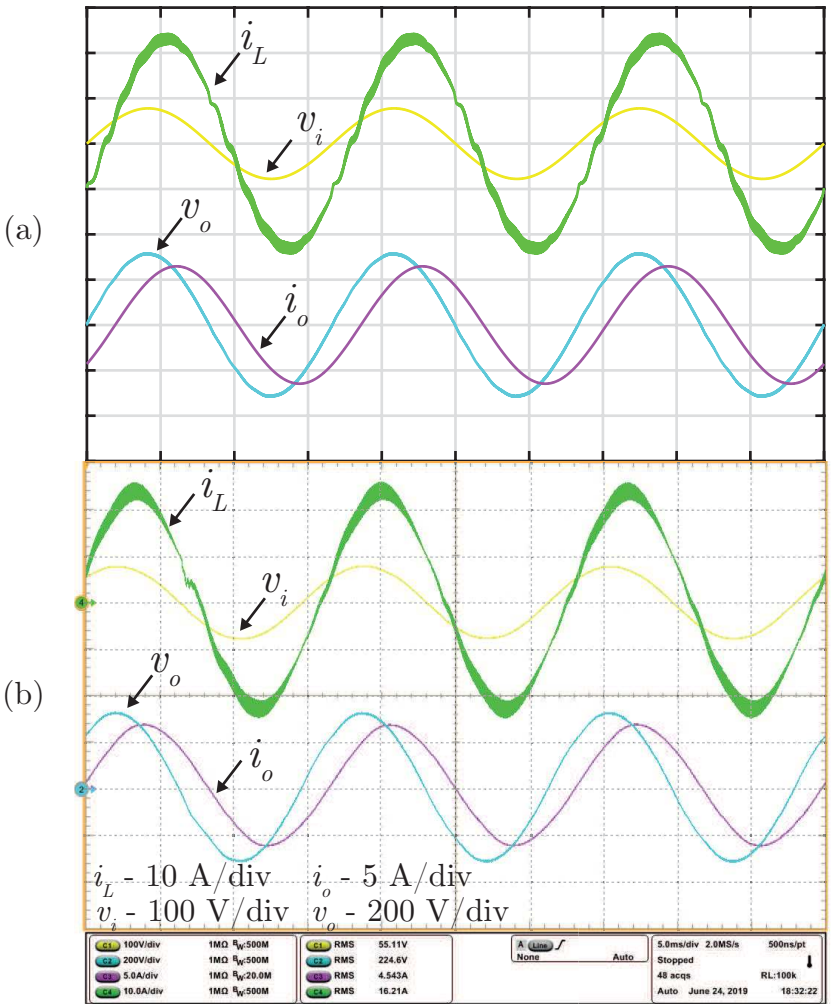
Source – Author.

Additionally, the power factor was measured for the same conditions in the efficiency test. Figure 5.10(b) provides the experimental data on power factor for different load values. There is a clear trend of the input power factor asymptotically approaching 1.0 for higher power levels. On the other hand, for light loads the reactive power overweights the active processed power. This is mainly caused by the capacitors, whose reactive power depends on the output voltage, that remained in range of 220 - 240 V when the test was carried out.

5.2 OPERATION WITH INDUCTIVE LOAD

The operation with inductive loads was also certified by experimental tests. The simulated and experimental results for an 1 kVA and 0.747 power factor output load are depicted in Figures 5.11(a) and 5.11(b), respectively. It should be observed that the input power factor is also inductive, but with a smaller phase angle difference than the output current and voltage. All waveforms are sinusoidal with low distortions.

Figure 5.11 – Simulation (a) and experimental (b) results for an inductive load. Time scale: 5 ms/div.



Source – Author.

Some tests were carried out with inductive loads, and the results are summarized in Table 5.2. It is noted that the converter compensates part of the output inductive reactive power, resulting in smaller input currents when compared to a resistive load with the same apparent power.

Table 5.2 – Experimental results for inductive loads.

Input			Output			
Power (VA)	Power factor	Current (A)	Power (VA)	Power factor	Current (A)	Eff. (%)
396	0.598 cap	7.16	218	0.992 ind	0.9	91.9
521	0.946 cap	9.48	486	0.954 ind	2.09	93.9
930	0.903 ind	16.9	1015	0.747 ind	4.54	90.5

Source – Author.

5.3 OPERATION WITH NON-LINEAR LOAD

Tests were also carried out for a non-linear load composed of a full bridge diode rectifier with an input inductance of 1 mH, an output capacitance of 1.5 mF and an 150 Ω load resistance, resulting in a crest factor of 3 (ratio between peak and effective current values). The input and output waveforms are shown in Figure 5.12(a), for simulation results, and in Figure 5.12(b), for experimental results. It should be noted that the results are similar but, in the experimentation, the oscillations on the input current tend to be smaller, given the parasitic resistances, which damp the transient response.

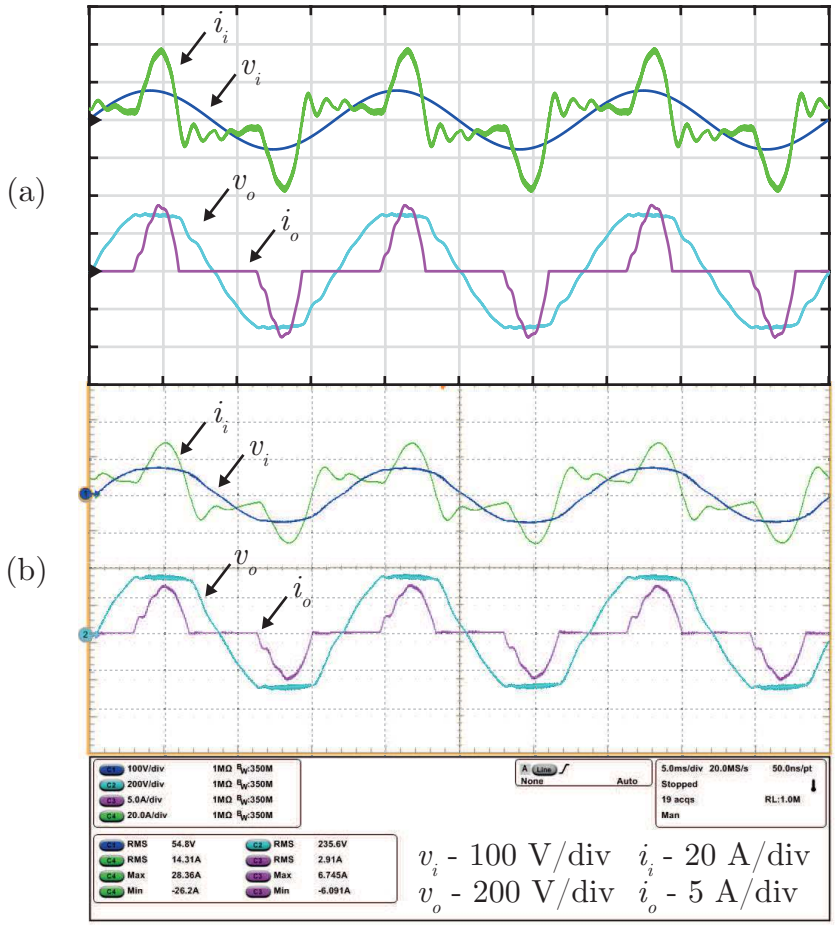
The measured data are summarized in Table 5.3. It should be noted that the load current is highly distorted, which causes also a distortion in the output voltage of the converter. Moreover, these distortions are also observed in the input current. The efficiency dropped around 3% in relation to the resistive load, given the increased input current effective value. Although there are distortions caused by the non-linear load, they are not highly modified by the converter. Thus, the converter still operates as an high gain non-isolated structure and the voltage over the output resistance is constant around 300 V.

Table 5.3 – Experimental results for non-linear load.

Parameter	Input	Output	Parameter	Input	Output
Voltage	55 V	235 V	Power factor	0.724	0.752
Current	14.84 A	3.00 A	THDv	5.6%	11.1%
Apparent power	816 VA	700 VA	THDi	76.2%	70.6%
Active power	591 W	527	Efficiency	89.2%	

Source – Author.

Figure 5.12 – Simulation (a) and experimental (b) results for a non-linear load. Time scale: 5 ms/div.



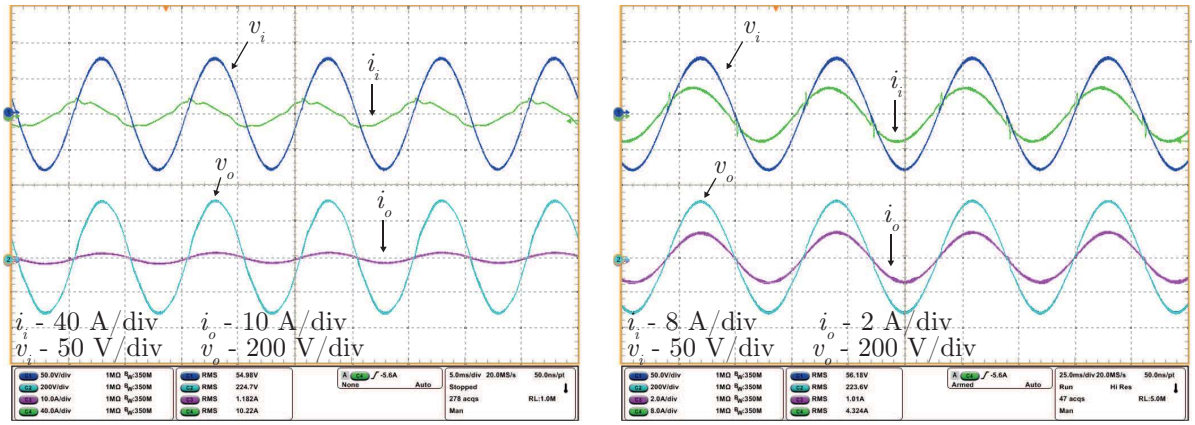
Source – Author.

5.4 OPERATION WITH DIFFERENT INPUT FREQUENCIES

A wide frequency operation range for the converter was tested. Given the limitations of the available voltage source, tests were performed at low power. Results for an input frequency of 100 Hz are depicted in Figure 5.13(a). It is observed that the voltage gain is maintained around 4. On the other hand, the input current is increased because of the higher reactive capacitive power. The converter was also tested for an input frequency of 16.7 Hz (Figure 5.13(b)). As it is a low frequency, the measured input power factor was 0.946 for an output load of 220 W, which is the best performance regarding the input frequency variation.

The results for an input frequency of 400 Hz are presented in Figure 5.14. As the operation frequency is much higher than the rated of 60 Hz, there is much reactive power on the converter, increasing the input current and losses. In order to avoid the operating limitations of the voltage source, the maximum input voltage was 13 V. Despite the high current levels, there is still a high voltage gain, as it begins to be influenced by the resonant frequency.

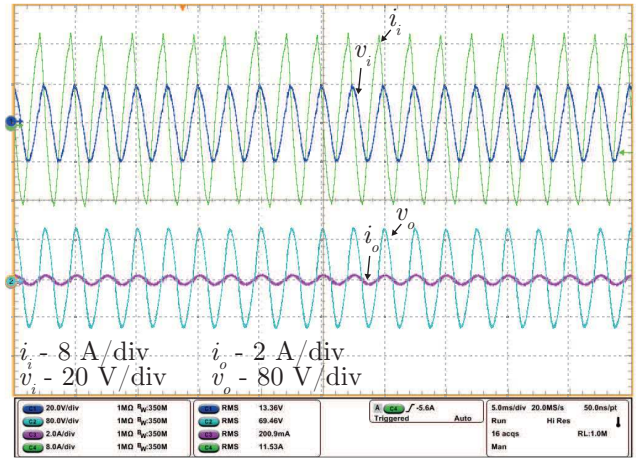
Figure 5.13 – Experimental results for input frequencies of (a) 100 Hz (5 ms/div) and (b) 16.67 Hz (25 ms/div).



(a) (b)

Source – Author.

Figure 5.14 – Experimental results for an input frequency of 400 Hz. Time scale: 5 ms/div.



Source – Author.

A complete list of measured data for different input frequencies is shown in Table 5.4. Although they were tested at different operating points, it can be observed that the higher the input frequency is, the lower is the input power factor. This is explained by the high reactive current caused by the capacitances.

5.5 OPERATION WITH TWO OUTPUT LOADS

A satisfactory operation also occurs when two loads are connected to two different output ports. Figure 5.15 shows the experimental results for a condition of 55 V input voltage and two 250 W resistive loads, each one connected to a different output voltage of 110 V and 220 V.

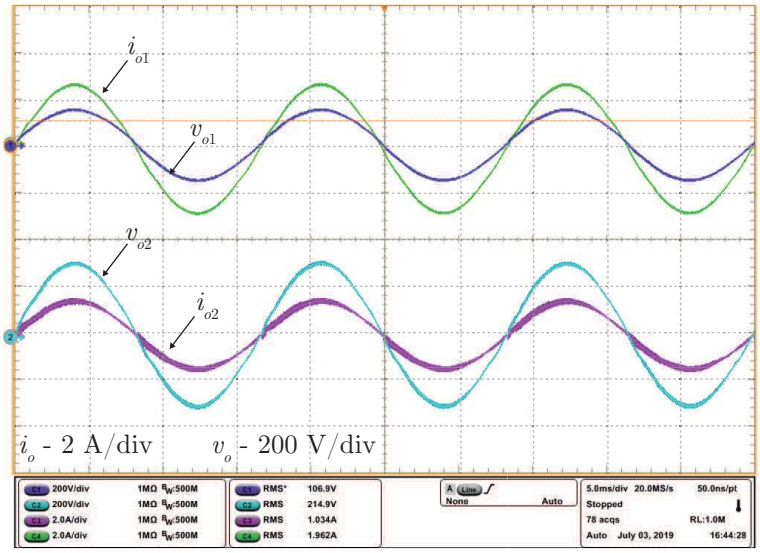
These results show that the converter is able to provide two different output voltage

Table 5.4 – Experimental results for different input frequencies.

Parameter	16.67 Hz	100 Hz	400 Hz
Input voltage	55 V	55 V	13.4 V
Input current	4.53 A	10.2 A	12.1 A
Input apparent power	250.1 VA	565 VA	161.6 VA
Input active power	236.4 W	270 W	52.7 W
Input power factor	0.946	0.477	0.326
Output voltage	218.8 V	223 V	69.5 V
Output current	1.03 A	1.05 A	0.16 A
Output power	226.3 W	235 W	11.3 W
Efficiency	95.7%	87.0%	21.4%

Source – Author.

Figure 5.15 – Experimental results for two output loads connected to both 110 V and 220 V outputs. Time scale: 5 ms/div.



Source – Author.

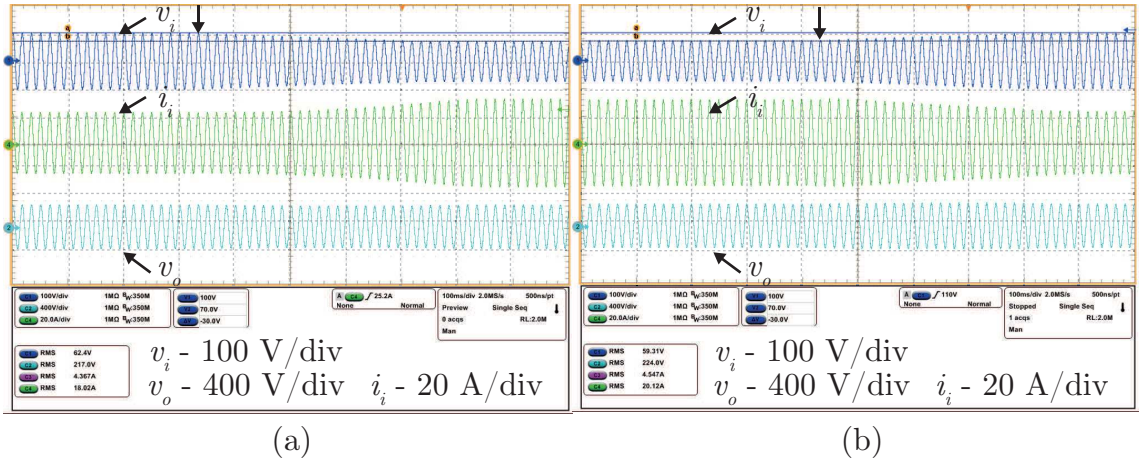
levels. However, the voltage control can be performed to only one output.

5.6 CLOSED-LOOP OPERATION

Experimental verification of the output peak voltage control was also performed. Figure 5.16(a) provides the results for an input effective value decreasing from 70 V to 50 V. It is observed that, as expected, the input current increases and the value of the output voltage remains controlled at 220 V. The test was also carried out for an increase in the input voltage. The results are shown in Figure 5.16(b). For both increase and decrease in the input voltage, an oscillation in the output voltage is barely noticed.

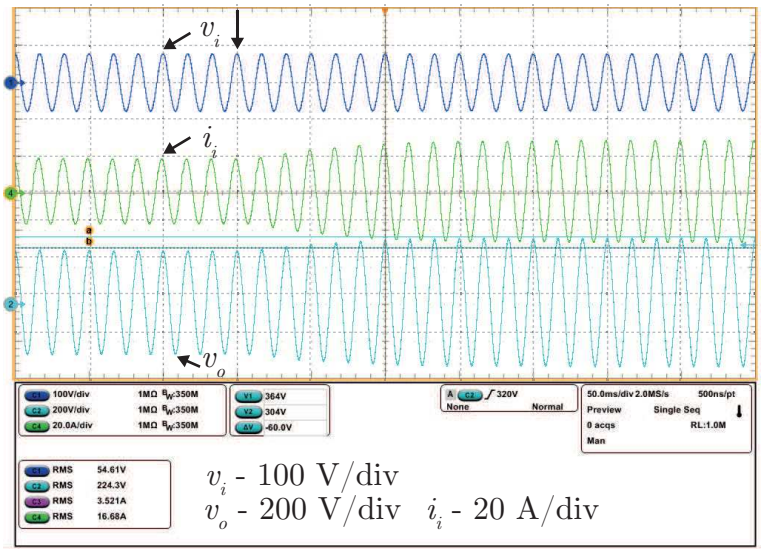
Results for a reference variation from 200 V to 240 V are shown in Figure 5.17. An increase in the output voltage and input current are observed.

Figure 5.16 – Experimental results for a linear variation in input voltage value with a controlled output voltage peak value.



Source – Author.

Figure 5.17 – Experimental results for an output voltage reference step from 200 V to 240 V (effective).



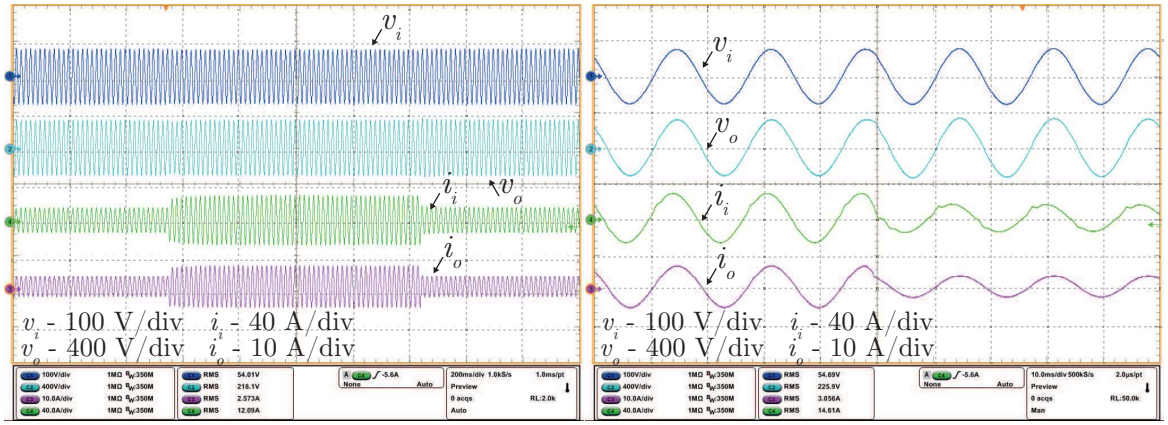
Source – Author.

A load-step response was also verified. Figure 5.18(a) shows the obtained waveforms for input and output voltages and currents with load steps from 50% to 100% then 50% again. Details for the transition are depicted in Figure 5.18(b). It is noted that the response is almost instantaneous.

5.7 110/400 V OPERATING POINT

The higher voltage operating point was tested for two different conditions: using a regulated voltage source, the test were carried out for loads from 0 to 1250 VA. Above this power level, the converter was connected to the grid using a transformer. Figure 5.19

Figure 5.18 – Experimental results for a load step from 50% to 100% and then 50% again.



(a) (b)

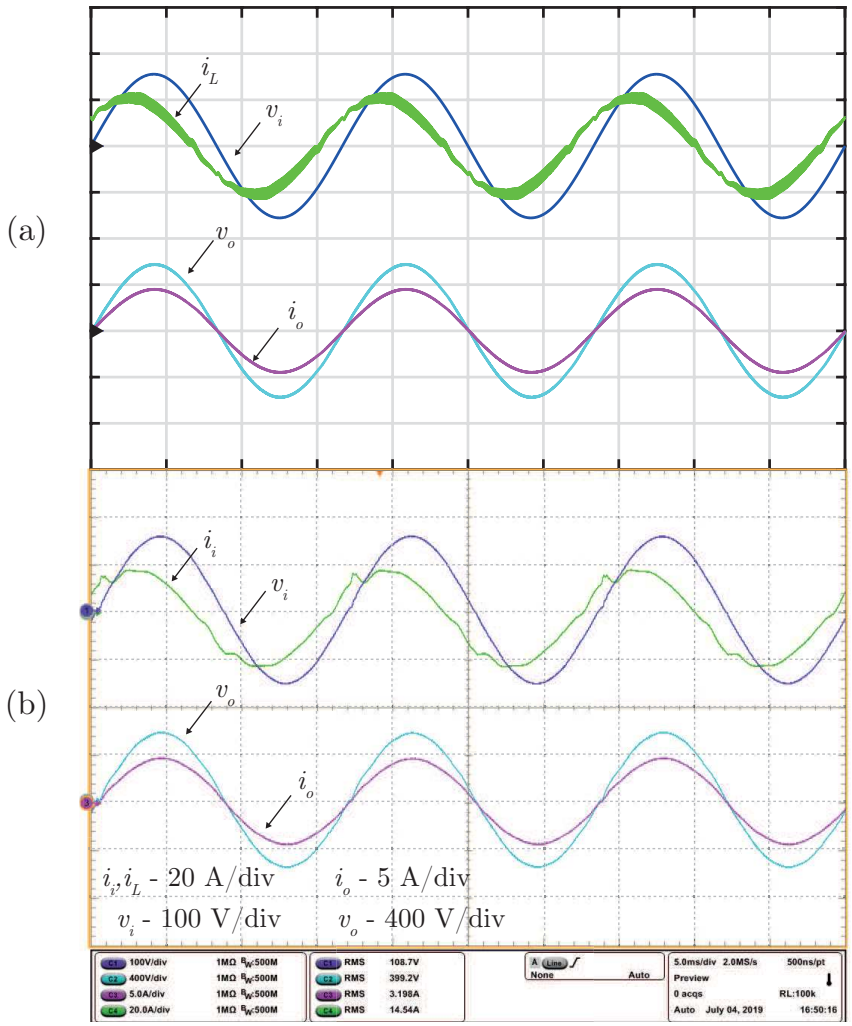
Source – Author.

shows the results for a 110/400 V conversion and 1250 VA output load. It can be seen that the effective value of the output voltage is 400 V for an 110 V input voltage. The measured input power factor is 0.813 and the efficiency, 93.8%, being one of the best operating points. Results show sinusoidal waveforms for input and output voltages and currents. It should be observed a distortion in the input current when the voltage changes polarity. This may be a result of the voltage clamping circuit and the change of modulation. One possibility to overcome this problem is to change the voltage clamping circuit for a passive snubber circuit, containing only capacitor and/or resistors. Further analysis would be necessary.

Figure 5.20 presents the results for a 2 kVA resistive load. It should be noted that the input voltage is distorted, which is reflected to the output voltage. Moreover, the same problem which was discussed in the previous result occurs: there is a distortion in the input current during the changing of the voltage polarity. The efficiency for this operating point is 93.1% and the input power factor, 0.909. The efficiency is better than the 55/220 V operating point because the current levels are approximately the same, but in this condition the processed power is doubled. Moreover, from the theoretical analysis, the conduction losses are much higher than the switching losses. Thus, the efficiency is more dependent on the current than on the voltage levels.

An operation with inductive load was also tested for a 1950 VA load with an inductive power factor equal to 0.916. The simulated and experimental waveforms are displayed in Figure 5.21(a) and 5.21(b), respectively. The voltage and current distortions still appear. Although the output power factor is 0.917 inductive, the input power factor is slightly capacitive, almost unitary. Thus, as the converter compensates the reactive power of the load, the input current is smaller if compared to the operation with a resistive load. That means a better efficiency, whose measured value was 94.6% for these operating conditions.

Figure 5.19 – Simulated (a) and experimental (b) waveforms for the input and output voltages and currents for an 1.25 kVA resistive load. Time scale: 5 ms/div.

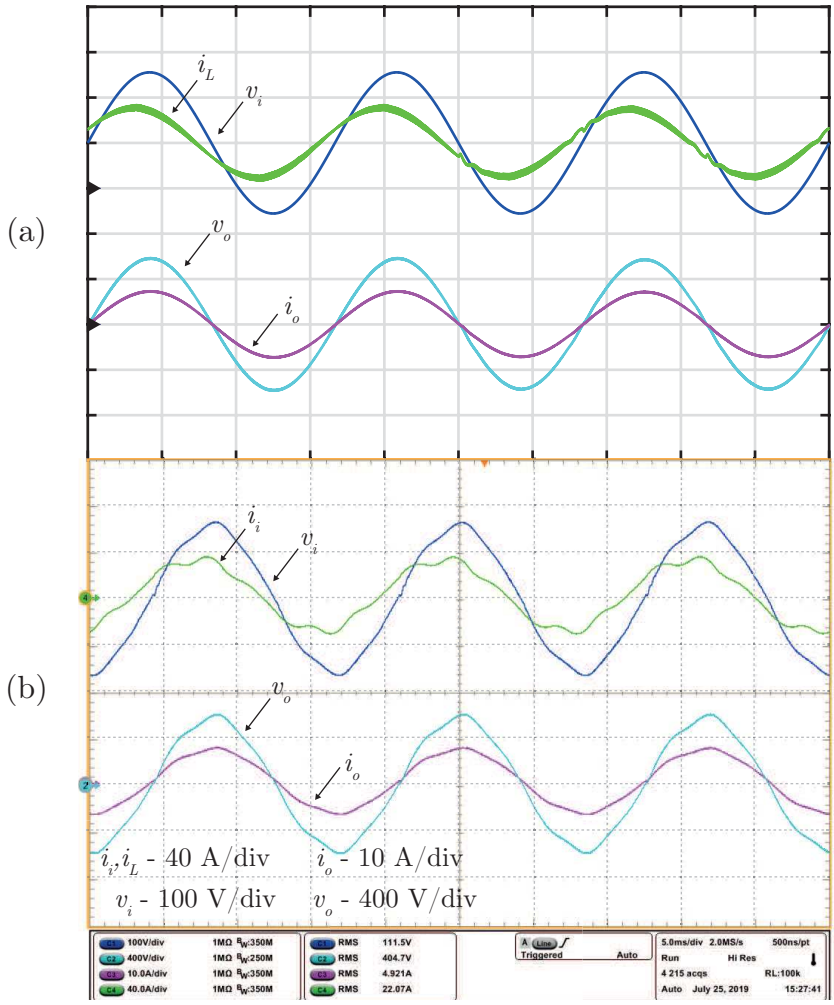


Source – Author.

The voltage balance among the capacitors was also verified for this operating point. Simulated and experimental results are shown in Figure 5.22(a) and Figure 5.22(b), respectively. It is observed that the voltages over the capacitors are approximately the same and equal to half of the output voltage, with a peak value of 300 V. Moreover, even with harmonic distortion in the input voltage, the voltage over the capacitors are balanced without any control strategy.

Experimental results for the voltage over the switches are depicted in Figure 5.23(a) for the MOSFETs S_{1_b} and S_{2_b}. As they are the upper MOSFETs in their respective four-quadrant switches, they block the voltage in the same grid half cycle, but complementary during a switching period. In Figure 5.23(b) the voltage over the MOSFETs of the same switch S_1 can be seen. In this case, each switch blocks the voltage in a different grid half cycle. In all situations, the maximum blocked voltage is half of the output voltage peak value plus some voltage ripple. This value was measured as 295 V. This result shows the

Figure 5.20 – Simulated (a) and experimental (b) waveforms for the input and output voltages and currents for a 2 kVA resistive load. Time scale: 5 ms/div.



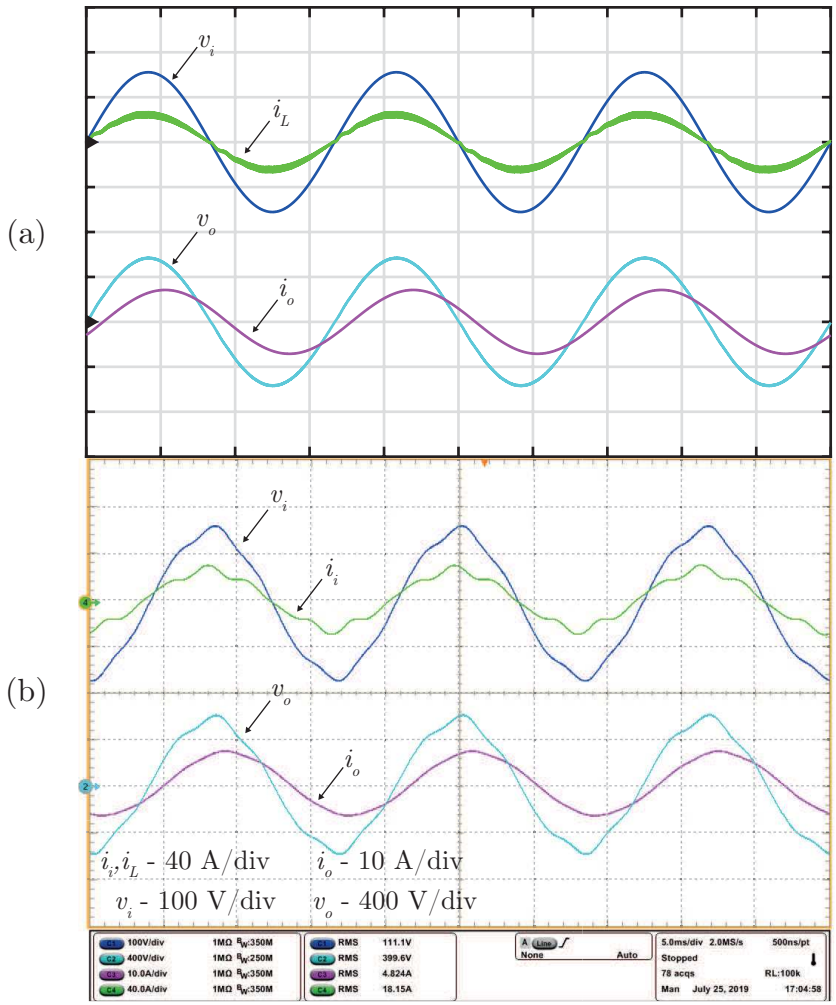
Source – Author.

main advantage of using a switching capacitor cell: it is possible to achieve high voltage levels using lower voltage components. Furthermore, there is no need of a specific control method to balance the voltage over the capacitors.

Experimental and theoretical results for the efficiency of the power stage are presented in Figure 5.24(a). The maximum efficiency is 93.9% at 1.44 kW output power and 93.1% at rated power. For light loads operation, the efficiency drops sharply, given the high level of reactive currents. It can be observed that the experimental and theoretical curves are similar, with a maximum difference of 0.7%.

Results for the input power factor are depicted in Figure 5.24(b). It should be noted that the input power factor increases with the output power, because the reactive power is almost constant regarding load variations, given that it depends mostly on the output voltage. The measured value of input power factor was 0.91 at rated power, while the expected was 0.927. The difference might be due the reactive power of an input capacitor

Figure 5.21 – Simulated (a) and experimental (b) waveforms for the input and output voltages and currents for an 1950 VA inductive load with 0.916 power factor. Time scale: 5 ms/div.



Source – Author.

that was employed during experimental tests, with a capacitance value of 20 μF. Overall, both curves are similar, although the experimental result is below the project specification of minimum 0.92 input power factor.

5.8 CONCLUSION

This chapter presented the simulation and experimental results for the HBSCC operating with 55/220 V and 110/400 V conversions. The main conclusions of this chapter are:

- For the 55/220 V operating mode, the efficiency could be improved by employing lower voltage MOSFETs, whose conduction resistances are usually smaller, given the fact that the maximum blocking voltage is 160 V in this mode. In addition, other solutions could be searched to reduce the losses due the high input current. This

Figure 5.22 – Simulated (a) and experimental (b) waveforms of the voltage over the capacitors for a 110/400 V conversion. Time scale: 5 ms/div.

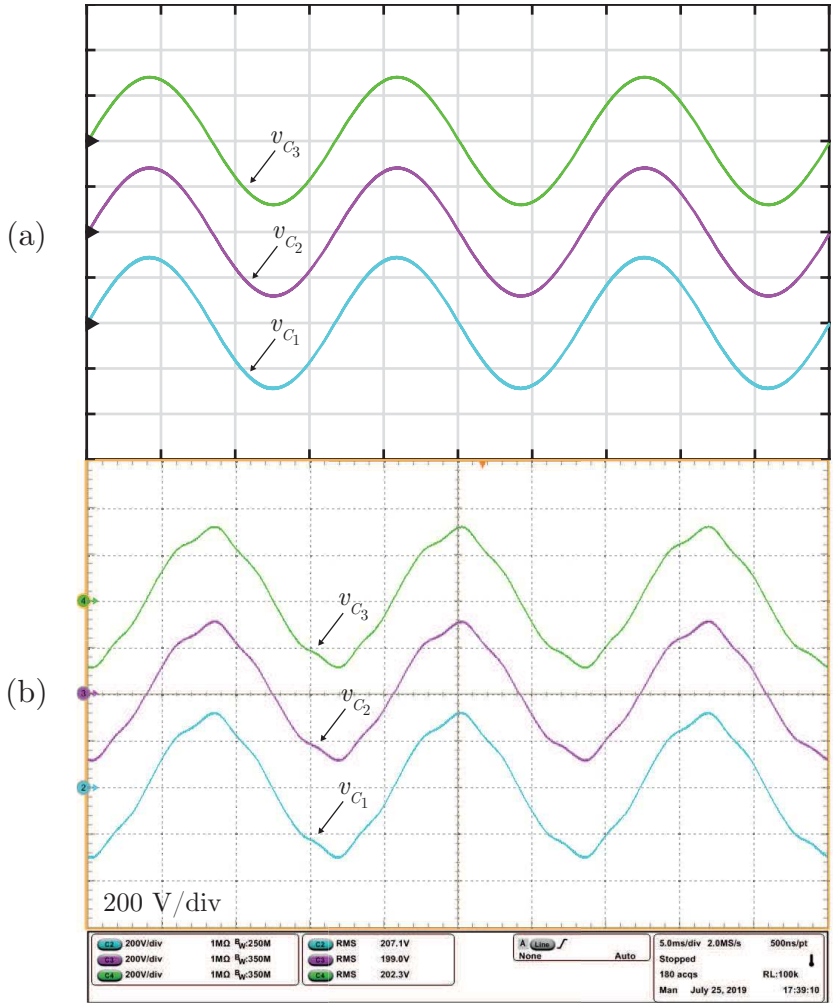


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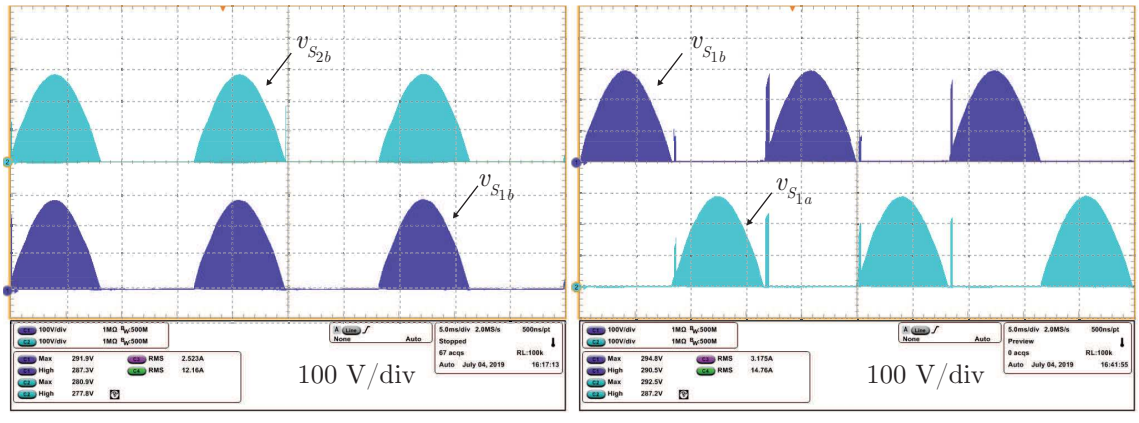
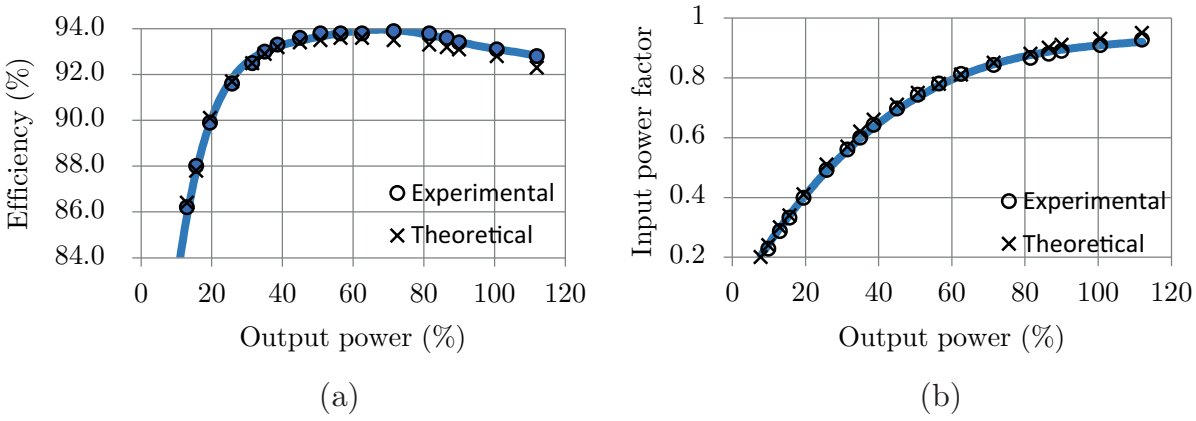
Figure 5.23 – Simulated (a) and experimental (b) waveforms of the voltage over the switches for a 110/400 V conversion. Time scale: 5 ms/div.



Source – Author.

Figure 5.24 – (a) Efficiency and (b) input power factor curves for the 110/400 V operation.



Source – Author.

mode also has shown a better input power factor, because the capacitive reactive power is smaller when compared to the 400 V output mode.

- The operation with different main frequencies has shown good results for lower frequencies, for example at 16.67 Hz, because of the smaller reactive component. On the other hand, the operation at 400 Hz resulted in high reactive values, low input power factor and low efficiency. Moreover, it might have suffered influence from the resonant frequency, given that the voltage gain was higher than 5. Thus, the main frequency limitation was verified for this converter.
- When operating as a 110/400 V converter, the efficiency was satisfactory. The input current distortion was possibly caused by the voltage clamping circuit. A better design approach could be performed or other simpler solutions could be found.
- The closed loop operation was also satisfactory, given that the slow control maintained the output voltage stable during the tests.

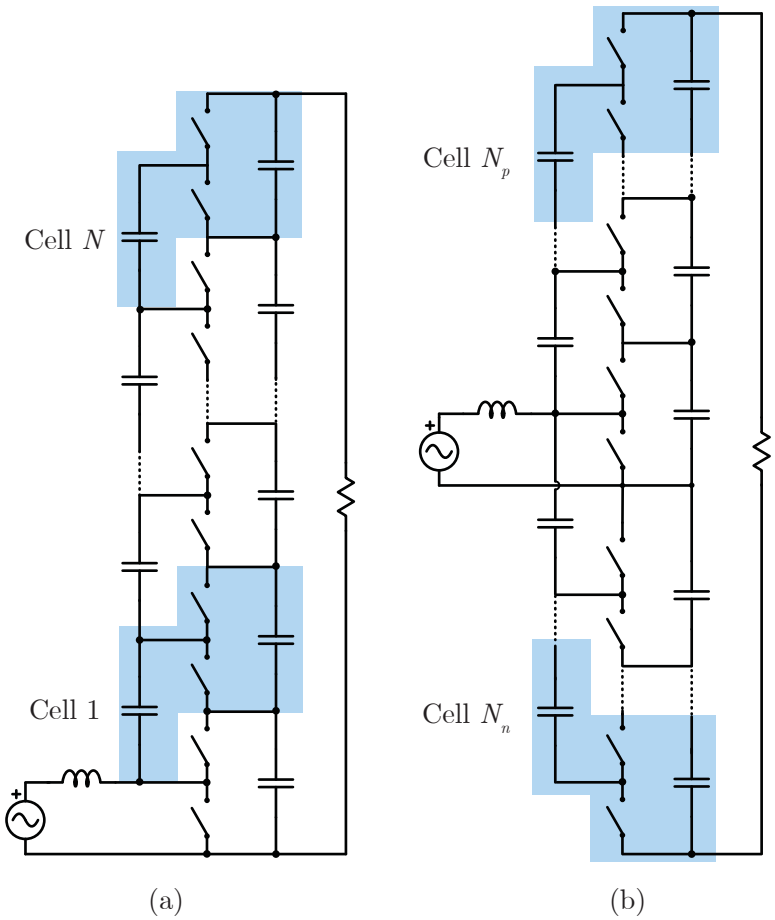
6 TOPOLOGICAL VARIATIONS

A theoretical analysis and experimental validation of a single phase hybrid boost switched-capacitor converter was presented previously. This chapter proposes topologic variations that can be applied to the studied topology to obtain new converters, different operating modes or better performance.

6.1 HYBRID CONVERTER WITH HIGHER NUMBER OF SWITCHED-CAPACITOR CELLS

The studied converter was composed of only one switched-capacitor cell. However, in order to achieve higher voltage gains, it is possible to connect more cascated ladder cells on the output stage. Figure 6.1(a) shows a hybrid boost composed by N ladder cells.

Figure 6.1 – Hybrid converter with more switched-capacitor cells. (a) Common ground configuration; (b) Symmetric configuration.



Source – Author.

The ideal voltage gain of this structure is given by (6.1), where N is the number of

switched-capacitor ladder cells.

$$G = \frac{N+1}{1-D}. \tag{6.1}$$

An advantage of the cascaded switched capacitor cells is that the output voltage is equally distributed among the output capacitors. It means that the voltage stresses over the capacitors and switches are all equal to

$$V_{S,max} = V_{C,max} = \frac{V_{op}}{N+1}. \tag{6.2}$$

Although it provides a high voltage gain with low voltage stresses over the switches and capacitors, the number of devices are increased, given that each cell contains two capacitors and two four-quadrant switches (four MOSFETs). In addition, the number of gate drivers increase in proportion to the switch count. The increment of component count results in reduced efficiency and reliability, because the failure of one switch stops the operation of the converter. The equivalent output resistance, supposing that the conduction resistances of all switches are equal to r_s, is

$$R_{out} = r_s \left(\frac{1+3d+N(1-d)}{d(1-d)^2} \right). \tag{6.3}$$

An another similar alternative is shown in Figure 6.1(b). The ladder cells are cascaded for both positive and negative voltages, and the total voltage gain is the same as the structure in Figure 6.1(a) using $N = N_p + N_n$. Differences are in the reduced losses for this structure, at the cost of no common ground between input and output.

An extra feature of these configurations is the range of available output voltages. By connecting the load to different output capacitors, it is possible to obtain output voltages as shown in (6.4).

$$V_{o,alternative} = k\frac{V_o}{N+1}, k = 1,2,...,N \tag{6.4}$$

Thus, this configuration might be applied as a multi-port converter, with multiple loads connected to the output capacitors.

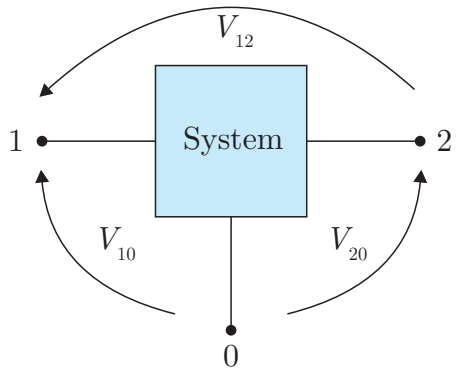
6.2 OTHER INPUT-OUTPUT CONFIGURATIONS

Another advantage from the HBSCC structure is the possibility to operate as a multi-port converter. By modifying the input and output connection points, other topologies are obtained, with different gains and efficiencies. In order to present all the variances, the concept of commutation cell is employed, which is hereafter described.

6.2.1 Commutation cell

A voltage switching converter can be generically defined as a system with multiple connection points. Knowing the voltage ratio between some ports allows to calculate the remaining unknown ratios. For example, Figure 6.2 shows a generic three-port system, which may represent a power converter.

Figure 6.2 – Three-port system.



Source – Author.

It is assumed that the voltage ratio between the voltages V_{20} and V_{10} is known and equal to G. By applying the Kirchhoff's voltage law, the voltage V_{12} can be written as:

$$V_{12} = V_{10} - V_{20} = V_{10} - G \cdot V_{10} = V_{10}(1-G). \tag{6.5}$$

The relation can also be described as:

$$V_{12} = V_{10} - V_{20} = \frac{V_{20}}{G} - V_{20} = V_{20}\left(\frac{1-G}{G}\right). \tag{6.6}$$

Thus, from one input/output relation it is possible to obtain other two voltage ratios. The concept is exemplified for PWM converters through the two commutation cells presented in Figure 6.3. Both are composed of three connection ports and the ratio between the voltages V_{20} and V_{10} is known. Table 6.1 compares the possible voltage gains for these structures.

The following analysis is performed to obtain a generalized concept for a N-port system. In order to obtain the differential voltage ratios among three ports it is necessary to know at least one of them. For an N-port system, at least N-2 independent voltage ratios must be previously determined. Then, the number of possible differential voltages (ports), N_{diff}, for an N-port system is

$$N_{diff} = \frac{N!}{2!(N-2)!} = \frac{N(N-1)}{2}. \tag{6.7}$$

Figure 6.3 – Examples of three-port commutation cells.

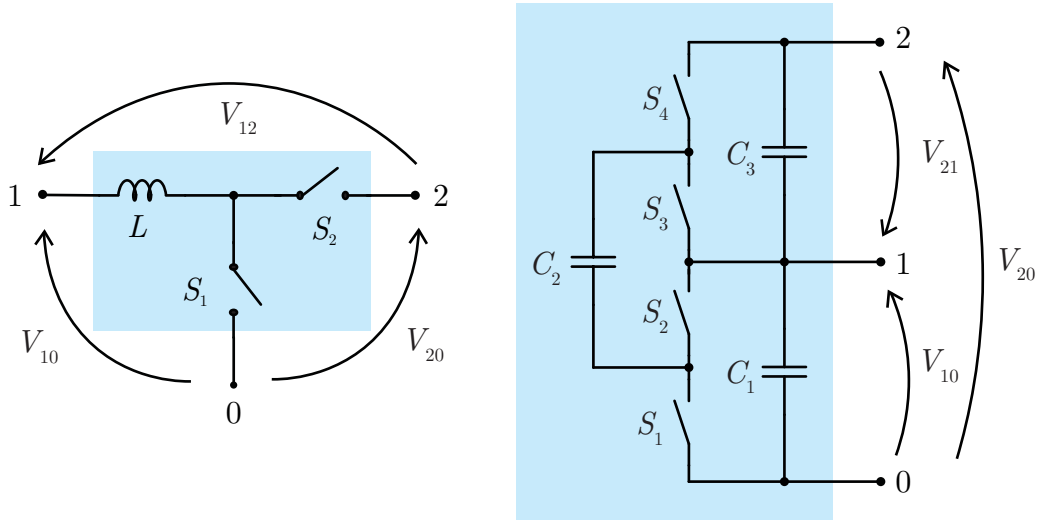


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Table 6.1 – Voltage ratios between ports.

Voltage ratio	$\frac{V_{20}}{V_{10}}$	$\frac{V_{10}}{V_{12}}$	$\frac{V_{20}}{V_{12}}$
Generic cell	G	$\frac{1}{1-G}$	$\frac{G}{1-G}$
Inductive cell	$\frac{1}{1-D}$	$-\left(\frac{1-D}{D}\right)$	$-\left(\frac{1}{D}\right)$
Ladder cell	2	-1	-2

Source – Author.

By combining each of these differential voltages, it is obtained the total amount of possible voltage ratios N_g:

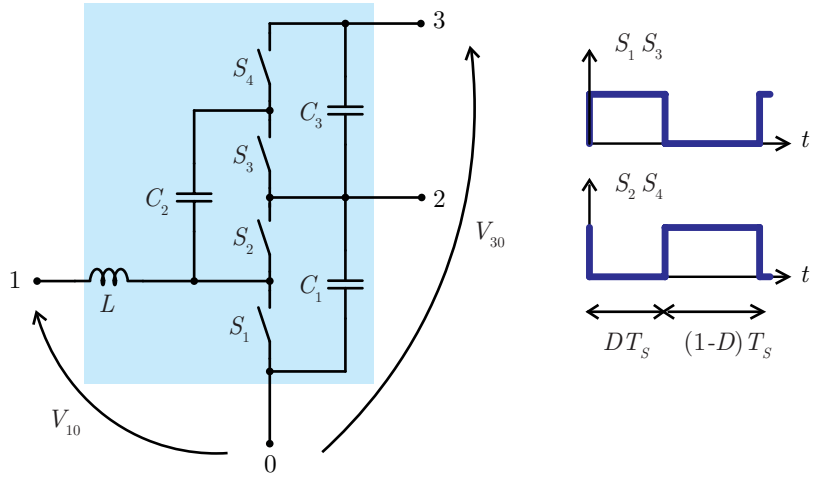
$$N_g = \frac{N_{diff}!}{2!(N_{diff}-2)!} = \frac{N(N^3-2N^2-N+2)}{8}. \tag{6.8}$$

It is noticed that N_g is proportional to the fourth power of the number of connection ports. For a 3-port system, there are three possible connections. This concept can be also evaluated for the hybrid switched capacitor converter, as shown in Figure 6.4.

The HBSCC consists on a four-port switching cell. From (6.8) it is concluded that there are 15 different connections for this topology. All the possible connections are depicted in Figure 6.5. The voltage sources and loads are distributed in order to provide a voltage step-up conversion (except for topology (c), whose gain is either greater or smaller than 1, depending on the duty cycle).

The ideal voltage gains (without considering the reactances and non-idealities) are summarized in Table 6.2. Some ratios do not depend on the duty cycle, leading to

Figure 6.4 – Hybrid switched-capacitor four-port cell.



Source – Author.

converters that cannot be controlled. Some interesting connections are: (d), which provides a voltage gain from 1 to infinite and has a common point; (j), whose voltage gain is dual to the hybrid boost, only changing the variable $1-d$ for d, but not sharing common connection points; and (m), which also provides a high voltage gain and has a common ground.

Some topologies also are not suitable because of the waste of components, for example the converters (a) and (i). These converters could operate better if some devices were removed from them.

Table 6.2 – Voltage ratios between ports for the hybrid switched capacitor converter.

Voltage ratio	Gain	Voltage ratio	Gain	Voltage ratio	Gain
(a) V_{20}/V_{10}	$\frac{1}{1-D}$	(b) V_{30}/V_{10}	$\frac{2}{1-D}$	(c) V_{21}/V_{10}	$\frac{D}{1-D}$
(d) V_{31}/V_{10}	$\frac{1+D}{1-D}$	(e) V_{32}/V_{10}	$\frac{1}{1-D}$	(f) V_{30}/V_{20}	2
(g) V_{20}/V_{21}	$\frac{1}{D}$	(h) V_{31}/V_{20}	$1+D$	(i) V_{32}/V_{20}	1
(j) V_{30}/V_{21}	$\frac{2}{D}$	(k) V_{30}/V_{31}	$\frac{2}{1+D}$	(l) V_{30}/V_{32}	2
(m) V_{31}/V_{21}	$\frac{1+D}{D}$	(n) V_{32}/V_{21}	$\frac{1}{D}$	(o) V_{31}/V_{32}	$1+D$

Source – Author.

Experimental results were collected by changing the input and output connections of the main converter. As the converter was not projected for other connections, tests were carried out for power levels near 400 W and an effective voltage value of 220 V between ports 3 and 0. The graphic of Figure 6.7 shows the experimental voltage gains and the ideal values for a duty cycle of 0.5.

It is noticed that, even if the connection (j) provides an equal voltage gain, its

Figure 6.5 – Possible connections for the hybrid boost switched capacitor switching cell.

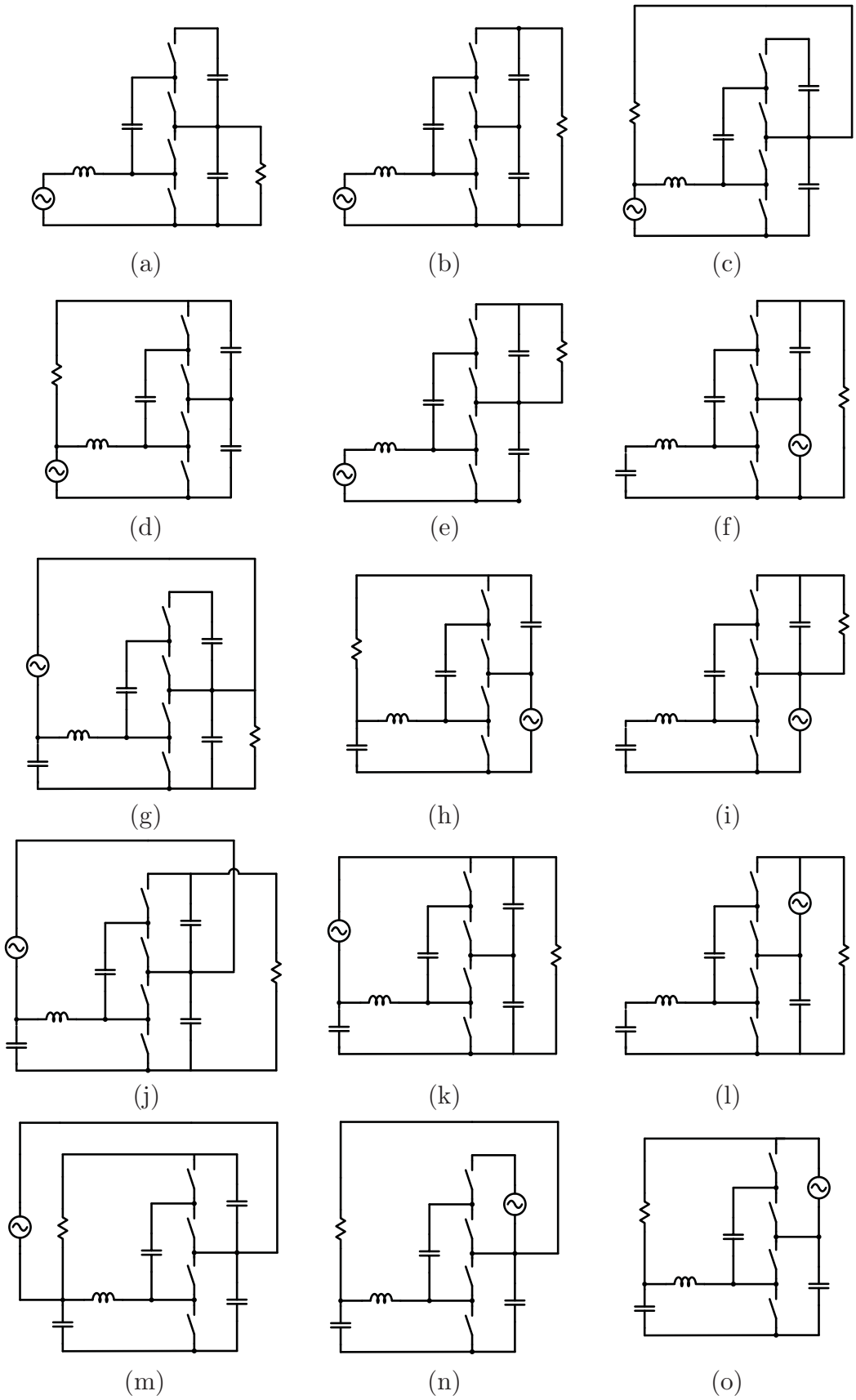


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Figure 6.6 – Experimental results for the input and output voltages of each connection.

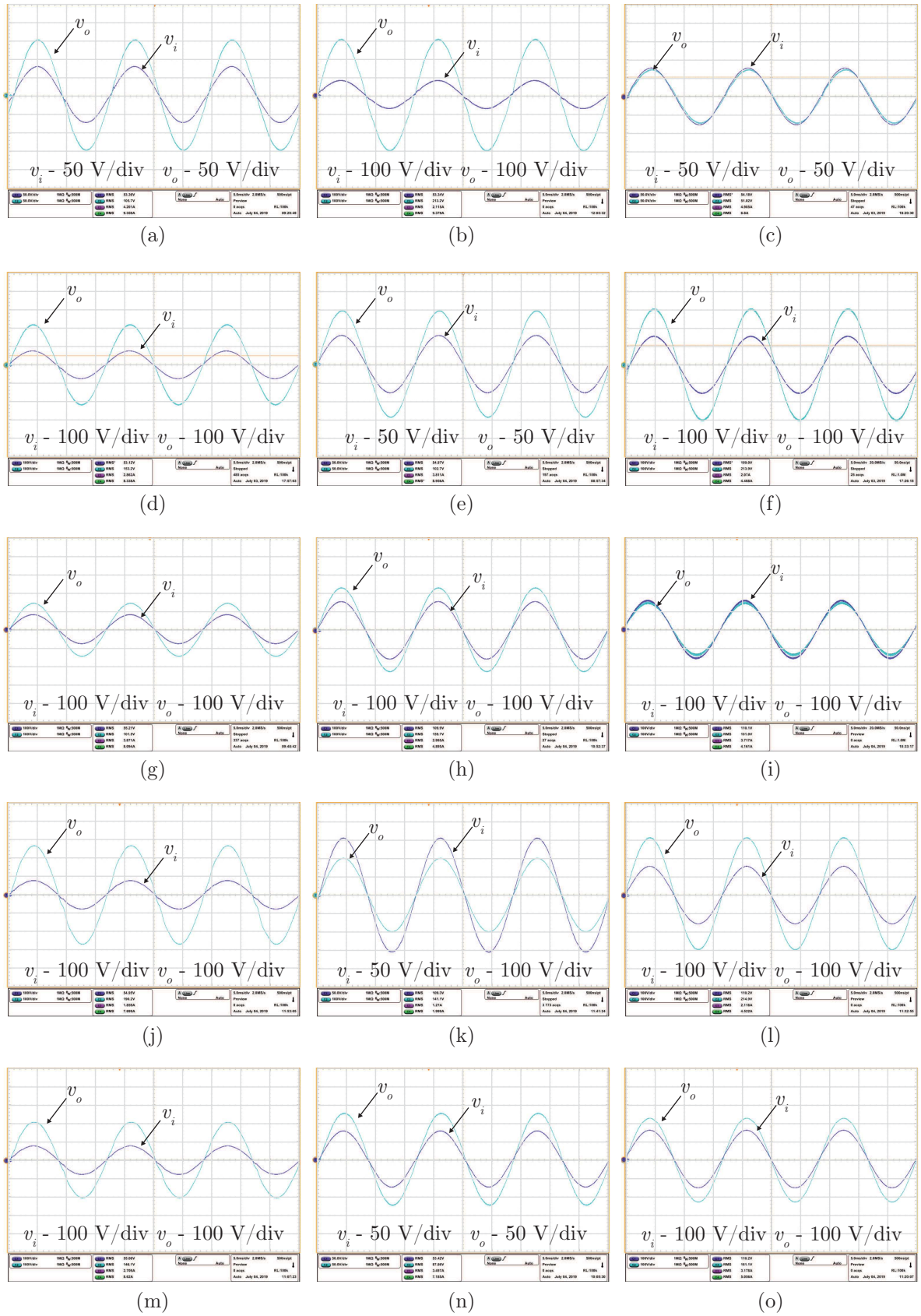

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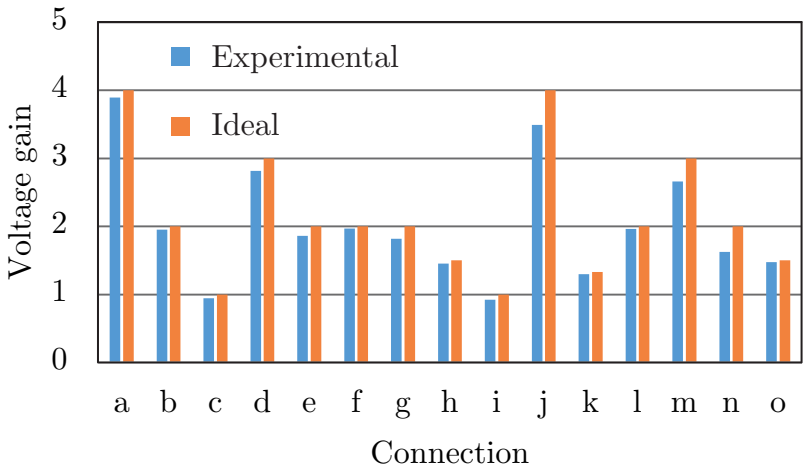
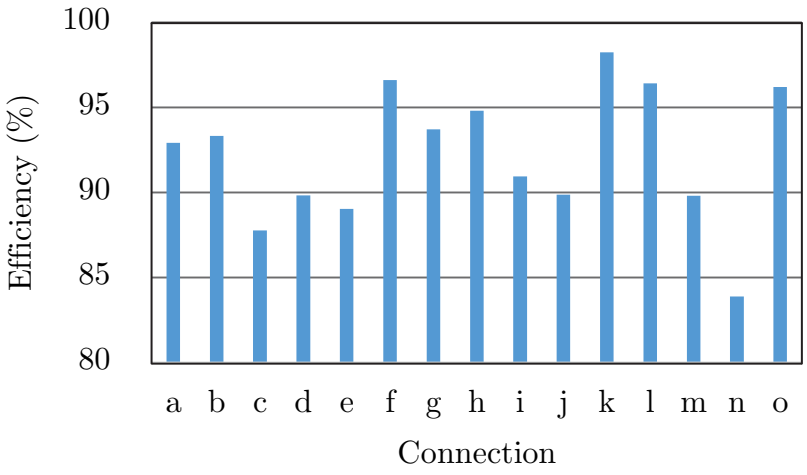
Figure 6.7 – Comparison between theoretical and experimental voltage gains for different input/output connections.



Source – Author.

voltage regulation is worse than the main topology (b). All connections worked and were validated. Figure 6.8 compares the efficiency among the connections for processed power of 400 W. The efficiency range is from 83% to 98%. One interesting point is for topology "j", which also provides ideally a voltage gain 4, but its efficiency is about 3% lower than the main configuration. The connection with higher efficiency was (k), however, its gain was lower than 1.5.

Figure 6.8 – Experimental efficiencies for different input/output connections.



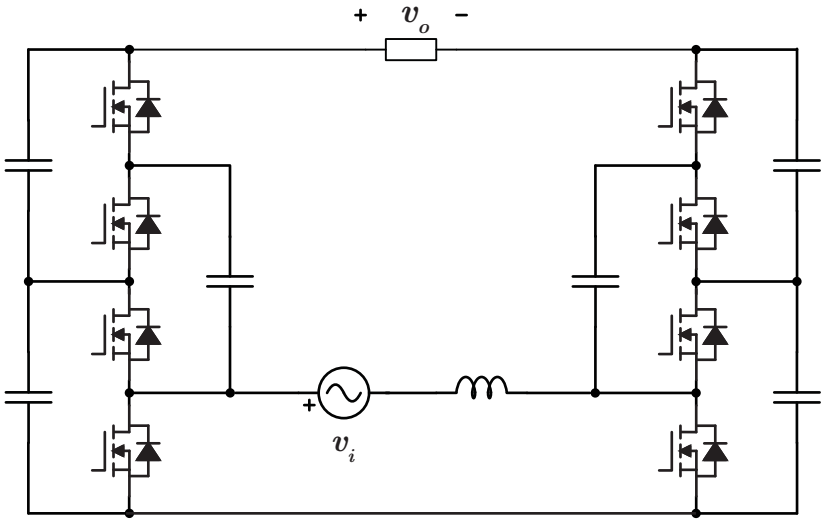
Source – Author.

All proposed connections were tested experimentally and operated as expected. Further analysis could be developed in future studies.

6.3 HYBRID CONVERTERS USING TWO-QUADRANT SWITCHES

One of the major issues of the proposed converter is the modulation schema. It requires voltage sensing and voltage clamping circuits, which diminishes the reliability and the efficiency of the converter. Furthermore, the effect of cross-talk among the switches is more present. As proposed in (LAZZARIN et al., 2012), some AC-AC switched capacitor converters employ only two-quadrant switches, being unable to block reverse voltage. They are able to operate with alternate voltages because the output is connected between two ladder cells. Then, a DC voltage level is imposed in all capacitors during the first grid cycles. As consequence, the voltage over the capacitors is composed of DC and AC components. Nonetheless, the peak voltage levels are the same of a single Ladder cell with four-quadrant switches. The major drawback of this structure is the capacitor count, which is doubled from the single-ladder topology. This structure of connecting two cells in a differential connection was already studied in grid-connected inverters (ANDRADE et al., 2018) and might also be applied to the hybrid converter, as shown in Figure 6.9.

Figure 6.9 – Single phase hybrid boost switched-capacitor converter employing two-quadrant switches.



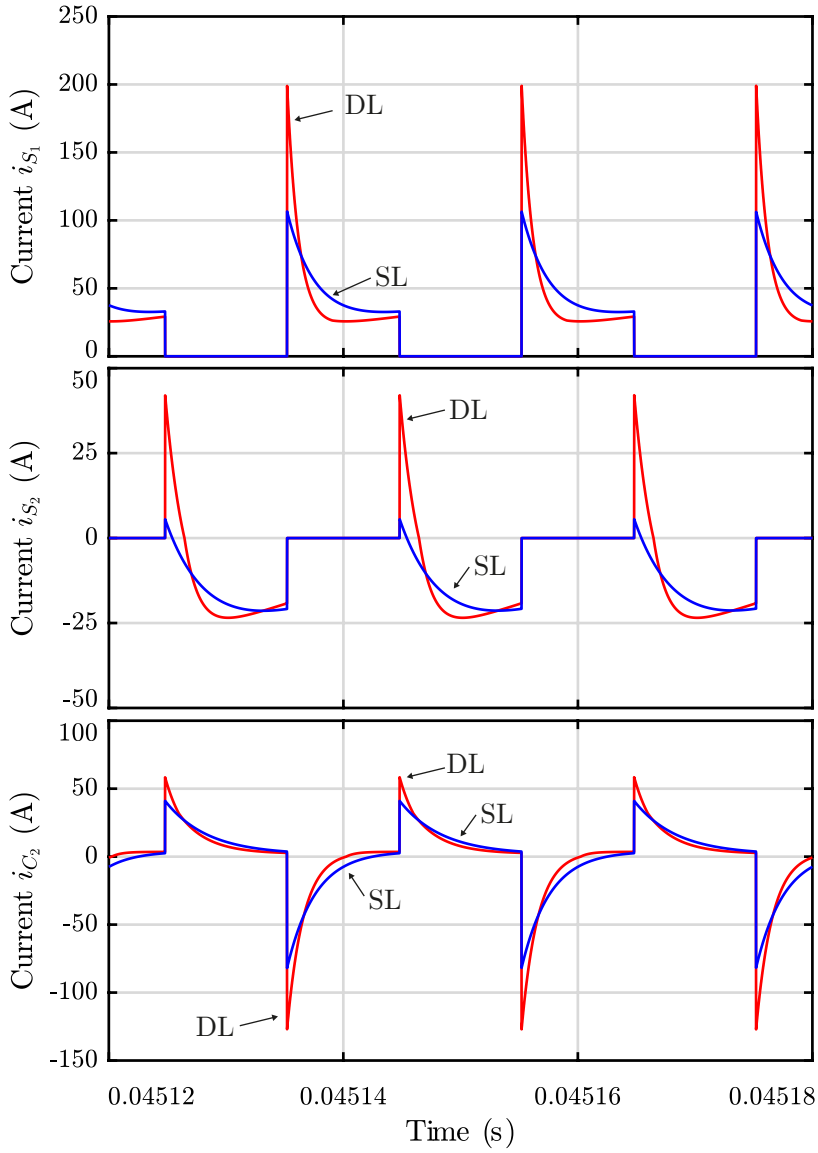
Source – Author.

The major advantage of this structure is the simplicity: it does not suffer from commutation problem and does not need information about the voltages over the capacitors to perform the modulation. However, the number of capacitors is doubled and the source and loads do not share a common ground. Regarding the switched capacitor characteristics, the time constant is half of the other topology, because each loop consists of only two capacitors and two MOSFETs (different from four MOSFETs and two capacitors in the single AC ladder). This leads to higher peak and effective current values.

Simulations were performed to compare both structures, considering equal devices and same operation conditions. Figure 6.10 shows the comparison between the structures.

It is observed that both peak and effective values of currents through the switches are higher for the double-ladder structure. Moreover, the voltages stresses seem to be equal. Because of the reduced AC component of voltage over the capacitors, the reactive power consumed by the converter is smaller for the double ladder topology, resulting in higher power factor levels.

Figure 6.10 – Simulation waveforms for both hybrid converter variances.



Source – Author.

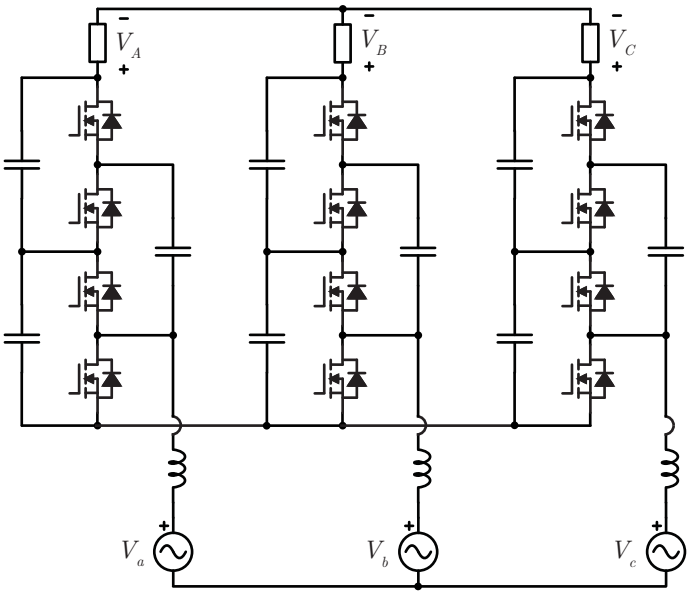
6.4 THREE-PHASE CONVERTER

Switched capacitor AC-AC converters have also been employed as three-phase electronic autotransformers. In (LAZZARIN; ANDERSEN; BARBI, 2015), a 110/220 V converter was proposed. It employs three ladder cells, which can be connected either in wye or delta configurations. A prototype was built and lead to a rated power of 6 kW and

an efficiency of 96.3%. Later on, a version employing two quadrant switches was presented (LUIZ et al., 2018). Its characteristics are similar two the double-ladder converter. The prototype was build to perform a 110/220 V conversion and obtained an efficiency of 95.1% at the rated power of 3.5 kW.

These configurations can also be extended to the hybrid topologies, as depicted in Figure 6.11. Their advantages are similar to the single-phase version. However, for the three phase four-quadrant version, at least two voltage sensors should be used. Thus, the reduced switch count topology may perform better, because of the simpler modulation schema.

Figure 6.11 – Three-phase AC-AC hybrid switched capacitor converter in a wye-wye-wye connnection.



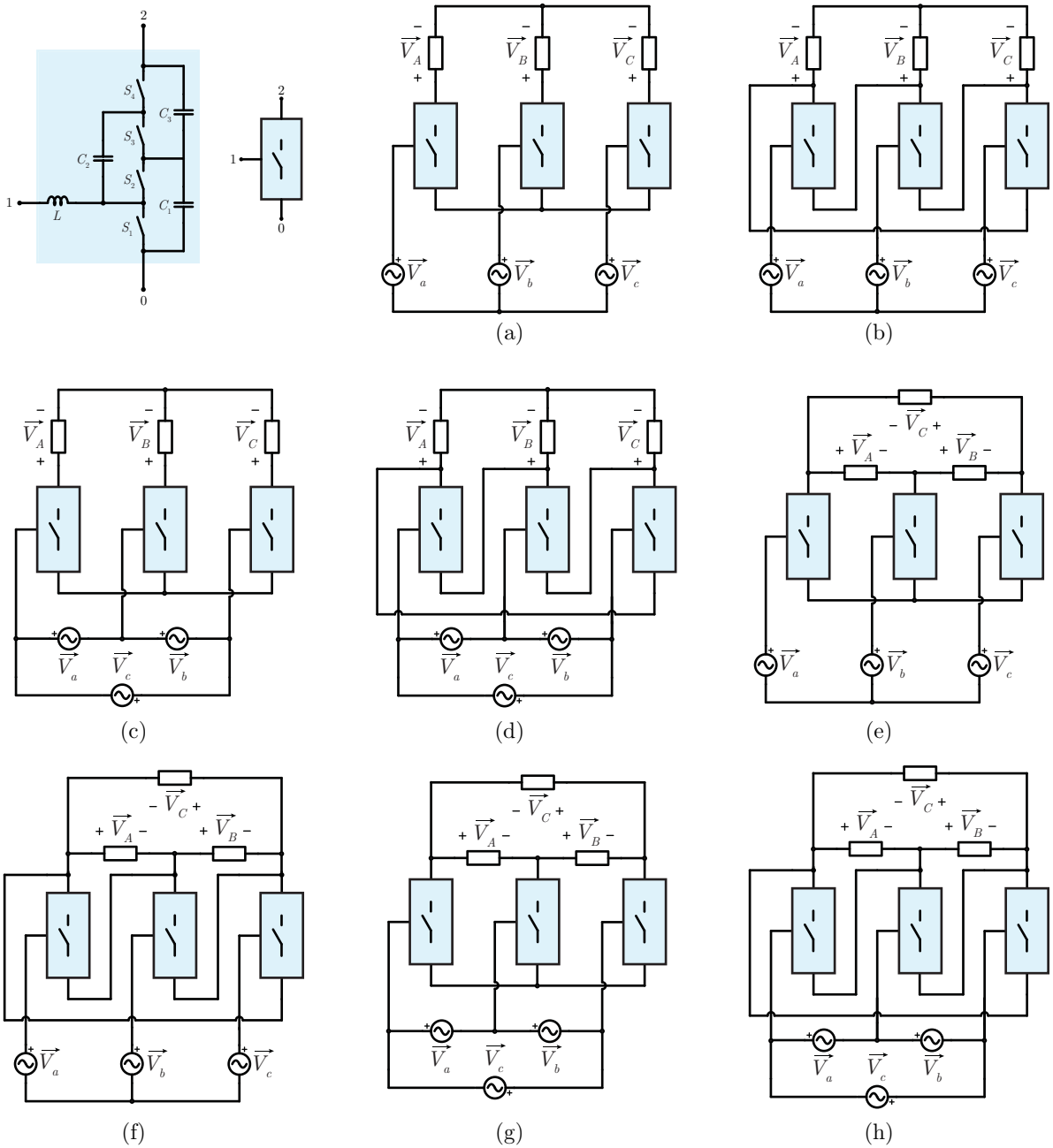
Source – Author.

Figure 6.12. presents a definition of the commutation cell and its simplified representation. All eight possible connections among three single-phase cells are presented in Figure 6.12(a)-(h).

6.5 SOFT SWITCHING

High peak values of currents in switched capacitor converters are usually inconvenient because they increase EMI problems as well as switching and conduction losses. In DC-DC switched capacitor converters, some authors tend to employ small inductances in series connection with the switched capacitor. Its function is to reduce the current's peak value during the commutations and provide soft-switching. The same could be applied to AC-AC converters.

Figure 6.12 – Possible connections for three-phase hybrid switched-capacitor cells.



Source – Author.

7 CONCLUSION

This thesis proposed and validated experimentally a single phase AC-AC hybrid boost switched capacitor converter.

In Chapter 2, the AC-AC switched capacitor basic cells were analyzed. Equations for the currents were obtained and two different methods were compared and verified by simulation results. The equivalent resistances for averaged model were obtained as function of the time constants, switching frequency and duty cycle. It is concluded that the accurate approximation is worth for low time constant-switching frequency product. Alongside the resistances, the active, reactive and apparent power were calculated, as well as the input power factor. It was concluded that the best operating point regarding the input power factor and current is for light inductive loads and high power levels.

Chapter 3 focused on the basic inductive AC-AC switching cell. The main operating waveforms and equations were obtained. An analysis of the equations was shown graphically, that highlighted the differences from a DC-DC and an AC-AC converter. The commutation problem was introduced, followed by a modulation strategy to overcome it. The modulation strategy is not employed at low voltage levels, thus, a voltage clamping circuit is necessary when traditional modulation schema is employed.

The AC-AC hybrid boost switched-capacitor topology was introduced and analyzed in Chapter 4. The steady-state analysis has shown results which consist of basic switched capacitor and inductive cell characteristics. An equivalent average model was obtained, as well as the dynamic transfer function. The effective current values were calculated by considering the charge flow quantity for no-charge and partial-charge operating modes. Project design considerations were stated and have shown the methodology to choose the capacitance values.

Experimental results were shown in Chapter 5. The operation in the rated operating points was validated. Tests were also carried out for different operating conditions, by changing: the input frequency, the load characteristic, the load value, the input/output connections and the duty cycles. In all tests the converter could operate, even though not at its best performance.

Chapter 6 expands the study area to other topologies, such as the structures which do not employ four-quadrant switches, the three-phase versions, different input-output connections, multiple outputs, higher number of voltage multiplier cells and resonant operation. Theoretically all these examples are feasible and require an especial study.

Overall, the positive characteristics of the hybrid AC-AC boost switched capacitor converter can be listed as:

- Provides the double of the gain comparing to a boost converter;
- Equal voltage sharing among the capacitors and switches, being the maximum value the half of peak output voltage;
- Output voltage peak/effective value is controllable via duty cycle variation;
- Easy control method, because its duty cycle is usually constant;
- Can operate at a wide range of input frequencies (from DC to some hundreds of Hz);
- Has multiple connections, allowing to obtain other gains;

Despite its positive characteristics, the converter presents some drawbacks:

- Needs the employment of bidirectional switches, leading to a high number of components;
- Employs high capacitance AC capacitors, which increases the area of the converter;
- Alternative modulation technique is necessary, needing the output voltage measurement, even in open-loop operation;
- Presents an internal reactive circulating current.

Other characteristics are dependent on the application:

- Input power factor varies with the load characteristics;
- Best operation is at light inductive loads;
- Can supply energy to a non-linear load. However, the input current presents more harmonic distortion than the current at the load and the output voltage is distorted;
- The efficiency is higher for medium range of duty cycles (between 0.3-0.6).

As a final conclusion, the converter is an alternative for AC-AC converters where isolation is not a requirement and a high controllable output voltage is necessary.

7.1 FUTURE WORKS

This thesis has contributed with the analysis and project of an hybrid AC-AC switched capacitor-based converter. Further possible studies include the following:

- Experimental verification of a three-phase structure;
- Analysis of different modulation schema for the resonant variation;
- Operation at higher switching frequencies;
- Experimental validation of other similar hybrid structures;
- Study of isolated topologies;
- Experimental analysis of increased number of switched-capacitor cells.

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APPENDIX A – INPUT INDUCTOR DESIGN

This appendix presents the procedure for the inductor design. Design equations are based on (KAZIMIERCZUK, 2009).

Regarding the inductor design, two necessary parameters are needed initially: the inductance and the current. Both are computed by analyzing the converter and setting a maximum desirable current ripple. The peak current is given by

$$I_{ip} = \sqrt{2} I_i \left(1 + \frac{\Delta I_{i\%}}{2} \right), \tag{A.1}$$

where I_i is the effective value of input current and $\Delta I_{i\%}$ the percentual peak-to-peak current ripple. The inductance value is determined by (A.2), where V_i is the effective value of input voltage, D is the duty cycle and f_s is the switching frequency.

$$L_i = \frac{V_i D}{I_i f_s \Delta I_{i\%}} \tag{A.2}$$

A first project equation relates the minimum product of areas of the selected core. It considers both the window area A_w and the magnetic area A_e. The equation (A.3) is employed to guarantee that the core do not saturate and there is enough place for the wire.

$$A_e A_w = \frac{L_i I_{ip}}{k_u J_{max} B_{sat}} \tag{A.3}$$

The project consider a toroidal amorphous powder core, whose saturation flux density is 1.5 T. Values considered in the project are summarized in Table A.1.

Table A.1 – Parameters and specifications for the inductor design.

Parameter	Symbol	Value
Inductance	L_i	130 H
Peak current	$I_{i,max}$	31.5 A
Effective current	I_i	20.2 A
Occupation factor	k_u	0.5
Current density	J_{max}	600 A/mm^2
Magnetic field density	B_{sat}	1.5 T
Area product	$A_e A_w$	28,680 mm^4

Among the available cores, the APH46P60 was chosen, which has a product of areas greater than the minimum specified. Informations about this core are presented in Table A.2.

As the core is toroidal, there is no gap do adjust the inductance. Thus, it can be

Table A.2 – Core parameters.

Parameter	Symbol	Value
Window area	A_w	426.4 mm^2
Magnetic length	L_e	107.4 mm
Magnetic area	A_e	199.0 mm^2
Magnetic volume	V_e	22,609 mm^2
Areas product	$A_e A_w$	84850 mm^4
Averaged turn length	L_{avg}	6.21 cm
Relative permeability	μ_r	60

adjusted only by the number of turns, with the following relation:

$$N_t = \sqrt{\frac{L_i L_e}{\mu_r \mu_0 A_e}}. \tag{A.4}$$

The relative permeability is a function from the magnetic field, which can be computed by (A.5). Based on this equation, it is possible to estimate the inductance value at the current's peak value.

$$H_{max} = \frac{N_t I_{i,max}}{L_e}. \tag{A.5}$$

In order to verify if the core will not saturate, the magnetic flux density is given by (A.6). The obtained value is shown in Table A.3. As it is smaller than 1.5 T, it diminish the possibility of saturation.

$$B_{max} = \frac{\mu_r \mu_0 N_t I_{i,max}}{L_e} \tag{A.6}$$

Core losses are tied to the variation of flux density, which at the switching frequency is given by

$$\Delta B(\omega_t) = \frac{D}{2 f_s N_t A_e} v_i(\omega_t). \tag{A.7}$$

Noting that the parameter ΔB is the peak variation value (not peak-to-peak). It is substituted in the power density equation, which is provided by the manufacturer:

$$p_{L,core} = \begin{cases} 36\Delta B^{2.22} f^{1.184} & if \quad 1kHz < f < 49kHz \\ 55.6\Delta B^{2.20} f^{1.65} & if \quad 50kHz < f < 99kHz \\ 820\Delta B^{2.19} f^{1.06} & if \quad 100kHz < f \end{cases} \tag{A.8}$$

As the magnetic flux variation is a function of ωt, the averaged losses in the core

are

$$P_{L,core} = \frac{V_e}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} p_{L,core}(\omega t) d(\omega t). \tag{A.9}$$

Regarding the conductors, there are some concerns: a) the maximum current density value must be satisfied; b) enough window area should be available for the minimum number of turns; c) the skin effect should be minimized and d) the project must the feasible.

The minimum conducting area is computed by (A.10) and the result for this project is displayed in Table A.3.

$$S_{cond} = \frac{I_i}{J_{max}}. \tag{A.10}$$

Table A.3 – Computed parameters

Parameter	Symbol	Value
Number of turns	N_t	31
Magnetic inductance variation	ΔB	0.061 T
Maximum magnetic field	H_{max}	112 Oe
Maximum magnetic inductance	B_{max}	0.675 T
Minimum conductor area	S_{cond}	0.034 cm^2

Based on the available wires, a Litz-wire 450x38 AWG was chosen. Its parameters are summarized in Table A.4 .

Table A.4 – Wire parameters

Parameter	Symbol	Value
Wire type	AWG 38	
Per length resistance	r_L	2.8917 Ω/m
Copper area	A_{cu}	$80{\cdot}10^{-6}$ cm^2
Isolated area	A_{wire}	$130{\cdot}10^{-6}$ cm^2
Number of parallel wires	N_p	450
Total isolated area	$A_{w,min}$	$1.789{\cdot}\ 10^{-4}$ m^2

If the relation shown in (A.11) is satisfied, then the project is feasible. It compares the total isolated are with the window area, considering the occupation factor.

$$\frac{N_p A_{wire}}{k_u A_w} \leq 1 \tag{A.11}$$

The total wire length is estimated by multipling the number of turns and the

averaged turn length:

$$L_{total} = N_t L_{avg}. \tag{A.12}$$

Thus, the equivalent resistance is

$$R_L = r_L \frac{L_{total}}{N_p}, \tag{A.13}$$

where N_p is the number of parallel conductors and r_L the resistance per length of a single conductor. Then, conduction losses can be estimated by

$$P_{L,cond} = I_i^2 R_L. \tag{A.14}$$

The total losses on the inductor are the sum of conduction and core losses:

$$P_L = P_{L,cond} + P_{L,core}. \tag{A.15}$$

APPENDIX B – SWITCHES LOSSES

The conduction losses in a MOSFET are estimated by (B.1), where I_{ef} is the effective value of the current and $r_{DS,on}$ the conduction resistance when the MOSFET is turned on.

$$P_{S,cond} = I_{ef}^2 r_{DS,on} \tag{B.1}$$

An important factor is the increase of $r_{DS,on}$ with the temperature. On SiC MOSFETs this temperature coefficient is usually smaller than on CMOS. Regarding switching losses, they are composed by turn-on and turn-off losses. It can be determined by

$$P_{S,sw} = V_{com}\left(I_{on}t_{on} + I_{off}t_{off}\right)f_s + \frac{1}{2}C_{oss}V_{com}^2 f_s, \tag{B.2}$$

however, as the converter operates as an AC-AC converter, the commutation voltage V_{com}, the currents during turn on and turn off (I_{on} and I_{off}), the commutation times t_{on} and t_{off}, and even the output capacitance C_{oss} are not constant. Thus, the switching losses are initially determined for a specific operation point, and then, generalized. Then, the rise time is computed as the necessary time the gate voltage needs to rise from the threshold voltage to the müller voltage. The obtained equation is:

$$t_r = -R_g C_{iss,i} ln\left(\frac{V_{gh} - V_{m,on}}{V_{gh} - V_{th}}\right). \tag{B.3}$$

The time to charge the müller capacitance from the plateau voltage to the commutation voltage is given by a simplified equation:

$$t_{d,on} = R_g \frac{C_{rss,i}V_{min} + C_{rss}(V_{com} - V_{min})}{V_{gh} - V_{m,on}}. \tag{B.4}$$

The total turn-on time equals to

$$t_{on} = t_r + t_{d,on}. \tag{B.5}$$

During the turn off, the equations are:

$$t_r = -R_g C_{iss} ln\left(\frac{V_{gl} - V_{th}}{V_{gl} - V_{m,off}}\right), \tag{B.6}$$

and

$$t_{d,on} = R_g \frac{C_{rss,i}V_{min} + C_{rss}(V_{com} - V_{min})}{V_{m,off} - V_{gl}}. \tag{B.7}$$

The total turn-off time is

$$t_{off} = t_f + t_{d,off}. \tag{B.8}$$

Considering the losses to charge the output capacitance C_{oss}, they are also time-varying. The total energy is computed by

$$E = \int_0^{V_{com}} v d(c_{oss}(v)v). \tag{B.9}$$

and, if the output capacitance is constant during the switching interval:

$$E = \frac{1}{2} C_{oss} V_{com}^2. \tag{B.10}$$

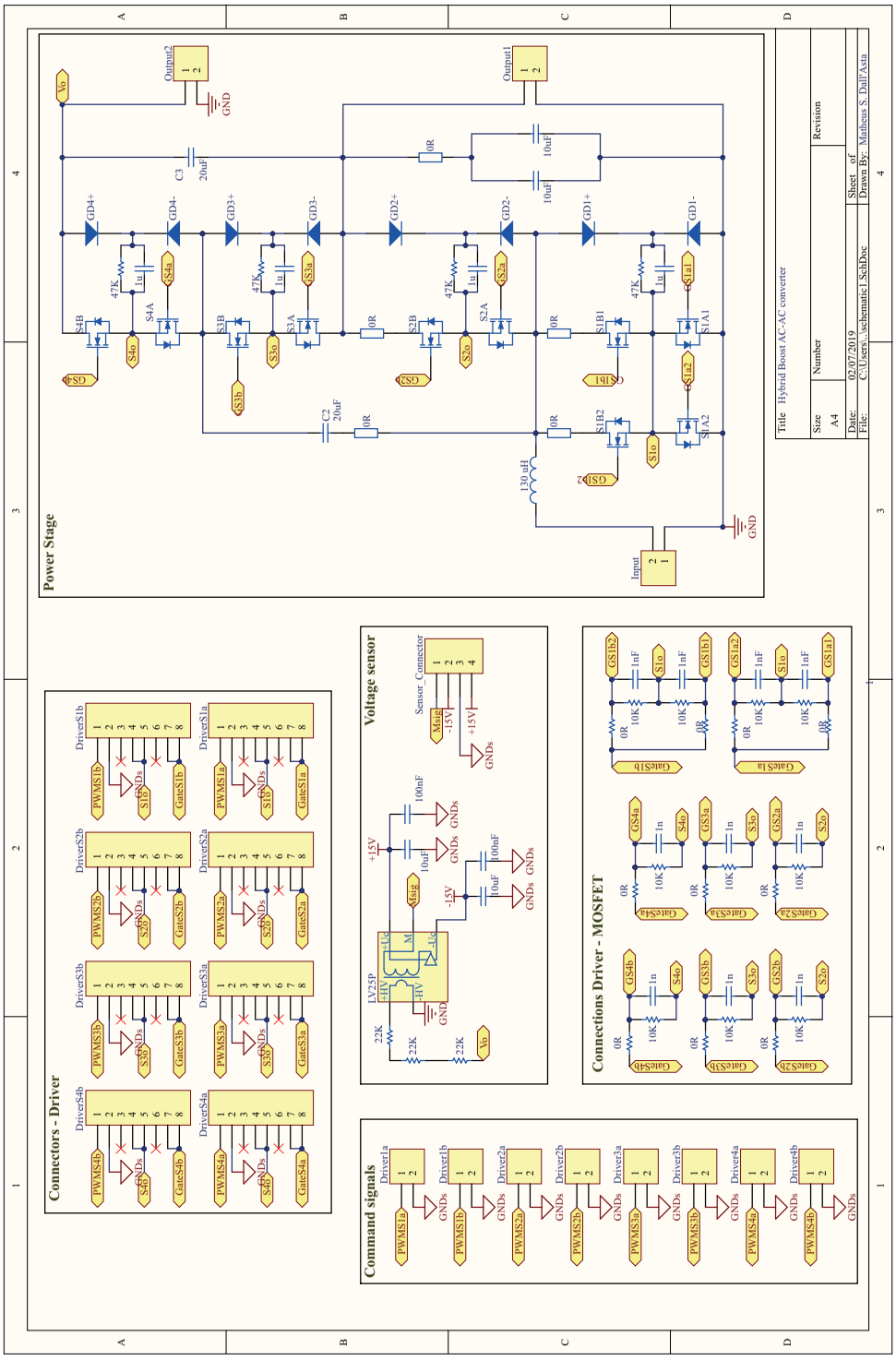
As the effective value of the current through switches S_1 are higher than switches S_2, S_3 and S_4 different MOSFETs were employed. Their parameters are displayed in Table B.1.

Table B.1 – Parameters of switches

SCT2120AF			
Parameter	Symbol	Value	Unit
Drain - Source voltage	$V_{DS,max}$	650	V
Continuous drain current (100 °C)	I_D	20	A
Conduction resistance (125 °C)	$R_{DS,on}$	149	mΩ
Output capacitance	C_{oss}	115	pF
Gate - Source voltage	V_{GS}	-6 to 22	V
Gate input resistance (internal)	R_G	13.8	Ω
SCT3080AL			
Parameter	Symbol	Value	Unit
Drain - Source voltage	$V_{DS,max}$	650	V
Continuous drain current (100 °C)	I_D	21	A
Conduction resistance (125 °C)	$R_{DS,on}$	105.6	mΩ
Output capacitance	C_{oss}	99	pF
Gate - Source voltage	V_{GS}	-4 to 22	V
Gate input resistance (internal)	R_G	13	Ω

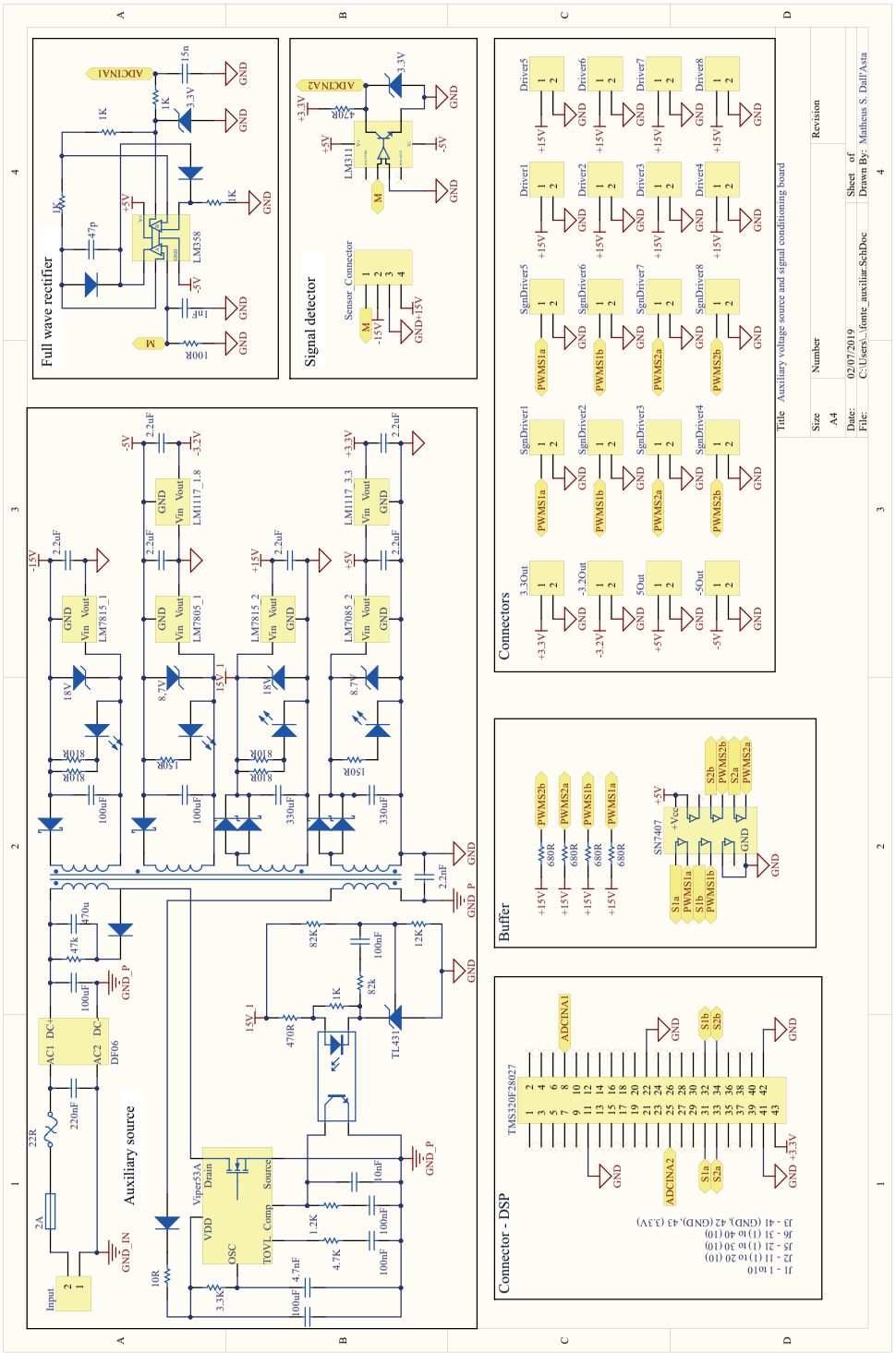
APPENDIX C – SCHEMATICS

Figure C.1 – Schematic of the power stage.



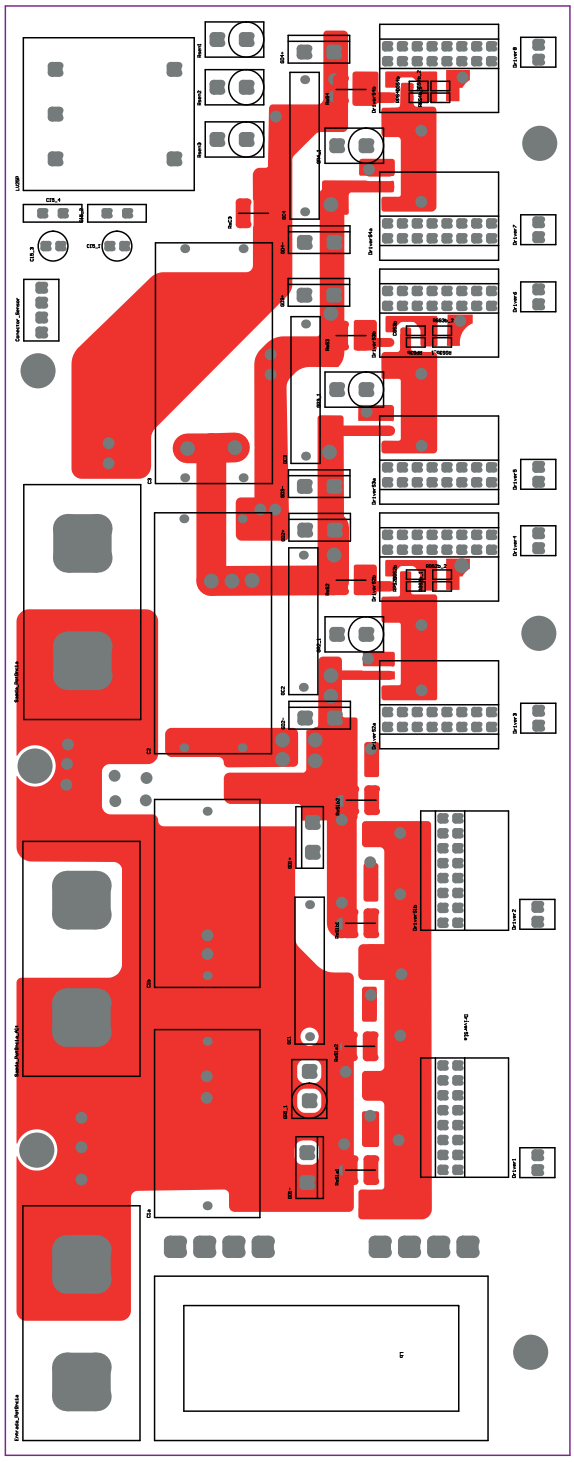
Source: Author.

Figure C.2 – Schematic of the auxiliary voltage source and signal conditioning board.



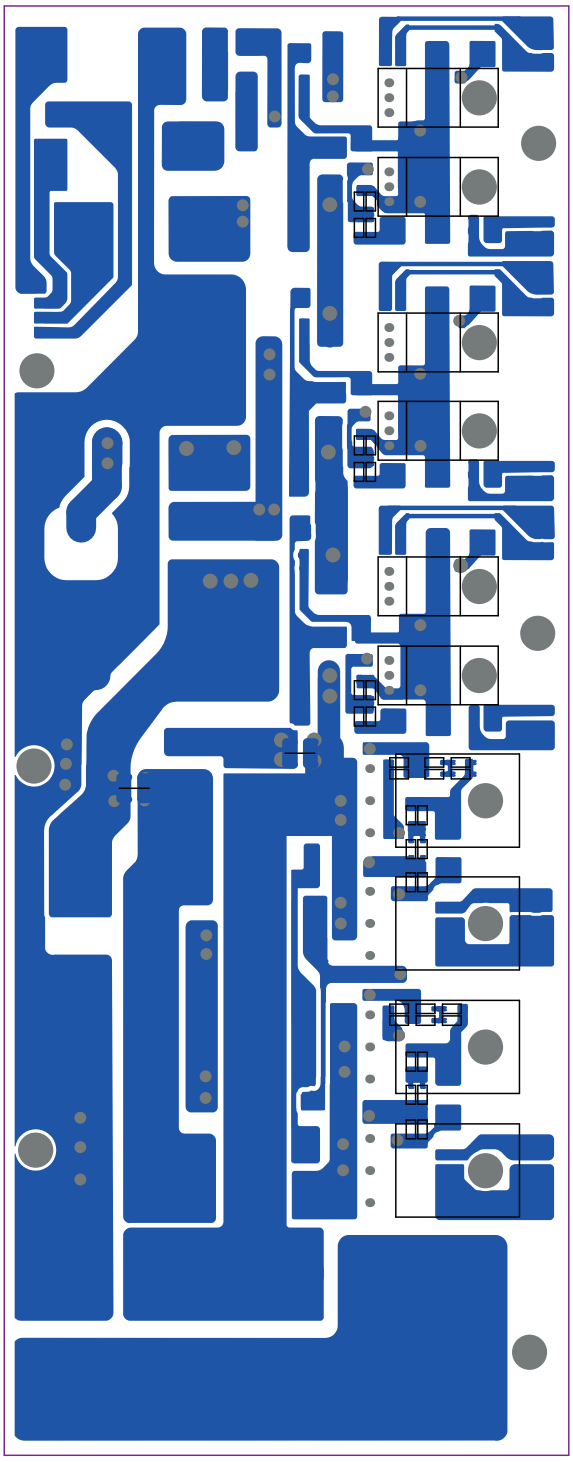
Source: Author.

Figure C.3 – Power stage PCB (top side).



Source: Author.

Figure C.4 – Power stage PCB (bottom side).



Source: Author.