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OPTIMAL DESIGN AND MODEL FOR CLLLC RESONANT CONVERTER

Florianópolis

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

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Resumo

O trabalho começa com uma revisão da literatura e contextualização do conversor CLLLC ressonante, o qual utiliza a modulação *Pulse Frequency Modulation* (PFM), empregada neste estudo. São analisadas as diferentes regiões possíveis de operação do conversor, sendo apenas a região indutiva operacional, onde os interruptores são capazes de operar com *Zero Voltage Switching* (ZVS). Dentro da região indutiva, existem três regiões operacionais diferentes, cada uma delas com características distintas que são detalhadas ao longo do trabalho. Além disso, é realizada uma análise para garantir que o conversor opere com ZVS nos interruptores da ponte completa do primário.

As principais contribuições deste trabalho estão voltadas para o modelo do conversor por *Dynamic Phasors* (DP) e a otimização do projeto do conversor baseado em seu modelo de perdas. O uso de DP para obter o modelo se faz necessário devido às correntes no tanque ressonante serem senoidais ou praticamente senoidais, dificultando a obtenção do modelo utilizando apenas o modelo por valor médio. O modelo dinâmico aplicado ao controle do conversor também é determinado. O projeto otimizado do conversor tem como objetivo minimizar as perdas globais do sistema e encontrar o melhor projeto possível para os componentes disponíveis. Para realizar esta otimização, todos os modelos de perdas do conversor e de cálculo dos parâmetros foram determinados e implementados via algoritmo utilizando o *Particle Swarm Optimization* (PSO). O protótipo projetado é testado em diferentes pontos de operação, validando o seu funcionamento. Assim, a eficiência obtida pelo algoritmo é comparada com a eficiência do protótipo, validando o modelo de perdas.

Palavras-chave: Conversor CLLLC ressonante, fasores dinâmicos, otimização de conversores.

ABSTRACT

The work begins with a literature review and contextualization of the resonant CLLLC converter, which employs Pulse Frequency Modulation (PFM), utilized in this study. The different possible operating regions of the converter are analyzed, with only the inductive operating region, where the switches are capable of operating with Zero Voltage Switching (ZVS), considered. Within the inductive region, there are three different operational regions, each with distinct characteristics detailed throughout the work. Additionally, an analysis is conducted to ensure that the converter operates with ZVS in the switches of the primary full-bridge.

The main contributions of this work are focused on the converter model by Dynamic Phasors (DP) and the optimization of the converter design based on its loss model. The use of DP to obtain the model is necessary due to the currents in the resonant tank being sinusoidal or practically sinusoidal, making it difficult to obtain the model using only the average model. The dynamic model applied to the converter control is also determined. The optimized converter design aims to minimize the overall system losses and find the best possible design for the available components. To perform this optimization, all converter loss models and parameter calculation models were determined and implemented via algorithm using Particle Swarm Optimization (PSO). The designed prototype is tested at different operating points, validating its operation. Thus, the efficiency obtained by the algorithm is compared with the prototype efficiency, validating the loss model.

Key-words:CLLLC resonant converter, dynamic phasors, converter optimization.

Resumo Expandido

Introdução

Nas últimas décadas, a crescente complexidade e prevalência de cargas elétricas no cotidiano impulsionam uma necessidade crescente de conversores de potência de alta qualidade. A busca por estágios de potência confiáveis e eficientes tornou-se primordial para garantir um desempenho ótimo dos sistemas elétricos. Essa evolução não apenas atende às crescentes demandas por energia, mas também ressalta a busca por soluções mais sustentáveis e eficazes.

Para enfrentar os numerosos desafios de um mundo sustentável, estão sendo realizadas pesquisas em diversas áreas da tecnologia, uma delas são os conversores cc-cc bidirecionais aplicados em carregamento de veículos elétricos. Conversores cc-cc ressonantes tornaram-se uma ótima opção para conversão de energia em aplicações de baixa e alta tensão [1]. Seu design incorpora características que reduzem efetivamente as perdas de comutação nos interruptores na ponte inversora e no retificador de saída. Essa característica permite que eles operem em frequências de comutação mais altas, resultando em maior eficiência e em conversores de menores tamanhos [2].

A ponte completa no lado primário inverte a tensão de entrada, gerando uma forma de onda quadrada que é aplicada ao tanque ressonante. Consequentemente, a corrente circulante no tanque ressonante torna-se predominantemente senoidal. Essa corrente é controlada ajustando a frequência de comutação (f_{sw}), seja mais próxima ou mais distante da frequência de ressonância (f_{res}) do tanque ressonante. Por fim, a corrente no tanque ressonante é retificada pela ponte completa no lado secundário e filtrada [3].

O tanque ressonante pode consistir em diferentes combinações de indutores e capacitores [4]. Entre essas topologias, as mais comuns incluem: o conversor série ressonante (SRC) [5], o conversor paralelo ressonante (PRC) [6], o conversor série-paralelo ressonante (LCC) [7], o conversor LLC ressonante [8] e o conversor CLLLC ressonante [9]. O conversor CLLLC ressonante é escolhido neste trabalho devido à sua maior densidade de potência e menor estresse de corrente no interruptores.

Objetivos

O objetivo principal deste trabalho é investigar o conversor CLLLC ressonante e suas possíveis aplicações em sistemas de eletrônica de potência caracterizados por uma ampla gama de variações de tensão sob carga. O foco principal é explorar a eficiência do conversor em diferentes condições de operação.

Os objetivos específicos deste trabalho são:

- Analisar a eficiência e o desempenho do conversor CLLLC ressonante para diferentes tipos de cargas empregando PFM. Desenvolver um modelo de perdas para o conversor e comparar os resultados teóricos com os práticos em termos de eficiência;

- Desenvolver um modelo DP para obter valores em regime permanente e o modelo dinâmico do conversor ressonante CLLLC;

- Desenvolver um algoritmo de otimização utilizando equações teóricas validadas para determinar o design ótimo para um conjunto especificado de componentes.

Resultados

Observando os resultados obtidos por meio da optimização proposta, percebe-se que é possível determinar o projeto ótimo do conversor para um conjunto de componentes específicos. A abordagem de otimização permite o refinamento contínuo do projeto do conversor, utilizando os parâmetros de construção disponíveis para assegurar a melhor configuração possível.

Os testes realizados em bancada corroboram os resultados obtidos no processo de otimização do conversor, apresentando uma eficiência de pelo menos 95% em todos os pontos e atingindo um máximo de eficiência próximo de 98%. Isso valida o método empregado para a construção do conversor.

Considerações Finais

Visando aumentar o desempenho do conversor, sugerem-se os seguintes tópicos para trabalhos futuros:

- Análise do conversor com modulação de fase-frequência.

- Desenvolvimento de uma metodologia para SR do circuito secundário empregando uma técnica sem sensor.

- Integração do indutor ressonante e do transformador em uma estrutura magnética unificada para alcançar uma maior redução no tamanho do conversor.

- Comparação do conversor CLLLC ressonante com outros conversores ressonantes listando as vantagens e desvantagens de cada topologia.

Palavras-chave: Conversor CLLLC ressonante, fasores dinâmicos, otimização de conversores.

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LIST OF ABBREVIATIONS AND ACRONYMS

ac	Alternate Current
dc	Direct Current
DP	Dynamic Phasors
EMI	Electromagnetic interference
ESL	Equivalent series inductance
ESR	Equivalent series resistance
LCC	Series-parallel resonant converter
PFM	Pulse Frequency Modulation
PRC	Parallel resonant converter
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
SRC	Series resonant converter
SR	Synchronous Rectification
ZCS	Zero current switching
ZVS	Zero Voltage Switching

LIST OF SYMBOLS

A_e Cross-sectional Area

A_t Radiating surface area

B_c Magnetic flux density

B_{pk} Peak of the magnetic flux density

C_1 Primary series capacitance

C_2 Secondary series capacitance

C_d Damping capacitor

C_{int} Integral controller

C_o Output capacitance

C_v Voltage controller

C_i Current controller

C_{oss} Output capacitance of the mosfet

ΔT Temperature variation

$\exp(\cdot)$ Exponential function

E_{on} Turn on energy

E_{off} Turn off energy

F_P Proximity effect factor

F_S Skin effect factor

$f_{g,peak}$ Resonant frequency peak

f_{res} Resonant frequency

f_{sw} Switching frequency

$f_{sw,max}$ Maximum switching frequency

f_n Normalized frequency

N	Number of turns
N_{Cap}	Number of parallel capacitors
N_L	Number of inductor turns
N_P	Number of turns in the transformer primary
N_S	Number of turns in the transformer secondary
$N_{C,p}$	Number of primary capacitors in parallel
$N_{C,s}$	Number of secondary capacitors in parallel
$N_{L,p}$	Number of primary inductor turns
$N_{L,s}$	Number of secondary inductor turns
n	Turns ratio of the transformer
n_k	Number of strands
$\overline{\eta}design$	Average efficiency
P_o	Output power
$Pcond$	Conduction losses
P_{core}	Core losses
P_{ESR}	Resistive losses of capacitor
P_{losses}	Power losses
P_{on}	Turn on losses
P_{off}	Turn off losses
P_{total}	Total loss
$P_{Winding}$	Winding losses
ψ	Surface power loss density
Q	Quality factor
R_{ac}	ac load impedance
R_d	Damping resistance
R_{DSon}	drain-to-source resistance
R_{Lo}	Output inductance resistance
R_L	Series inductor resistance
R_o	Output Resistance

$R_{w,ac}$	ac resistance
$R_{w,dc}$	dc resistance
t_{db}	Dead band time
T	Length of the window
$\Re c$	Core reluctance
$\Re g$	Gap reluctance
$\Re eq$	Equivalent reluctance
$\Re\left\{\cdot\right\}$	Real part of a complex number
Vab	Square wave voltage input
V_{cd}	Square wave voltage output
V_{in}	Input voltage
V_o	Output voltage
$V_{o_{nom}}$	Nominal output voltage
v_{bat}	Battery voltage
v_{C1}	Voltage in the primary capacitor
v_{C2}	Voltage in the secondary capacitor
v_{Cd}	Voltage in damping capacitor
v_{Co}	Voltage in output capacitor
$\vec{P}_{out}$	Output power vector
$\vec{V}_i$	Input voltage vector
$\vec{V}_{out}$	Output voltage vector
d_l	Diameter of the conductor of the litz-wire strand
H_c	Magnetic field intensity
η	Efficiency
η_p	Litz wire porosity factor
ϕ	Magnetic flux
$\left|\cdot\right|$	Absolute value of the variable
$\text{sign}\left(\cdot\right)$	Sign of the variable
ω_s	Angular frequency

CONTENTS

1

INTRODUCTION

1.1 MOTIVATION

In recent decades, the rising complexity and prevalence of electrical loads in daily life have spurred an increasing need for high-quality power converters. The quest for reliable and efficient power stages has become paramount to ensure optimal performance of electrical systems. This evolution not only addresses the growing demands for energy but also underscores the pursuit of more sustainable and effective solutions.

Power converters serve an important role in connecting electrical loads to sources, direct current (dc), and alternating current (ac). These components are integral in a wide range of power output, which is required for specific applications; from low-power LED lighting to high-power battery chargers designed for electric vehicles.

The demand for power from different dc loads, such as data centers [13, 14], electric vehicle charging stations [15, 16, 17], LED lamps [18], etc., has increased substantially. Consequently, dc distribution systems have attracted considerable interest across different industry sectors. This interest is particularly notable in the renewable energy field, which includes, photovoltaic modules (PV) , fuel cells, and storage batteries. The potential benefits of these systems in terms of efficiency and cost reduction have made them a compelling subject for research [19].

Bidirectional dc-dc converters are attracting considerable interest in both academic research and industrial applications. They are essential for optimizing system performance and serve as the connection points between batteries and supercapacitors, which are used as storage devices [20]. These applications include, but are not limited to, energy storage systems, uninterruptible power supplies, electric vehicles, and renewable energy systems, among others.

1.2 LITERATURE REVIEW

1.2.1 Battery charging applications

Over the past decade, the energy crises and reliance on fossil fuels intensified the demand for cleaner technologies. Transportation and energy sectors, being major contributors to CO_2 emissions, are undergoing a transition to electrification, aided by smart electrical grids, to significantly reduce emissions. Electric vehicles have emerged as a promising ecological alternative to internal combustion engines, gaining popularity worldwide. Collaborative efforts between researchers and governments are promoting technological advancements and widespread adoption of clean energy solutions [21].

Currently, charging levels are classified into three tiers, by [22], determined according to factors such as power capacity, charging duration, and charger infrastructure. The characteristics of each tier directly influence considerations of cost, network topology, and the impacts generated on the grid. The charging levels for electric vehicles are categorized as follows:

- Level-1 (ac): This is the slowest method. It is usually used in households. Additional infrastructure is not necessary. The power reaches around 1.44 kW to 1.92 kW;

- Level-2 (ac): Typically used in public and private environments, Level-2 charging requires additional infrastructure and can deliver up to 19.2 kW;

- Level-3 (dc): This method is referred to as fast chargers and includes dc chargers, where the power conversion occurs externally, directly injecting energy into the battery. These chargers have a power capacity ranging from 50 kW to 350 kW.

In Level-1 and Level-2 charging, the energy conversion is performed by on-board chargers located inside the electric vehicle, whereas in Level-3 charging, the energy conversion is carried out by off-board chargers, meaning the conversion of energy occurs externally to the vehicle.

Table 1.1 presents the specifications of some electric vehicles available in the market. As can be seen in Table 1.1, most of the electric vehicles listed have a nominal battery voltage of around 400 V. However, currently, electric vehicle chargers are designed to be compatible with potential electric vehicles capable of charging at 800 V. The 800 V voltage is achieved by modularizing 400 V converters, allowing for different voltage levels for the same charging infrastructure.

Electric vehicle charging structures typically operate in two stages. Initially, an ac-dc converter is utilized to convert electrical energy sourced from the grid. Subsequently, an isolated dc-dc converter adjusts voltage and current levels for delivery to the battery. Figure 1.1 illustrates this electric vehicle charging framework.

Table 1.1 – Charging specifications of some commercially available electric vehicles [12].

Model	Battery Voltage	Rated Energy	On-board charging Power (Time)	Maximum charging Power (Time)
eCitaro	400 V	182 kWh	N/A	300 kW (29min)
7900 Electric	600 V	150 kWh	11 kW (10.9 h)	300 kW (24 min)
Model S	400 V	100 kWh	11.5 kW (10.25 h)	250 kW (38 min)
E-tron 55 Quattro	396 V	95 kWh	11 kW (9.25 h)	150 kW (26 min)
EQC 400 4Matic	405 V	85 kWh	7.4 kW (10.5 h)	150 kW (31 min)
Taycan 4S	800 V	79.2 kWh	11 kW (9h)	270 kW (21 min)
Model 3	360 V	75 kWh	11.5 kW (7.75h)	250 kW (22 min)
Polestar 2	450 V	75 kWh	11 kW (7.75h)	150 kW (31 min)
Bolt	350 V	62.2 kWh	7.4 kW (8.3 h)	50 kW (66 min)
Leaf e+	360 V	62 kWh	6.6 kW (11.5 h)	100 kW (35 min)
Zoe ZE50	400V	54.7 kWh	22 kW (3 h)	50 kW (56 min)
Ioniq	320 V	40.4 kWh	7.2 kW (6.25 h)	100 kW (20.6 min)
Leaf	360 V	40 kWh	6.6 kW (6.5 h)	50 kW (40 min)
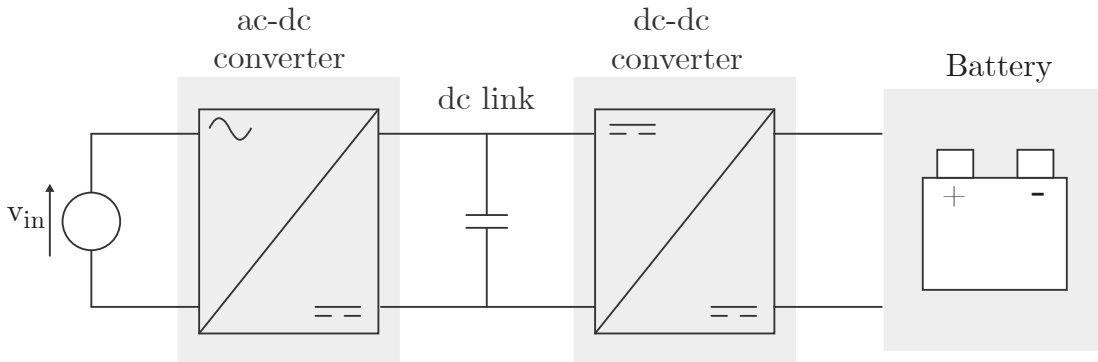
Figure 1.1 – Electric vehicle charging structure.

1.2.2 Resonant dc-dc converters

Resonant dc-dc converters have become the favored option for power conversion in which ones low- and high-voltage applications [1]. Their design incorporates features that effectively reduce switching losses at the inverter switches and output rectifier. This characteristic allows them to operate at higher switching frequencies, resulting in increased efficiency and smaller converter sizes [2].

Figure 1.2 portrays a general representation of the stages of isolated resonant converters. The full bridge on the primary side inverts the input voltage, generating a square waveform that is applied to the resonant tank. Consequently, the current circulating in the resonant tank becomes predominantly sinusoidal. This current is managed by adjusting the switching frequency (f_{sw}), either closer to or farther from the resonant frequency (f_{res}) of the tank. Eventually, the current in the resonant tank is rectified and filtered [3].

The resonant tank can consist of different combinations of inductors and capacitors
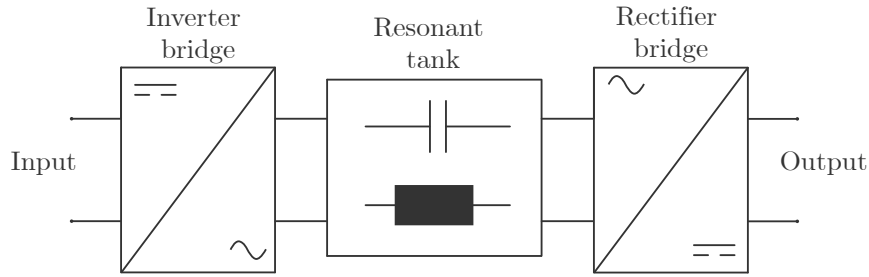
Figure 1.2 – General block diagram of resonant converters.

[4]. Among these topologies, the most common ones include: the series resonant converter (SRC) [5], the parallel resonant converter (PRC) [6], the series-parallel resonant converter (LCC) [7], the LLC resonant converter [8] and the CLLLC resonant converter [9].

The SRC converter is show in Figure 1.3. This converter operates with ZVS above the resonance frequency and zero current switching (ZCS) below it. At the resonance frequency, its voltage gain is unity. The current flowing through the resonant tank and the turn-off current are low at frequencies close to resonance. However, under light load and high input voltage, voltage regulation becomes difficult to achieve, and the circulating current increases. Furthermore, the efficiency of the SRC decreases as the switching frequency deviates from the resonant frequency [5].
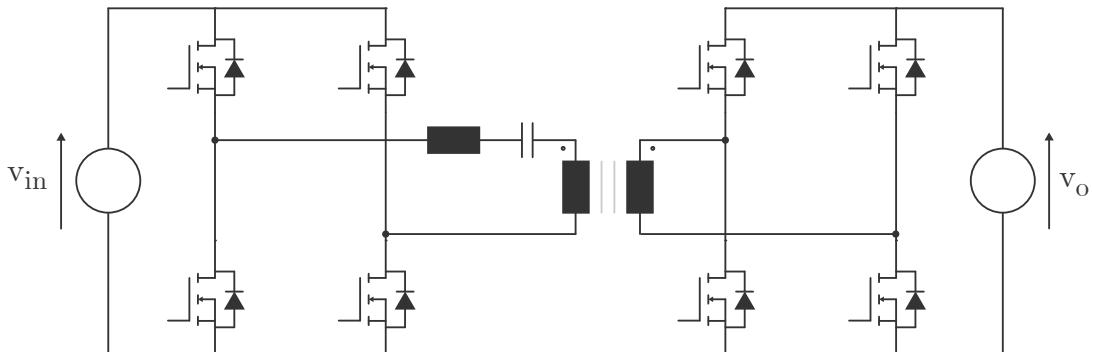
Figure 1.3 – SRC topology.

The PRC, portrayed in Figure 1.4, functions as a step-up converter capable of achieving ZVS and ZCS depending on the demanded current and voltage. However, this converter has notable disadvantages, including high circulating current and elevated turn-off current [6].

The LCC resonant converter, illustrated in Figure 1.5, integrates features from both the SRC and PRC converters. It has been demonstrated that the circulating current compared to the PRC and diminished load sensitivity compared to the SRC. However, it encounters heightened conduction and switching losses under high input voltage conditions [7].

The LLC resonant converter, as shown in Figure 1.6, has gained significant popularity due to its inherent advantages, which encompass wide voltage gain, a broad soft-switching region, galvanic isolation, high efficiency, and a high switching frequency.
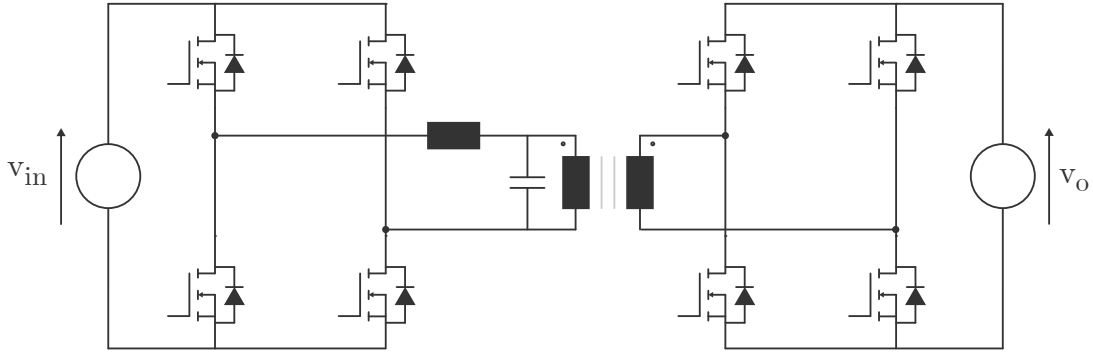
Figure 1.4 – PRC topology.
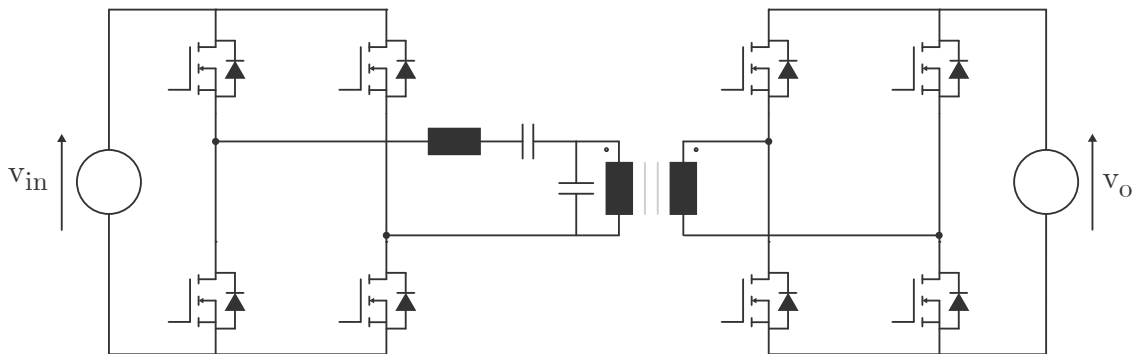
Figure 1.5 – LCC topology.

Furthermore, the primary switches of these converters operate with ZVS, while the output rectifier operates in ZCS. This characteristic yields lower switching losses and circulating currents in comparison to SRC, PRC, and LCC converters across a wide range of loads [8].
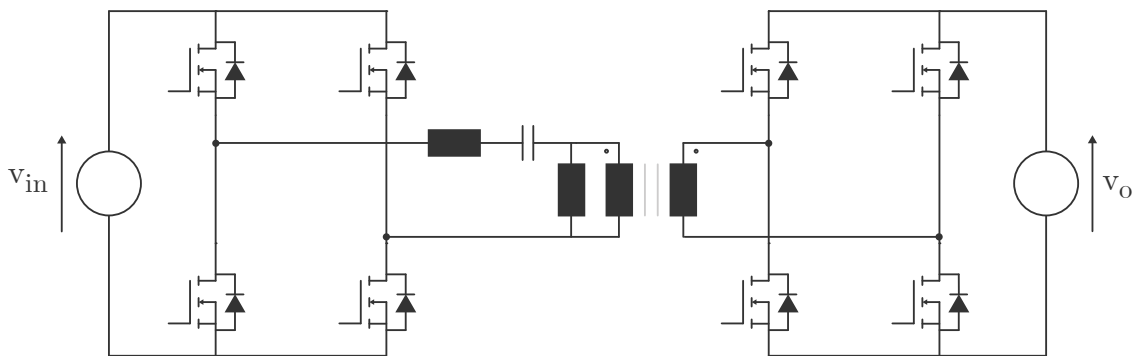
Figure 1.6 – LLC topology.

Bidirectional resonant topologies, particularly the CLLLC resonant converter topology shown in Figure 1.7, have attracted significant attention, especially in the context of electric vehicle charging applications [4, 9]. Another prevalent application of this topology is within dc microgrid systems [23]. This converter represents the bidirectional version of the LLC resonant converter [24]. The resonant tank comprises inductors, the transformer, and the resonant capacitors, which segregate the two full bridges of active switches. The transformer plays a pivotal role by providing galvanic isolation between the primary and secondary sides. The magnetizing and leakage inductances of the transformer are integrated

into the power stage, while the resonant capacitors not only shape the resonant tank but also prevent dc voltage shifts in the square wave generated by the inverter bridge [9].
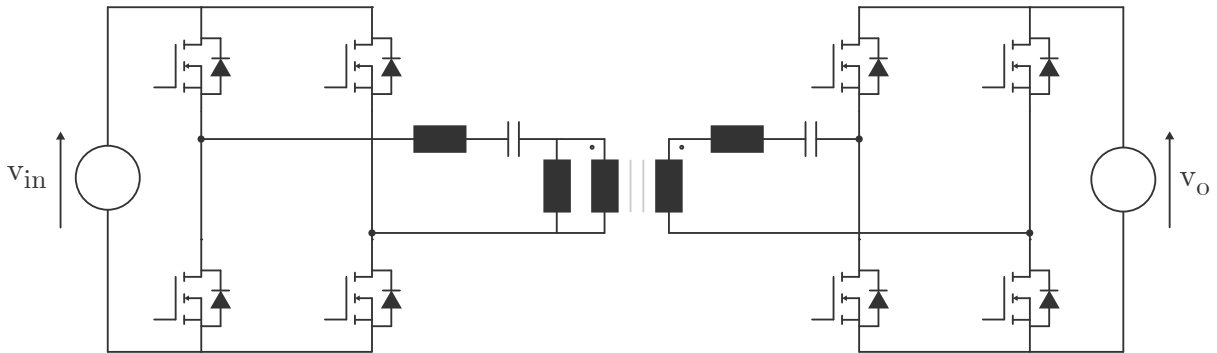
Figure 1.7 – CLLLC topology.

The CLLLC resonant converter is chosen in this work due to its higher power capability and lower ripple current on both the input and output sides. This results in reduced filter volume and consequently higher power density.

1.3 OBJECTIVES

The primary objective of this work is to investigate the CLLLC resonant converter and its potential applications in power electronic systems characterized by a wide range of voltage variations under load. The main focus is to explore the efficiency of the converter across different operating conditions.

The specific objectives of this work are:

- Analyze the efficiency and performance of the CLLLC resonant converter for different types of loads employing PFM. Develop a loss model for the converter and compare theoretical results with practical ones in terms of efficiency;

- Develop a DP model to obtain steady-state values and the dynamic model of the CLLLC resonant converter;

- Develop an optimization algorithm utilizing validated theoretical equations to determine the optimal design for a specified set of components.

1.4 WORK STRUCTURE

This work consists of six chapters and three apendices.

- **Chapter 1**: This chapter provides an overview of the topic, focusing on electric vehicles and various resonant dc-dc topologies.

- **Chapter 2**: This chapter provides a comprehensive review of the CLLLC resonant converter, encompassing analyses of its operation, impedance characteristics, and voltage gain of the resonant tank. Additionally, it explores PFM and SR techniques.

- **Chapter 3**: The focus revolves around DP applied in power electronics. This technique is utilized to ascertain the steady-state model of the CLLLC resonant converter. Its dynamic model is also determined, alongside its control strategy.

- **Chapter 4**: The loss model of the CLLLC resonant converter is presented, along with the calculation of passive elements for its resonant tank. An algorithm is implemented to optimize its design for maximum efficiency using specific sets of components.

- **Chapter 5**: The section details the construction of the converter prototype and its practical outcomes.

- **Chapter 6**: This section presents the conclusions and final insights derived from the dissertation, accompanied by proposals for future research paths.

- **Apendix A**: Representation state space systems.

- **Apendix B**: Testing of inductors and transformer.

- **Apendix C**: CLLLC resonant converter prototype.

CLLLC RESONANT CONVERTER REVIEW

This chapter provides a comprehensive review of the CLLLC resonant converter. It begins by outlining the distinction between resonant converters operating in the capacitive and inductive regions. Subsequently, an impedance-based analysis of the resonant tank is conducted to determine the gain characteristic curve of the converter for different output loads. Operating regions are defined, along with the minimum magnetizing inductance of the transformer required for ZVS operation in the primary switches. Modulation techniques for both primary and secondary switches are elucidated. Finally, simulations are presented to differentiate between the operating regions of the converter.

2.1 OPERATING PRINCIPLES

The resonant tank of the CLLLC resonant converter, presented previously in Figure 1.7, consists of inductors, capacitors, and a transformer. The transformer connects the primary full bridge to the secondary full bridge. The circuit of the CLLLC resonant converter can be simplified by adding an input source V_{ab} which symbolizes the square wave voltage input, activated or deactivated by the primary side switch, and output voltage source, V_{cd} which symbolizes the square wave voltage output applied to the secondary side switches. This simplification results in the model presented in Figure 2.1. Depending on the operational frequency, this tank exhibits either capacitive or inductive behavior, resulting in two distinct regions with different characteristics.
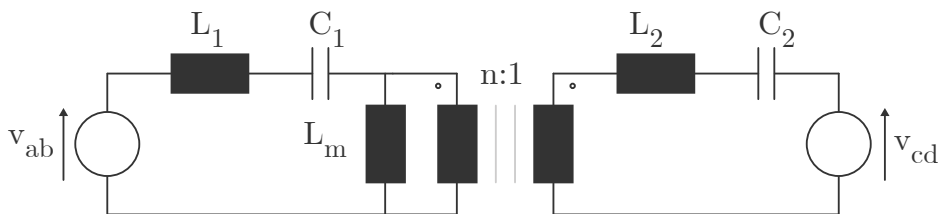
Figure 2.1 – Resonant CLLLC converter tank.

In the capacitive operating region, as demonstrated in Figure 2.2(a), the voltage and current waveforms of the resonant tank are displayed. In this scenario, the current
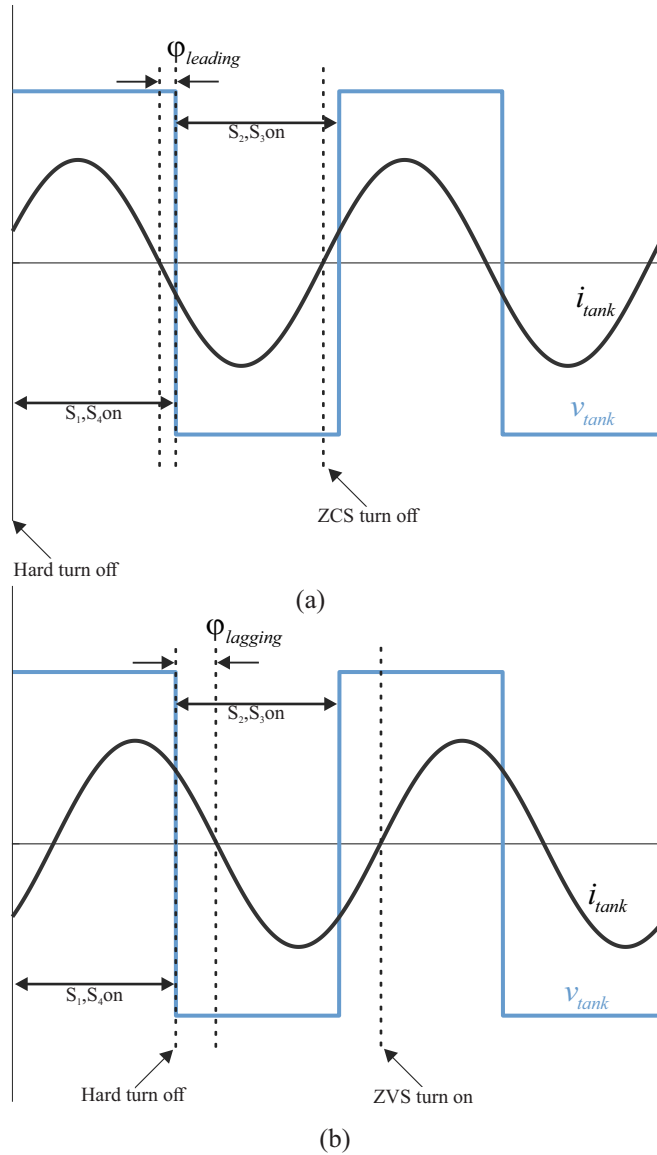
Figure 2.2 – CLLLC tank effect on current/voltage (a) capacitive region and (b) inductive region.

leads the voltage with a phase angle denoted as $\varphi_{leading}$. The switches undergo ZCS during turn-off. However, during switch activation and the subsequent deactivation of freewheeling diodes, a phenomenon of hard switching occurs. The reverse recovery process inherent to freewheeling introduces notable switching losses alongside substantial electromagnetic interference (EMI) noise. Given these challenges, it is advised to exercise caution when employing capacitive operation for high-frequency applications [25, 26].

In contrast, Figure 2.2(b) elucidates the waveforms of the resonant tank voltage and current when the circuit operates within the inductive domain. Here, the current lags behind the voltage by a phase angle designated as $\varphi_{lagging}$. As evident in the illustration, even though the switch turn-off procedure entails hard switching, the switch activation involves soft switching. Notably, the freewheeling diodes achieve soft switching during both their turn-on and turn-off phases.

This configuration eliminates reverse recovery losses attributable to the diodes and substantially reduces EMI noise. Given this analysis, in contexts characterized by high-frequency and high-power demands, the operation of the CLLLC converter necessitates functioning within the inductive region [25].

2.2   IMPEDANCE AND GAIN ANALYSIS

To determine the impedance of the CLLLC resonant converter tank, the equivalent circuit is illustrated in Figure 2.3. Here, v_{Rac} represents the resulting square-wave voltage, which emerges after undergoing processing through the resonant circuit and transformer [27].
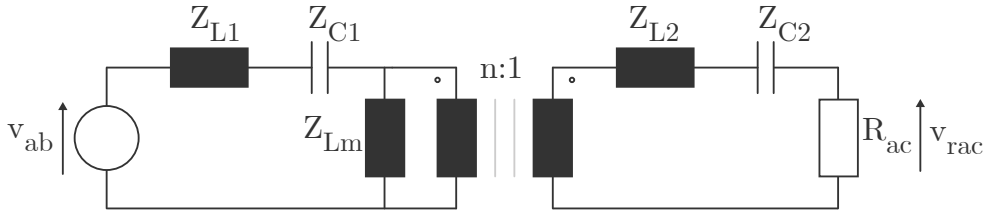
Figure 2.3 – Equivalent circuit diagram of the CLLLC resonant converter for impedance analysis.

The parameters denoted as Z_{L1}, Z_{L2}, Z_{Lm}, Z_{C1}, Z_{C2}, and R_{ac} represent key elements within the system: Z_{L1} designates the primary-side resonant inductance, Z_{L2} corresponds to the secondary-side resonant inductance, Z_{Lm} pertains to the magnetizing inductance, Z_{C1} pertains to the primary-side resonant capacitance, Z_{C2} signifies the secondary-side resonant capacitance, and R_{ac} signifies the equivalent primary-side ac load impedance, derived from the output load impedance, which is determined by

$$R_{ac} = n^2 \frac{8}{\pi^2} \frac{V_o}{I_o} = n^2 \frac{8}{\pi^2} R_o, \tag{2.1}$$

where n is the turns ratio of the transformer and R_o represents the effective output load.

The derivation of the voltage gain function between v_{Rac} and v_{ab} is accomplished through the application of a voltage divider, which adequately describes the relationship. The transfer function $G(j\omega)$ of the converter is elucidated in Equation 2.2.

$$G(j\omega) =$$
$$\frac{j\omega L_m R_{ac}}{\left(j\omega L_m + j\omega L_2' + R_{ac} + \frac{1}{j\omega C_2'} \right) \left(j\omega L_1 + \frac{1}{j\omega C_1} \right) + j\omega L_m \left(j\omega L_2' + R_{ac} + \frac{1}{j\omega C_2'} \right)}. \tag{2.2}$$

The parameters f_{res}, f_n, Q, k, m, and g have been explicitly defined with Equation 2.3 configuring the resonant parameters. These parameters are instrumental in the

design phase, enabling the utilization of software tools to generate a voltage gain curve based on the transfer function delineated in Equation 2.2.

$$f_{res} = \frac{1}{2\pi\sqrt{L_1 C_1}}, \quad f_n = \frac{f_{sw}}{f_{res}}, \quad Q = \frac{\sqrt{\frac{L_1}{C_1}}}{R_{ac}},$$
$$k = \frac{L_m}{L_1}, \quad g = \frac{C_2'}{C_1}, \quad m = \frac{L_2'}{L_1},$$

(2.3)

where f_{res} represents the resonant frequency, f_n signifies the relationship between switching frequency and resonant frequency, and Q denotes the quality factor.

The derivation of the equivalent circuit for the CLLLC resonant converter involves substituting Equation 2.3 into Equation 2.2, followed by a simplification process. During this transformation, the angular frequency is converted into the frequency domain. Consequently, the transfer function, denoted as G(fn), is represented by Equation 2.4.

$$G(f_n) = \frac{1}{\sqrt{A + B}},$$

(2.4)

where,

$$A = \left(1 + \frac{1}{k} - \frac{1}{k f_n^2}\right)^2,$$

$$B = Q^2 \left(\frac{1}{k g f_n^3} + f_n + \frac{m f_n}{k} + m f_n - \frac{1}{f_n} - \frac{m}{k f_n} - \frac{1}{k g f_n} - \frac{1}{g f_n}\right)^2.$$
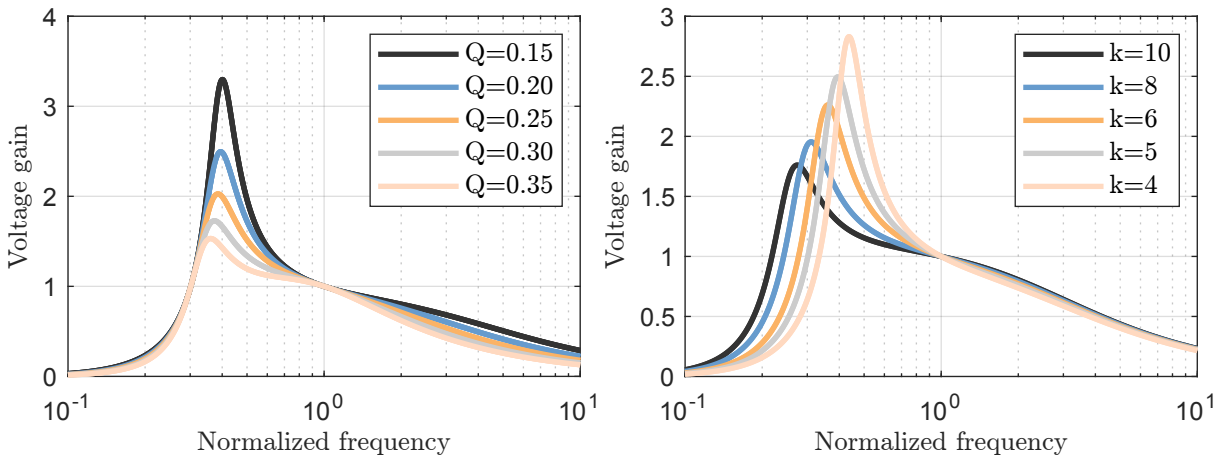
(a) Voltage gain curve for different Q values.

(b) Voltage gain curve for different k values.

Figure 2.4 − Voltage gain for different Q and k.

Figure 2.4a illustrates the converter gain relationship for different values of Q,

demonstrating that each variation in load characteristic results in a distinct response from the converter's resonant tank.

The same trend is observed in Figure 2.4b when varying the ratio between magnetizing inductance and leakage inductance. For lower values of k, the tank operates over a wider voltage range. However, a low k ratio indicates lower magnetizing inductance, resulting in increased current circulation, higher current ripple in the transformer, and consequently, greater conduction losses.

On the other hand, for higher values of k, the resonant tank's ability to provide gain in the system decreases. With higher magnetizing inductance, there is a reduction in circulating current in the transformer and a decrease in conduction losses, leading to higher efficiency in the converter.

It is important to highlight that for proper operation of the CLLLC resonant converter, there needs to be a balance in the k ratio to ensure that the converter delivers the necessary gain and operates efficiently.

2.3   SUITABLE OPERATING REGION

Illustrated in Figure 2.4a and 2.4b are the inductive and capacitive regions of resonance within the CLLLC circuit. The different operating regions of the converter are presented in Figure 2.5.
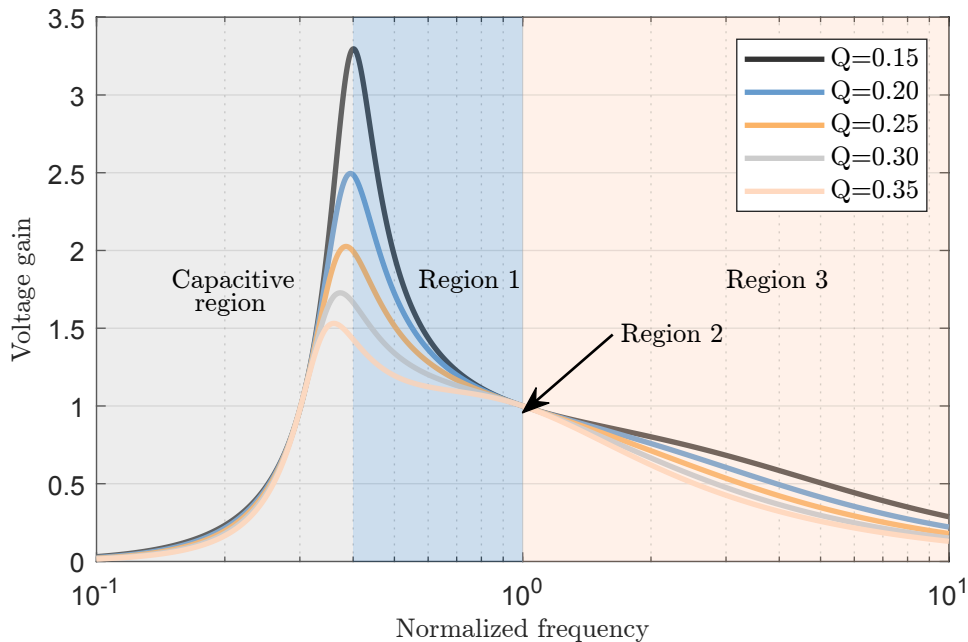
Figure 2.5 – Voltage gain curve for different Q values.

Where:

- **Capacitive region**: Switching frequencies before the voltage gain peak.

- **Region 1**: Switching frequencies between the peak of the voltage gain and the resonant tank frequency.

- **Region 2**: Switching frequency equal to the resonant tank frequency.

- **Region 3**: Switching frequencies higher than the resonant tank frequency.

The peak voltage gain in these figures delineates the capacitive and inductive operating regions of the converter. For frequencies up to the voltage gain peak, the tank impedance is capacitive, resulting in significant voltage variations and high losses, as the primary-side mosfets switch throughout this range without ZVS. It is not advisable to operate the CLLLC resonant converter in this region.

On the other hand, for frequencies beyond the peak voltage gain, the converter operates in the inductive region. In this region, the primary-side mosfets switch with ZVS, reducing the converter's switching losses. This represents the ideal operating region for the CLLLC resonant converter.

To determine the equation describing the frequency at the peak of the voltage gain, the following expression is used

$$f_{g,peak} = \frac{1}{2\pi\sqrt{(L_m + L_1)\, C_1}}. \tag{2.5}$$

As elucidated earlier, achieving soft switching is feasible within the inductive range. Ensuring ZVS during the switching of primary switches requires a sufficiently substantial magnetizing inductor current. This current facilitates the complete charging or discharging of the output capacitors of the mosfets within the dead band interval. The upper limit for the value of L_m is derived in [1] as follows

$$L_m \leq \frac{t_{db}}{16\, C_{oss}\, f_{sw,max}} \tag{2.6}$$

where t_{db} represents the duration of the dead band time, C_{oss} signifies the output capacitance of the mosfet, and $f_{sw,max}$ corresponds to the maximum switching frequency.

2.4   MODULATION STRATEGY

The most basic modulation for resonant converters is PFM. Unlike traditional modulation techniques such as Pulse Width Modulation (PWM), where the duty cycle of pulses is altered, PFM adjusts the frequency of switching pulses while keeping their widths constant [1, 28, 29].

In PFM, the duty cycle is fixed at 50%, and the switching frequency is varied [30]. The frequency variation that regulates the magnitude of the output voltage and current.Figure 2.6 presents the block diagram describing the strategy for implementing frequency modulation.

PFM is used to drive the switches of the full bridge on the primary side of the CLLLC resonant converter. For driving the switches of the full bridge on the secondary side, a SR strategy is implemented, where the mosfets operate in the same manner as
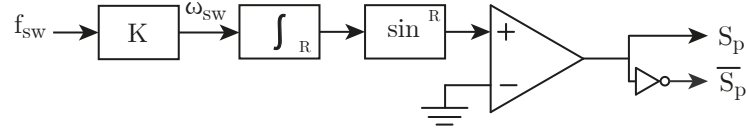
Figure 2.6 – PFM scheme for CLLLC resonant converter.

diodes. The motivation behind this approach is to reduce losses attributed to the voltage drop across the diodes. When employed, the secondary full bridge loss becomes just the resistance between the drain and source channels of the mosfets.

To implement the SR strategy, it is necessary to monitor the current on the secondary side of the transformer and trigger the switch activation pulse when the current value crosses zero, effectively causing the switches to operate like diodes. The block diagram in Figure 2.7 illustrates the strategy for generating the pulses to drive the secondary switches.
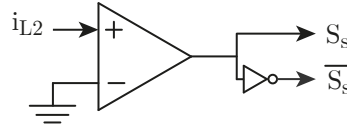
Figure 2.7 – SR scheme for CLLLC resonant converter.

2.5 DIFFERENT OPERATING CHARACTERISTICS WITHIN THE INDUCTIVE REGION

As discussed earlier, the CLLLC resonant converter should operate in the inductive region of its resonant circuit. However, the behavior of the resonant circuit varies at three points within this region: below the resonant frequency, above the resonant frequency, and exactly at the resonant frequency. It is important to recall that this resonant frequency is calculated by

$$f_{res} = \frac{1}{2\pi\sqrt{L_1 C_1}}. \tag{2.7}$$

To explore these three points, numerical simulations were conducted using the parameters specified in Table 2.1.

Table 2.1 – CLLLC resonant converter simulation parameters.

Parameters	Values
Primary and secondary resonant inductors (L_1, L_2)	24.8 μH
Primary and secondary resonant capacitors (C_1, C_2)	102.1 nF
Magnetizing inductance (L_m)	124 μH
Input Voltage (V_{in})	400 V
Turns ratio (n)	1
Output capacitor (C_o)	20 μF
Load resistance (R_L)	54 Ω

2.5.1   Region 1: below the resonant frequency

Figure 2.8 illustrates the currents in the resonant tank, transformer current, currents in the secondary switches during each half cycle, switching frequency and output voltage for a CLLLC resonant converter operating below the resonant frequency.

When the switching frequency is lower than the resonant frequency, the resonant tank functions as a boost converter, resulting in an output voltage higher than the input voltage. As the half-resonant cycle completes, the primary inductor current reaches the transformer's magnetizing current. At this point, the diodes in the primary full-bridge operate as freewheeling diodes, which is unique to this operating condition. Consequently, the secondary transformer current reaches zero, and the secondary-side rectifier disconnects. This phenomenon initiates and persists until the end of the switching cycle, as illustrated by the secondary transformer's inductor current in Figure 2.8. Conduction losses on the primary side increase due to the rise in circulating energy.

2.5.2   Region 2: at the resonant frequency

Figure 2.9 presents the currents in the resonant tank, transformer current, currents in the secondary switches during each half cycle, switching frequency, and output voltage for a CLLLC resonant converter operating at the resonant frequency.

This operating point occurs when the switching frequency equals the resonant frequency. Operating the converter at this frequency allows its resonant tank to achieve unity gain and operate optimally, resulting in the highest efficiency. During each half of the switching period, the resonant cycle completes fully. At the end of each switching period, the primary inductor current reaches the transformer's magnetizing current. At this moment, the secondary inductor current reaches zero, and the secondary full bridge switches with zero current. Additionally, the tank currents appear purely sinusoidal, transferring power only in one harmonic.

2.5.3   Region 3: above the resonant frequency

Figure 2.10 illustrates the currents in the resonant tank, transformer current, currents in the secondary switches during each half cycle, switching frequency, and output voltage for a CLLLC resonant converter operating above the resonant frequency.

In this scenario, the operating point occurs when the switching frequency is higher than the resonant frequency. When the converter operates at this point, the resonant tank functions as a voltage step-down (buck) converter. However, the resonant half-cycle is not fully completed and is interrupted by the beginning of the other half of the switching cycle. As a result, the primary-side mosfets experience higher output conduction losses. As illustrated in Figure 2.10, the current waveform deviates from being purely sinusoidal, indicating energy transfer across multiple harmonics.
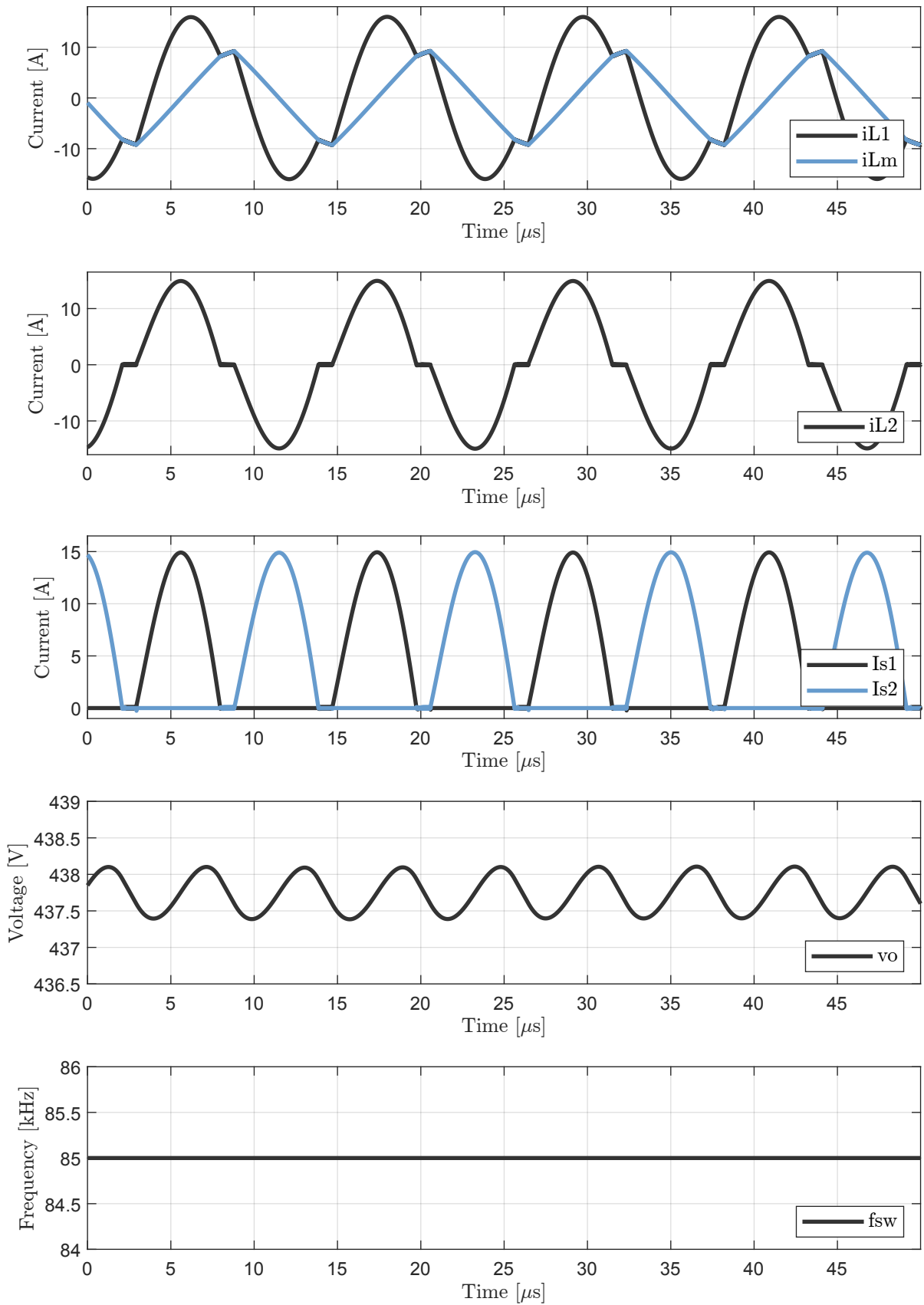
Figure 2.8 − Resonant CLLLC converter operating with $f_{sw} < f_{res}$.
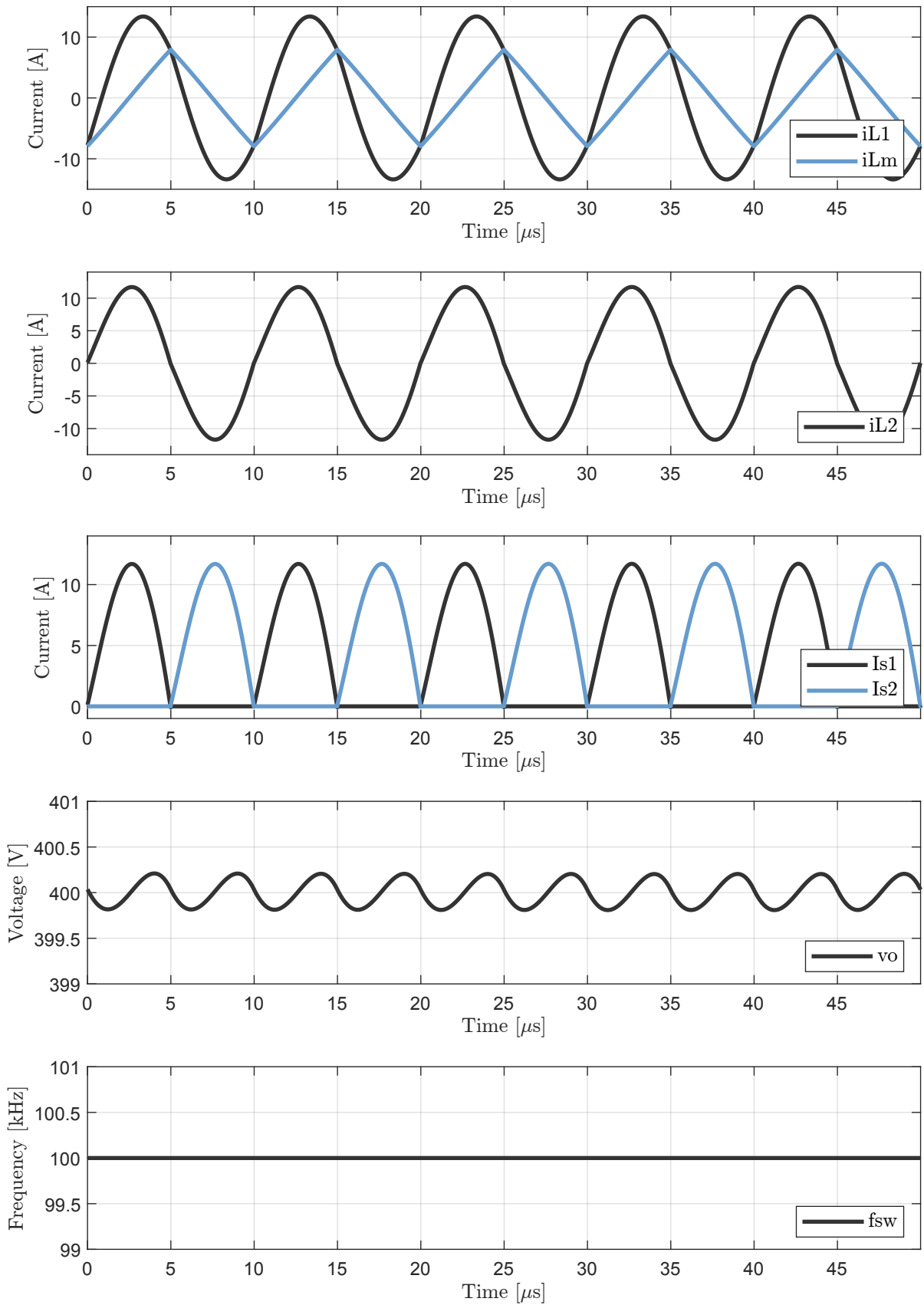
Figure 2.9 − Resonant CLLLC converter operating with $f_{sw} = f_{res}$.
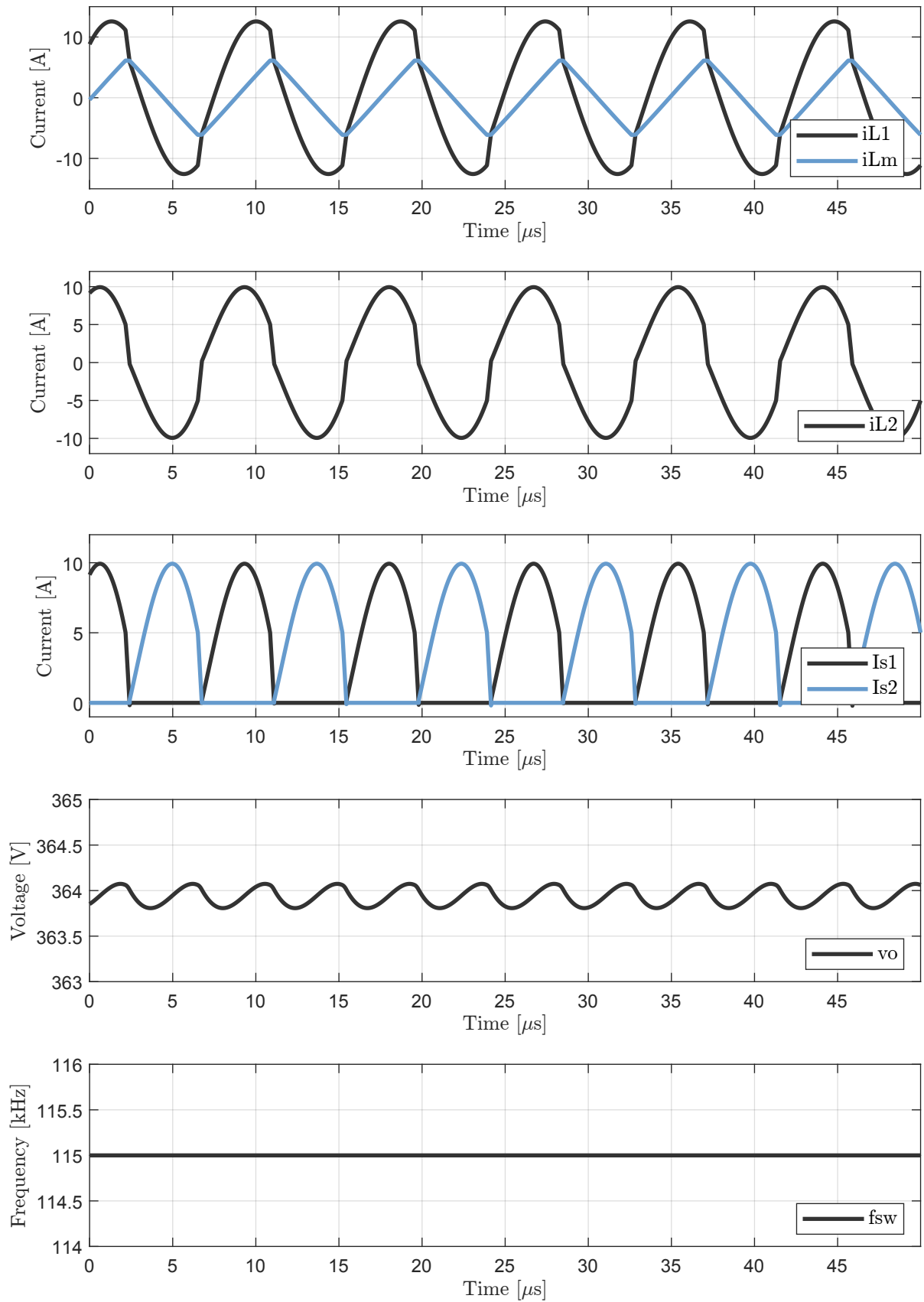
Figure 2.10 – Resonant CLLLC converter operating with $f_{sw} > f_{res}$.

2.6   SUMMARY

This chapter reviews the CLLLC resonant converter, beginning with an overview of resonant converters. Operating in the capacitive region implies minimal switching losses at the output during conduction, whereas the inductive region minimizes losses at the input.

The focus then shifts to the resonant tank analysis of the CLLLC converter. An impedance equation is derived, incorporating inductive and capacitive elements along with output load resistance. Plots depicting voltage gain versus frequency illustrate the tank's performance variability with quality factor (Q) and the ratio (k) between series inductance and transformer magnetizing inductance. Emphasis is placed on the converter's optimal operation within its inductive region.

Further discussions cover the equation determining the maximum inductance for achieving soft switching on the primary-side, as well as the modulation strategy. The CLLLC converter employs frequency modulation on primary switches and SR on secondary switches to minimize secondary-side switching losses.

Finally, the chapter explores the three operational regions within the inductive range of the CLLLC converter. Waveforms for each region are illustrated and discussed, providing a comprehensive understanding of the converter's performance characteristics.

3
MODELING AND CONTROL

In this chapter, the primary focus is on the theory of DP applied to power electronics. The contribution in this domain is delineated in the article "Generalized Averaging Method for Power Conversion Circuits" [31], which explains DP as time-varying coefficients of a generalized Fourier series. These coefficients represent electrical quantities in practical applications and are computed using a generalized averaging method. The necessity of using DP to obtain the model arises because the resonant tank currents of the CLLLC converter are nearly sinusoidal, making it impossible to model them using the average circuit method. To facilitate understanding of the presented concept, the application of DP to an LC series circuit is demonstrated. Finally, the model of the CLLLC resonant converter is determined and validated.

3.1 DYNAMIC PHASORS

Phasor analysis is a technique used to express steady-state sinusoidal quantities as complex numbers, considering only their magnitude and phase [32]. This type of analysis shifts the frequency spectra of the original system, transforming it so that constant complex numbers represent real sinusoidal quantities [33].

The DP model is based on the premise that an almost periodic signal, $x(\tau)$, oscillating at the fundamental frequency f and potentially containing high-order harmonics, can be adequately approximated within an interval $\tau \in (\text{t-T, t})$ using the complex exponential Fourier Series. [34, 35]. The basic principle of DP is represented by

$$x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega_s\tau}, \ \tau \, \epsilon \, (t-T, t), \tag{3.1}$$

$$\langle x \rangle_k(t) = \frac{1}{T}\left[\int_{t-T}^{t} x(\tau)e^{-jk\omega_s\tau}d\tau\right]. \tag{3.2}$$

where $\langle . \rangle_k$ denotes the kth DP and $\langle x \rangle_k$ is composed of real and imaginary parts, as shown

$$\langle x \rangle_k (t) = \frac{1}{T} \int_{t-T}^{t} x(\tau) \cos(k\omega_s \tau) \, d\tau$$
$$- \jmath \frac{1}{T} \int_{t-T}^{t} x(\tau) \sin(k\omega_s \tau) \, d\tau. \tag{3.3}$$

Since DP are essentially time-varying Fourier coefficients, they remain constant during steady-state conditions and exhibit slow variation during transient processes [36]. When utilizing the DP method for waveform and mathematical model representation, larger step sizes become feasible for simulations [37].

Figure 3.1 provides a graphical representation of the DP, which are defined at both the fundamental frequency and all of its harmonics. The coefficients of the series are calculated for a portion of $x(t)$ determined by a moving window of duration T [31]. This window subsequently moves across the waveform, computing a fresh set of DPs at each time point [10].
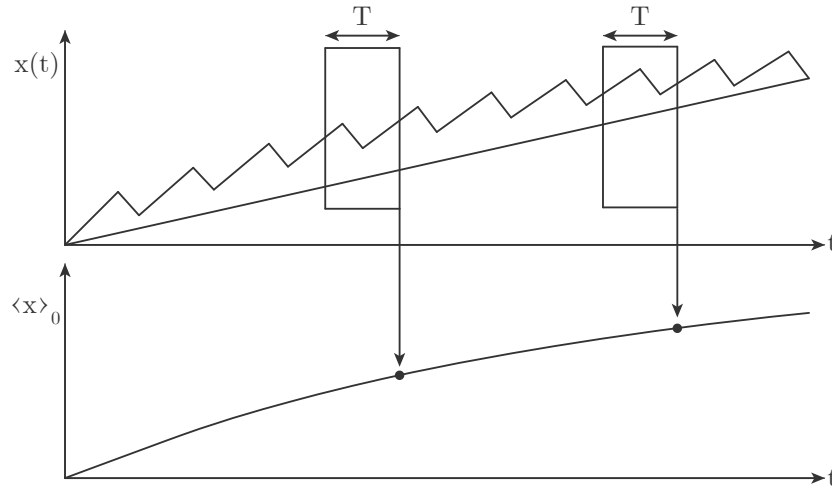
Figure 3.1 – Exemplification of the DP method [10].

The operator in Equation 3.2 can be applied to time-domain equations, transforming them into a new set of equations in terms of DP. Consider a set of nonlinear state equations provided as follows

$$\frac{\mathrm{d}x}{\mathrm{d}t} = f(t, x, u), \tag{3.4}$$

where $x(t)$ represents $n \times 1$ vector of state variables and $u(t)$ is an $m \times 1$ vector of input variables. Applying the DP operator (Equation 3.2) in Equation 3.4 yields the DP form of the state equations, which is given by

$$\left\langle \frac{\mathrm{d}x}{\mathrm{d}t} \right\rangle_k = \langle f(t, x, u) \rangle_k. \tag{3.5}$$

The left-hand side of Equation 3.5 can be evaluated using the DP differentiation

property, expressed as

$$\left\langle \frac{\mathrm{d}x}{\mathrm{d}t} \right\rangle_k = \jmath \, k\omega_s \langle x \rangle_k + \frac{\mathrm{d}\langle x \rangle_k}{\mathrm{d}t}. \tag{3.6}$$

A general form for the right-hand side of Equation 3.5 does not exist, as each individual system is different and requires special consideration. Furthermore, it is generally not possible to obtain a closed-form expression for the right-hand side of Equation 3.5. Therefore, approximations are required to model nonlinear systems using DP. An important exception is polynomial nonlinearities, where DPs may be obtained analytically using the convolution property given by

$$\langle xy \rangle_k = \sum_{l=-\infty}^{\infty} \langle x \rangle_{k-l} \langle y \rangle_l. \tag{3.7}$$

The final DP form of Equation 3.4 can be derived using Equation 3.5 and 3.6, and is given by

$$\frac{\mathrm{d}\langle x \rangle_k}{\mathrm{d}t} = -\jmath \, k\omega_s \langle x \rangle_k (t) + \langle f(t, x, u) \rangle_k. \tag{3.8}$$

This equation illustrates how the DP operator converts a set of equations described in terms of time-domain quantities into a new set of equations expressed in terms of DP.

In the case of real-valued time-domain signals $x(t) = x^*(t)$, the following conjugation property is obtained

$$\langle x \rangle_{-k} = \langle x \rangle_k^* \tag{3.9}$$

where "*" denotes the complex conjugated. Utilizing the conjugation property from Equation 3.9, the real-valued time-domain signals can be restored from the DP signals as

$$x(t) = \langle x \rangle_0(t) + 2 \sum_{k=1}^{\infty} \Re \left[\langle x \rangle_k(t) e^{\jmath k\omega_s t} \right], \tag{3.10}$$

where $\langle x \rangle_0$ represents the dc component and $\langle x \rangle_k$ denotes the k-th harmonics of the operator. The envelope of the signal can be obtained using the following operation

$$x_{env}(t) = \langle x \rangle_0 + 2 \sum_{k=1}^{\infty} | \langle x \rangle_k |. \tag{3.11}$$

3.1.1 DP model example

To illustrate the DP model discussed in the previous subsection, an example demonstrating the application of this technique will be presented. Consider the electrical circuit shown in Figure 3.2. In this parallel LC circuit, the system includes the states: the voltage across the inductor and the current through the capacitor.

Through circuit analysis, one can derive the following expressions
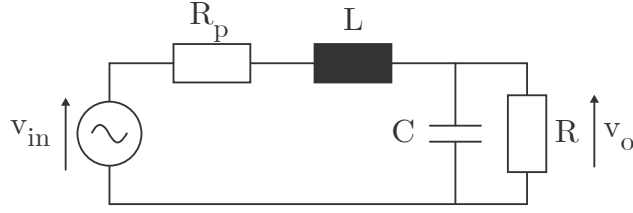
Figure 3.2 – LC parallel circuit.

$$L\frac{\mathrm{d}}{\mathrm{d}t}i_L = v_{in} - v_o - R_p i_L,\tag{3.12}$$

$$C\frac{\mathrm{d}}{\mathrm{d}t}v_o = i_L - \frac{v_o}{R}.\tag{3.13}$$

In terms of state-space matrices, Equations 3.12 and 3.13 can be written as

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \underbrace{\begin{bmatrix} -\dfrac{R_p}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix}}_{A}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \underbrace{\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}}_{B}\begin{bmatrix} v_{in} \end{bmatrix},\tag{3.14}$$

where A represents the dynamic matrix and B denotes the input matrix.

Applying the concept from DP model, Equation 3.8 to Equation 3.12 and Equation 3.13 yields

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle i_L\rangle_1 = -\jmath\,\omega_s\langle i_L\rangle_1 + \frac{\langle v_{in}\rangle_1}{L} - \frac{\langle v_o\rangle_1}{L} - \frac{R_p}{L}\langle i_L\rangle_1,\tag{3.15}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle v_o\rangle_1 = -\jmath\,\omega_s\langle v_o\rangle_1 + \frac{\langle i_L\rangle_1}{C} - \frac{\langle v_o\rangle_1}{RC}.\tag{3.16}$$

Equations 3.15 and 3.16 have real and imaginary parts, denoted as R and I, respectively. Therefore, four equations are formulated to describe the states of this circuit.

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle i_L\rangle_1^R = \omega_s\langle i_L\rangle_1^I + \frac{\langle v_{in}\rangle_1^R}{L} - \frac{\langle v_o\rangle_1^R}{L} - \frac{R_p}{L}\langle i_L\rangle_1^R,\tag{3.17}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle i_L\rangle_1^I = -\omega_s\langle i_L\rangle_1^R + \frac{\langle v_{in}\rangle_1^I}{L} - \frac{\langle v_o\rangle_1^I}{L} - \frac{R_p}{L}\langle i_L\rangle_1^I,\tag{3.18}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle v_o\rangle_1^R = \omega_s\langle v_o\rangle_1^I + \frac{\langle i_L\rangle_1^R}{C} - \frac{\langle v_o\rangle_1^R}{RC},\tag{3.19}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle v_o\rangle_1^I = -\omega_s\langle v_o\rangle_1^R + \frac{\langle i_L\rangle_1^I}{C} - \frac{\langle v_o\rangle_1^I}{RC}.\tag{3.20}$$

Equations 3.17, 3.18, 3.19, and 3.20 can also be represented in matrix form as follows

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \langle i_L \rangle_1^R \\ \langle v_o \rangle_1^R \\ \langle i_L \rangle_1^I \\ \langle v_o \rangle_1^I \end{bmatrix} = \begin{bmatrix} -\dfrac{R_p}{L} & -\dfrac{1}{L} & \omega_s & 0 \\ \dfrac{1}{C} & -\dfrac{1}{RC} & 0 & \omega_s \\ -\omega_s & 0 & -\dfrac{R_p}{L} & -\dfrac{1}{L} \\ 0 & -\omega_s & \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} \langle i_L \rangle_1^R \\ \langle v_o \rangle_1^R \\ \langle i_L \rangle_1^I \\ \langle v_o \rangle_1^I \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & 0 \\ 0 & \dfrac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \langle v_{in} \rangle_1^R \\ \langle v_{in} \rangle_1^I \end{bmatrix}. \tag{3.21}$$

From Equation 3.21, it can be observed that there is a pattern in the DP matrix, here matrices A and B from Equation 3.14 appear twice in the Equation 3.21. Therefore, the transformation matrix from steady-state equations to DP equations can be determined. This transformation matrix can be denoted as

$$\frac{d}{dt} \begin{bmatrix} \langle x \rangle_k^R \\ \langle x \rangle_k^I \end{bmatrix} = \begin{bmatrix} A & \omega_s I_n \\ -\omega_s I_n & A \end{bmatrix} \begin{bmatrix} \langle x \rangle_k^R \\ \langle x \rangle_k^I \end{bmatrix} + \begin{bmatrix} B & 0_m \\ 0_m & B \end{bmatrix} \begin{bmatrix} \langle u \rangle_k^R \\ \langle u \rangle_k^I \end{bmatrix}, \tag{3.22}$$

where $\langle x \rangle_k$ and $\langle u \rangle_k$ represent the state and the input variables, respectively. ω_s is the angular frequency in rad/s. A represents the dynamic matrix and B denotes the input matrix I_n denotes the identity matrix, where, n which is the order of the matrix A.

To validate the derived equations for the parallel LC circuit using the DP model, the signals were plotted in the time domain and compared with the results obtained by reconstructing the phasor signals in the time domain. Figure 3.3 illustrates the comparison between the inductor current and the capacitor voltage in the time domain, alongside the reconstructed phasor signals.

The reconstruction of the signals in the time domain can be achieved by applying Equations 3.17 and 3.18 for the inductor current, and Equations 3.19 and 3.20 for the capacitor voltage, in Equation 3.10. This process results in the signals shown in Figure 3.3.
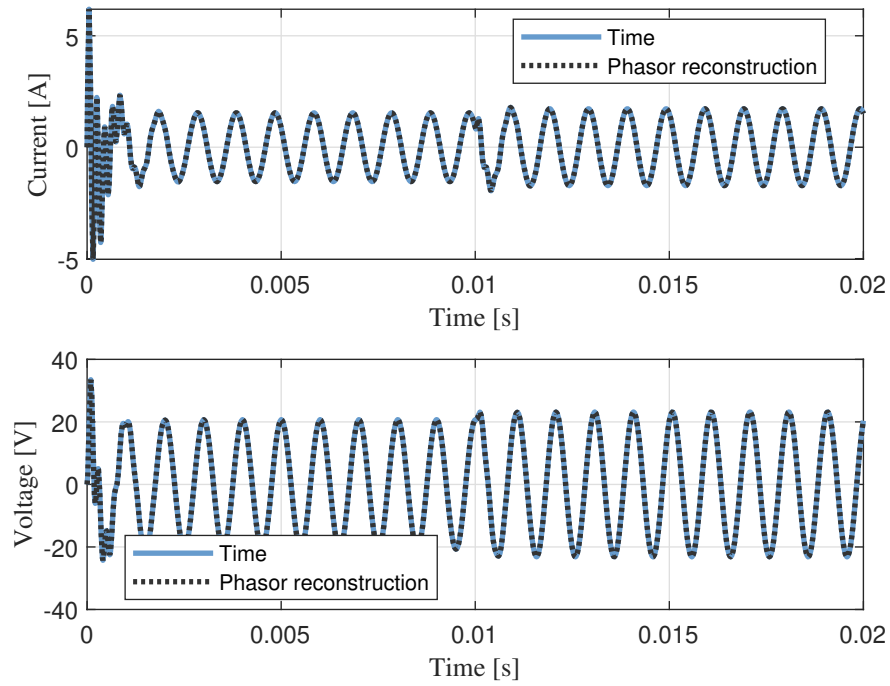
Figure 3.3 – Comparison DP model and phasor reconstruction.

Given the interest in modeling the envelope of the signal, the DP is applied to Equation 3.11, resulting in Figure 3.4.
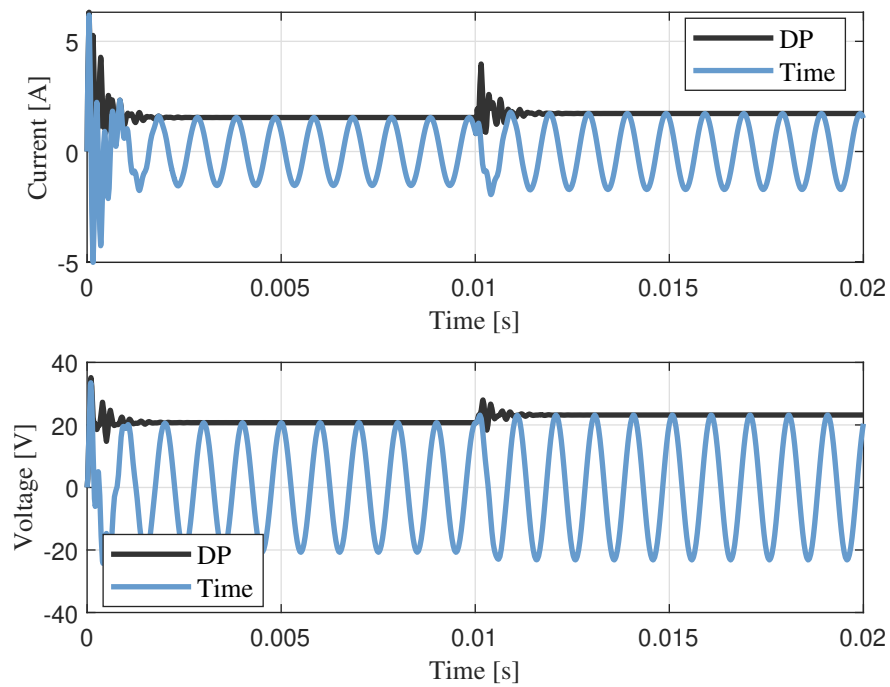
Figure 3.4 – Comparison absolute DP model and time.

Finding the solution in Equation 3.21, the result is:

$$\begin{bmatrix} \langle i_L \rangle_1^R \\ \langle v_o \rangle_1^R \\ \langle i_L \rangle_1^I \\ \langle v_o \rangle_1^I \end{bmatrix} = \begin{bmatrix} 0.4355 \\ 10.3568 \\ 0.6372 \\ -0.3373 \end{bmatrix}. \tag{3.23}$$

3.2 ANALYSIS OF THE CLLLC RESONANT CONVERTER

In this subsection, the model obtained for the resonant CLLLC converter will be determined and validated.

3.2.1 Equations of state of the resonant CLLLC converter

The model of the CLLLC resonant converter is divided into two parts: the ac part, which includes the resonant tank model, and the dc part, which involves the output filter model.

3.2.1.1 Resonant tank model

The ac part involves deriving the model for the CLLLC resonant converter, as represented in Figure 3.5. This derivation utilizes the DP technique under the following set of assumptions:

1. All secondary Full-Bridge are ideal with no reverse recovery and no junction capacitance.

2. Resonant capacitors currents, i_{L1} and i_{L2} are pure sinusoidal waveform.

3. Dead-time is neglected, so the input voltage, v_{ab} is a pure square wave.

4. Duty cycle of 50%.

5. Only the fundamental harmonic is considered in the resonant tank.

6. The input voltage, v_{ab}, is the reference voltage. The phase of all currents and voltages in the converter are measured to this voltage.
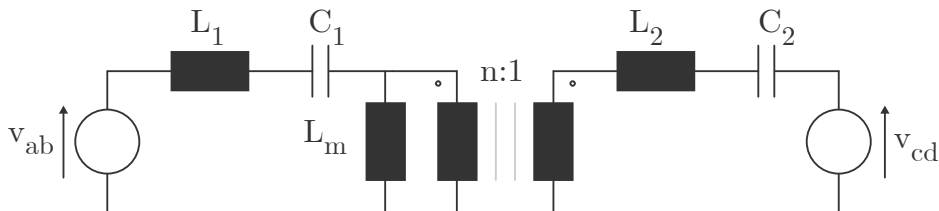
Figure 3.5 − Resonant tank equivalent circuit.

Due to the complexity of the system involving five elements, it is necessary to derive five differential equations that correspond to the state of the system. These equations describe the dynamics of the current in the inductors and the voltage across the capacitors. Using Kirchhoff's laws, one can then obtain

$$v_{ab} = R_L i_{L1} + L_1 \frac{\mathrm{d}}{\mathrm{d}t} i_{L1} + v_{C1} + L_m \frac{\mathrm{d}}{\mathrm{d}t} i_{Lm}, \tag{3.24}$$

$$\frac{1}{n} L_m \frac{\mathrm{d}}{\mathrm{d}t} i_{Lm} = R_L i_{L2} + v_{C2} + L_2 \frac{\mathrm{d}}{\mathrm{d}t} i_{L2} + v_{cd}, \tag{3.25}$$

$$i_{L1} = C_1 \frac{\mathrm{d}}{\mathrm{d}t} v_{C1}, \tag{3.26}$$

$$i_{L2} = C_2 \frac{\mathrm{d}}{\mathrm{d}t} v_{C2}. \tag{3.27}$$

The magnetizing current, denoted as i_{Lm}, can be expressed as follows

$$i_{Lm} = i_{L1} - \frac{i_{L2}}{n}. \tag{3.28}$$

By substituting the equation referred to in Equation 3.28 into Equations 3.24 and 3.25, the system's order can be reduced to four differential equations, eliminating the dependence on the derivative of the magnetizing inductance. Following this reduction, a solver is used to isolate the differential equations.

$$
\begin{aligned}
\frac{di_{L1}}{dt} = {}& \frac{n^2 L_2 + L_m}{L_{eq}} v_{ab} - \frac{R_L(n^2 L_2 + L_m)}{L_{eq}} i_{L1} - \frac{n L_m R_L}{L_{eq}} i_{L2} - \frac{n^2 L_2 + L_m}{L_{eq}} v_{C1} \\
& - \frac{n L_m}{L_{eq}} v_{C2} - \frac{n L_m}{L_{eq}} v_{cd}
\end{aligned}
\tag{3.29}
$$

$$
\begin{aligned}
\frac{\mathrm{d}}{\mathrm{d}t} i_{L2} = {}& \frac{n L_m}{L_{eq}} v_{ab} - \frac{n L_m R_L}{L_{eq}} i_{L1} - \frac{n^2(L_1 R_L + L_m R_L)}{L_{eq}} i_{L2} - \frac{n L_m}{L_{eq}} v_{C1} - \frac{n^2(L_1 + L_m)}{L_{eq}} v_{C2} \\
& - \frac{n^2(L_1 + L_m)}{L_{eq}}
\end{aligned}
$$
$$\tag{3.30}$$

$$\frac{\mathrm{d}}{\mathrm{d}t} v_{C1} = \frac{i_{L1}}{C_1} \tag{3.31}$$

$$\frac{\mathrm{d}}{\mathrm{d}t} v_{C2} = \frac{i_{L2}}{C_2} \tag{3.32}$$

where:

$$L_{eq} = L_1 L_m + n^2 L_1 L_2 + n^2 L_2 L_m \tag{3.33}$$

After isolating the variables as functions of their derivatives, the matrices A and B describing the model can be easily determined using Equations 3.29 through 3.32. To obtain the differential equation describing the resonant tank of this converter, it is necessary to apply the transformation matrix equation (Equation 3.22).

To validate the derived model, voltages v_{ab} and v_{cd} were applied and compared with the simulation results in the time domain. This comparison is illustrated in Figure 3.6, which shows the currents through the resonant inductors, and in Figure 3.7, which shows the voltages across the resonant capacitors. As demonstrated, the DP model exhibits the same behavior as the time-domain model, thereby validating the resonant tank model equations.
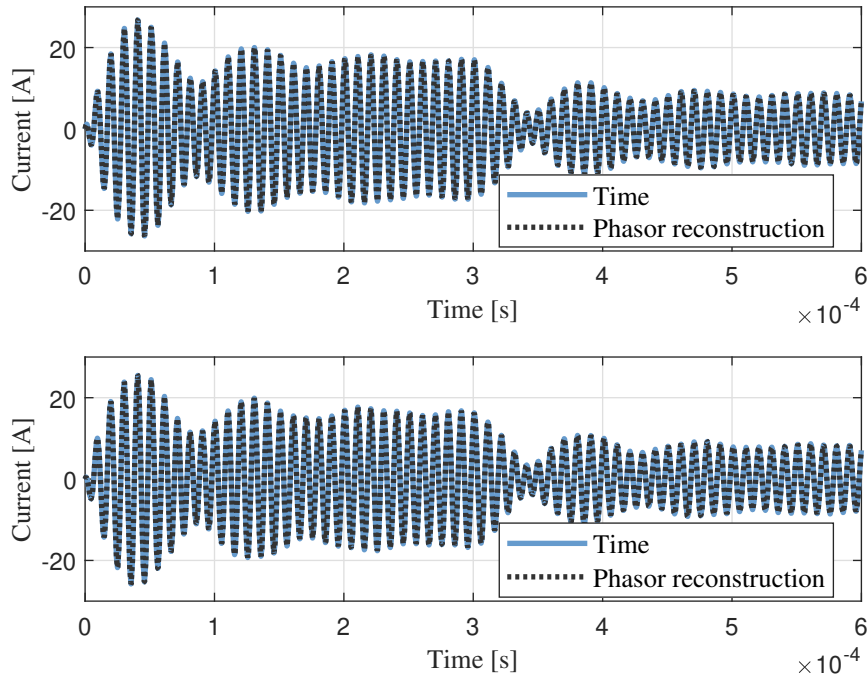
Figure 3.6 – Current validation on resonant tank (i_{L1} and i_{L2}).

3.2.1.2 Output filter model

After determining the state equations of the resonant tank, the equations for the converter's output filter are derived. The output filter of the power converter is shown in Figure 3.8, which includes a current source corresponding to the output of the rectifier stage, an output capacitor, an output capacitor with a damping branch, and a common-mode choke modeled as an inductor. The output load is represented as a battery, consisting of a series resistance and a voltage source.
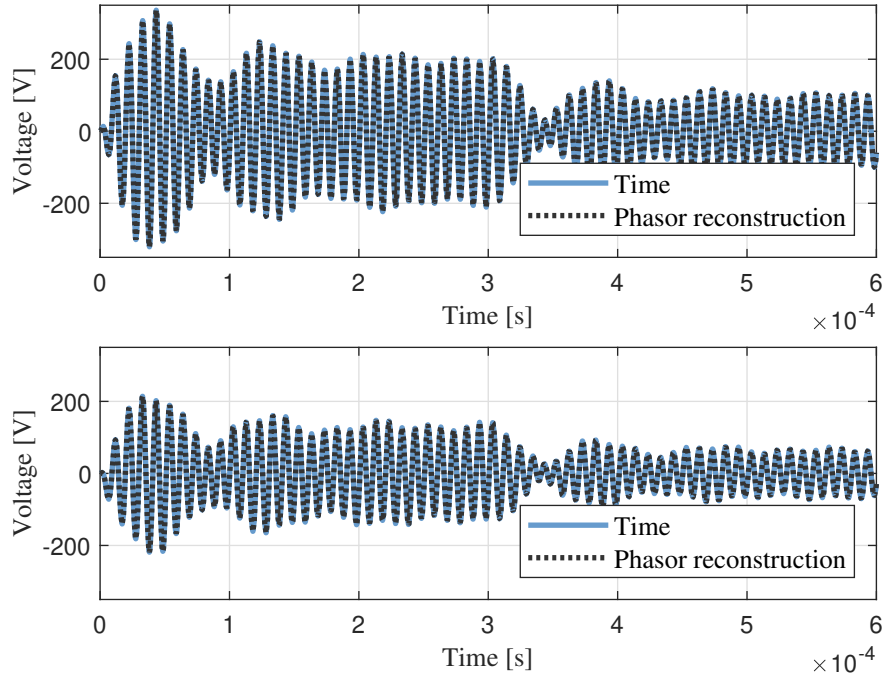
Figure 3.7 – Voltage validation on resonant tank (v_{C1} and v_{C2})

The state equations of the output filter are presented in Equations 3.34, 3.35 and 3.36.
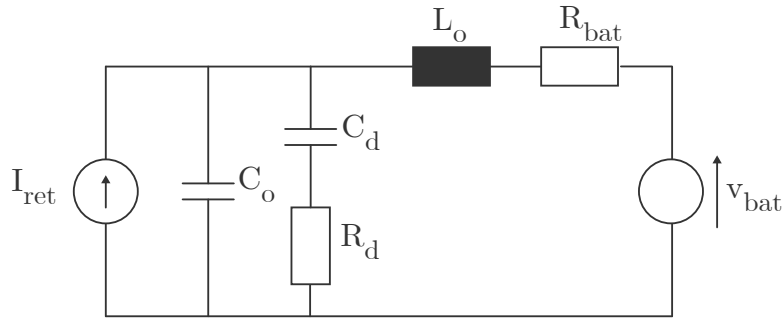
Figure 3.8 – Output filter equivalent circuit.

$$I_{ret} = C_o \frac{\mathrm{d}}{\mathrm{d}t} v_{Co} + C_d \frac{\mathrm{d}}{\mathrm{d}t} v_{Cd} + i_o, \tag{3.34}$$

$$v_{Co} = v_{Cd} + R_d C_d \frac{\mathrm{d}}{\mathrm{d}t} v_{Cd}, \tag{3.35}$$

$$v_{Co} = L_o \frac{\mathrm{d}}{\mathrm{d}t} i_o + I_{bat}(R_{Lo} + R_{bat}) + V_{bat}. \tag{3.36}$$

3.2.2 Complete model of the converter

To obtain the complete model of the converter, it is necessary to combine the DP model with the output filter model, resulting in a set of equations and/or matrices that describe the resonant CLLLC converter. The resonant tank and the output filter model equations contain three nonlinear terms: the inverter output voltage (v_{ab}), the rectifier input voltage (v_{cd}), and the output current of the rectifier bridge (I_{ret}).

When employing the DP technique, it becomes imperative to explicitly express all terms concerning the amplitude of the specific harmonic index under scrutiny. This consideration is particularly significant when dealing with nonlinear functions, encompassing signal and module characterization.

The voltage v_{ab} exhibits an infinite number of harmonics. The resonant network is tuned to the resonant frequency, which suppresses all higher harmonics. Therefore, the higher-order harmonics in v_{ab} can be neglected without introducing considerable error. By assuming the phase angle of v_{ab} as the reference, this voltage can be represented as a pure sine wave

$$v_{ab}(t) = V_{ab}(t)\, sign(\sin(\omega_s t)), \tag{3.37}$$

with

$$V_{ab}(t) = \begin{cases} V_{ab}, & \text{if } \sin(\omega_s t) > 0 \\ -V_{ab}, & \text{if } \sin(\omega_s t) < 0 \end{cases}. \tag{3.38}$$

The applying Equation 3.2 in Equation 3.37, can be obtained

$$\langle v_{ab} \rangle_k = \frac{1}{T}\left[\int_{t-T}^{t-\frac{T}{2}} V_{ab}e^{-jk\omega_s\tau}d\tau + \int_{t-\frac{T}{2}}^{t} -V_{ab}e^{-jk\omega_s\tau}d\tau\right], \tag{3.39}$$

considering the first harmonic index $(k = 1)$,

$$\langle v_{ab} \rangle_1 = -j\frac{2\,V_{ab}}{\pi}. \tag{3.40}$$

The voltage across the input of the secondary full-bridge switches, V_{cd}, depends on the direction of the rectifier input current, i_{L2}. If i_{L2} is positive, this voltage is $+v_o$; if i_{L2} is negative, this voltage is $-v_o$. Consequently, v_{cd} behaves similarly to v_{ab} in terms of its waveform, exhibiting a square wave pattern. However, unlike v_{ab}, this voltage contains both sine and cosine terms due to its phase difference with respect to v_{ab}. The DP analysis of this square-shaped voltage shows that it has an infinite number of odd harmonics. Since all higher harmonics can be neglected because the resonant network is tuned to the fundamental harmonic, this voltage can be expressed by the following equation

$$v_{cd} = sign(i_{L2})\, v_{Co}, \tag{3.41}$$

where,

$$i_{L2} \approx I_{L2}(t)sin(\omega_s t + \varphi_i). \tag{3.42}$$

By applying Equation 3.2 to Equation 3.42 and considering the first harmonic $(k = 1)$, the following equation can be obtained

$$\langle sign(i_{L2})\rangle_1 = \frac{1}{T}\int_{t-T}^{t} sign(i_{L2})(\tau)e^{-\jmath\omega_s\tau}d\tau, \tag{3.43}$$

solving and substituting in Equation 3.41,

$$\langle v_{cd}\rangle_1 = \frac{2\langle v_{Co}\rangle_0}{\pi}\left(\frac{\langle i_{L2}\rangle_1^R + \jmath\langle i_{L2}\rangle_1^I}{|\langle i_{L2}\rangle_1|}\right). \tag{3.44}$$

It is important to highlight that, unlike the voltage v_{ab}, which contains only an imaginary part because it is a sine function, the voltage v_{cd} has both real and imaginary parts.

Finally, the rectifier output dc current can be mathematically represented by the absolute value of the current at the rectifier input

$$I_{ret} = |i_{L2}|. \tag{3.45}$$

Applying Equation 3.2 in Equation 3.45, with index harmonic $k = 0$,

$$\langle i_o\rangle_0 = \frac{1}{T}\int_{t-T}^{t}|i_{L2}(\tau)|e^{-\jmath 0\omega_s\tau}d\tau, \tag{3.46}$$

the equation can be derived to describe the average current at the output of the converter, as represented by Equation 3.47.

$$\langle i_o\rangle_0 = \frac{4}{\pi}\sqrt{\left(\langle i_{L2}\rangle_1^R\right)^2 + \jmath\left(\langle i_{L2}\rangle_1^I\right)^2}. \tag{3.47}$$

It is important to highlight that the output current (i_o) is a dc current; therefore, the harmonic index of the current is zero.

Combining the resonant tank model with the output filter model enables the determination of a comprehensive model that describes the functioning of the power converter.

The DP model obtained for the converter can be validated by comparing it with the temporal model. Figure 3.9 illustrates this comparison. To validate the obtained model, the frequency is varied by -5% at a specific instant in time. As shown, the DP model accurately represents the temporal model.
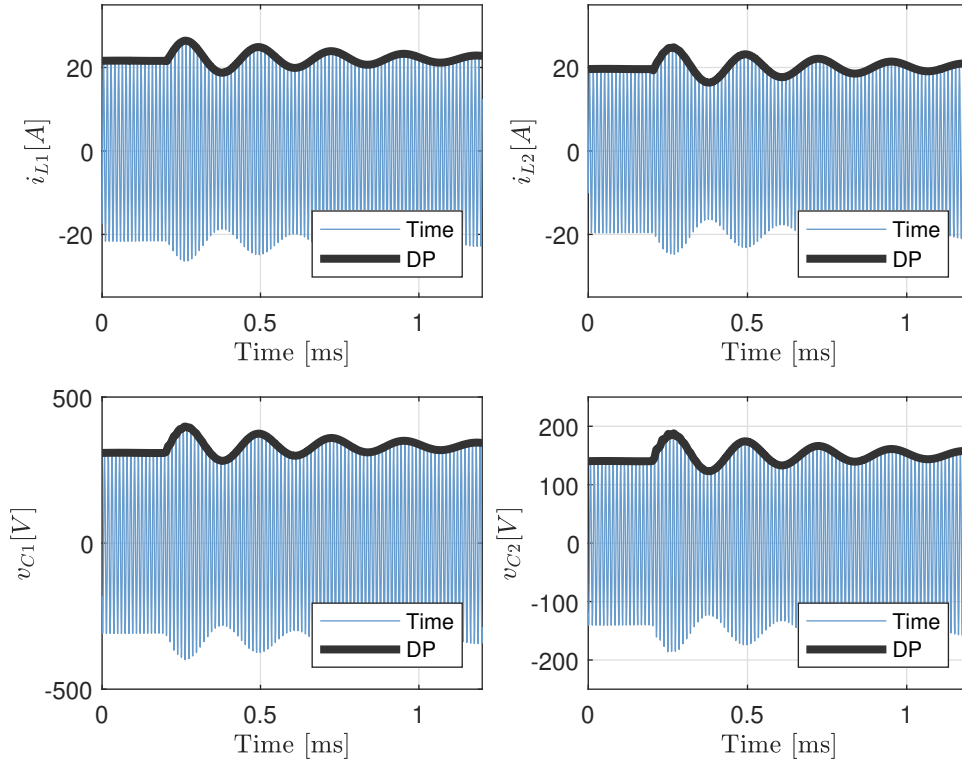
Figure 3.9 – Validation of the DP model of the CLLLC resonant converter.

3.2.2.1 Dynamic model

The current model retains nonlinear characteristics, which complicate the use of tools such as Bode diagrams for control system design. Therefore, linearizing the model is essential. A commonly used approach in the literature for this purpose involves employing the Jacobian matrix, as detailed in subsection A.1.2.

The model equations of the CLLLC resonant converter include eleven distinct transfer functions. However, the focus is on controlling the load, specifically examining the impact of the switching frequency disturbance $\hat{f}_{sw}$ on the voltage across the output capacitor and the current through the output inductor.

To obtain the transfer function describing the voltage as a function of frequency, equation Equation A.7 is employed.

$$G_{vf}(s) = \left. \frac{\hat{v}_{Co}(s)}{2\pi \hat{f}_{sw}(s)} \right|_{\hat{v}_{in}=0}. \tag{3.48}$$

Following this, the Bode diagram describing the voltage in relation to frequency can be plotted in Figure 3.10.

Similarly, the transfer function of the output current in relation to the switching frequency is determined by Equation 3.49. The corresponding Bode diagram is presented in Figure 3.11.
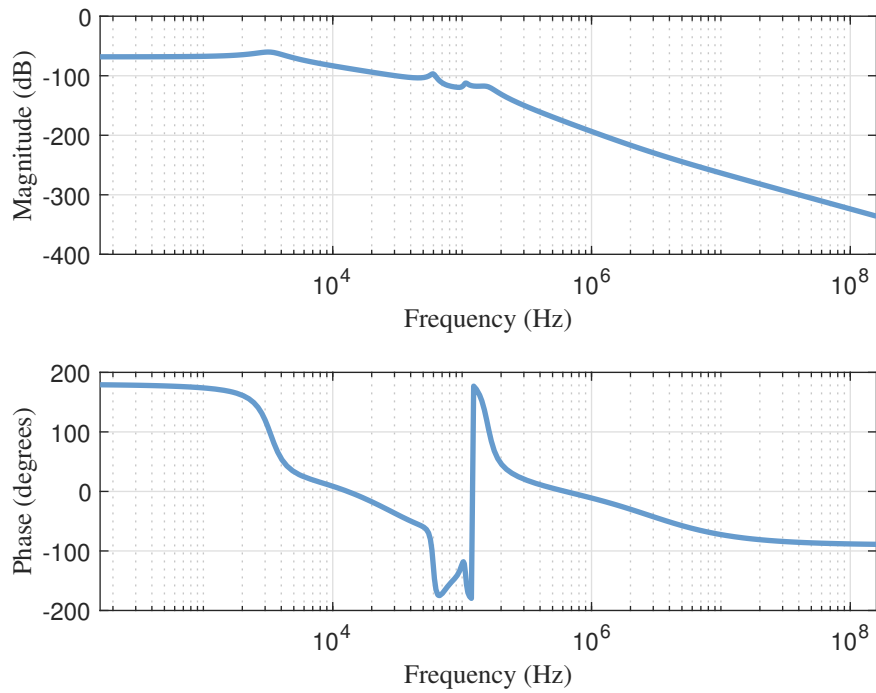
Figure 3.10 – Output voltage (v_{Co}) transfer function.

$$G_{if}(s) = \left.\frac{\hat{i}_o(s)}{2\pi\hat{f}_{sw}(s)}\right|_{\hat{v}_{in}=0}. \tag{3.49}$$
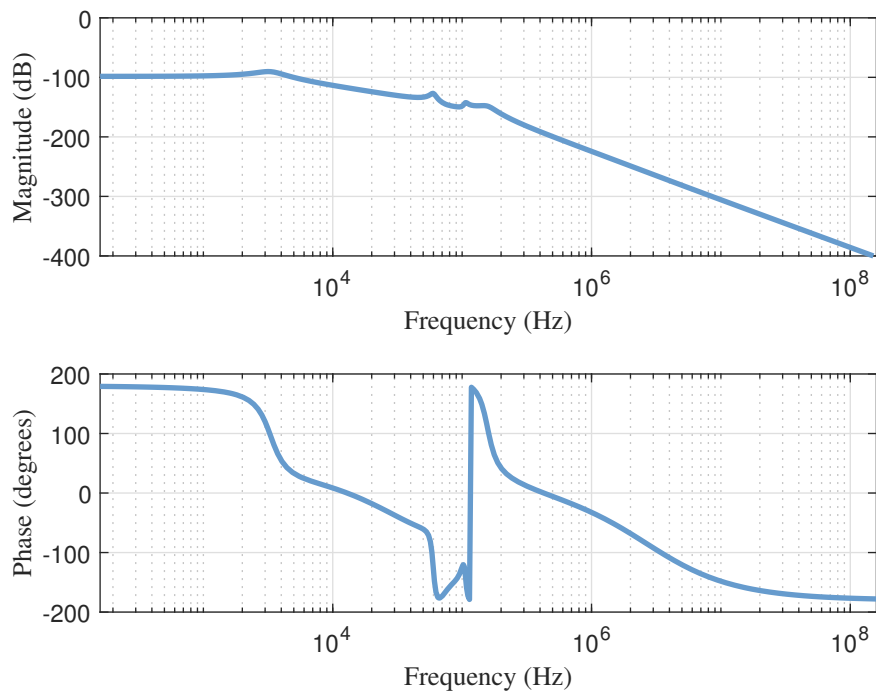
Figure 3.11 – Output current (i_o) transfer function.

After determining the transfer functions of the output voltage and current of the

converter, it is possible to design the control system and evaluate the dynamic performance of the system.

Evaluating the Bode diagrams of Figure 3.10 and Figure 3.11, it is interesting to note that, at lower frequencies, both the transfer function of the output voltage with respect to the switching frequency and the transfer function of the output current with respect to the switching frequency show that the CLLLC resonant converter behaves like a gain. This characteristic makes it easily controllable in this frequency range.

3.3 CONTROL STRATEGY

The strategy for implementing dual-loop control in the CLLLC resonant converter is similar to that used in basic dc-dc converters, consisting of an inner, faster current loop and an outer, slower voltage loop. Illustrated in Figure 3.12, the block diagram showcases this dual-loop control configuration. A consideration within the inner current loop is the summation of the resonance frequency with the output signal of the controller. This adjustment accounts for the potential scenario wherein the converter might operate at two distinct switching frequencies, resulting in an identical output voltage. These frequencies correspond to operation in the capacitive and inductive regions, respectively. By incorporating the resonance frequency into the control signal, it ensures that the control reference avoids convergence towards operation in the inductive region.
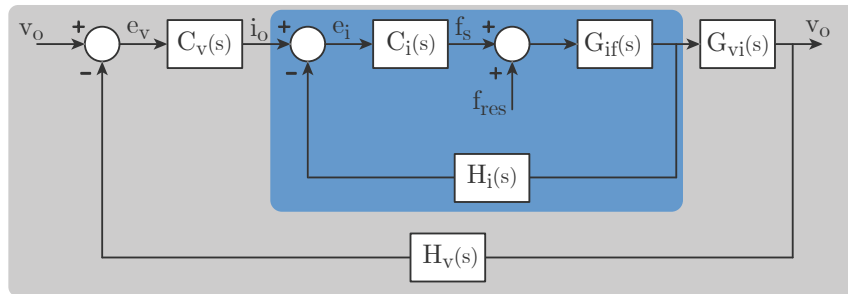
Figure 3.12 − Block diagram of the dual loop control.

To validate the presented control strategy, it is essential to obtain the transfer function from the output voltage to the output current. This can be easily achieved by dividing Equation 3.49 by Equation 3.48, results in Equation 3.50.

$$G_{vi}(s) = \frac{G_{vf}(s)}{G_{if}(s)}, \tag{3.50}$$

and its Bode diagram is shown in Figure 3.13.

To design the controllers $C_v(s)$ and $C_i(s)$, the PID tuner tool in the MATLAB software was utilized. For both voltage and current control, integrator-type controllers were chosen.

$$C_{int}(s) = K_i \frac{1}{s}, \tag{3.51}$$
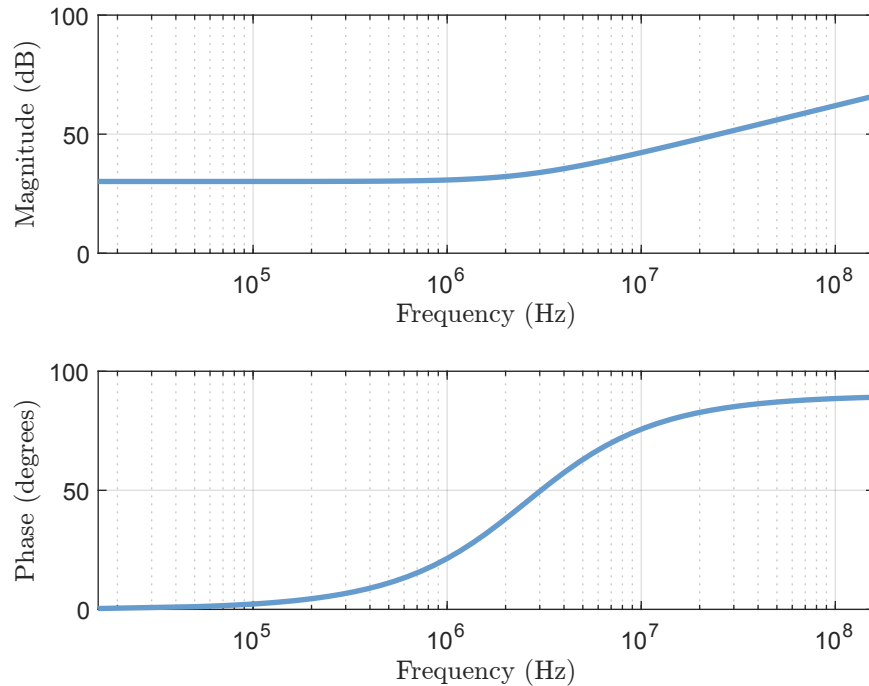
Figure 3.13 – Transfer function of output voltage by output current.

where k_i is the integral gain of the controller.

For the voltage controller, the determined integral gain was $K_{i_v} = 62.8319$, and for the current controller, the determined gain was $K_{i_i} = -8.436M$.

Figures Figure 3.14 and Figure 3.15 present the Bode diagrams of the transfer functions controlled with the designed controllers. This analysis is essential as it provides insights into the frequency response, and overall performance of the control systems. The controllers, designed, aim to enhance system behavior under varying conditions.
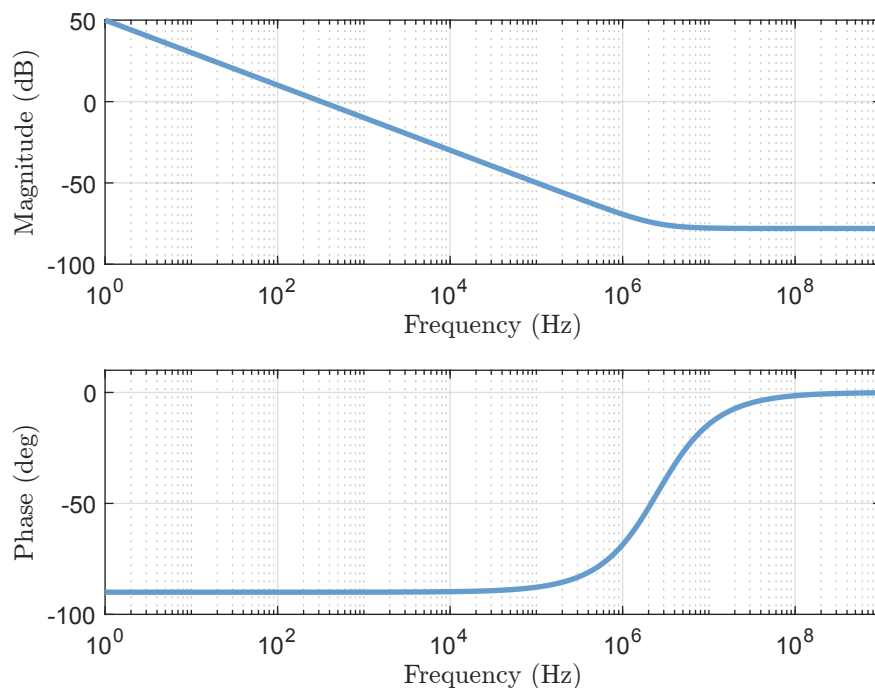
Figure 3.14 – Compensated transfer function of output voltage by output current.
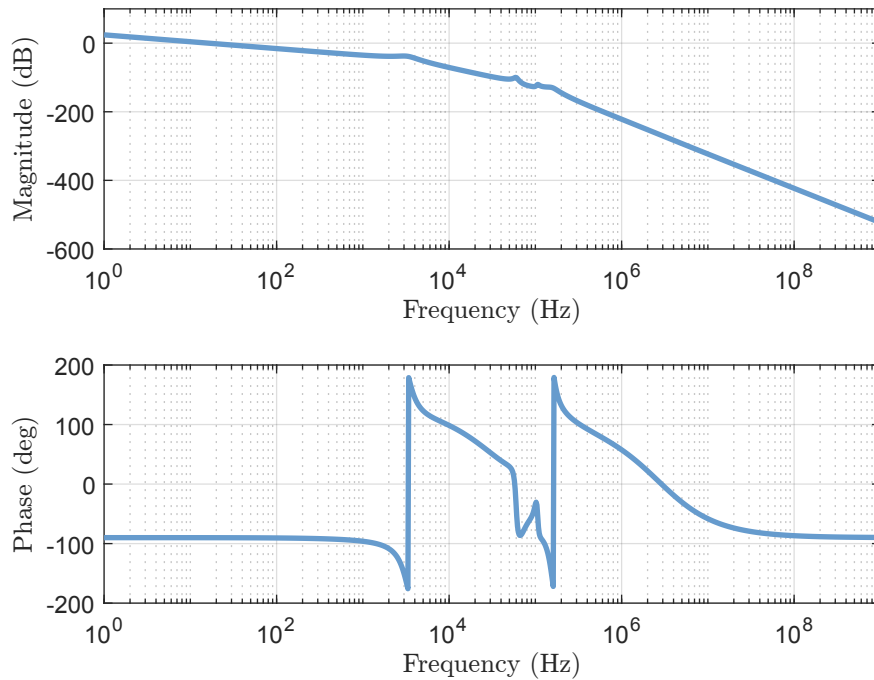
Figure 3.15 – Compensated transfer function of output current by switching frequency.

To validate the designed control system, the converter was simulated, considering its operation with the battery in the output voltage varying from 200 V to 400 V. The simulation of the voltage and current loop control can be observed in Figure 3.16.
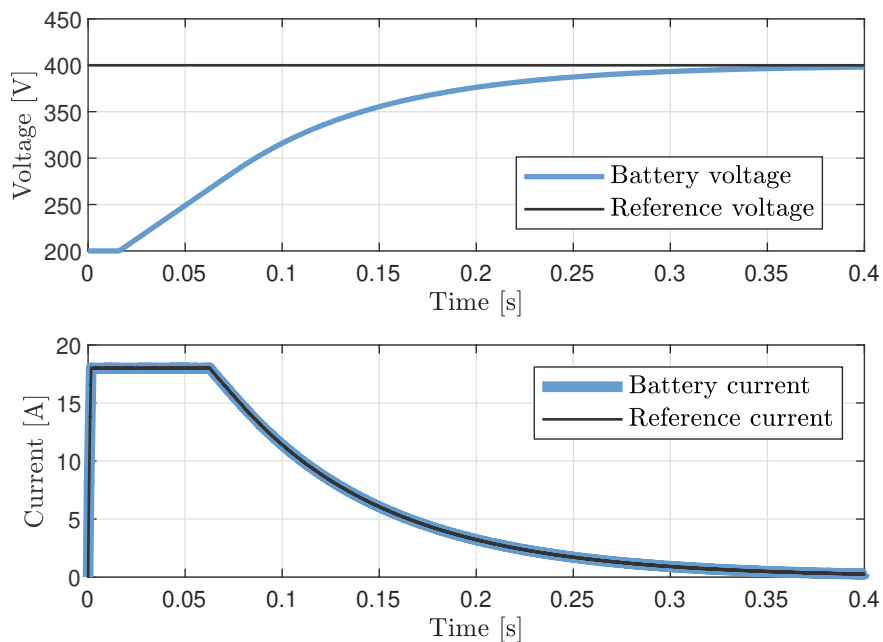
Figure 3.16 – Battery voltage and current control.

As can be seen in Figure 3.16, the charging current is kept constant, limited by the maximum current provided by the converter. The battery voltage gradually increases as it is charged. When the battery voltage reaches a certain predefined limit, usually close to

its nominal voltage, in this case 300 V, the control system gradually reduces the current delivered to the battery.

When the charging current reaches a very low level, or after a predetermined period of time, the charger interrupts the power supply to the battery. TThis is essential to prevent overcharging, which can damage the battery or even cause dangerous conditions such as overheating or leakage.

3.4 SUMMARY

This chapter introduces the concept of DP, which is necessary to develop the model for the CLLLC resonant converter. This concept becomes essential because the currents and voltages within the resonant tank exhibit sinusoidal or nearly sinusoidal behavior. Consequently, common approaches like circuit averaging, widely employed in models determined by their average values, are not applicable here.

In the initial phase, a model of the parallel LC circuit is introduced with the objective of providing a simple representation and aiding understanding of DP model. Through this example, the equations outlined in the text are used to reconstruct the phasors in the time domain. This reconstruction is then compared with the time model to validate the DP model, while also enabling the calculation of real and imaginary phasor amplitudes. From this, a matrix for the transformation of DP models is determined. Once the time-domain derivatives of the circuit are established, the DP matrix can be readily determined.

After exemplifying the concept of DP, the model of the CLLLC resonant converter is developed, which is divided into two parts: the ac part composed of the resonant tank and the dc part composed of the output filter. Subsequently, both parts are integrated and validated in the complete converter model.

Finally, the dynamic model, expressed in terms of transfer functions representing the relationship between input and output variables, is derived. This model captures the behavior of the CLLLC resonant converter under varying operating conditions and load scenarios. With this comprehensive understanding of the converter's dynamics, it becomes possible to devise control design strategies to attain desired performance objectives.

4   OPTIMIZATION AND DESIGN

In this chapter, the design and optimization of the CLLLC will be presented. First, the most common design methodology employed in the literature is presented. Subsequently, the models for loss and temperature estimation will be reviewed. Subsequently, the overall design of the CLLLC will be presented, focusing on the resonant tank parameters, the design of the transistors, and the transformer. Finally, the results will be discussed.

4.1   PREDOMINANT DESIGN APPROACH IN LITERATURE

To design the CLLLC resonant converter tank, the methodology proposed by [38] is widely used. The methodology underscores several key considerations that must be taken into account, namely:

1. Increase operating frequency to reduce magnetics and output capacitor size. Voltage across resonant capacitor inversely tied to switching frequency; higher frequency means lower capacitor stress. Design converter for high normal operating frequency.

2. Aim for ZVS in primary switches and soft commutation in secondary switches for high efficiency and very high-frequency operation.

3. Minimize circulating reactive energy in resonant tank by keeping phase angle, φ, between input voltage and current small.

4. Ensure converter meets voltage gain requirements in both energy flow directions.

The converter design involves determining the turns ratio of the transformer (n), magnetizing inductance (L_m), leakage inductances $(L_1$ and $L_2)$, and series capacitances $(C_1$ and $C_2)$.

4.1.1 Transformer turns ratio

In resonant converters, efficiency peaks at the primary side series resonant frequency (f_{res}). Thus, operation at this frequency under nominal conditions is optimal. Assuming ideal primary and secondary switches, the transformer turns ratio can be calculated.

$$n = \frac{N_1}{N_2} = \frac{V_{in}}{V_{o_{nom}}}, \tag{4.1}$$

where N_1 represents the number of turns of the primary, N_2 denotes the number of turns of the secondary, V_{in} signifies the input voltage, and $V_{o_{nom}}$ stands for the nominal output voltage.

4.1.2 Magnetizing inductance

Achieving ZVS in the primary side switches requires ensuring that the current through these switches is negative when they turn on. During the dead time, the primary current should effectively charge and discharge the output capacitance of the primary side switches. The magnitude of this current depends on factors such as magnetizing inductance and dead time duration, which influence ZVS alongside the switch output capacitance and operating switching frequency. This relationship is given by

$$L_m \leq \frac{t_{db}}{16\,C_{oss}\,f_{sw}}, \tag{4.2}$$

where t_{db} represents the dead time, C_{oss} denotes the output capacitance of the switch, and f_{sw} signifies the switching frequency.

4.1.3 Leakage inductances and k ratio

Leakage inductance L_1 is assumed equal to inductance L_2, considering the transformer transformation ratio. Furthermore, it is necessary to obtain a relationship between the magnetizing inductance and the leakage inductance, which is defined by k and determined by the following equation

$$k = \frac{L_m}{L_1}. \tag{4.3}$$

The voltage gain and operational switching frequency range depend on the inductance ratio, k. A narrow operating frequency range requires a small k. However, this leads to larger leakage inductances and larger magnetics. On the other hand, a large k limits the converter gain while widening the operating frequency range.

4.1.4 Resonant capacitances

The maximum efficiency of the system occurs at the primary side series resonant frequency, f_{res}. This frequency is selected for nominal operation, defining the operating

frequency range.

$$C_1 = \frac{1}{L_1 \left(2\pi f_{res}\right)^2}. \tag{4.4}$$

4.2   LOSS MODELS FOR OPTIMAL DESIGN

4.2.1   Problem statement

Power converters are complex systems with multiple design parameters that can be optimized. The primary parameter to minimize in power converters is power losses (P_{losses}). By reducing the converter's losses, its efficiency increases, as calculated by the following equation

$$\eta = \frac{P_o}{P_o + P_{losses}}, \tag{4.5}$$

where P_o expresses the output power.

Designing a power converter with a loss model is essential for ensuring energy efficiency and optimal system performance. This approach enables a detailed analysis of the loss sources within the converter. Additionally, using a loss model provides a solid foundation for selecting appropriate components to enhance performance. Ultimately, designing based on a loss model not only results in a more efficient converter but also can improve the longevity of the overall system.

The optimization results will depend on the technology used for different components. Factors such as switch technology, transformer winding configuration, and magnetic core materials are among the parameters that can be defined and will impact the outcomes of the optimization algorithm.

4.2.2   Modeling of losses

4.2.2.1   Magnetic component losses

Losses in magnetic components are categorized into core and winding losses. These two types of losses have distinct mechanisms, which are briefly reviewed below.

Core Losses:

Core losses occur due to two different phenomena

- Hysteresis [39];

- Eddy Currents [40].

Hysteresis loss refers to the thermal energy dissipated within a magnetic material during the reversal of its magnetization. When exposed to varying magnetic fields, magnetic

materials experience hysteresis, a process in which their internal magnetic domains are reoriented. This phenomenon results in the conversion of energy into heat, which reduces the efficiency of devices using magnetic components [39].

Eddy current loss arises from electromagnetic induction. When alternating current flows through inductor or transformer coils, it generates a fluctuating magnetic field. This field induces eddy currents in adjacent conductive materials, such as the core. These currents circulate within the core, causing localized heating due to material resistance and resulting in energy dissipation.

At low frequencies, hysteresis losses predominate, being associated with the energy expended during the cycles of magnetization and demagnetization of the core. At high frequencies, eddy currents predominate. Both types of losses depend directly on the material of the core [41, 42].

To estimate the total core losses, the Steinmetz equation is used. This empirical equation is given by

$$P_{core} = k_c \, f^\alpha \, B_{pk}^\beta, \tag{4.6}$$

where f represents the frequency applied to the magnetic core, in this case is the switching frequency, B_{pk} is the peak of the magnetic flux density in the core, and k_c, α, and β are the Steinmetz coefficients.

The three Steinmetz coefficients can be approximated using information available in the manufacturer datasheet, as presented in Figure 4.1. These parameters are obtained through quadratic minimization techniques detailed in [43].
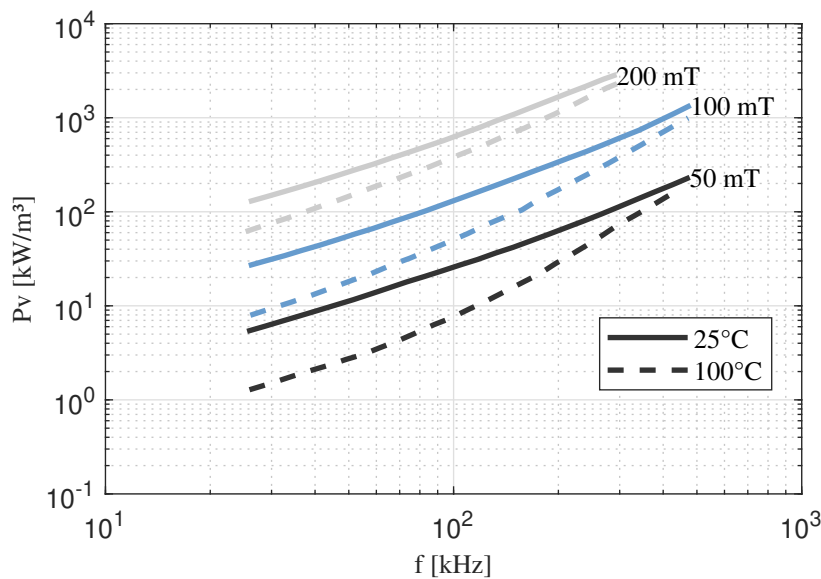
Figure 4.1 – Power loss as a function of frequency at different flux levels for N87 material[11].

he magnetic flux density waveform can be obtained from either the voltage or

current across the magnetic component. When current is applied to the component, such as in the series inductor of the resonant tank of the CLLLC resonant converter, it is typical to derive the flux density from the current, as follows

$$B(t) = \frac{i(t)L}{A_e N},$$ (4.7)

with L representing the inductance, N being the number of turns, A_e the cross-sectional area, and $i(t)$ the current as a function of time.

When voltage is applied, as in the case of a transformer, the applied voltage directly influences the flow. This is because the current must be divided into transformer current and magnetizing current to use the current equation effectively, as only the magnetizing component generates flux [42]. The magnetic flux density is given by

$$B(t) = \frac{1}{N A_e} \int_0^t v(t) \, dt.$$ (4.8)

The Steinmetz empirical approach was initially developed for sinusoidal waveforms. Recent advances have led to several modifications of the standard Steinmetz equations, including the Improved Generalized Steinmetz Equation (iGSE). This customized approach enhances the accuracy of power loss estimation, particularly for square voltage waveforms. However, since the converter waveforms are practically sinusoidal, and considering the discrepancy of around 10% between methods, the conventional Steinmetz equation is adopted in this study for simplicity and computational efficiency.

Winding Losses:

The winding losses consist of the power losses created in the conductors of a magnetic component by Joule law. These losses are caused by two different effects:

- Skin effect [44]

- Proximity effect [40]

All high-frequency effects can be explained by a single concept: the external or internal magnetic field, generated by the windings or other external sources, induces a current distribution that reduces the effective cross-sectional area of the wires. Considering these high-frequency effects, the following Equation 4.9 can be used to estimate the winding losses [45].

$$P_{W_{inding}} = \sum_{j=1}^{\infty} R_{w,ac,j} \, I_{rms,j}^2.$$ (4.9)

where $R_{w,ac,j}$ signifies the resistance of the jth harmonic, and $I_{rms,j}$ represents the rms current of the jth harmonic.

Litz wire is engineered specifically to mitigate these losses. By employing a multistrand conductor, the total cross-sectional area is divided among numerous conductors with smaller diameters. As a result, litz wire can achieve a more uniform distribution of current density compared to solid wire configurations [46, 47].

The Dowell equation is used to compute the winding resistance of the adapted foil inductor, specifically for characterizing the resistance of the litz wire winding [47]. The parameter denoted as the ratio F_R, which represents the ratio of dc resistance $R_{w,dc}$ to ac resistance $R_{w,ac}$, can be determined using the following equation

$$F_R = \frac{R_{w,ac}}{R_{w,dc}} = A(F_P + F_S). \tag{4.10}$$

The determination of F_R relies on several factors, including the skin effect factor F_S, which is expressed as:

$$F_S = \frac{\sinh(2A) + \sin(2A)}{\cosh(2A) - \cos(2A)}, \tag{4.11}$$

the computation of F_R also considers the proximity effect factor F_P, which is represented as

$$F_P = \frac{2(N_t^2 n_k - 1)}{3} \frac{\sinh(A) - \sin(A)}{\cosh(A) + \cos(A)}, \tag{4.12}$$

furthermore, the effective litz-wire diameter, denoted as A, contributes to the calculation of F_R, and is defined as

$$A = \left(\frac{\pi}{4}\right)^{0.75} \frac{d_l}{\delta_w} \sqrt{\eta_p}. \tag{4.13}$$

The skin depth of winding conductor is given by

$$\delta_w = \sqrt{\frac{\rho_w}{\pi \mu_0 f}}. \tag{4.14}$$

The variables used in Equations 4.10-4.13 are defined as follows: d_l represents the diameter of the conductor of the litz wire strand; N_t denotes the number of winding layers; ρ_w is the resistivity of the material; n_k signifies the number of strands and η_p is the porosity factor for litz wire[46].

The $R_{w,dc}$ is given by

$$R_{w,dc} = \frac{4\rho_w N_t}{n_k \pi d_l^2}. \tag{4.15}$$

thus, $R_{w,ac}$ can be calculated

$$R_{w,ac} = F_R R_{w,dc} \tag{4.16}$$

Therefore, these equations are instrumental in determining the resistance necessary

for calculating Equation 4.9.

4.2.2.2 Magnetic components thermal model

The surface power loss density of an inductor/transformer is given by

$$\psi = \frac{P_{total}}{A_t}, \tag{4.17}$$

where A_t is the radiating surface area, and P_{total} is the total loss (copper and core loss). The temperature rise for steady-state operation is given by

$$\Delta T = 450 \, \psi^{0.826} \, [°C]. \tag{4.18}$$

4.2.2.3 Capacitor losses

Capacitors are known to have different loss mechanisms, including dielectric loss and losses due to the Joule effect. However, in high-power topologies and at voltage levels of a few hundred volts, dielectric losses can be neglected.

A real capacitor exhibits parasitic elements such as equivalent series resistance (ESR) and equivalent series inductance (ESL). The following equation can be used to calculate the resistive losses of capacitors.

$$P_{ESR} = \frac{ESR}{N_C} \, I^2_{rms,Cap}, \tag{4.19}$$

where $I_{rms,Cap}$ is the rms current flowing through the capacitor, N_C is the number of parallel capacitors used, and ESR is the equivalent series resistance of the capacitor, which can be found in the manufacturer datasheet.

The ESL of the capacitor typically has a negligible effect on the ripple, in the case of filter capacitors. However, for a resonant capacitor, the ESL must be considered, as it becomes part of the resonant tank and can influence the value of the resonant frequency of the tank.

4.2.2.4 Semiconductors losses

Power switch losses encompass two primary sources: conduction losses and switching losses.

Conduction Losses:

Conduction Losses in a mosfet can be calculated using the following equation

$$P_{cond} = R_{DSon} \, I^2_{Drms}, \tag{4.20}$$

where I_{Drms} represents the drain current flowing through the mosfet, and R_{DSon} denotes the drain-to-source resistance of the mosfet in its on-state.

This Equation 4.20 represents the power dissipated as heat due to the resistance encountered by the current flowing through the mosfet when it is in its conducting state. By knowing the drain current and the drain-to-source resistance of the mosfet (specified in the datasheet), one can calculate the conduction losses, which contribute to the overall power dissipation of the device.

Switching Losses:

Switching losses in mosfets refer to the energy dissipation during state transitions, which occur due to the charging and discharging of internal capacitances. These losses can be calculated based on the mosfet energy curves.

Figure 4.2a and Figure 4.2b illustrate the turn on and turn off energies, respectively, based on the current and voltage applied to the mosfet.

(a) Turn on energy.
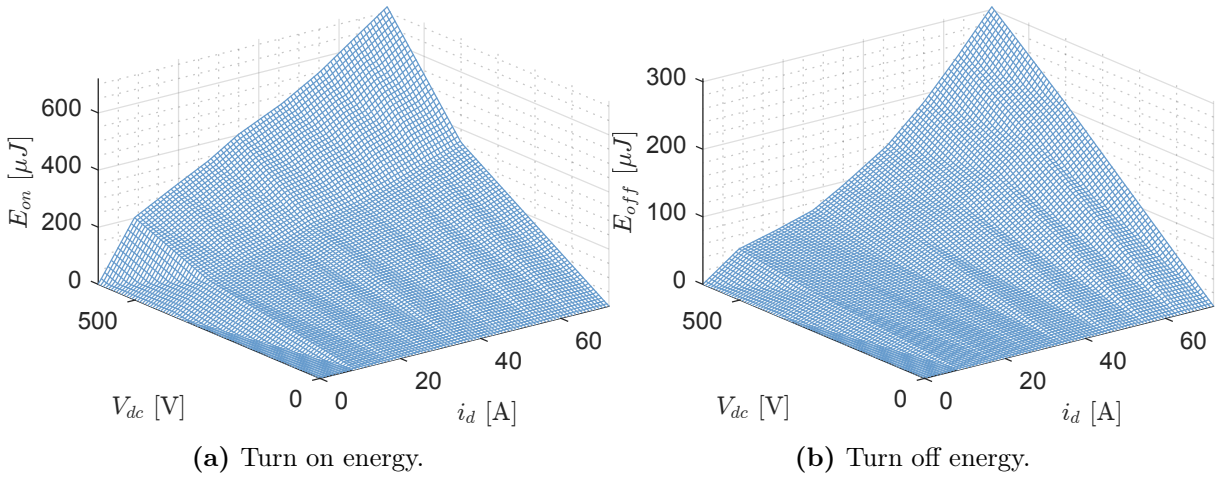
(b) Turn off energy.

Figure 4.2 – Turn on and turn off energies at the mosfet.

Once the turn on and turn off energies are obtained, the turn on and turn off losses can be calculated as follows

$$P_{on} = E_{on}\, f_{sw}, \ \ P_{off} = E_{off}\, f_{sw}. \tag{4.21}$$

The total switching losses are given by

$$P_{sw} = P_{on} + P_{off}. \tag{4.22}$$

4.2.3 Parameters model

4.2.3.1 Inductors Model

To design the inductor, the methodology used is described in [48]. The process begins with the application of the Ampere law.

$$\oint_C = H_c\, dl = Ni. \tag{4.23}$$
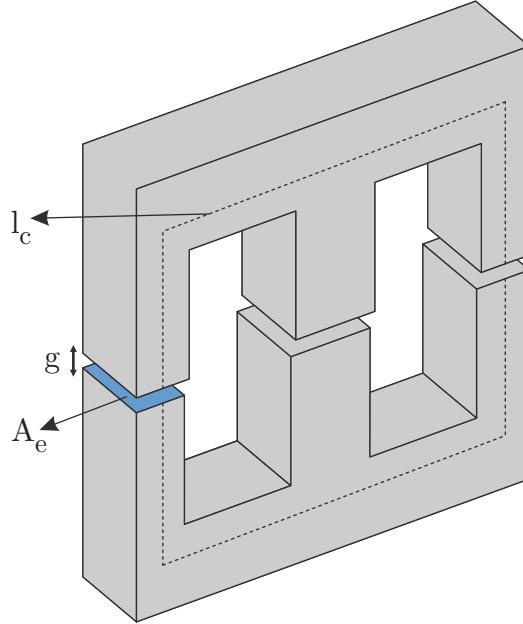
Figure 4.3 − E core representantion of the inductor.

To simplify, a constant cross-section along the core length is assumed. Additionally, uniform flux density across the cross-sectional area and a constant magnetic field intensity (H_c) around the loop C are assumed. This assumption holds as long as there is no flux leakage from the core. Thus, applying Equation 4.23 in Figure 4.3.

$$H_c\, l_c = Ni. \tag{4.24}$$

Equation 4.24 show the magnetic field intensity in terms of the product Ni. This magnetic field intensity produces a magnetic flux density (B_c)

$$B_c = \mu_r\, \mu_0\, H_c. \tag{4.25}$$

where μ_r represents the relative permeability, and μ_0 denotes the permeability of free space.

The ampere turns product, Ni, operates analogously to the electromotive force (emf) in an electrical circuit, propelling the magnetic field around the core, akin to how emf drives current through conductors. The flux (ϕ) in the core is given by

$$\phi = B_c\, A_e = \mu_r\, \mu_0\, H_c\, A_e, \tag{4.26}$$

rearranging the terms of the equation in function of H_c

$$H_c = \frac{\phi}{\mu_r\, \mu_0\, A_e}. \tag{4.27}$$

So, applying Ampere law (Equation 4.24) to Equation 4.27

$$N\,i = \phi \frac{l_c}{\mu_r\,\mu_0\,A_e} = \phi\,\mathfrak{R}_c,$$

(4.28)

where $\mathfrak{R}_c$ is the reluctance of the core, that is given by

$$\mathfrak{R}_c = \frac{l_c}{\mu_r\,\mu_0\,A_e}.$$

(4.29)

And the reluctance of the gap ($\mu_r = 1$) is given by

$$\mathfrak{R}_g = \frac{g}{\mu_0\,A_g},$$

(4.30)

here g is the length of the air gap. The, the equivalent reluctance of the gapped core presented in Figure 4.3 is

$$\mathfrak{R}_{eq} = \mathfrak{R}_c + 2\,\mathfrak{R}_g = \frac{l_c}{\mu_r\,\mu_0\,A_e} + \frac{2\,g}{\mu_0\,A_g}.$$

(4.31)

The cross-sectional area of the core is set to be equal to the cross-sectional area of the gap. So, simplifying Equation 4.31

$$\mathfrak{R}_{eq} = \frac{l_c}{\mu_{eff}\mu_0 A_e}.$$

(4.32)

This means that the reluctance of the gapped core is equivalent to the reluctance of a core of length l_c and relative permeability μ_{eff}, with

$$\mu_{eff} = \frac{1}{\dfrac{1}{\mu_r} + \dfrac{1}{l_c/2\,g}}.$$

(4.33)

So, finally the inductance of the inductor can be derived using the following equation

$$L = \frac{N_L^2}{\mathfrak{R}_{eq}},$$

(4.34)

where N_L is the number of turns of the inductor.

It can be observed that the inductance value is directly influenced by the variation in the number of turns and the length of the gap, while other parameters remain fixed based on the core used. These parameters are variables in the optimization methodology that will be implemented in this chapter.

4.2.3.2 Transformer model

The model employed to design the transformer is very similar when compared to that of the leakage inductor. The methodology employed for designing the transformer is derived from [49]. The difference is given by the reluctance of the magnetic circuit, which

is approximated by the reluctance of the gap.

The operation of the resonant CLLLC converter is directly linked to the magnetization inductance of the transformer to achieve ZVS on the primary side. Consequently, the transformer design is carried out to directly determine this inductance.

The magnetizing inductance on the primary side is calculated as follows

$$L_m = \frac{N_P^2}{\mathfrak{R}_g}.$$

(4.35)

Likewise, it is noted that the magnetizing inductance depends solely on the gap length and the number of turns on the primary side. These parameters are variables in the optimization methodology throughout this chapter.

4.2.3.3   Capacitors Model

The resonant tank capacitance is given by the number of capacitors in parallel, how to is presented by

$$C = N_C C_n,$$

(4.36)

where N_C is the number of the capacitor in parallel and C_n is the capacitance of each capacitor.

4.3   AN ALGORITHMIC APPROACH TO OPTIMAL DESIGN

The models presented in preceding sections will serve as the foundation for optimizing components used in power electronic applications. The optimization process in this work is based on the methodology proposed by [50].

The design optimization methodology employed adopts a unified approach, integrating all previously discussed main converter losses into a single routine. This optimization routine determines the optimal design based on the loss model, resulting in the highest efficiency.

4.3.1   Aim of the converter design

As part of this topic, output power and output voltage matrices are provided to identify specific points for optimizing the converter. Following this, the switching frequency is determined, considering both the operating point and the resonant frequency of the resonant tank.

The objectives outlined for the converter design in this work are arranged according to their priorities, as follows:

1. Achieve the highest possible converter efficiency at the operating points and with the components described in Table 4.1.

2. Optimize the ratio between the magnetizing inductance and the leakage inductance of the resonant tank, denoted by $k = \frac{L_m}{L_1}$. This balance is essential to manage the voltage gain of the resonant tank and the magnetizing inductance of the transformer. The value of k should ideally range between 4 and 6, as excessively low or high values are undesirable.

3. Set the switching frequency to at least 80% of the resonant frequency to avoid operation in a highly gain-sensitive region.

The initial step involves selecting the design variables, which include: the number of turns of the primary inductor $(N_{L,p})$; the primary inductor air gap length $(l_{g,p})$; the number of primary capacitors in parallel $(N_{C,p})$; the number of turns in the primary winding (N_p); the number of turns in the secondary winding (N_s); the transformer air gap length $(l_{g,tr})$; the number of turns of the secondary inductor $(N_{L,s})$; the secondary inductor air gap length $(l_{g,s})$; and the number of secondary capacitors in parallel $(N_{C,s})$.

The parameters of the selectable converter (namely $N_{L,p}$, $l_{g,p}$, $N_{C,p}$, N_p, N_s, $l_{g,tr}$, $N_{L,s}$, $l_{g,s}$, and $N_{C,s}$) are calculated to ensure that the design process maximizes the average efficiency $\left(\overline{\eta}_{design}\right)$,

$$\overline{\eta}_{\text{design}} = \frac{1}{3} \sum_{j=1}^{3} \left(\eta \Big|_{V_{out}=\vec{V}_{out,j},\, P_{out}=\vec{P}_{out,j}} \right), \tag{4.37}$$

which considers the three different points described below

$$\begin{aligned}
\vec{V}_i &= 400\,\text{V}, \\
\vec{V_{\text{out}}} &= \left(200\,\text{V}\ \ 400\,\text{V}\ \ 450\,\text{V} \right)^T, \\
\vec{P_{out}} &= \left(3\,\text{kW}\ \ 5\,\text{kW}\ \ 3.5\,\text{kW} \right)^T.
\end{aligned} \tag{4.38}$$

In Equation 4.38, three different operating points are defined, encompassing the lowest and highest output voltages of the converter, as well as the corresponding power levels at which the converter must operate for each voltage.

The materials used in the optimization routine are described in Table 4.1.

4.3.2 Particle swarm optimization (PSO)

PSO employs an algorithm to minimize the total loss for operational points. In PSO, an optimization problem is defined with a specific objective function to minimize or maximize. Search space boundaries are established to define the valid solution space. The swarm is configured with parameters such as the number of particles and the dimensional problem. Each particle is initialized with random positions and velocities within the search space [51].

Table 4.1 – List of materials used in optimization.

Components	Code
Inductor core (L_1, L_2)	E55/28/25-N87
Inductor wire (L_1, L_2)	392x37 AWG Litz
Resonant Capacitor (C_1, C_2)	R76PI23304030J
Transformer core	E59/31/22 - N97
Transformer wire	392X37 AWG Litz
Primary Power Switches	C3M0030090K
Secondary Power Switches	C3M0030090K

The optimization process begins by defining the goals and constraints of the power converter project. This establishes the desired efficiency for a specific converter operating points, for power density, and other pertinent performance metrics. The aim is to identify the optimal design that maximizes efficiency while adhering to specified constraints [52].

The methodology for the CLLLC resonant converter project involves the using equations detailed in the preceding section, which are then applied to PSO. The PSO algorithm is employed to identify the global optimum of an objective function defined by Equation 4.37. Within this algorithm, a population of potential solutions traverses the search space to discover the most favorable solution.

Setting upper and lower bounds for the initial population is fundamental for initiating the optimization process. These bounds define the permissible range of values for decision variables, guiding the algorithm in exploring a meaningful solution space. By constraining the search to viable regions, the optimization process becomes more efficient, converging towards optimal or near-optimal solutions while avoiding infeasible outcomes. The upper and lower bounds are described in Table 4.2.

Table 4.2 – Optimization Parameters.

Parameter	Lower Bound	Upper Bound
N_L (L_1, L_2)	5	10
l_g (L_1, L_2)	0.05 mm	2 mm
N_C (C_1, C_2)	2	7
N_P	5	13
N_S	5	13
$l_{g,tr}$	0.05 mm	2 mm

4.3.3 Project Definition

The methodology outlined in this chapter relies on the utilization of Table 4.1 and Table 4.2. Consequently, it enables the determination of all parameters associated with the CLLLC resonant tank. By using these tables, the optimization process acquires

the necessary constraints and material properties essential for accurately defining the parameters of the resonant tank.

It is worth noting that optimization is used to determine the parameters of the resonant tank of the converter. The model established in Chapter 3 is modified for the design of the resonant tank. This modification involves replacing the output filter with a voltage source, as shown in Figure 4.4. Since the system inputs consist of voltage and power vectors, the load and output current can be calculated. The output current, derived from the vectors, must precisely match the current obtained from the determined DP model, as given in Equation 4.39. This modification ensures that the resonant tank processes the required power for the specified point.
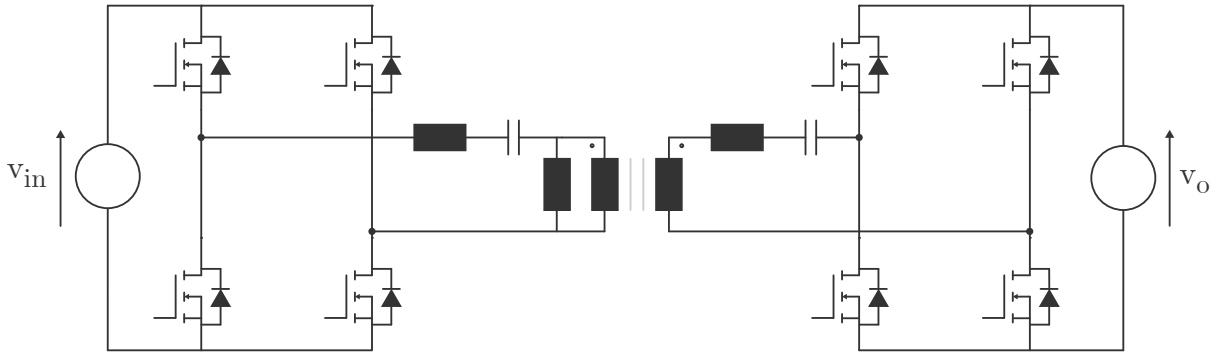

Figure 4.4 – CLLLC resonant converter optimization model.

$$\langle i_o \rangle_0 = \frac{4}{\pi} \sqrt{\left(\langle i_{L2} \rangle_1^R \right)^2 + \jmath \left(\langle i_{L2} \rangle_1^I \right)^2}. \tag{4.39}$$

The rationale behind the modification of the previously obtained model is to ensure that the resonant tank of the converter processes the required power specified for that particular point. By employing Equation 4.39 and the clamped output voltage, the power processed by the resonant tank can be readily determined.

The optimization algorithm is outlined in Figure 4.5. This algorithm adjusts iteratively vary the converter parameters in order to find an optimized solution. It calculates the total losses for different operating points using Equation 4.37. This systematic approach allows for the exploration of various parameter combinations and facilitates the identification of the most efficient converter design.

The algorithm is designed to optimize the converter for N_{points} operating conditions. Its goal is to minimize the total losses of the converter across these conditions, which can be weighted using the vector λ. If the converter fails to operate under any of the specified conditions, the parameters are adjusted, and the algorithm seeks to identify a solution set where all conditions are met, resulting in the optimal design with the lowest overall losses.

The optimization begins by initializing the particle swarm and determining the parameters needed to calculate the resonant tank parameters. Next, the resonant frequency of the tank is calculated, followed by determining the switching frequency and steady-state

```
┌─────────────────────────┐
│  Initial Population:     │
│  N_{L,p}, l_{g,p}, N_{C,p}, N_P, │
│  N_S, l_{g,tr}, N_{L,s}, l_{g,s}, N_{C,s}. │
└─────────────────────────┘
```
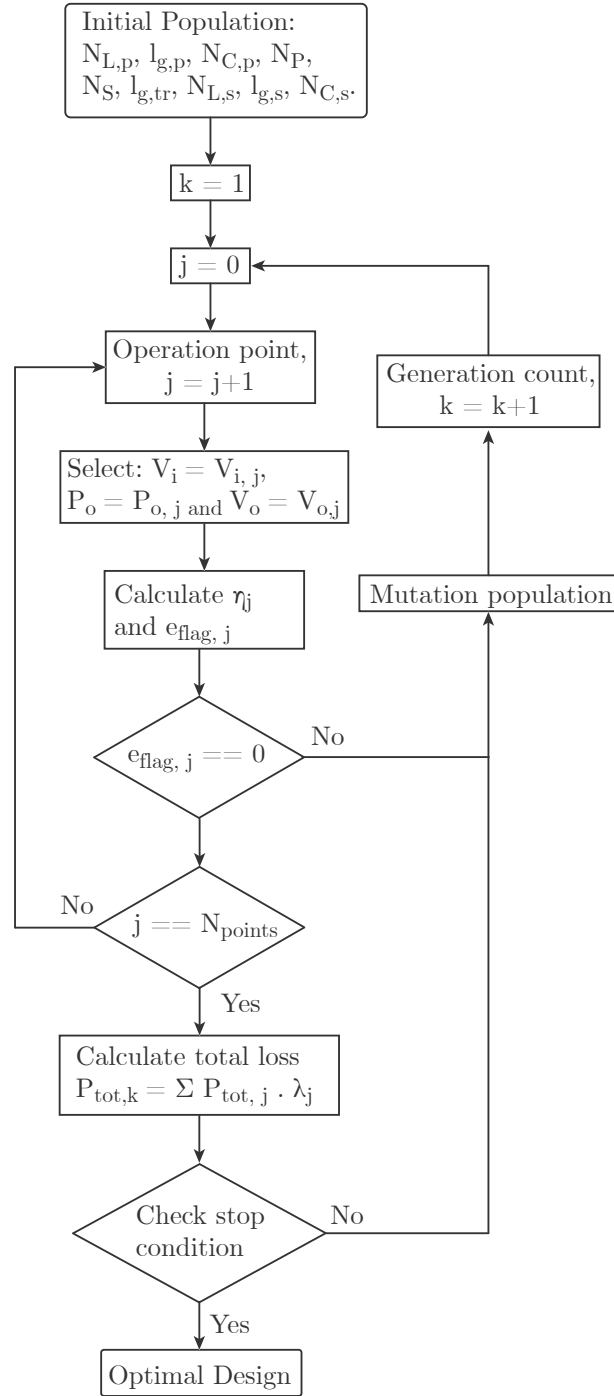
Figure 4.5 – Flowchart for Optimizing Parameters in CLLLC Resonant Converter Design.

values based on the operating point. Finally, the algorithm calculates the losses and returns the construction parameters for the project.

4.4   OPTIMIZATION RESULTS

The PSO-based algorithm used to optimize the CLLLC resonant converter tank, as proposed in this work, yielded the design parameters presented in Table 4.3.

With these parameters, all components of the resonant tank can be calculated and are presented in the Table 4.4.

Table 4.3 – Results obtained in optimization.

Number of turns in the primary inductor $(N_{L,p})$	10
Length of the primary inductor gap $(l_{g,p})$	0.99 mm
Number of primary capacitors in parallel $(N_{C,p})$	4
Number of turns in the primary (N_P)	10
Number of turns in the secondary (N_S)	10
Length of the transformer gap $(l_{g,tr})$	0.42 mm
Number of turns in the secondary inductor $(N_{L,s})$	7
Length of the secondary inductor gap $(l_{g,s})$	0.85 mm
Number of secondary capacitors in parallel $(N_{C,s})$	8

Table 4.4 – Parameters obtained in optimization.

Parameters	Values
Primary resonant inductor (L_1)	25.985 μH
Primary resonant capacitor (C_1)	132 nF
Magnetizing inductance (L_m)	111.94 μH
Secondary resonant inductor (L_2)	14.815 μH
Secondary resonant capacitor (C_2)	264 nF
Turns ratio (n)	1
Resonant frequency (f_{res})	85.936 kHz

The results obtained from the optimization algorithm are demonstrated in Equation 4.40, depicting efficiency across three specified operating points as illustrated in Equation 4.38. Following the implementation of the routine, an optimal point was achieved that satisfied the predefined constraints and objectives.

$$\begin{pmatrix} \eta_1\left(\vec{V}_{out,1}, \vec{P}_{out,1}\right) \\ \eta_2\left(\vec{V}_{out,2}, \vec{P}_{out,2}\right) \\ \eta_3\left(\vec{V}_{out,3}, \vec{P}_{out,3}\right) \end{pmatrix} = \begin{pmatrix} 95.02\% \\ 98.05\% \\ 97.80\% \end{pmatrix} \tag{4.40}$$

The temperature rise calculated by the optimization algorithm is shown in Table 4.5.

Table 4.5 – Components temperature rise.

Parameter	η_1	η_2	η_3
$L_{1_{Temp}}[°C]$	65.78	39.91	30.14
$L_{2_{Temp}}[°C]$	49.69	25.73	20.27
$T_{R_{Temp}}[°C]$	120.54	100.25	110.32

The steady-state values of these three operation points are presented by Figure 4.6, Figure 4.7 and Figure 4.8.
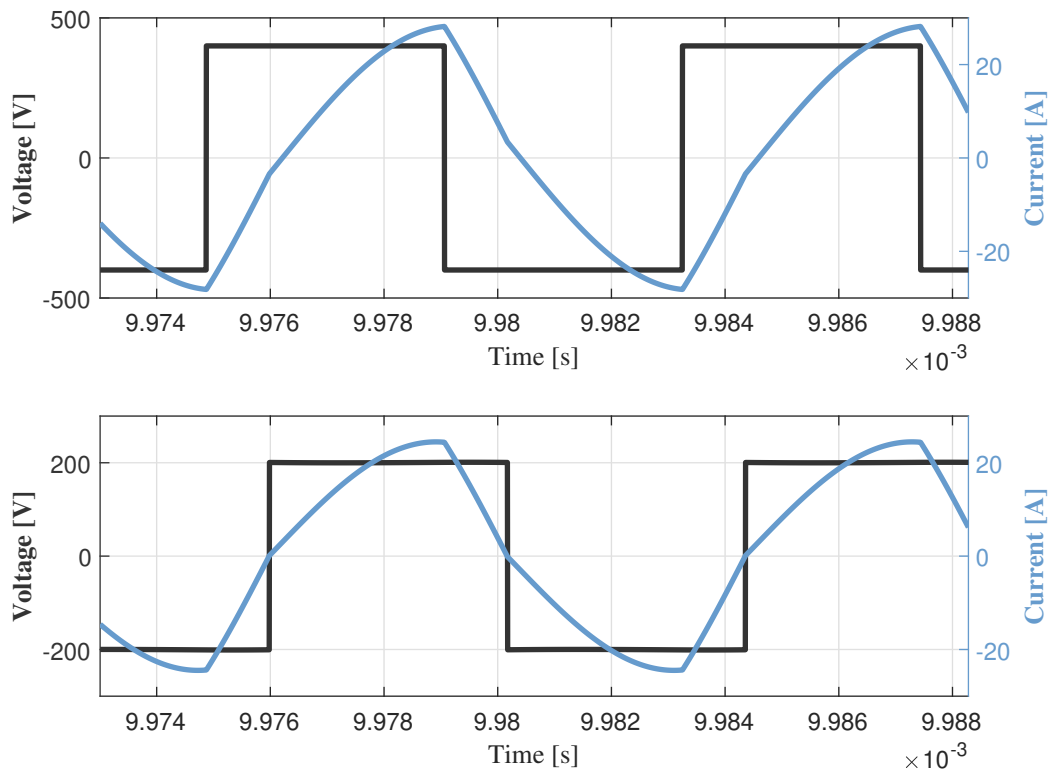
Figure 4.6 – Currents and voltages in the resonant tank for point η_1.

In Figures 4.6,4.7 and 4.8, the power converter demonstrates ZVS on the primary side during turn on, indicated by its negative current, while undergoing hard switching during turn off. On the secondary side, the converter operates with SR, functioning similarly to diodes. Consequently, the current on this side of the converter is typically very close to zero. The concept of substituting diodes with switches aims to minimize losses. This substitution significantly reduces losses on the secondary side to essentially the conduction losses of the switches, thereby eliminating the voltage drop caused by the diodes and, consequently, minimizing losses.
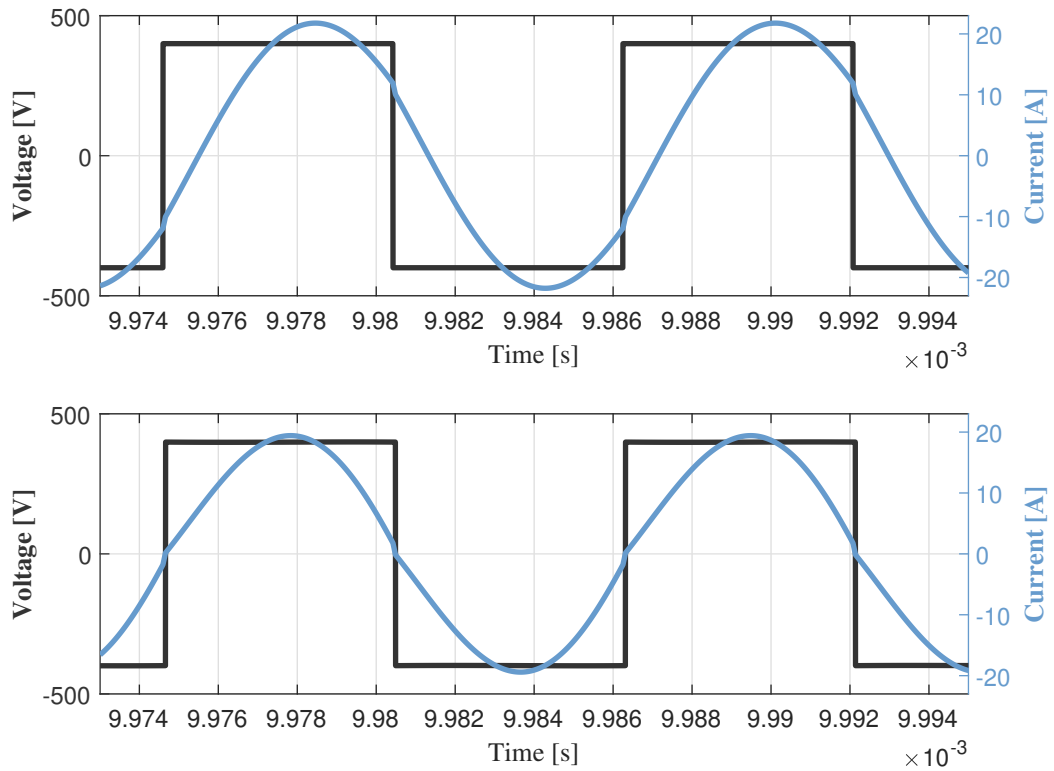
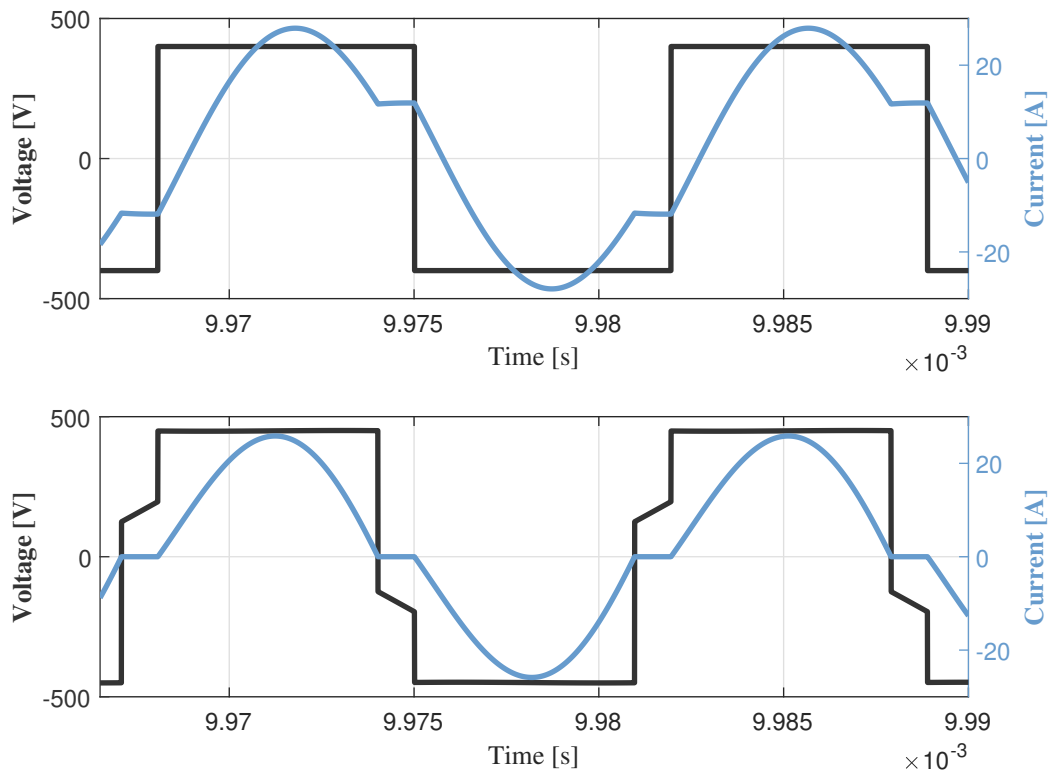**Figure 4.7** – Currents and voltages in the resonant tank for point η_2.

Figure 4.8 – Currents and voltages in the resonant tank for point η_3.

4.5 DISCUSSION ABOUT THE DESIGN METHODS

Firstly, the most commonly employed design methodology in the literature for the CLLLC resonant converter is presented. This methodology involves straightforward steps, directly utilizing voltage gain curves to design the converter. Additionally, passive elements of the resonant tank are designed to ensure smooth switching by the magnetizing inductance. Based on this, the series inductance and tank capacitance are determined to achieve the desired resonance frequency in the project. However, this approach, which determines inductance values, necessitates another physical design of the inductors and transformer. This may lead to efficiency issues since losses in both magnetic elements and switches are not considered in this design methodology, potentially resulting in suboptimal utilization of the components.

In contrast to the previously mentioned methodology, the approach employed in this chapter integrates all converter parameters. The optimization algorithm not only provides values for the inductance and capacitance of the resonant tank but also returns their construction aspects such as the number of turns and gap size in the inductors. Similarly, it optimizes parameters for the transformer and capacitors, including the number of capacitors connected in parallel to achieve the necessary capacitance. Furthermore, the algorithm aims to find the best possible design from the available component list for constructing the converter, optimizing its resonance frequency. The switching frequency is calculated to meet the power and voltage requirements defined in the project.

Designing the converter based on the loss model enables better utilization of the components, extracting maximum performance from each. The use of an integrated methodology also facilitates the physical construction of the topology.

4.6 SUMMARY

This chapter focuses on the design of the CLLLC resonant converter. It begins by presenting the most commonly used methodology in the literature for designing this type of converter. Next, a comprehensive loss model is developed to accurately calculate all global losses associated with the CLLLC resonant converter. Additionally, equations for determining all parameters within the resonant tank are established.

A PSO-based algorithm is then employed to design the converter, incorporating the previously mentioned parameter and loss models. This algorithm aims to deliver the most efficient design using the materials available for the project.

The chapter presents the results of the optimized design, including both physical and electrical parameters. An efficiency vector is also provided for the specified operating points outlined in the optimization objectives. Finally, a comparison is made between the traditional design method and the optimized approach, highlighting the importance of optimization in improving the performance of this type of converter.

5 CLLLC RESONANT CONVERTER RESULTS

5.1 PROTOTYPE CONSTRUCTION

With the results obtained from the optimization algorithm in Chapter 4, the converter was implemented to experimentally validate the concepts studied. For the practical assembly of the converter, the materials listed in Table 4.1 were used, along with the results from the optimization algorithm presented in Table 4.3.

It is noteworthy that the optimization algorithm exclusively considered the magnetizing inductance of the transformer. However, in practical applications, the transformer also exhibits leakage inductances, which must be incorporated into its design. These leakage inductances are integrated in series with the series inductance of the resonant tank on both the primary and secondary sides. Consequently, the series inductance of the resonant tank comprises the sum of the series inductance of the tank and the leakage inductance of the transformer.

Table 5.1 presents the parameters obtained in practice for the CLLLC resonant converter.

The Figure 5.1 showcases the prototype developed for the experimental validation of this work. The image features the LaunchPad F28379D from Texas Instruments, which is used to provide the control pulses, alongside two full-bridge inverters, one for the primary side and the other for the secondary side. Furthermore, the picture displays the input filter, comprised of electrolytic capacitors and film capacitors, as well as the output filter consisting of film capacitors and a common-mode choke. It is noteworthy that the magnetics (components of the resonant tank) are positioned on the exterior of the PCB.

The inductors of the resonant tank and the transformer are presented in Figure 5.2, while the capacitors of the resonant tank are shown in Figure 5.3.

5.1.1 Test Setup

To conduct tests on the CLLLC resonant converter, a test setup configuration was assembled, as described in Figure 5.4.

Table 5.1 – CLLLC resonant converter prototype parameters.

Parameters	Values
Primary resonant inductor (L_1)	24.332 μH
Primary resonant capacitor (C_1)	132 nF
Leakage primary inductance (L_{tr1})	1.332 μH
Magnetizing inductance (L_m)	121.067 μ H
Leakage secondary inductance (L_{tr2})	1.331 μH
Secondary resonant inductor (L_2)	13.143 μH
Secondary resonant capacitor (C_2)	264 nF
Turns ratio (n)	1
Output capacitor (C_o)	12 μF
Damping capacitor (C_d)	12 μF
Damping Resistance (R_d)	2 Ω
Common mode choke (L_o)	2 μH

Figure 5.1 – Converter Prototype.

Figure 5.4 describes an illustration of the input source, along with the wattmeter connected to both the input and output, as well as a bank of resistors. The input and output power of the CLLLC resonant converter are measured using the wattmeter, enabling the calculation of its efficiency.

The equipment used for the experiments includes:

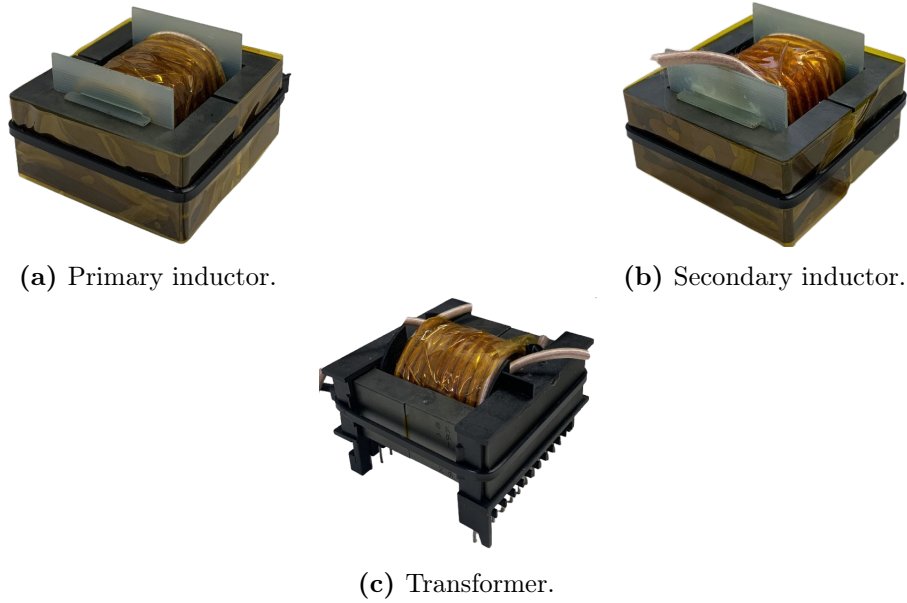- Wattmeter: WT1800 High Performance Power Analyzer.

(a) Primary inductor.

(b) Secondary inductor.

(c) Transformer.

Figure 5.2 – Resonant tank inductors and transformer.

(a) Primary resonant capacitors.
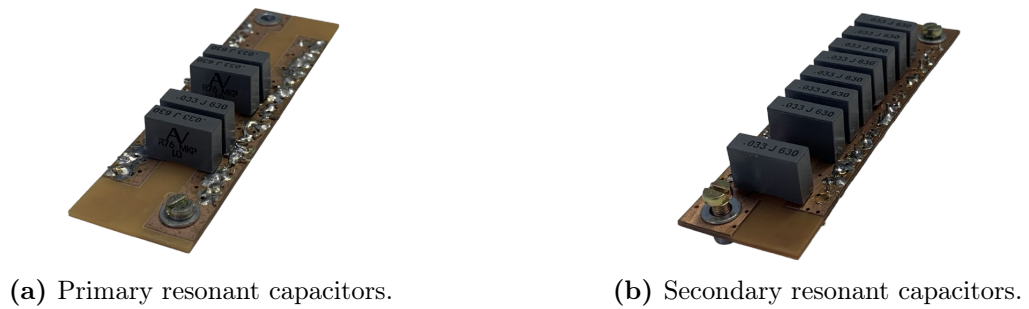

(b) Secondary resonant capacitors.

Figure 5.3 – Resonant tank capacitors.

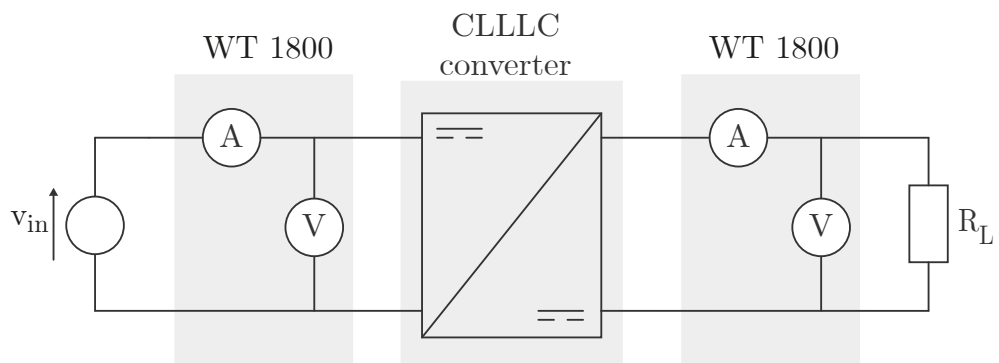**Figure 5.4** – CLLLC resonant converter test setup schematic.

- Voltage Source: Spitzenberger & Spies 4-Quadrant Amplifier APS 5000.

- Osciloscope: DPO4034 Tektronix Digital Oscilloscope 350 MHz.

5.2   VALIDATION OF CONVERTER OPERATION AND OPTIMIZATION

To validate the operation of the prototype and the designed resonant tank, experimental tests were conducted using the test setup presented in Figure 5.4.

To validate the operation of the CLLLC resonant converter, a test was conducted using a load resistance of $31.9\,\Omega$. This test was also simulated using MATLAB/Simulink. The comparison between the resonant tank currents in practice and in simulation can be seen in Figure 5.5, thus validating the functionality of the prototype.
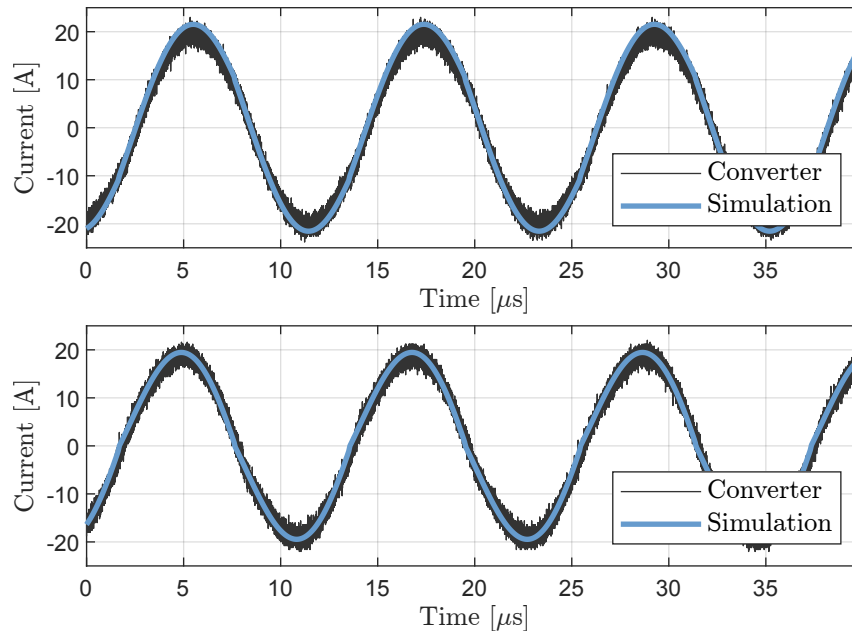

Figure 5.5 – Comparison between practical results and simulation.

Similarly, to validate the optimization implemented in Chapter 4, the central operating point was chosen, which coincides with the point depicted in Figure 5.5, where the converter operates with a switching frequency equal to the resonant tank frequency. This choice is motivated by the decreasing accuracy of the DP model as the converter's switching frequency deviates from the resonance frequency.

In Figure 5.6, a comparison is drawn between the measured practical losses and the calculated theoretical losses. Furthermore, the theoretical losses are qualitatively described with respect to the inductors, capacitors, switches, and transformer. It is evident that the primary source of losses in the converter is attributed to the switches, predominantly due to conduction losses. Concerning the magnetic components, the transformer emerges as the major source of losses, with losses distributed between the core and the windings. Inductor losses contribute slightly to the overall losses, while capacitor losses make a negligible contribution.

Observing Figure 5.7, the practical efficiency achieved by the converter at this point was 97.621%, whereas the theoretically calculated efficiency for this point stood at 98.05%.

To have a sense of the difference between the calculated theoretical losses and the measured practical losses, the relative error was calculated to be 16.55%. Several factors could account for this magnitude of relative error. Firstly, the optimization algorithm was used to design the components of the converter's resonant tank, without considering the
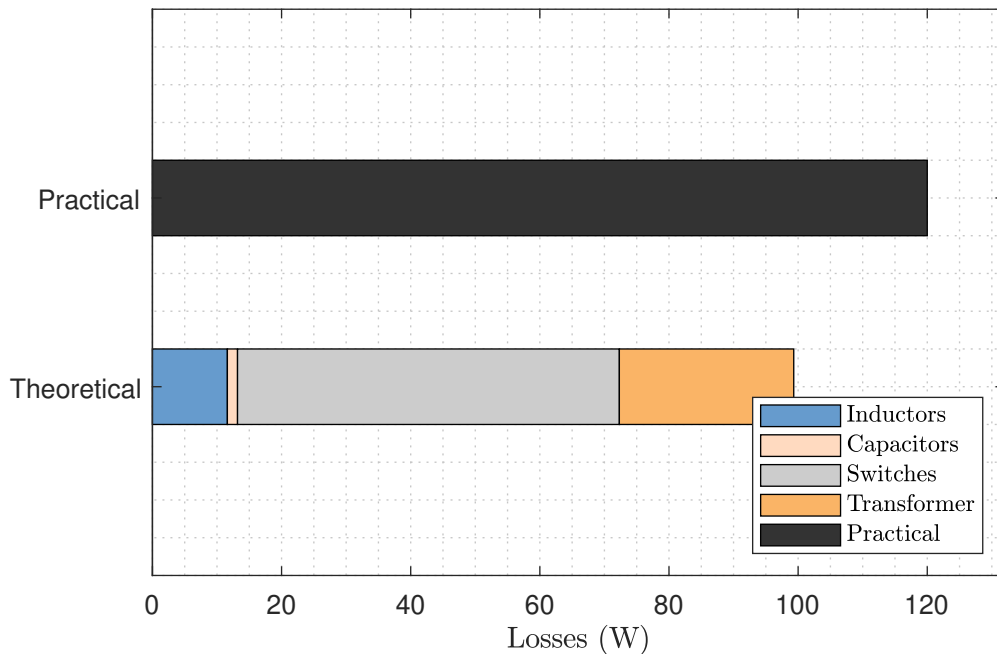
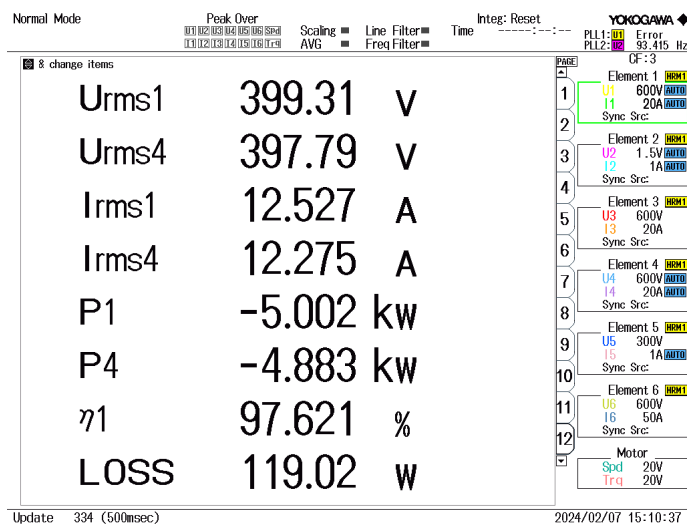**Figure 5.6** – Comparison between practical and theoretical losses.

Figure 5.7 – Efficiency at nominal power.

input filter capacitors, the output filter capacitors and the common-mode choke. These components contribute to additional energy losses in practical terms. Another factor that could explain this difference is SR. The optimization algorithm assumed that switching always occurs with zero current. In practical terms, however, there is always some current during switching, however minimal, which leads to switching losses in the system. All these factors contribute to the overall losses of the converter.

5.3 TESTING FOR DIFFERENT LOADS

The results were acquired by utilizing the body diodes of the secondary side mosfets. Given the dynamic operation of the CLLLC resonant converter in response to output load

variations, two distinct output loads and various operating points were initially selected. These points were determined by adjusting the frequency.

5.3.1 Results for a load resistance of 58 Ω

These tests were conducted with a load resistance of $58\,\Omega$ and switching frequencies of 80, 90, 100, and 110 kHz. The rationale for selecting these frequencies is to observe the converter across various operating regions. Consequently, the resonant tank processes different power levels at each of these points and delivers varying output voltages, sometimes functioning as a voltage step-down converter and other times as a voltage step-up converter.

The Figures 5.8, 5.9, 5.10, and 5.11 present the output voltage of the primary full bridge, the current in the primary tank inductor, the voltage applied across the secondary full bridge, and the current in the secondary tank inductor for switching frequencies of 80, 90, 100, and 110 kHz, respectively.

In Figure 5.8, the converter operates below the resonant frequency of the tank, indicating that it functions as a step-up converter. This is evident in Figure 5.12a, where the output voltage exceeds the input voltage.

It is worth mentioning that on the secondary side, conduction is carried out by the body diodes of the mosfets. For the C3M0030090K switch from Wolfspeed, the voltage drop across each of these diodes is around 4.3 V. Since two diodes are conducting in each stage, the total voltage drop is approximately 9 V.
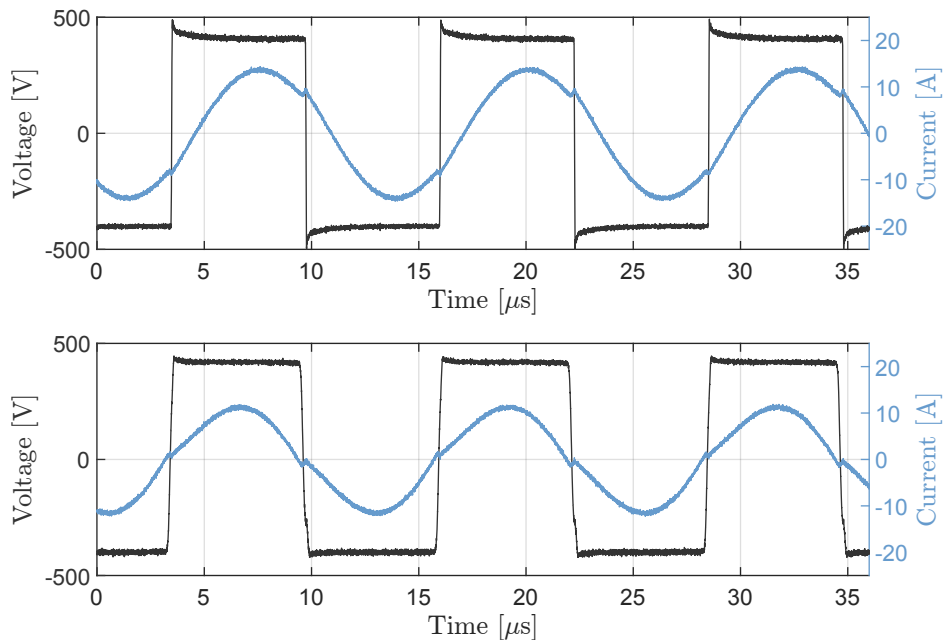
Figure 5.8 – Currents and voltages in the resonant tank for $f_{sw} = 80$ kHz and $R_L = 58\,\Omega$.

Furthermore, the switches on the primary side undergo ZVS at the turn on, as switching occurs when the current is negative. However, they experience hard switching at the turn off, as the current is positive. On the secondary side, switching occurs when the current reverses its polarity, causing the body diodes of the mosfets to conduct
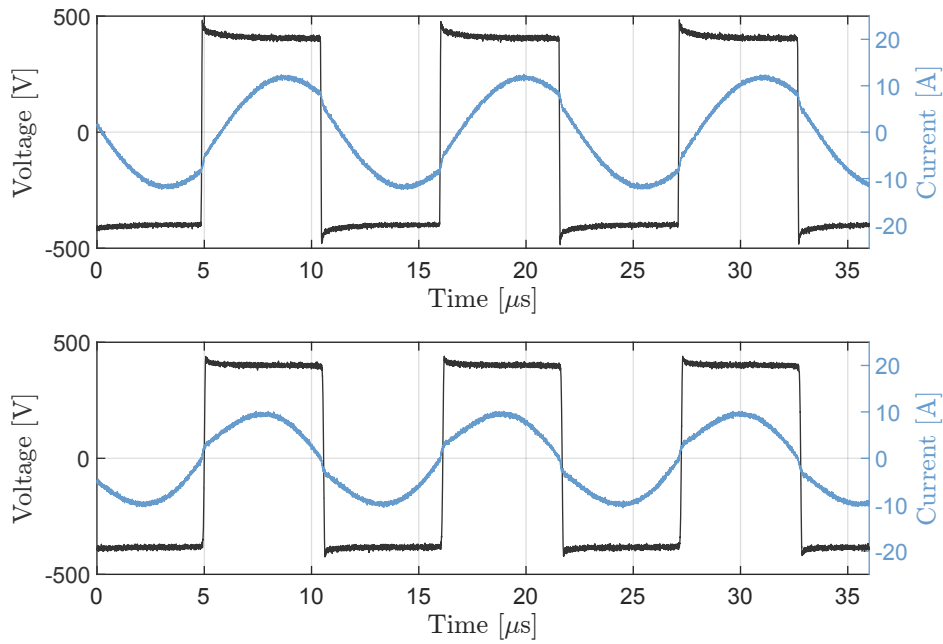
Figure 5.9 − Currents and voltages in the resonant tank for $f_{sw} = 90$ kHz and $R_L = 58\,\Omega$.

In Figure 5.9, the converter begins to operate in the step-down mode as shown in Figure 5.12a. At this operating point, it is noticeable that for frequencies higher than the resonant frequency, the resonant half-cycle is not fully completed due to the beginning of the next resonant half-cycle, as explained in Chapter 2. This is further evident when looking at Figures 5.10 and 5.11.
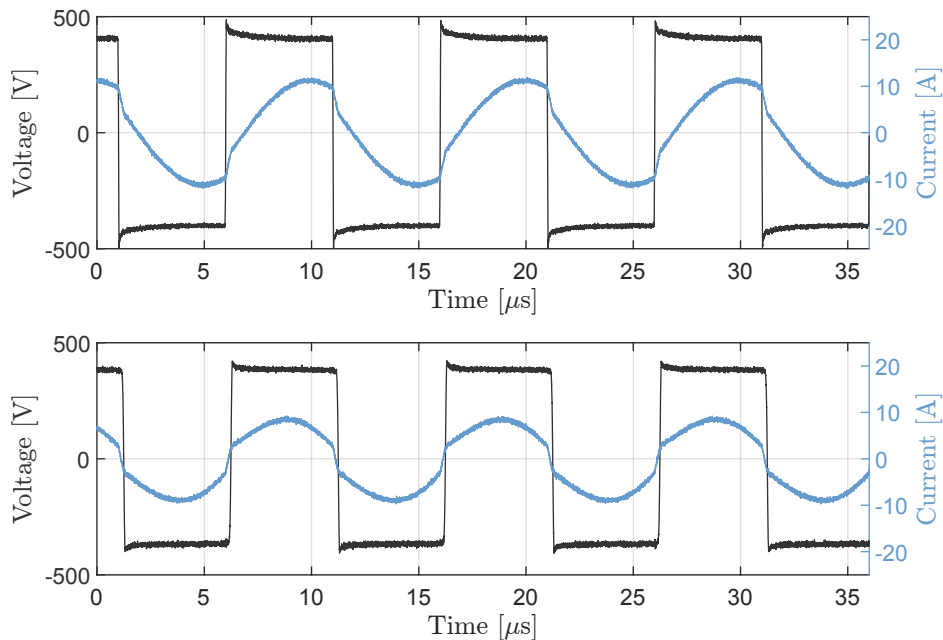

Figure 5.10 − Currents and voltages in the resonant tank for $f_{sw} = 100$ kHz and $R_L = 58\,\Omega$.

As the primary switching frequency is increased, in addition to the voltage being reduced, there is a decrease in power processing in the converter, resulting in lower current amplitudes both in the resonant tank and at the converter output. This is evident in
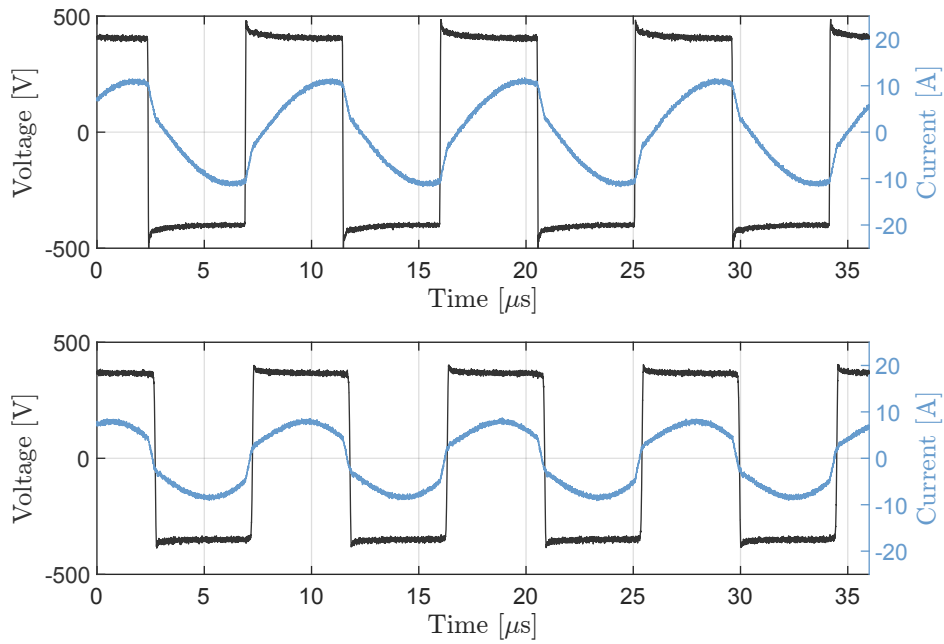
Figure 5.11 − Currents and voltages in the resonant tank for $f_{sw} = 110$ kHz and $R_L = 58\,\Omega$.
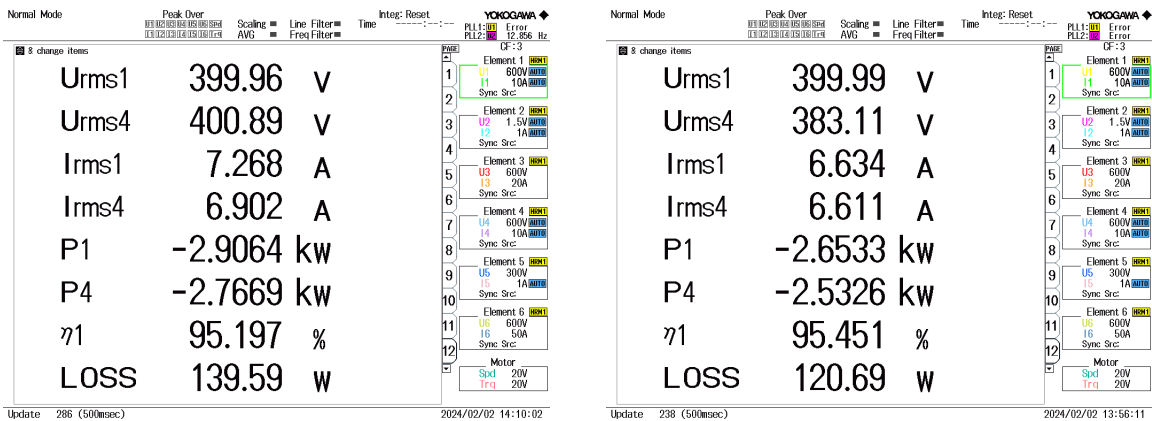
Figure 5.12.

(a) Efficiency with $fsw = 80$ kHz and $R_L = 58\,\Omega$.

(b) Efficiency with $fsw = 90$ kHz and $R_L = 58\,\Omega$.
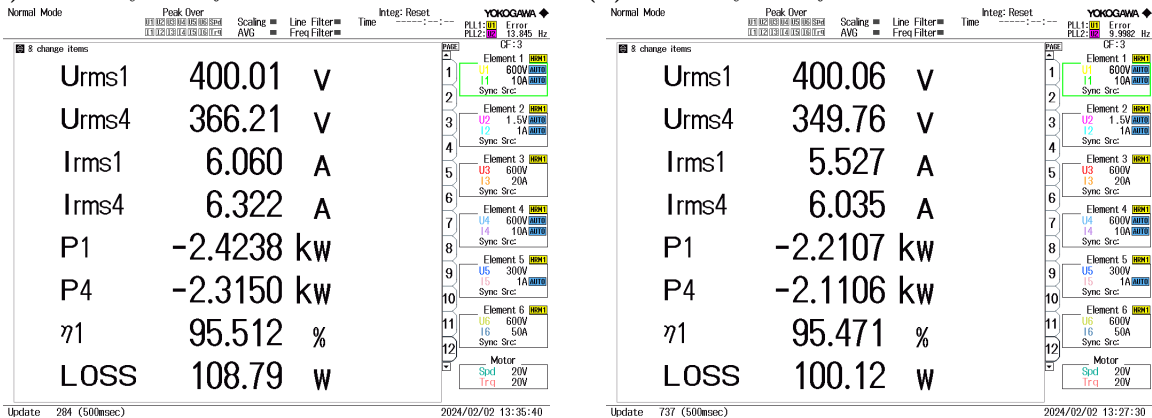
(c) Efficiency with $fsw = 100$ kHz and $R_L = 58\,\Omega$.

(d) Efficiency with $fsw = 110$ kHz and $R_L = 58\,\Omega$.

Figure 5.12 − Efficiencies for different switching frequencies and $R_L = 58\,\Omega$.

5.3.2 Results for a load resistance of 41.9 Ω

In the pursuit of comprehensively understanding the behavior of the resonant tank in the converter under varying load conditions, the impact of load resistance variation was meticulously investigated. This involved subjecting the converter to the same four operating points previously tested with a load resistance of 58 Ω, but this time with a load resistance of 41.9 Ω.

The rationale behind this examination lies in the fundamental principle that the resonant tank circuit's behavior is intrinsically linked to the load it drives. As load resistance changes, it directly influences the resonant frequency and the overall performance of the converter. Therefore, by exploring the converter's response to different load resistances, valuable insights can be gleaned into its operating characteristics.

The visual representations provided in Figures 5.13, 5.14, 5.15, and 5.16 offer a nuanced understanding of how the converter behaves at various switching frequencies (80 kHz, 90 kHz, 100 kHz, and 110 kHz) with a load resistance of 41.9 Ω. These figures vividly illustrate key parameters such as the output voltage of the primary full bridge, the current flowing through the primary tank inductor, the voltage applied across the secondary full bridge, and the current through the secondary tank inductor.
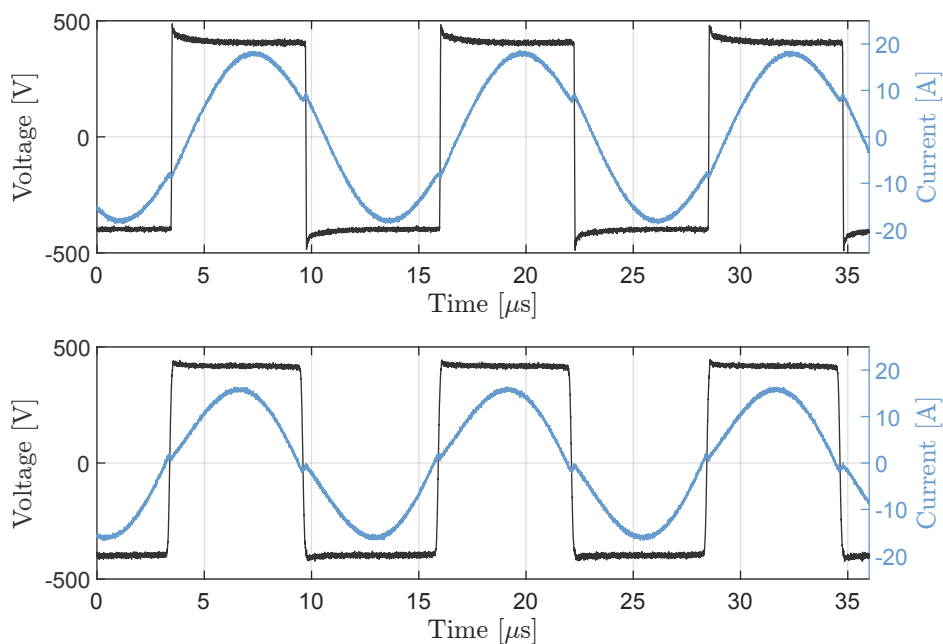
Figure 5.13 − Currents and voltages in the resonant tank for $f_{sw} = 80$ kHz and $R_L = 41.9\,\Omega$.

A meticulous analysis of these Figures reveals intriguing insights into the converter's behavior. For instance, when comparing Figure 5.12d with Figure 5.17d, it becomes apparent that the output voltage exhibits greater susceptibility to variations for lower load resistances. Specifically, in Figure 5.12d, the output voltage is recorded at 349.76 V for a switching frequency of 110 kHz, whereas in Figure 5.17d, it drops to 334.77 V for the

same frequency. This discrepancy underscores the significant influence of load resistance on the converter's output characteristics.
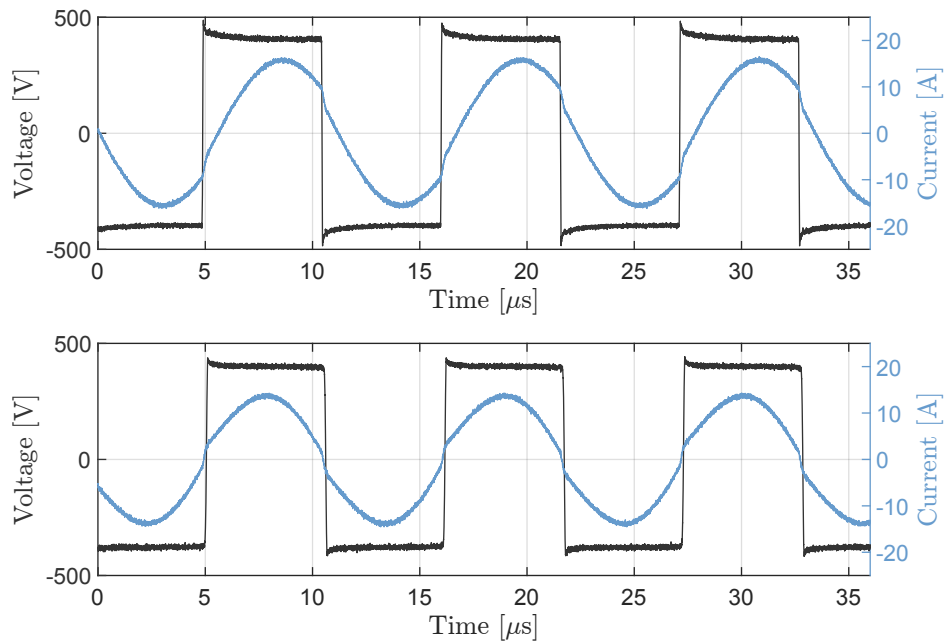
Figure 5.14 – Currents and voltages in the resonant tank for $f_{sw} = 90$ kHz and $R_L = 41.9\,\Omega$.
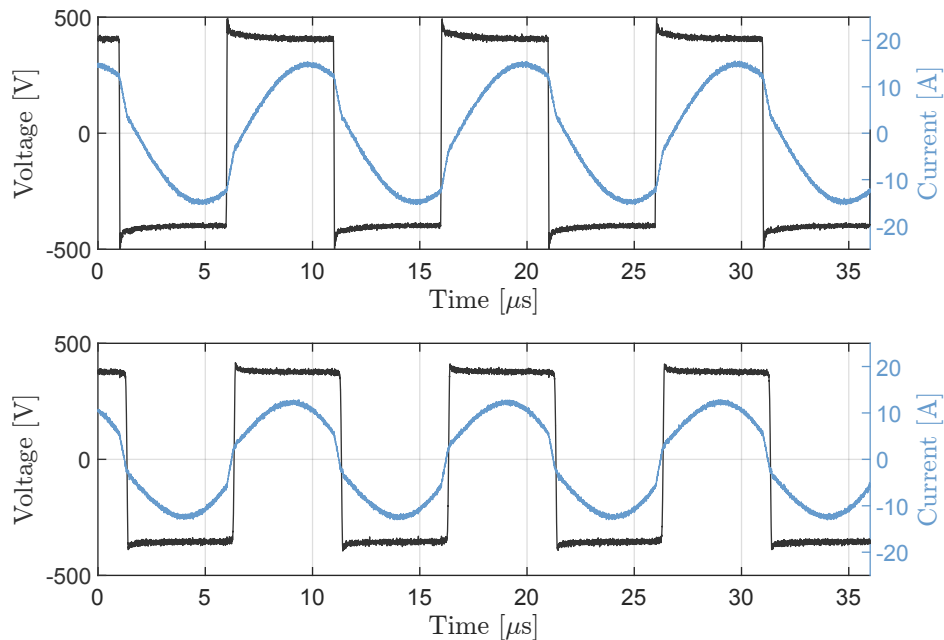
Figure 5.15 – Currents and voltages in the resonant tank for $f_{sw} = 100$ kHz and $R_L = 41.9\,\Omega$.

Moreover, the comparative analysis between the results obtained for the 58 Ω load resistance and the 41.9 Ω load resistance sheds light on the nuanced behavior of the converter under different load conditions. By juxtaposing these scenarios, it becomes evident that variations in load resistance can lead to notable differences in the converter's
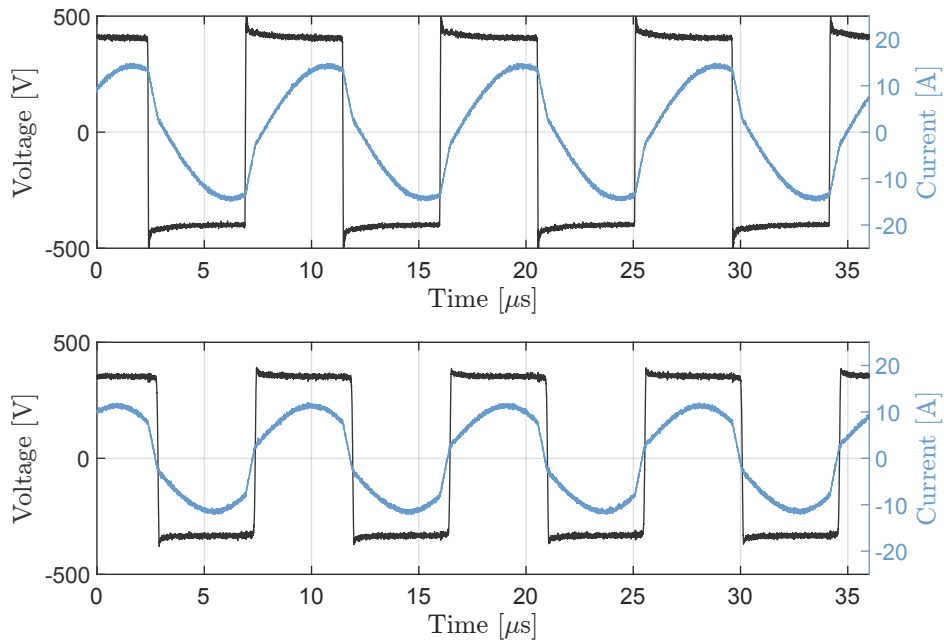
Figure 5.16 – Currents and voltages in the resonant tank for $f_{sw} = 110$ kHz and $R_L = 41.9\,\Omega$.

performance, particularly in terms of output voltage stability and response to switching frequency changes.

In conclusion, the findings of this investigation offer valuable insights into the intricate interplay between load resistance and the behavior of the resonant tank in the converter. By elucidating the impact of load variation on key performance parameters, this research contributes to a deeper understanding of converter dynamics and lays the groundwork for further advancements in resonant converter design and optimization.
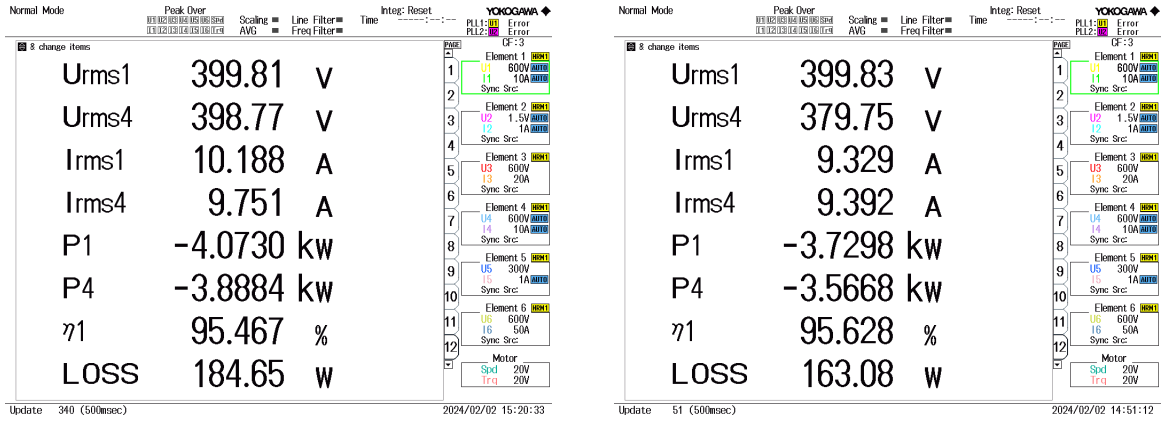
(a) Efficiency with $fsw = 80$ kHz and $R_L = 41.9\,\Omega$.

(b) Efficiency with $fsw = 90$ kHz and $R_L = 41.9\,\Omega$.
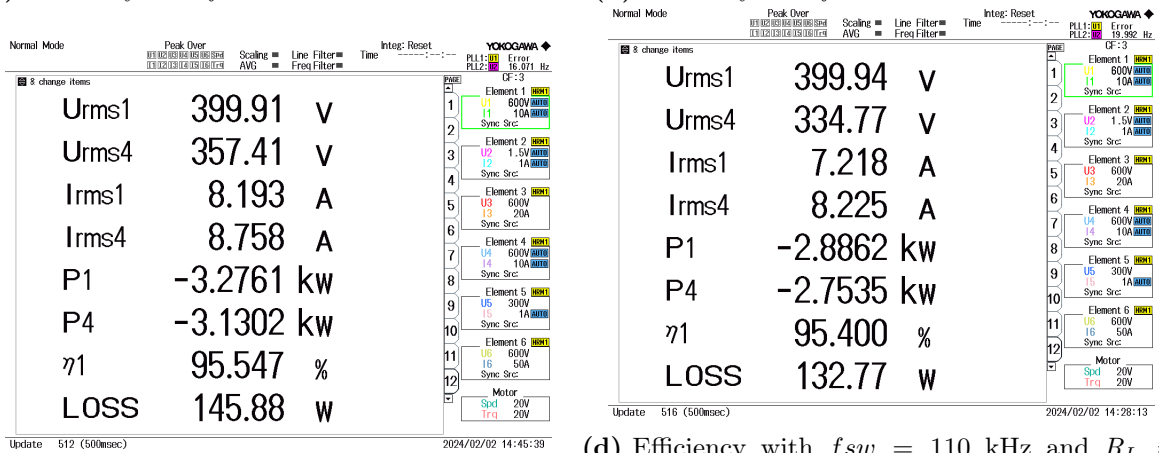
(c) Efficiency with $fsw = 100$ kHz and $R_L = 41.9\,\Omega$.

(d) Efficiency with $fsw = 110$ kHz and $R_L = 41.9\,\Omega$.

Figure 5.17 − Efficiencies for different switching frequencies and $R_L = 41.9\,\Omega$.

5.3.3 Discussion of results for different output loads

The Figure 5.18 illustrates the relationship between switching frequency and output voltage for two distinct load resistances, $R_L = 41.9\,\Omega$ and $R_L = 58\,\Omega$. As the switching frequency increases from 80 kHz to 110 kHz, the output voltage for both load resistances shows a generally downward trend. However, the rate of increase and the maximum output voltages differ between the two load resistances. For $R_L = 41.9\,\Omega$, the output voltage starts around 330V and rises steadily, peaking slightly below 400V at the lowest switching frequency. In contrast, the output voltage for $R_L = 58\,\Omega$ begins at a higher initial value of approximately 350V and similarly increases with frequency, reaching up to about 410V at the lowest frequency.

Comparing the two load resistances, it is evident that the system with $R_L = 58\,\Omega$ consistently achieves a higher output voltage than the system with $R_L = 41.9\,\Omega$ across the entire range of switching frequencies. This difference can be attributed to the higher load resistance allowing less current to flow through the circuit, resulting in a higher voltage drop across the load and subsequently a higher output voltage.

Similarly, Figure 5.19 shows the relationship between output current and switching frequency for two distinct load resistances, $R_L = 41.9\,\Omega$ and $R_L = 58\,\Omega$. As the switching
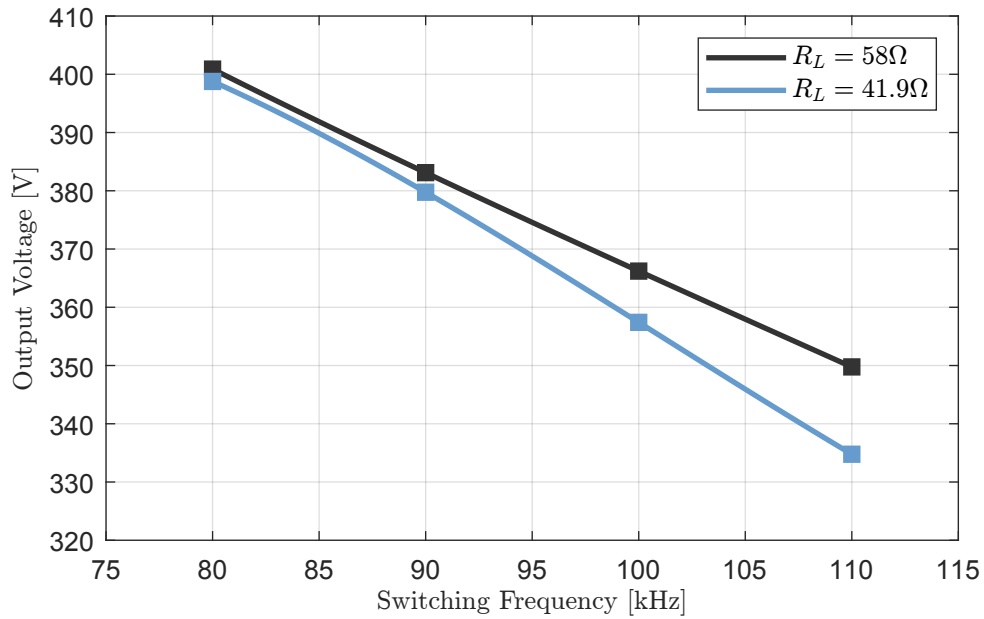
Figure 5.18 − Output voltage vs. switching frequency for different load resistances.

frequency increases from 80 kHz to 110 kHz, the output current for both load resistances generally exhibits a downward trend.
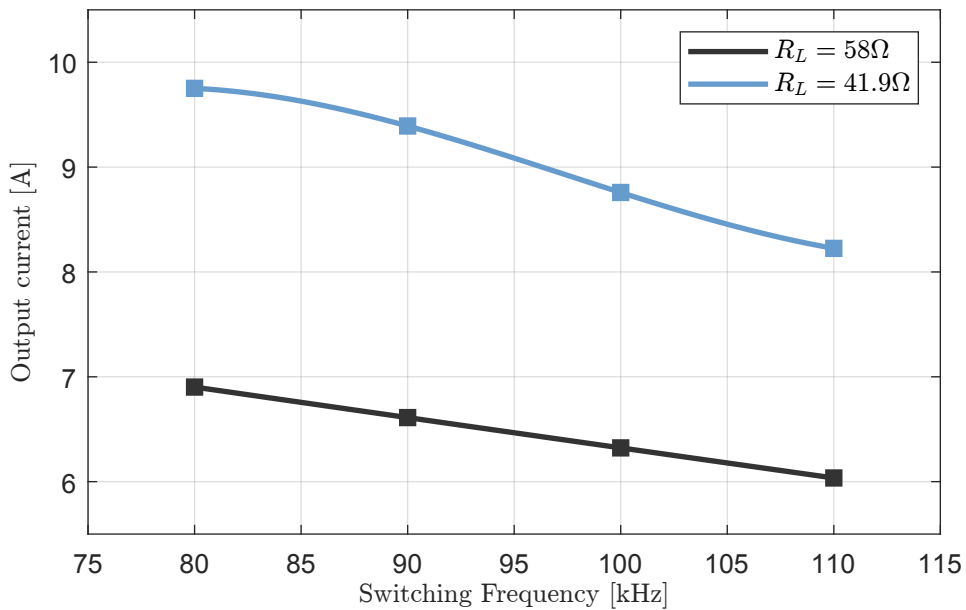
Figure 5.19 − Output current vs. switching frequency for different load resistances.

In general, for higher load resistances, the CLLLC resonant converter is more prone to exhibiting voltage gain in the system. Conversely, for lower load resistances, the converter is more susceptible to reductions in the output voltage. It is important to note that as the switching frequency increases, the power processed by the converter decreases.

5.4 SR

This subsection aims to validate the operation using SR at nominal power, which is 5 kW. For this purpose, command signals with the exact frequency of the resonant tank were sent to the switches. At this point, the converter operates with unity gain, meaning that the input voltage is equal to the output voltage. This is also where the converter exhibits its best efficiency because the resonance half-cycles are always completed. This can be observed in Figure 5.20 and Figure 5.21, where both primary and secondary currents are purely sinusoidal.

Figure 5.22 presents a comparison of the efficiency of the CLLLC resonant converter operating with and without SR. In Figure 5.22a (without SR), the converter operation with the switching frequency equal to the resonance frequency achieves an efficiency of 95.544 %. However, it also exhibits a significant voltage drop at the output due to diode conduction, totaling approximately 9V. Conversely, in Figure 5.22b, under the same operating conditions, the converter achieves an efficiency of 97.621 % with a slightly different output voltage from the input voltage. In this case, the secondary full-bridge conducts through the mosfets drain-source channel.
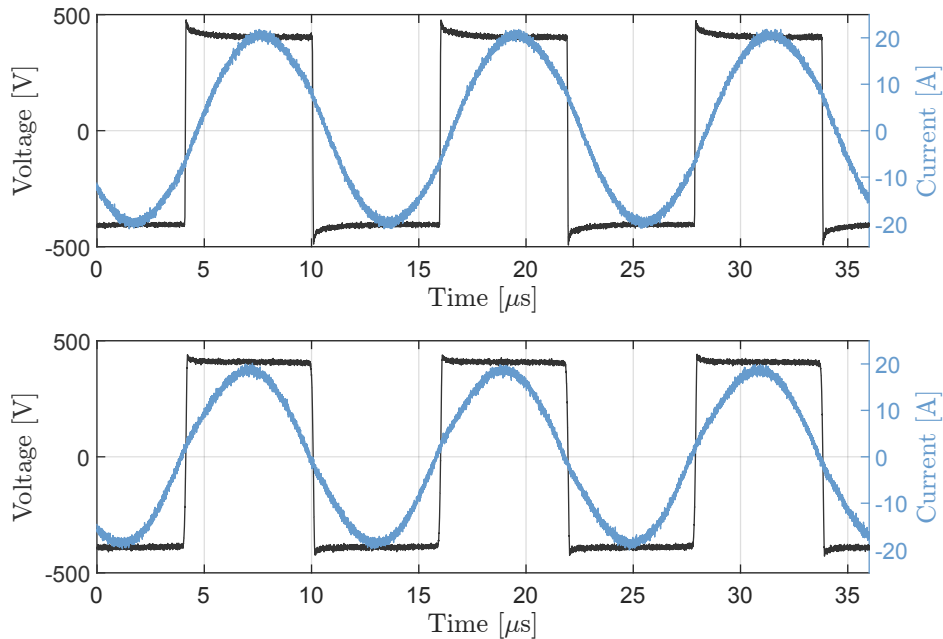
Figure 5.20 – Currents and voltages in the resonant tank for $f_{sw} = f_{res}$, $R_L = 31.9\,\Omega$ and without SR.

5.4.1 Implementation of the SR strategy

To implement the SR strategy on the secondary side of the converter, the current sensor ACS733KLATR-40AB-T from Allegro MicroSystems was used due to its bandwidth of 1 MHz. The output signal from the sensor is compared to generate the control pulses for driving the mosfets of the secondary bridge.
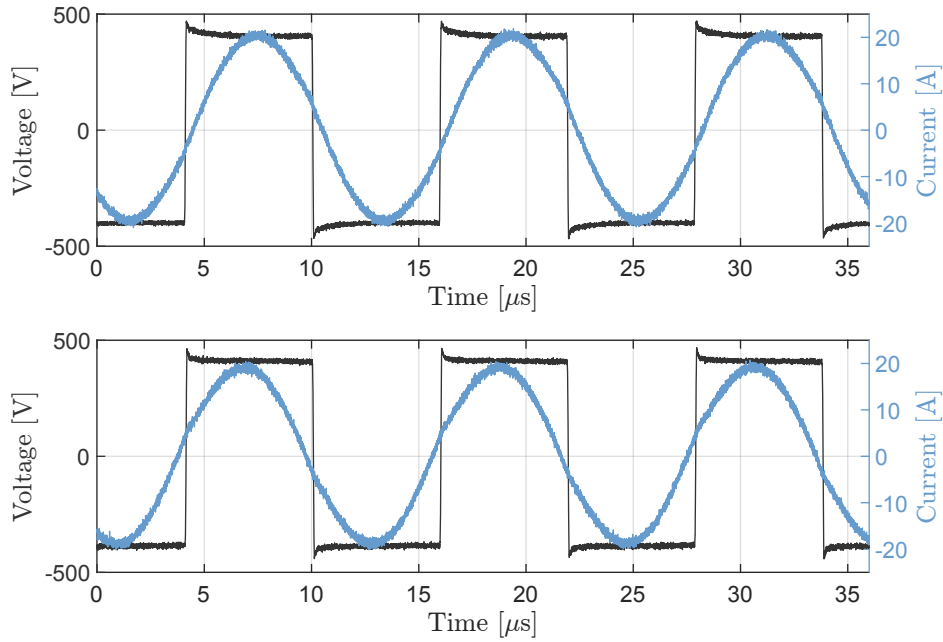
Figure 5.21 – Currents and voltages in the resonant tank for $f_{sw} = f_{res}$, $R_L = 31.9\,\Omega$ and with SR.
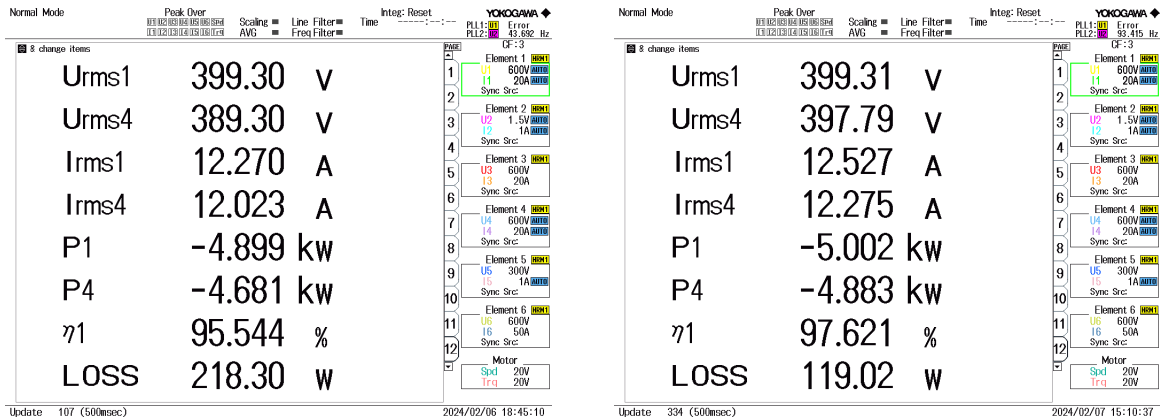
(a) Efficiency without SR.

(b) Efficiency with SR.

Figure 5.22 – Efficiencies for without SR and with SR.

Although the sensor bandwidth is approximately 10 times higher than the switching frequency, the SR strategy encountered some issues due to a delay of 374 ns in the system caused by the current sensor. This delay shifts the converter away from its operating point, resulting in differences in its operation when it conducts through the diodes instead. This issue occurs for switching frequencies lower than the resonance frequency. The study of implementing SR using a current sensor in the tank is still ongoing, as the conclusions drawn are not definitive.

Alternative methods for implementing SR include the approach presented in [53] by Infineon Technologies, where a current transformer is used to read the current from the resonant tank. A bridge rectifier is then employed, and its output signal is compared with a 0 V reference through an operational amplifier, generating pulses that are compared with those delivered to the primary full-bridge of the converter.

Another approach is described in [54], where a detection mechanism based on a Rogowski coil is used to detect the high-frequency current in the tank in an isolated manner. An operational amplifier is also used to compare the signal and generate the switching pulses for the secondary side switches.

5.5 RESULTS FOR EV CHARGING APPLICATION

The versatility of the CLLLC converter makes it an attractive choice for electric vehicle battery charging applications, particularly due to its capacity to provide a wide range of output voltages when properly designed.

To assess its suitability as a battery charger, a series of tests were conducted to evaluate its performance under varying voltage levels. The efficiency curve depicted in Figure 5.23 highlights optimal efficiency points near the resonance frequency (unity gain), with a noticeable decline in efficiency as the converter operates further away from this frequency. It is important to note that these results are based on experimental data, and that the SR was not utilized in this study.
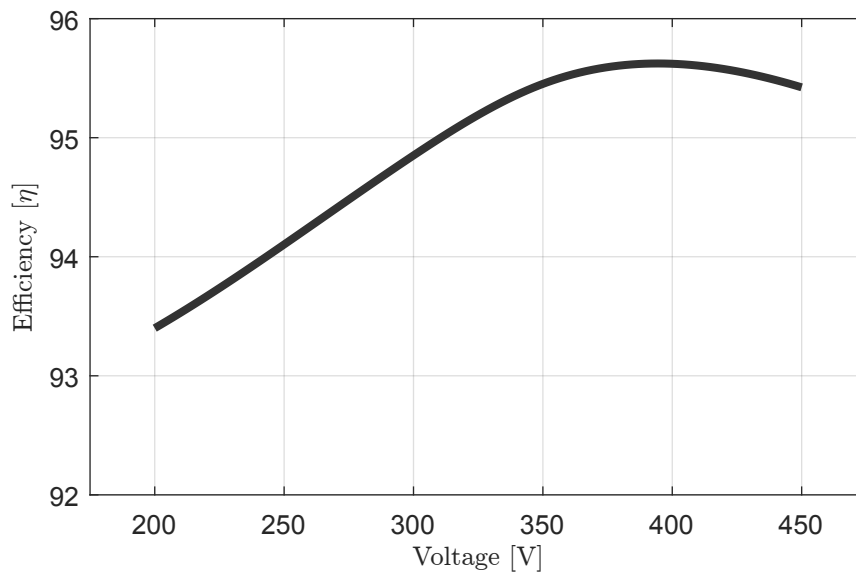
Figure 5.23 − Efficiency of the converter operating as an electric vehicle charger.

5.6 SUMMARY

This chapter is dedicated to the practical construction of the prototype and the presentation of the results obtained from the resonant CLLLC converter. Firstly, the electrical quantities of the parameters of the resonant tank constructed in practice are exposed. The developed prototype and the connection scheme used for practical tests are also presented, along with the equipment utilized.

Following this, the operation of the prototype was validated through tests conducted at different operating points and with varying output loads. It is noteworthy that electrical

quantities such as output voltage and current vary with different output loads at the same operating point. The converter exhibits greater susceptibility to output voltage variations with lower load resistance and less susceptibility with higher load resistances.

Subsequently, the operation of the converter at its nominal operating point and power is elaborated upon. The adopted SR strategy is outlined, along with commentary on the challenges and hurdles encountered during its implementation. Furthermore, alternative SR strategies are briefly explored.

A comparison is made between the efficiency results obtained from the optimization algorithm and those achieved in practical implementation, followed by a discussion of the findings. Finally, the performance curve of the converter as an electric vehicle charger, operating within the range of 200 to 450 V, is presented, along with its efficiency.

6

CONCLUSION

The CLLLC converter holds significant importance in power electronics, particularly in applications ranging from medium to high power. It emerges as a viable solution in various critical domains, including battery charging, electric vehicles, data centers, renewable energy, and other energy conversion technologies. This topology demonstrates versatility due to its diverse operational points and holds promise in addressing sustainability and energy efficiency challenges.

Chapter 2 introduces the CLLLC resonant converter, highlighting its operation in capacitive and inductive regions without respective output or input losses. It analyzes the resonant tank impedance, deriving an equation dependent on component values and load resistance. The discussion extends to the maximum inductance for ZVS in the primary and modulation strategies that enhance frequency modulation and SR to minimize losses. Additionally, it outlines three operating regions within the inductive region, concluding with waveform illustrations and analysis. Overall, the chapter provides a thorough examination of CLLLC converter operation and performance considerations.

Chapter 3 introduces DP as a fundamental concept for modeling the CLLLC resonant converter, due to the sinusoidal behavior of currents and voltages within the resonant tank. Unlike traditional approaches such as circuit averaging, DP accommodates sinusoidal behavior effectively. The transformation matrix for DP models is derived, simplifying the process of finding time-domain derivatives. Subsequently, the CLLLC converter model is developed, comprising the ac part (resonant tank modeled by DP) and the dc part (output filter). Integration and validation of both parts yield the complete converter model. Finally, a dynamic model expressed in transfer functions is derived, enabling analysis of the converter behavior under diverse operating conditions and load scenarios, and facilitating the design of effective control strategies for desired performance objectives.

Chapter 4 focuses on the design of the CLLLC resonant converter, starting with a review of common design methodologies. A detailed loss model is developed to accurately calculate all global losses of the converter, along with equations for resonant tank param-

eters. An optimization algorithm based on PSO is utilized to design the converter for maximum efficiency using available materials. Results of the optimized design, including physical and electrical parameters, are presented alongside an efficiency vector. A comparison between traditional and optimized design methods underscores the importance of optimization for this converter type.

Chapter 5 delves into the practical construction of a prototype CLLLC resonant converter, presenting the electrical parameters of the resonant tank and details of the prototype development and connection scheme for testing, including the equipment used. Validation tests at various operating points and output loads highlight variations in electrical quantities such as output voltage and current, notably showing higher susceptibility to voltage variations with lower load resistance. Operation at nominal power and point is discussed, emphasizing the SR strategy and the challenges encountered, with a brief exploration of alternative strategies. A comparison of efficiency results from optimization and practical implementation is conducted, followed by a discussion. Finally, the converter performance curve as an electric vehicle charger, ranging from 200 to 450 V, is presented alongside efficiency performance.

6.1   FUTURE WORKS

The following themes are proposed for future work:

- Analysis of the converter with Phase-Frequency modulation.

- Development of a methodology for SR of the secondary circuitry employing a sensorless technique.

- Integration of the resonant inductor and transformer into a unified magnetic structure to achieve further reduction in converter size.

- Comparison of the CLLLC resonant converter with other resonant converters by listing the advantages and disadvantages of each topology.

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[52] H. Visairo, M. A. Medina, and J. M. Ramirez, "Use of evolutionary algorithms for design optimization of power converters," in *CONIELECOMP 2012, 22nd International Conference on Electrical Communications and Computers*, pp. 268–272, 2012.

[53] *1 kW bi-directional CLLC DC-DC converter with 1200 V and 1700 V CoolSiC™ MOSFETs.* Infineon Technologies.

[54] *Bidirectional CLLLC Resonant Dual Active Bridge (DAB) Reference Design for HEV/EV Onboard Charger.* Texas Instruments.

APPENDIX

A STATE SPACE MODEL

A.1 REPRESENTATION OF STATE-SPACE SYSTEMS

The concept of a dynamic system state involves a core set of variables, known as state variables, which fully describe the system and its response to any given inputs.

Linear Time-Invariant state-space models offer a linear representation of a dynamic system in either discrete or continuous time. Converting a model into state-space form is fundamental to many techniques in process dynamics and control analysis. The continuous-time representation is shown below

$$\begin{cases} \dot{x} & = Ax + Bu \\ y & = Cx + Du \end{cases}, \tag{A.1}$$

where:

- $x \in \mathbb{R}^n$ and $\dot{x} = \frac{dx}{dt} \in \mathbb{R}^n$ are the state vector and its derivatives. The notation $\in \mathbb{R}^n$ means that x and $\dot{x}$ are real-numbered vectors of length n.

- $y \in \mathbb{R}^p$ is the output vector.

- $u \in \mathbb{R}^m$ is the input vector.

- $A \in \mathbb{R}^{n \times n}$ is the state transition matrix.

- $B \in \mathbb{R}^{n \times m}$ is the input matrix.

- $C \in \mathbb{R}^{p \times n}$ is the output matrix.

- $D \in \mathbb{R}^{p \times m}$ is the feedforward matrix. Typically, D is zeros because the inputs do not typically affect the outputs directly.

A.1.1 Steady-state model

In dynamic systems, a steady-state refers to a condition where the system's state variables remain constant over time. This means the system has reached equilibrium and

its behavior no longer changes. This state is significant as it represents a stable operating condition or equilibrium point for the system.

For Linear Time-Invariant systems described by state-space models, the steady-state condition is achieved when the derivatives of the state variables are zero. In other words, at steady-state

$$\dot{x} = 0. \tag{A.2}$$

When $\dot{x} = 0$, the equilibrium points are easily calculated using Equation A.1.

A.1.2 Linearization model

In the context of linearizing state-space models, the Jacobian matrix is essential for approximating the behavior of a nonlinear dynamic system around an operating point. State-space models typically describe system dynamics through differential equations, which are often nonlinear. However, linearization around an operating point simplifies the analysis and design of control systems.

The Jacobian matrix captures the sensitivity of the system's dynamics to small changes in the state variables around the operating point, providing a linear approximation of the nonlinear system dynamics.

Consider a nonlinear state-space model represented as follows,

$$\begin{cases} \dot{x} &= f(x, u) \\ y &= h(x, u) \end{cases} \tag{A.3}$$

where:

- x is the state vector of the system.

- u is the input vector.

- $\dot{x}$ represents the derivative of the state vector x with respect to time.

- y is the output vector.

- $f(x, u)$ represents the nonlinear dynamics of the system.

- $h(x, u)$ represents the nonlinear output equation.

Linearization around an operating point $(\bar{x}, \bar{u})$ entails calculating the Jacobian matrices of the nonlinear functions $f(x, u)$ and $h(x, u)$ evaluated at that operating point.

$$
\begin{cases}
\dfrac{\mathrm{d}}{\mathrm{d}t}\hat{x}(t) &= A_j\hat{x}(t) + B_j\hat{u}(t) \\[2mm]
\hat{y}(t) &= C_j\hat{x}(t) + D_j\hat{u}(t)
\end{cases},
\tag{A.4}
$$

where $\hat{x}(t)$ and $\hat{u}(t)$ represent the state and input variables, respectively. A_j and B_j denote the Jacobian matrices associated with the nonlinear equations concerning the states and inputs, respectively. C_j is the output matrix, and D_j is the direct transmission matrix.

To calculate the coefficients A_j and B_j according to the equations below

$$
a_{ij} = \left.\frac{\partial f\left(x(t), u(t)\right)_i}{\partial x_j(t)}\right|_{x_{ss}, u_{ss}},
\tag{A.5}
$$

$$
b_{ij} = \left.\frac{\partial f\left(x(t), u(t)\right)_i}{\partial u_j(t)}\right|_{x_{ss}, u_{ss}}.
\tag{A.6}
$$

The coefficients are contingent upon the steady state values of both the states and the inputs. Consequently, it is imperative to solve the set of equations governing the power converter model, accounting for the fact that derivatives are null, given that in steady state, variables converge to their equilibrium points.

Through the linearized state space system, one can derive the transfer functions of interest in the Laplace domain using the operation described in Equation A.7.

$$
G_{ij}(s) = C_j(sI - A_j)^{-1}B_j + D_j.
\tag{A.7}
$$

In summary, the Jacobian matrix for linearizing state-space models offers a linear approximation of the system dynamics around an operating point, which is beneficial for analysis and control design purposes.

APPENDIX

B ⬛ Magnetic tests

Determining the inductance of the primary and secondary side inductors of the resonant tank and transformer, tests were conducted using the Agilent 4294A impedance analyzer.

B.1 INDUCTORS

For the inductors, it is very simple to obtain their inductance. It only requires measuring the series inductance on the impedance analyzer. Figure B.1 shows the series inductance of the primary inductor as a function of frequency.
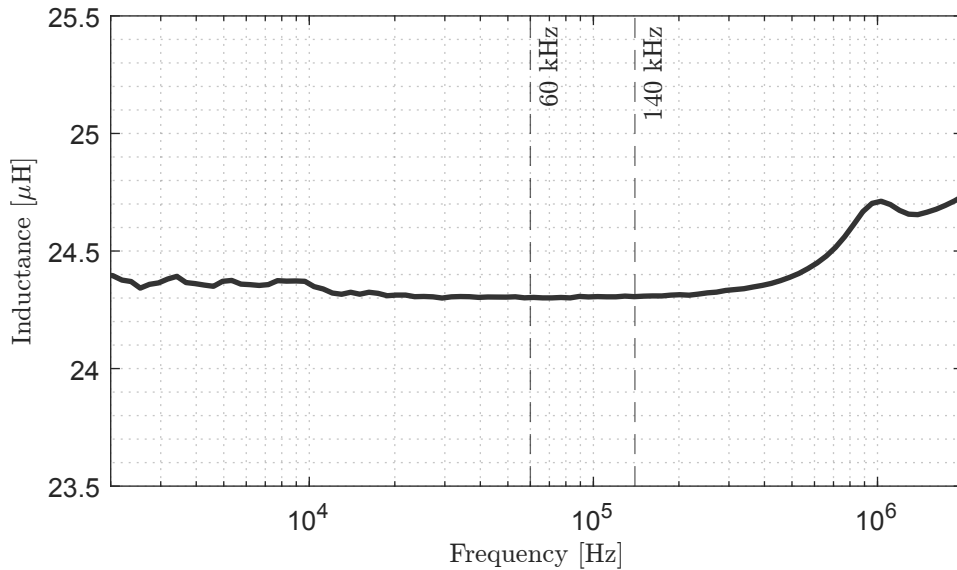

Figure B.1 – Primary Inductance test.

Figure B.2 shows the series inductance of the secondary inductor as a function of frequency.
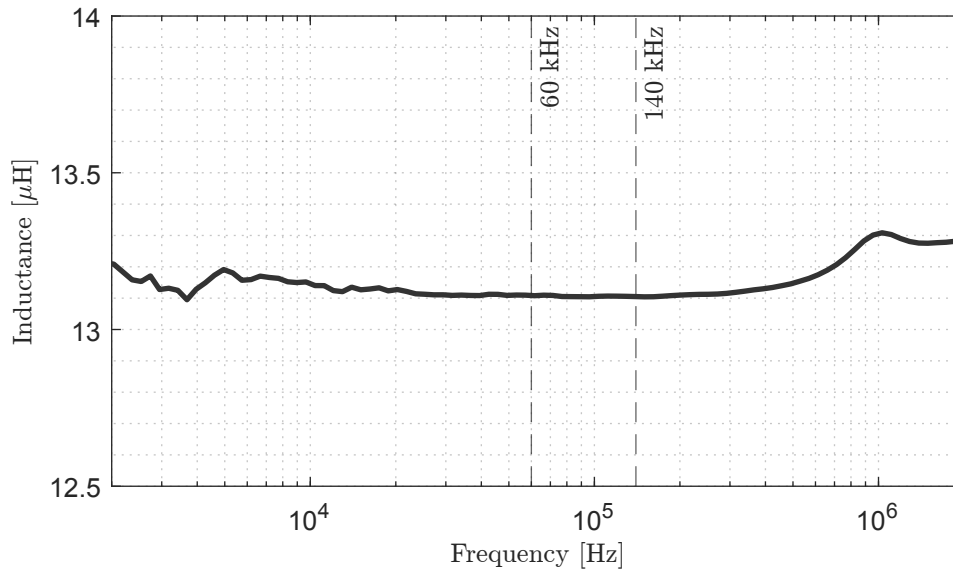
Figure B.2 – Secondary Inductance test.

B.2 TRANSFORMER

To obtain the leakage inductances and the magnetizing inductance of the transformer, three tests must be performed. Firstly, the total primary inductance (L_{T1}) must be measured, i.e., the measurement is performed on the primary with the secondary in open circuit. After this, the total secondary inductance (L_{T2}) must be measured, i.e., the measurement is performed on the secondary with the primary in open circuit. Finally, the inductance seen by the primary with the secondary in short circuit (L_x) must be measured.

Figures B.3, B.4 and B.5 represents L_{T1}, L_{T2} and L_x, respectively.
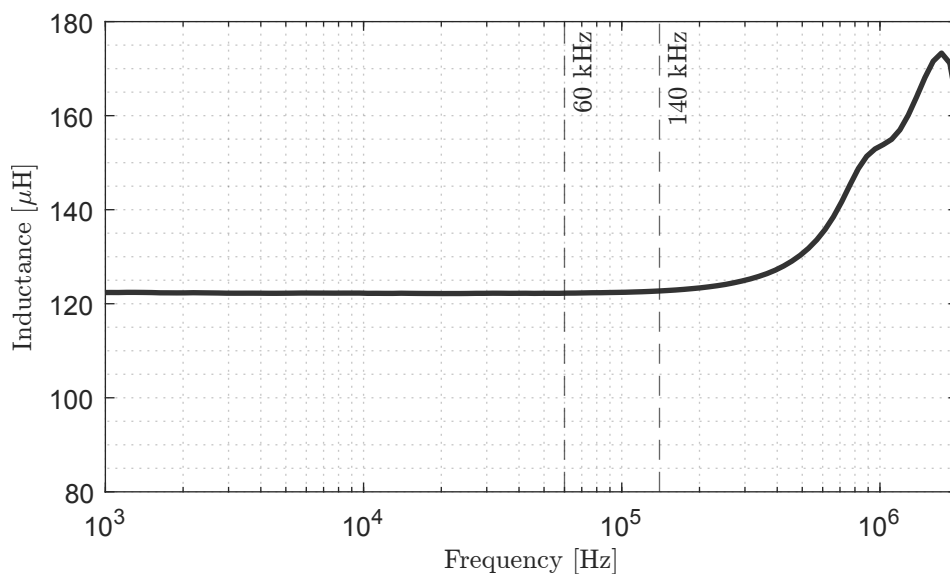

Figure B.3 – Open circuit test on the primary side transformer.

With the three measurements performed, we can use a set of equations (B.1) to determine the transformer's magnetizing inductance and the primary and secondary
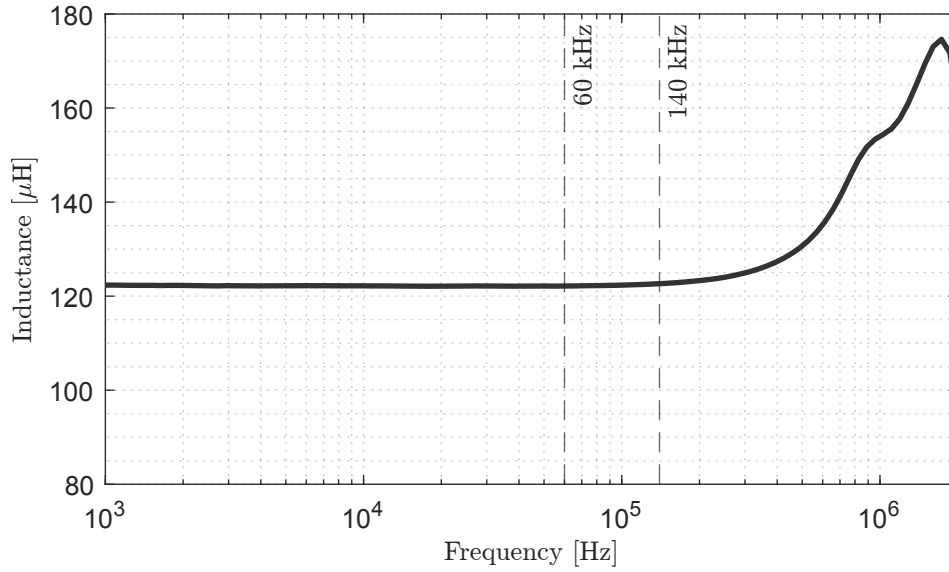
Figure B.4 – Open circuit test on the secondary side transformer.
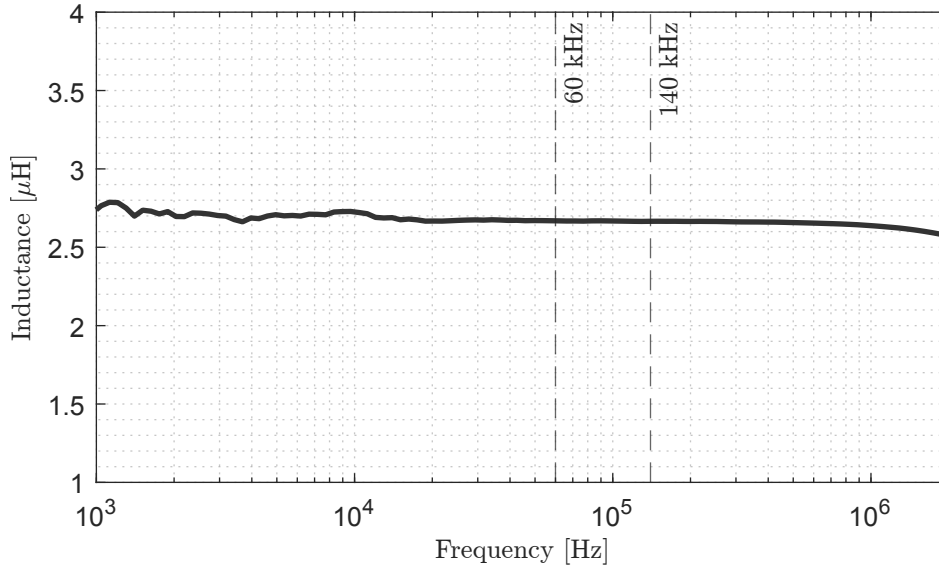

Figure B.5 – Short circuit test on the primary side transformer.

leakage inductances. Remember that these equations describe the inductance observed in each of the measurements.

$$
\begin{cases}
L_{T1} = L_{tr1} + L_m, \\
L_{T2} = L_{tr2} + \dfrac{L_m}{n^2}, \\
L_x = L_{tr1} + \dfrac{L_m \, n^2 L_{tr2}}{L_m + n^2 L_{tr2}}.
\end{cases}
\tag{B.1}
$$

To determine the primary and secondary leakage inductances (L_{tr1} and L_{tr2}) and the transformer's magnetizing inductance (L_m), a MATLAB solve is performed, isolating these variables. The results are presented by Equation B.2.
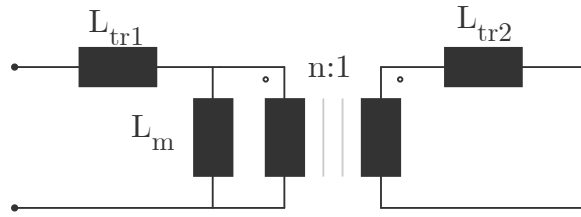
(a) Transformer measurement in open circuit.
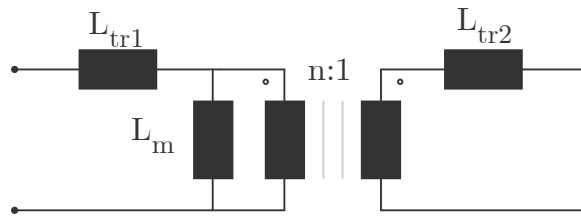
(b) Transformer measurement in short circuit.
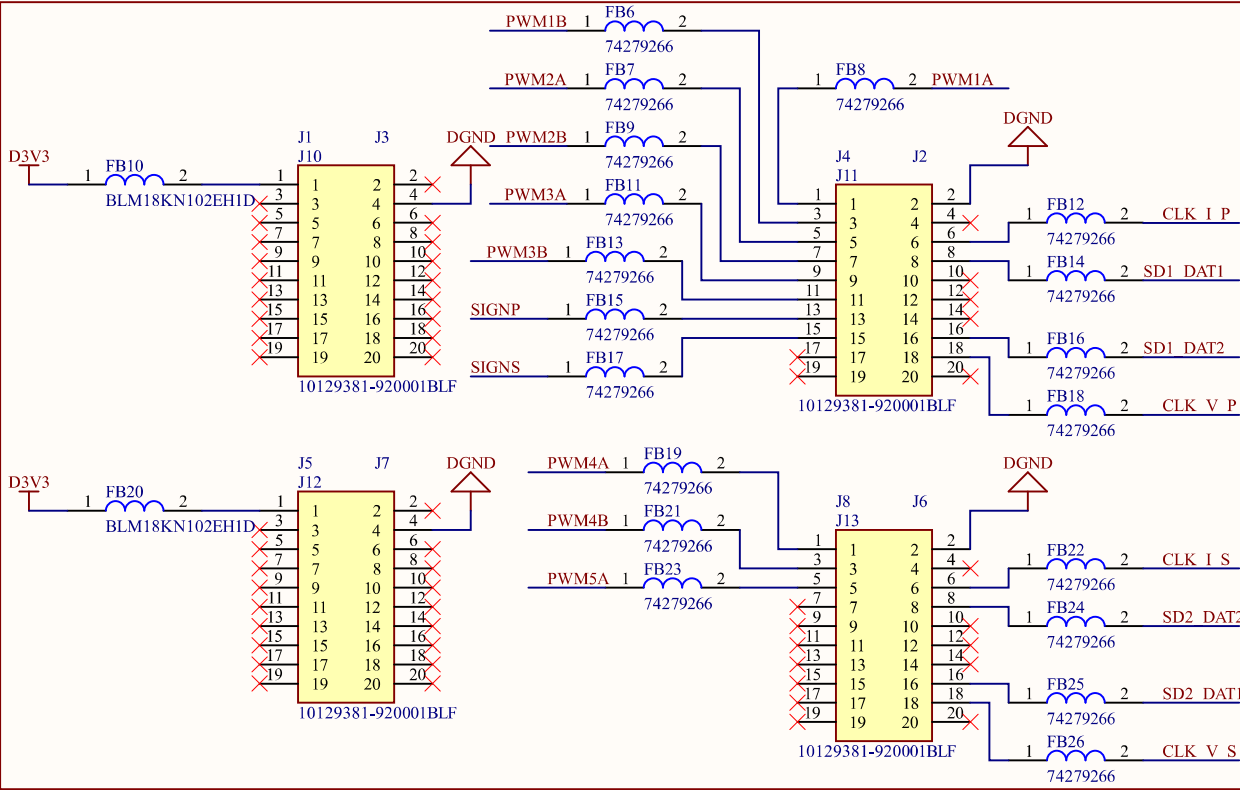
Figure B.6 − Transformer measurements.

$$\begin{cases} L_{tr1} = 1.332\,\mu\text{H}, \\ L_{tr2} = 1.331\,\mu\text{H}, \\ L_{m} = 121.067\,\mu\text{H}. \end{cases} \tag{B.2}$$

APPENDIX

C

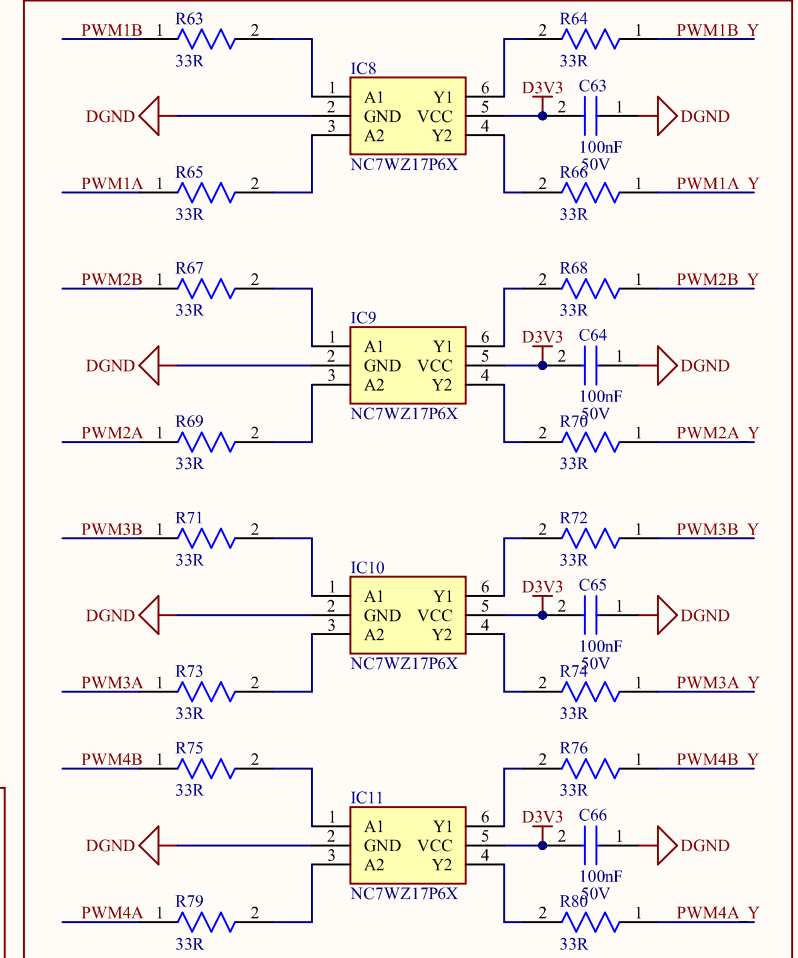# CLLLC RESONANT CONVERTER PROTOTYPE

This appendix provides a detailed description of the design features of the prototype converter, which was constructed to obtain the experimental results presented in this work.

The schematics for the CLLLC resonant converter project are shown on the last pages. These include the primary and secondary components, the DSP command board, and the measurement components for current and voltage, which are intended for further studies in future work. Following the schematics, the PCB layout of the converter is presented, displaying the top layer to the bottom layer.
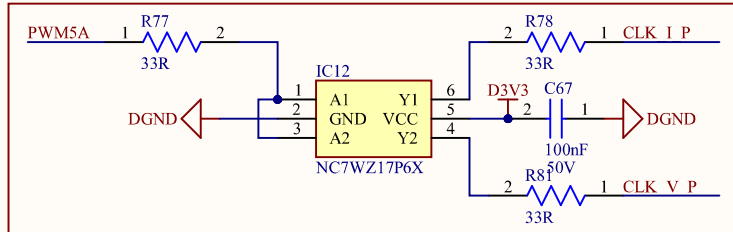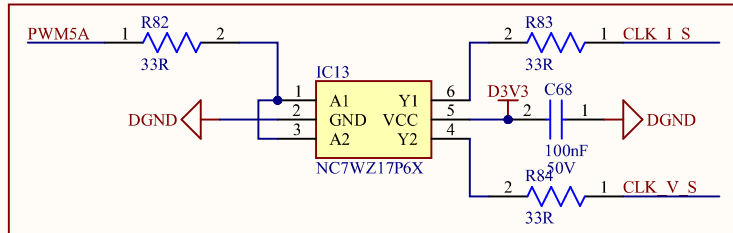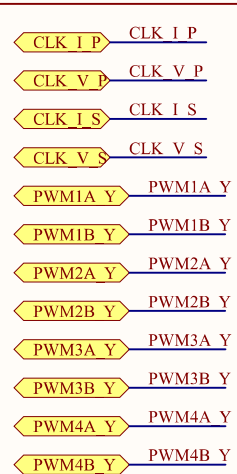
LAUNCHPAD TEXAS F28379D

PWM1B — FB6 — 74279266
PWM2A — FB7 — 74279266
PWM1A — FB8 — 74279266
PWM2B — FB9 — 74279266 — DGND
PWM3A — FB11 — 74279266
PWM3B — FB13 — 74279266
SIGNP — FB15 — 74279266
SIGNS — FB17 — 74279266

D3V3 — FB10 — BLM18KN102EH1D

J1 / J3 / J10 — 10129381-920001BLF

J4 / J2 / J11 — 10129381-920001BLF

DGND

FB12 — 74279266 — CLK_I_P
FB14 — 74279266 — SD1_DAT1
FB16 — 74279266 — SD1_DAT2
FB18 — 74279266 — CLK_V_P

D3V3 — FB20 — BLM18KN102EH1D

J5 / J7 / J12 — 10129381-920001BLF — DGND

PWM4A — FB19 — 74279266
PWM4B — FB21 — 74279266
PWM5A — FB23 — 74279266

J8 / J6 / J13 — 10129381-920001BLF

DGND

FB22 — 74279266 — CLK_I_S
FB24 — 74279266 — SD2_DAT2
FB25 — 74279266 — SD2_DAT1
FB26 — 74279266 — CLK_V_S

BUFFER PWMS

PWM1B — R63 33R
DGND
PWM1A — R65 33R
IC8 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
D3V3 — C63 100nF 50V — DGND
R64 33R — PWM1B_Y
R66 33R — PWM1A_Y

PWM2B — R67 33R
DGND
PWM2A — R69 33R
IC9 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
D3V3 — C64 100nF 50V — DGND
R68 33R — PWM2B_Y
R70 33R — PWM2A_Y

PWM3B — R71 33R
DGND
PWM3A — R73 33R
IC10 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
D3V3 — C65 100nF 50V — DGND
R72 33R — PWM3B_Y
R74 33R — PWM3A_Y

PWM4B — R75 33R
DGND
PWM4A — R79 33R
IC11 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
D3V3 — C66 100nF 50V — DGND
R76 33R — PWM4B_Y
R80 33R — PWM4A_Y

BUFFER CLOCK PRIMARY

PWM5A — R77 33R
IC12 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
DGND
R78 33R — CLK_I_P
D3V3 — C67 100nF 50V — DGND
R81 33R — CLK_V_P

BUFFER CLOCK SECONDARY

PWM5A — R82 33R
IC13 — NC7WZ17P6X (A1, GND, A2 / Y1, VCC, Y2)
DGND
R83 33R — CLK_I_S
D3V3 — C68 100nF 50V — DGND
R84 33R — CLK_V_S

OUTPUTS

CLK_I_P — CLK_I_P
CLK_V_P — CLK_V_P
CLK_I_S — CLK_I_S
CLK_V_S — CLK_V_S
PWM1A_Y — PWM1A_Y
PWM1B_Y — PWM1B_Y
PWM2A_Y — PWM2A_Y
PWM2B_Y — PWM2B_Y
PWM3A_Y — PWM3A_Y
PWM3B_Y — PWM3B_Y
PWM4A_Y — PWM4A_Y
PWM4B_Y — PWM4B_Y

INPUTS/OUTPUTS

SD1_DAT1 — SD1_DAT1
SD1_DAT2 — SD1_DAT2
SD2_DAT1 — SD2_DAT1
SD2_DAT2 — SD2_DAT2
SIGNP — SIGNP
SIGNS — SIGNS

INPUT FILTER

ACSP — FB4 — R55 10R — VIN1+
BLM18KN102EH1D
C58 500pF
R56 10R — VIN1−
DGND
DGND

ACSS — FB5 — R57 10R — VIN2+
BLM18KN102EH1D
C60 500pF
R60 10R — VIN2−
DGND

RESONANT TANK CURRENT MEASUREMENTS
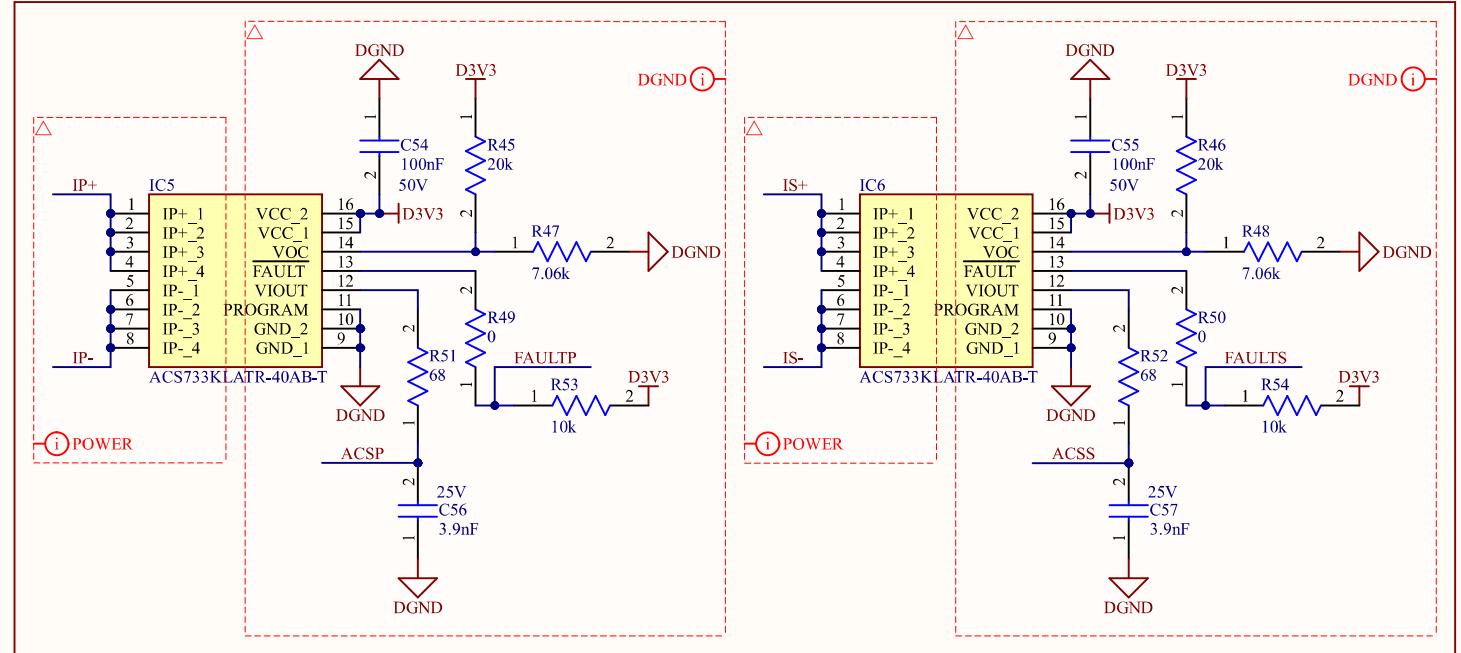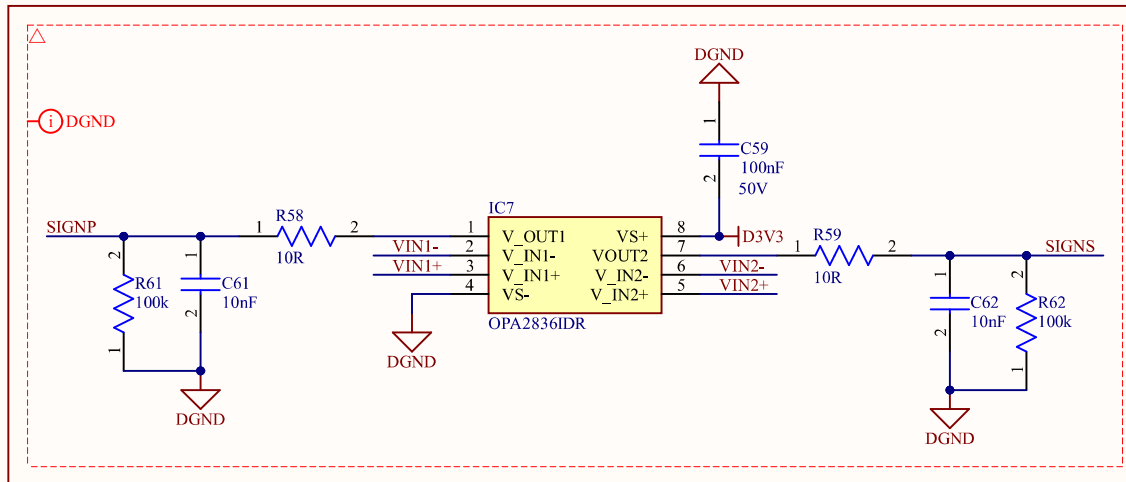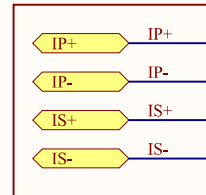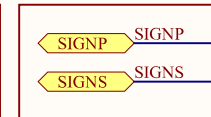
DGND
D3V3
C54 100nF 50V
R45 20k
DGND

IC5
IP+ — 1 IP+_1   VCC_2 16 — D3V3
2 IP+_2   VCC_1 15
3 IP+_3   VOC 14 — R47 7.06k — DGND
4 IP+_4   FAULT 13
5 IP−_1   VIOUT 12
6 IP−_2   PROGRAM 11
7 IP−_3   GND_2 10
IP− — 8 IP−_4   GND_1 9
ACS733KLATR-40AB-T

R49 0
R51 68
FAULTP
R53 10k — D3V3
DGND
ACSP
25V C56 3.9nF
DGND

POWER

DGND
D3V3
C55 100nF 50V
R46 20k
DGND

IC6
IS+ — 1 IP+_1   VCC_2 16 — D3V3
2 IP+_2   VCC_1 15
3 IP+_3   VOC 14 — R48 7.06k — DGND
4 IP+_4   FAULT 13
5 IP−_1   VIOUT 12
6 IP−_2   PROGRAM 11
7 IP−_3   GND_2 10
IS− — 8 IP−_4   GND_1 9
ACS733KLATR-40AB-T

R50 0
R52 68
FAULTS
R54 10k — D3V3
DGND
ACSS
25V C57 3.9nF
DGND

POWER

AMPOP 2836

DGND

SIGNP
R58 10R
R61 100k C61 10nF
DGND
DGND

DGND
C59 100nF 50V
D3V3

IC7
V_OUT1   VS+ 8
V_IN1−   VOUT2 7 — VIN1−
V_IN1+   V_IN2− 6 — VIN1+
VS−   V_IN2+ 5 — VIN2−
OPA2836IDR   VIN2+
DGND

R59 10R — SIGNS
C62 10nF R62 100k
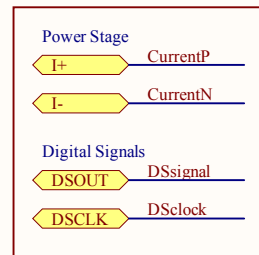DGND

INPUTS
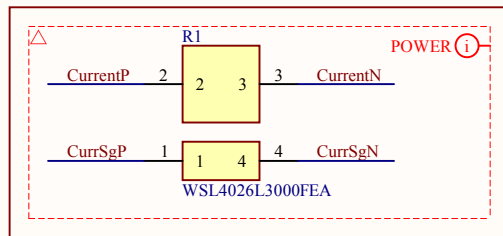IP+ — IP+
IP− — IP−
IS+ — IS+
IS− — IS−

OUTPUTS
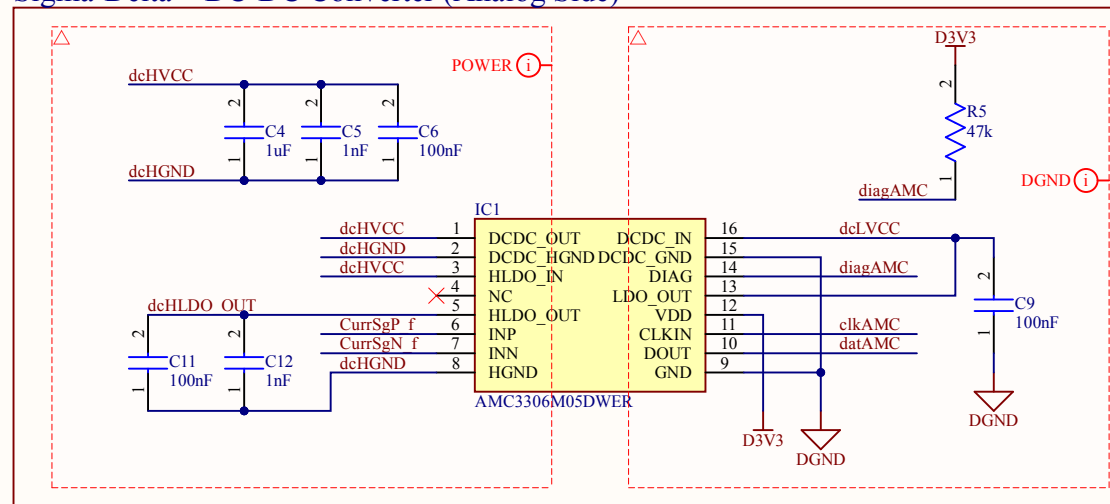SIGNP — SIGNP
SIGNS — SIGNS

Current Measurement (Shunt) - Input/Output

Ports
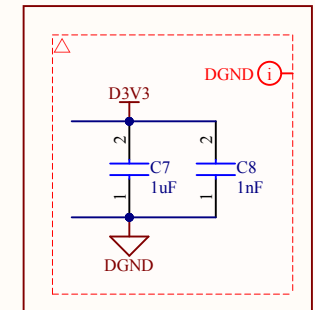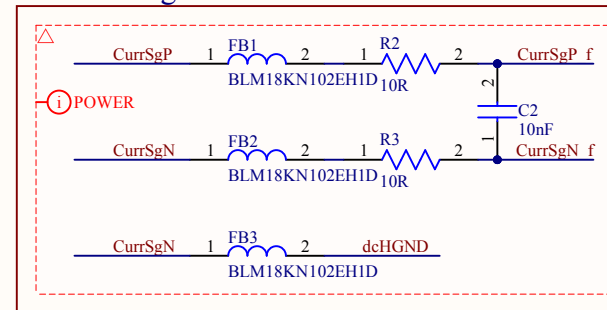
Power Stage
- I+ — CurrentP
- I- — CurrentN

Digital Signals
- DSOUT — DSsignal
- DSCLK — DSclock

Shunt Resistor

R1

CurrentP	2	2 ... 3	3 CurrentN
CurrSgP	1	1 ... 4	4 CurrSgN

WSL4026L3000FEA

POWER (i)

Shunt Voltage Filter

POWER (i)

CurrSgP — FB1 — R2 (10R) — CurrSgP_f
BLM18KN102EH1D

CurrSgN — FB2 — R3 (10R) — CurrSgN_f
BLM18KN102EH1D

C2 10nF

CurrSgN — FB3 — dcHGND
BLM18KN102EH1D

DGND (i)

D3V3

C7 1uF   C8 1nF

DGND

Sigma-Delta + DC-DC Converter (Analog Side)

POWER (i)

dcHVCC
C4 1uF   C5 1nF   C6 100nF
dcHGND

dcHLDO_OUT
C11 100nF   C12 1nF

IC1 — AMC3306M05DWER

Pin	Name	Name	Pin	Net
1	DCDC_OUT	DCDC_IN	16	dcLVCC
2	DCDC_HGND	DCDC_GND	15	
3	HLDO_IN	DIAG	14	diagAMC
4	NC	LDO_OUT	13	
5	HLDO_OUT	VDD	12	
6	INP	CLKIN	11	clkAMC
7	INN	DOUT	10	datAMC
8	HGND	GND	9	

CurrSgP_f → 6
CurrSgN_f → 7
dcHGND → 8

D3V3   DGND

D3V3
R5 47k
diagAMC
DGND (i)

C9 100nF
DGND

Digitals Signals Filter

clkAMC — R4 (50R) — DSclock
C3 3p3F
DGND

DGND (i)

datAMC — R6 (50R) — DSsignal
C10 3p3F
DGND
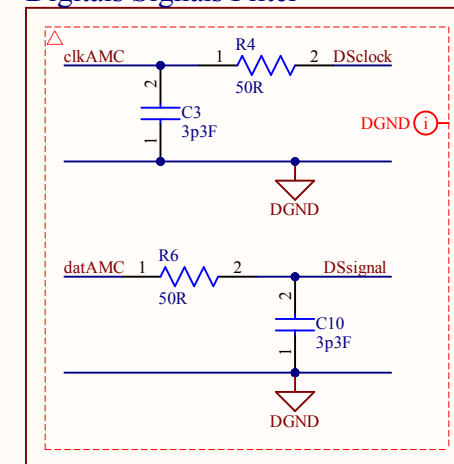
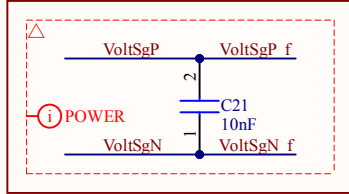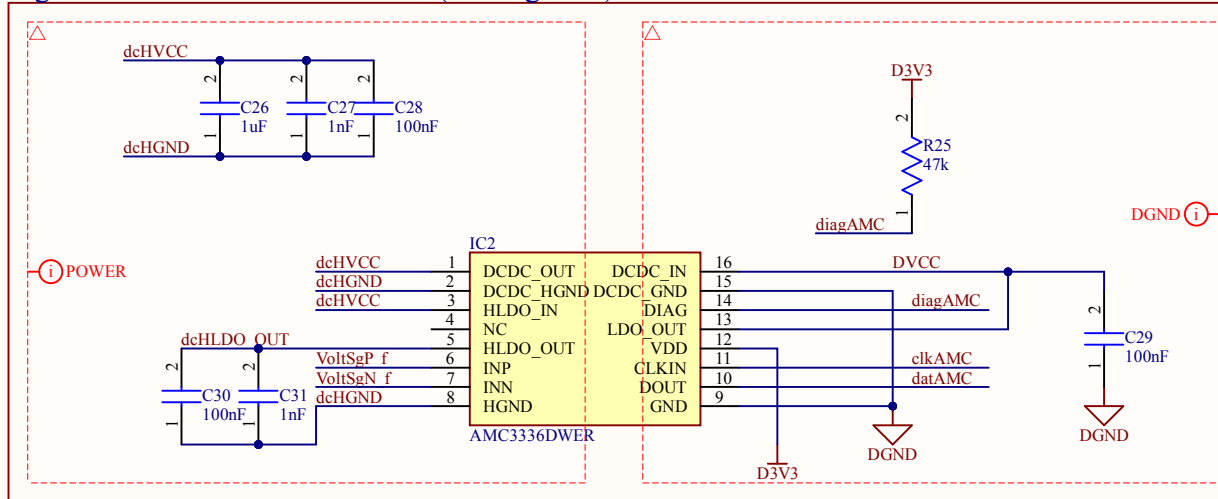# Voltage Measurement Input/Output

Power Stage

V+	VoltSgP
V-	VoltSgN
HGND	dcHGND

Digital Signals

DSOUT	DSsignal
DSCLK	DSclock

Voltage Filter

VoltSgP — VoltSgP_f
POWER
C21
10nF
VoltSgN — VoltSgN_f

Digitals Signals Filter

clkAMC — R23 50R — DSclock
C22 3p3F
DGND
DGND

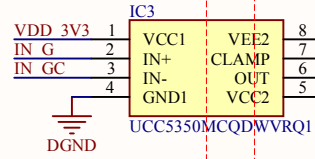datAMC — R24 50R — DSsignal
C25 3p3F
DGND

D3V3 — DGND
C23 1uF — C24 1nF
DGND

Sigma-Delta + DC-DC Converter (Analog Side)

dcHVCC
C26 1uF | C27 1nF | C28 100nF
dcHGND

POWER

dcHLDO_OUT
C30 100nF | C31 1nF
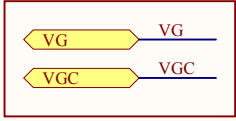
IC2 — AMC3336DWER

Pin	Name		Name	Pin
1	dcHVCC / DCDC_OUT		DCDC_IN	16
2	dcHGND / DCDC_HGND		DCDC_GND	15
3	dcHVCC / HLDO_IN		DIAG	14
4	NC		LDO_OUT	13
5	dcHLDO_OUT / HLDO_OUT		VDD	12
6	VoltSgP_f / INP		CLKIN	11
7	VoltSgN_f / INN		DOUT	10
8	dcHGND / HGND		GND	9

D3V3 — R25 47k — diagAMC — DGND

DVCC
diagAMC
clkAMC
datAMC
C29 100nF
DGND

D3V3
DGND

GATE DRIVER - UCC 5350

D3V3

VDD_3V3

C36 1uF 50V
C37 0.1uF 10V

DGND   DGND

DGND (i)

PGATE (i)

+15V_A

D1 CMS06(TE12L,Q,M)

10R / 0.25W
R34

D2 CMS06(TE12L,Q,M)

GATE

IC3

VDD_3V3	1	VCC1	VEE2	8	-4V_1A
IN_G	2	IN+	CLAMP	7	
IN_GC	3	IN-	OUT	6	
	4	GND1	VCC2	5	+15V_A

UCC5350MCQDWVRQ1

DGND

R35
4R7 / 0.25W

R36 10K
C38 1nF 50V
R37 10K

GND_1A

D3 CMS06(TE12L,Q,M)

-4V_1A

C39 10nF 50V

GND_1A

F
Source Gate Driver.SchDoc
+15V_1A → +15V_A
-4V_1A → -4V_1A
GND_1A → GND_1A

VG   R38 100   IN_G

C40 100pF 50V   R39 10K

DGND   DGND

+15V_A

C42 10uF
C41 1uF

GND_1A

C44 1uF

-4V_1A

VGC   R40 100   IN_GC

C43 100pF 50V   R41 10K

DGND   DGND

INPUTS

VG   VG
VGC   VGC

OUTPUTS

GATE   GATE
GND_1A   GND_1A

INPUTS/OUTPUTS

+15V_1A → +15V_1A
-4V_1A → -4V_1A
GND_1A → GND_1A

SOURCE GATE DRIVER

B1
+VIN +VOUT 7
0V 6
-VIN -VOUT 5
MGJ2D121505SC

+12

C47 0.1uF 50V

DGND

C45 0.1uF
C46 1uF
C50 0.1uF
C51 1uF

IC4
GND NR 4
IN OUT 5
EN
TPS72301QDBVRQ1

+15V_1A

R42 68k
R43 47k
GND_1A

R44 68k

-4V_1A

PGATE

C48 1uF
C49 0.1uF
GND_1A
C52 1uF
C53 0.1uF

+15V_1A

-4V_1A

DGND

CLLLC Primary

INPUTS

VIN+	VIN+
VIN-	VIN-
PWMAp	PWMAp
PWMAn	PWMAn
PWMBp	PWMBp
PWMBn	PWMBn

OUTPUTS

VA	VA
VB	VB
VIN_M+	VIN_Meas_p
VIN_M-	VIN_Meas_n

Voltage divider - Primary

VIN+

R16 330k   R17 330k   R18 330k

R19 330k   R20 330k   R21 330k

VIN_Meas_p

VIN_Meas_p   R22 2.49k   VIN_Meas_n

PGND

Input Filter + Full-Bridge

VIN+

C13 10uF 1100V

C16 10uF 1100V

R13 3 2W

R7 1M   R8 1M
R9 1M   R10 1M

C14 470uF 450V   C15 470uF 450V

Cap Eletrolítico

R11 1M   R12 1M

C19 470uF 450V   C20 470uF 450V

R14 1M   R15 1M

RES SMD 2010 3/4W

C17 0.25uF 900V   C18 0.25uF 900V

Cap Ceralink

Q1 D S_2 S1 / S_1 G G1   C3M0030090K

VA

Q3 D S_2 S2 / S_1 G G2   C3M0030090K

Q2 D S_2 S3 / S_1 G G3   C3M0030090K

VB

Q4 D S_2 S4 / S_1 G G4   C3M0030090K

VIN-

PGND

Gate Drivers

D1 Gate Driver A.SchDoc
PWMAp — VG GND_1A — S1
PWMAn — VGC GATE — G1

D2 Gate Driver A.SchDoc
PWMAn — VG GND_1A — S2
PWMAp — VGC GATE — G2

D3 Gate Driver A.SchDoc
PWMBp — VG GND_1A — S3
PWMBn — VGC GATE — G3

D4 Gate Driver A.SchDoc
PWMBn — VG GND_1A — S4
PWMBp — VGC GATE — G4

CLLLC Secondary

INPUTS

- VC — VC
- VD — VD
- PWMCp — PWMCp
- PWMCn — PWMCn
- PWMDp — PWMDp
- PWMDn — PWMDn

OUTPUTS

- VOUT+ — VOUT+
- VOUT- — VOUT-
- V_MED — V_MED

FULL-BRIDGE

VCD

Q5 C3M0030090K
- 1 D S_2 3 — S5
- 2 S_1 G 4 — G5

Q6 C3M0030090K
- 1 D S_2 3 — S7
- 2 S_1 G 4 — G7

VC

VD

Q7 C3M0030090K
- 1 D S_2 3 — S6
- 2 S_1 G 4 — G6

Q8 C3M0030090K
- 1 D S_2 3 — S8
- 2 S_1 G 4 — G8

SGND

OUTPUT FILTER

VCD — VOUT+

- C34 0.25uF 900V
- C35 0.25uF 900V
- C32 30uF 1500V
- C33 30uF 1500V
- R33 3 2W

VOUT-

SGND

Voltage Divider - Secondary

VOUT+

- R26 330k
- R27 330k
- R28 330k
- R29 330k
- R30 330k
- R31 330k

V_MED

V_MED — 2 R32 2.49k 1 — SGND

Gate Drivers

D5 Gate Driver A.SchDoc
- PWMDp — VG GND_1A — S5
- PWMDn — VGC GATE — G5

D7 Gate Driver A.SchDoc
- PWMCp — VG GND_1A — S7
- PWMCn — VGC GATE — G7

D6 Gate Driver A.SchDoc
- PWMDn — VG GND_1A — S6
- PWMDp — VGC GATE — G6

D8 Gate Driver A.SchDoc
- PWMCn — VG GND_1A — S8
- PWMCp — VGC GATE — G8