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Reliability enhanced electrical power system for nanosatellites

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In memory of Vinicius Fernandes Figueiredo and Zita Luciano Figueiredo. You will be ever missed and eternally loved.

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“Trust in the LORD with all your heart;
and lean not to your own understanding.
In all your ways acknowledge him,
and He shall direct your paths."
Proverbs 3:5-6

RESUMO

A baixa confiabilidade dos subsistemas elétricos de potência (EPS) é um dos principais fatores responsáveis pelo alto número de falhas em missões de nanossatélites. Embora diversas técnicas de melhoria de confiabilidade tenham sido propostas no passado, a maior parte destes estudos não considera sua aplicabilidade, ignorando o custo, a energia e a área da placa requerida para que estas técnicas sejam implementadas. Em vista disto, o presente trabalho propõe uma arquitetura de EPS que incorpora quatro técnicas de melhoria de confiabilidade em um projeto de baixo custo e tamanho reduzido, a saber: seleção metódica de componentes de prateleira, projeto sem processador, redundância passiva parcial, e monitoramento e controle de cargas. Cada uma destas técnicas foi cuidadosamente selecionada para aprimorar a confiabilidade do EPS sem que outras áreas do projeto fossem comprometidas. Para melhor assegurar a viabilidade da arquitetura, três estratégias de projeto para redução de consumo energia foram também colocadas em prática. A mais importante delas é o uso de conversores de carga customizados, de alta eficiência e baseados em transistores de nitreto de gálio (GaN). Além disto, a arquitetura utiliza majoritariamente componentes de baixo consumo de energia e disponibiliza suporte para modos de operação de baixa dissipação, o que pode reduzir significativamente o desperdício de energia durante períodos de eclipse ou de inatividade. Toda a proposta foi fundamentada por diagramas de blocos, análises teóricas, equações de projeto e pelo esquema elétrico da placa de circuito impresso (PCB). A eficiência dos conversores de ponto de carga, o mecanismo de ativação das redundâncias passivas e todas as outras principais funcionalidades do EPS foram verificadas e validadas através de simulações de circuito SPICE. Ademais, um sistema de três métricas para avaliar e comparar a confiabilidade de arquiteturas de EPS também foi proposto. Baseado neste modelo de avaliação, foi possível comparar a arquitetura aqui apresentada, com aquela utilizada na versão anterior da mesma plataforma e com a NanoPower P31U, que é projetada pela GomSpace. Resultados comparativos confirmaram a efetividade das técnicas que foram incorporadas ao EPS, indicando que ele apresenta a arquitetura mais confiável dentre as três que foram consideradas para esta análise.

Palavras-chave: Arquitetura de subsistema. Confiabilidade. Subsistema elétrico de potência (EPS). Eficiência de energia. Nanossatélite.

RESUMO EXPANDIDO

INTRODUÇÃO

Nanossatélite é um termo utilizado para descrever satélites de pequeno porte que geralmente pesam menos de 10 kg. A classe mais amplamente difundida de nanossatélite é o CubeSat, um satélite de pesquisa, de formato cúbico, usualmente feito apenas com componentes de prateleira (COTS). Em virtude do baixo custo e do menor tempo de desenvolvimento, o padrão CubeSat facilitou o acesso ao espaço e causou um grande salto no número de lançamentos de nanossatélites. Apenas nos últimos 10 anos, de 2012 a 2022, este número aumentou cerca de 2600%, saindo de 25 para 646 lançamentos. A estrutura de um nanossatélite é dividida em subsistemas, os quais são distribuídos e conectados de acordo com suas funcionalidades. Um dos subsistemas mais vitais para esta estrutura é o sistema elétrico de potência (EPS), que é responsável por coletar, condicionar, armazenar, e distribuir energia para o nanossatélite. Isto significa dizer que todos os demais subsistemas dependem do bom funcionamento do EPS para que possam implementar suas próprias funções. Por consequência, é possível observar que uma falha no EPS geralmente se traduz na falha da missão. Além de sua importância inata, estudos estatísticos conduzidos na última década revelam também que o EPS é o subsistema responsável pelo maior número de falhas de missões de nanossatélites. Isto expõe não apenas que este subsistema é indispensável, mas também que existe uma necessidade latente de que sua confiabilidade seja aprimorada. É dentro deste contexto que este trabalho está inserido, visando compreender melhor os motivos pelos quais este subsistema vem falhando com tanta frequência e, promover alternativas para solucioná-los de forma factível e prática, a fim de se elevar a taxa de sucesso das missões de nanossatélites.

OBJETIVOS

O objetivo geral deste trabalho é propor uma arquitetura de EPS confiável e viável para utilização em missões de nanossatélites de órbita terrestre baixa. Visto que o objetivo geral é bastante amplo, alguns objetivos específicos foram também estabelecidos, a saber: identificar e propor técnicas de melhoria de confiabilidade que possibilitem um projeto de baixo custo e tamanho reduzido; identificar e propor técnicas de redução de consumo de energia para assegurar a viabilidade de projeto; elaborar e propor uma arquitetura de EPS que incorpore as técnicas de melhoria de confiabilidade e as estratégias de redução de consumo de energia; verificar e validar as principais funcionalidades da EPS; propor um sistema e avaliação de confiabilidade que possibilite a comparação de diferentes arquiteturas; aplicar o sistema de avaliação para atestar a

efetividade das técnicas de melhoria de confiabilidade que foram propostas; projetar o esquema elétrico da placa de circuito impresso da EPS.

METODOLOGIA

A primeira etapa deste trabalho envolveu estudar o tema proposto e examinar o projeto da arquitetura de EPS utilizada na plataforma FloripaSat-1. Deste estudo preliminar, detectou-se uma lacuna a ser preenchida na literatura, que reside na escassez de soluções de EPS de alta confiabilidade que sejam adequadas para projetos de nanossatélite, em especial de CubeSats. Então, trabalhou-se para encontrar técnicas de melhoria de confiabilidade que pudessem ser incorporadas a uma arquitetura de EPS sem que outros aspectos importantes do projeto fossem comprometidos. Estas técnicas foram então implementadas em conjunto com outras estratégias de projeto para propor uma arquitetura de EPS de confiabilidade aprimorada. Simulações SPICE foram executadas para validar a funcionalidade e verificar a performance dos principais circuitos presentes na arquitetura. Além disso, foi também proposto um sistema de três métricas para avaliar confiabilidade de diferentes arquiteturas. A aplicação deste sistema foi demonstrada ao avaliar e comparar três EPS distintas. Por fim, visando futura fabricação e realização de testes experimentais, o esquema elétrico da placa de circuito impresso da EPS foi projetado utilizando a ferramenta Altium Designer.

RESULTADOS E DISCUSSÃO

Esta dissertação apresentou uma visão geral sobre o problema de confiabilidade das EPS de nanossatélite a das técnicas de melhoria que vem sendo propostas nas últimas décadas. Em vista da escassez de alternativas de projeto que sejam viáveis e práticas, especialmente para utilização na plataforma FLoripaSat-2, uma arquitetura EPS de confiabilidade aprimorada foi proposta. Quatro principais técnicas foram incorporadas à esta arquitetura para melhorar sua confiabilidade. A saber, seleção metódica de componentes de prateleira, projeto sem processador, redundância passiva parcial, e monitoramento e controle de cargas. Além disto, três estratégias para redução de consumo de energia foram colocadas em prática. Sendo a mais importante delas o uso de conversores de carga customizados, de alta eficiência, e baseados em transistores de nitreto de gálio (GaN). Ademais, um sistema de três métricas para avaliar e comparar a confiabilidade de arquiteturas EPS também foi proposto. Assim, foi possível comparar a nova arquitetura de EPS com sua predecessora, que foi utilizada na plataforma FloripaSat-1, e com a NanoPower P31U, uma EPS comercial da GomSpace. Neste sistema de avaliação, onde 0 representa o nível mais baixo de confiabilidade e 9 o mais elevado, a arquitetura proposta foi considerada a mais confiável, recebendo a nota máxima. A arquitetura da GomSpace ficou em segundo lugar, com nota 4. E

a arquitetura do FloripaSat-1, em terceiro, com nota 3. Em termos de eficiência dos conversores de carga, em virtude das customizações que foram realizadas, a arquitetura atual também apresenta melhorias significativas quando comparada a sua versão anterior. Simulações de circuito mostram que a eficiência média dos conversores Buck de 5,0 V e 3,3 V são de 98% e 96%, respectivamente.

CONSIDERAÇÕES FINAIS

Pode-se afirmar que os objetivos estabelecidos para esta dissertação foram alcançados com sucesso. O caráter inovador e a relevância deste estudo para literatura, puderam ser evidenciados através da aprovação do investimento no projeto 407174/2022-2 e da submissão do artigo para revista de alto fator de impacto. Ademais, tudo que foi apresentado neste estudo, sejam as técnicas de melhoria de confiabilidade, as estratégias de redução de consumo de energia, ou o sistema de avaliação de confiabilidade de arquitetura, pode ser aproveitado por outras universidades e centros de pesquisa para facilitar e acelerar o projeto de novas arquiteturas de EPS de alta confiabilidade.

Palavras-chave: Arquitetura de sistema. Confiabilidade. Subsistema elétrico de potência (EPS). Eficiência de energia. Nanossatélite.

ABSTRACT

The low reliability of the Electrical Power Systems (EPS) is one of the major factors responsible for the high number of nanosatellite mission failures. Although several reliability-enhancing techniques have been proposed in the past, most studies do not take into account their applicability, overlooking the cost, power, and board area required for them to be implemented. In light of this, the present work proposes an EPS architecture that incorporates four reliability-enhancing techniques into a low-cost, small-footprint design. Namely, methodical COTS selection, processor-less design, partial standby redundancy, and load monitoring and control. Each technique was thoughtfully chosen to enhance the EPS reliability without compromising other design areas. To further ensure the viability of the architecture, three power reduction design strategies were also put in place. The most important of which was the use of customized high-efficiency GaN-based point-of-load (PoL) converters. In addition, the architecture features mostly low-power components and provides support for low-power modes of operation, which can greatly reduce the power wasted during an eclipse or an idle period. The entire proposal was backed up by block diagrams, theoretical analysis, design equations, and a printed circuit board (PCB) schematic design. The efficiency of the PoL converters, the standby redundancy activation mechanism, and all other main EPS functionalities, were verified and validated through SPICE circuit simulations. Furthermore, this work also proposes a three-metric system for evaluating and comparing the reliability of different EPS architectures. Based on this evaluation method, it was possible to compare the EPS architecture presented herein with its previous version and with the NanoPower P31U, which is designed by GomSpace. Comparison results confirmed the effectiveness of the techniques that were incorporated into this EPS, indicating that it exhibits the highest architecture reliability among the three candidates that were considered for this analysis.

Keywords: Electrical power system (EPS). Energy efficiency. Nanosatellite. Reliability. System architecture.

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LIST OF ABBREVIATIONS AND ACRONYMS

ACS	Attitude Control System
BJT	Bipolar Junction Transistor
BOM	Bill of Materials
CCM	Continuous Conduction Mode
CERN	The European Organization for Nuclear Research
CNPq	National Council for Scientific and Technological Development
COTS	Commercial-off-the-Shelf
DCM	Discontinuous Conduction Mode
DCP	Data Collector Platform
DET	Direct Energy Transfer
DoD	Depth of Discharge
EDC	Environmental Data Collector
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EOL	End of Life
EPS	Electrical Power System
GaAs	Gallium arsenide
GaInP	Gallium indium phosphide
GaN	Gallium Nitride
Ge	Germanium
GEO	Geostationary Orbit
GSFC	Goddard Space Flight Center
HEMT	High-Electron-Mobility Transistor
IEEE	Institute of Electrical and Electronics Engineers
I^2C	inter-integrated circuit
JPL	Jet Propulsion Laboratory
LEO	Low Earth Orbit
Li-ion	Lithium-Ion
MI	Module Integrated
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
MPPV	Maximum Power Point Voltage
NASA	National Aeronautics and Space Administration
NMOS	N-Channel Metal-Oxide Semiconductor
NPN	Negative-Positive-Negative
OBDH	On-Board Data Handling
PCB	Printed Circuit Board

PMOS	P-Channel Metal-Oxide Semiconductor
PoL	Point of Load
PPT	Peak Power Transfer
PV	Photovoltaic
PWM	Pulse-Width Modulation
RBD	Reliability Block Diagram
RBF	Remove Before Flight
RCC	Ripple Correlation Control
SEB	Single-Event Burnout
SEEs	Single-Event Effects
SEGR	Single-Event Gate Rupture
SOI	Silicon-on-Insulator
SpaceLab	Space Systems Research Laboratory
SPICE	Simulation Program with Integrated Circuit Emphasis
SPoF	Single Point of Failure
TID	Total Ionizing Dose
TTC	Telemetry Tracking and Command

LIST OF SYMBOLS

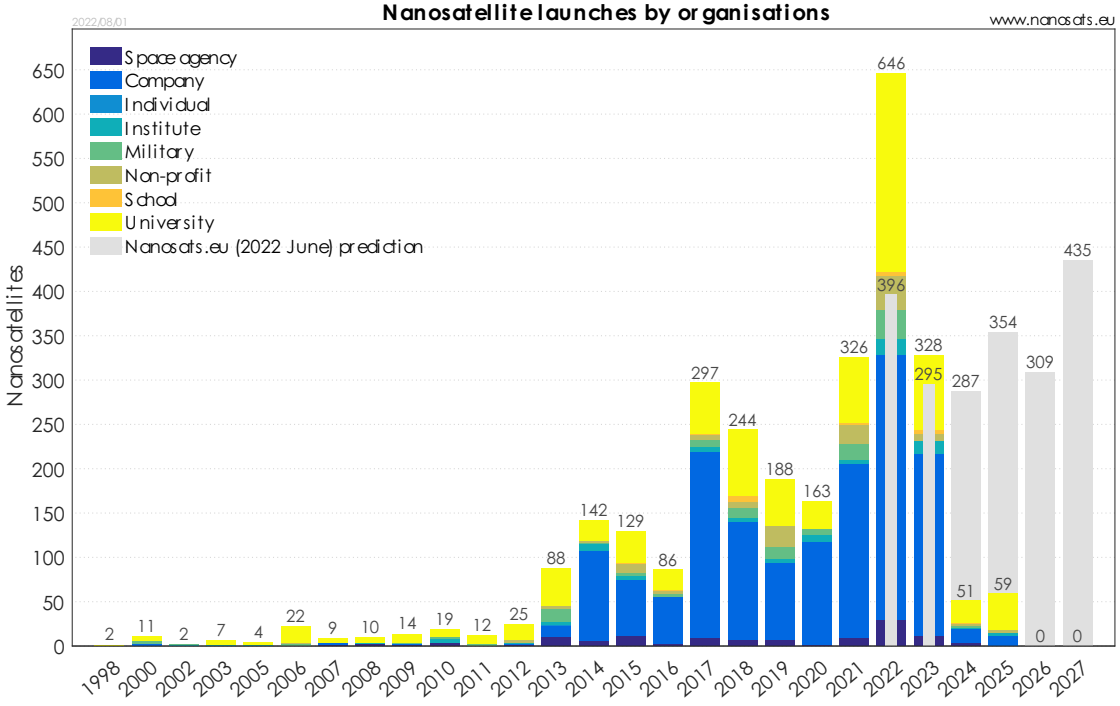
I_L	Light intensity
I_d	Diode current
I_0	Reverse saturation current
e	Electron charge
k	Boltzmann constant
T	Temperature
R_x	Component reliability
R_s	System reliability
V_G	Gate voltage
T_r	Rise time
T_f	Fall time
F_c	Unity gain frequency
t	Time
d	Duty Cycle

CONTENTS

1 INTRODUCTION

Nanosatellite is a term used to describe any satellite weighing less than 10 kilograms. The most widespread class of nanosatellites is the CubeSat, which is a low-cost, square-shaped research spacecraft, usually made with commercial-off-the-shelf components (COTS). According to international specifications, the standard 1U CubeSat must measure 10x10x10 cm and weigh less than 2kg. In the same way, a 2U CubeSat must measure 10x10x20 cm and weigh no more than 4kg, a 3U CubeSat must measure 10x10x30 cm and weigh no more than 6kg, and so forth (THE CUBESAT PROGRAM, 2022). Due to its reduced cost and shorter development time, the CubeSat standard promoted greater accessibility to space and caused a rapid surge in the overall number of nanosatellite launches. As shown in Figure 1, only in the last decade, from 2012 to 2022, this number increased by over 2400%, leaping from 25 to 646 launches a year. Research institutes, non-profit organizations, companies, and aerospace agencies, have all embarked on this initiative, and nowadays, it is possible to identify several universities around the globe performing tests and conducting experiments in space (KULU, 2022).

Figure 1 – Yearly nanosatellite launches by organizations.

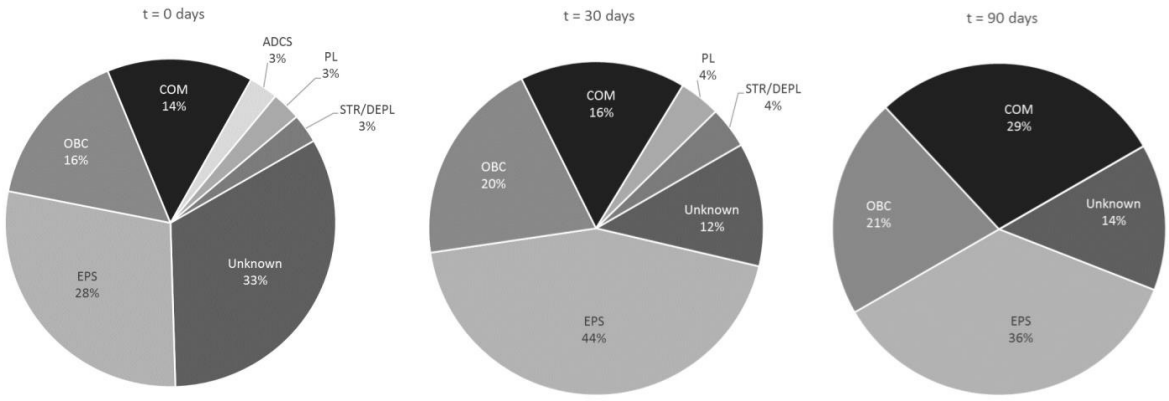


Source: (KULU, 2022)

The structure of a nanosatellite is broken down into subsystems that are distributed and connected by their functions. One of the most vital subsystems of this structure is the electrical power system (EPS), which is responsible for harvesting,

conditioning, storing, and delivering energy to the whole satellite. This means to say that every subsystem depends on the proper operation of the EPS to implement its own functions and, for this reason, a failure in the EPS usually translates into a mission failure (LASHAB et al., 2020). Besides its innate importance, statistical studies conducted in the recent past have shown that the EPS is the most failure-prone subsystem in a CubeSat (GUO; MONAS; GILL, 2014; TAFAZOLI, 2009; SWARTWOUT, 2013; LANGER; BOUWMEESTER, 2016). Particularly, a prominent research (LANGER; BOUWMEESTER, 2016) led by the Delft University of Technology, took into account data from 178 individual CubeSats and made parametric and non-parametric reliability assessments to determine which subsystem contributed the most to mission failures. As shown in Figure 2The same assessment was conducted for three different scenarios (right after ejection, 30 days after ejection, and 90 days after ejection), and, setting aside the unknown causes, the EPS was found to be the largest contributor to failures in all of them.

Figure 2 – Subsystems contribution to CubeSat failures.



Source: (LANGER; BOUWMEESTER, 2016)

Besides bringing attention to how critical the EPS is to ensure the success of a nanosatellite mission, this and other studies also reveal that there is great potential and opportunity for research in this area. Especially related to understanding the underlying reasons why the EPS has been failing so much and proposing alternatives for addressing these issues.

1.1 OBJECTIVES

1.1.1 General Objective

The general objective of this work is to propose a reliable and viable EPS architecture for use in low earth orbit (LEO) nanosatellite missions.

1.1.2 Specific Objectives

As the general objective is a broad statement and different approaches could be used to achieve it, more specific objectives were defined to determine the scope and the nature of the study.

1. Identify and propose reliability-enhancing techniques to enable a low-cost, small-footprint design
2. Identity and propose power reduction strategies to further ensure the viability of the design
3. Propose an EPS architecture that incorporates the reliability enhancing techniques and the power reduction design strategies
4. Verify and validate the main functionalities of the EPS
5. Propose a reliability evaluation system for comparing different EPS architectures
6. Apply the evaluation system to confirm the effectiveness of the reliability-enhancing techniques that were proposed
7. Design the printed circuit board (PCB) schematic of the EPS

1.2 TEXT STRUCTURE

Including the introduction, this master thesis is divided into eight chapters, which are further divided into sections and subsections. This structure is intended to facilitate the reading of the text and make it easier to navigate through the content. For quick reference, an overview of each chapter is provided below.

- **Chapter 2** Presents an overview of the state of the art. The chapter opens by explaining the EPS subsystem and its main functions. It delves into the EPS reliability issue and exposes why it is so important to address this problem. Then, it introduces the different reliability-enhancing techniques that have been proposed in the past and reveals a gap in the literature, that sets the stage for the work to be presented. Lastly, a case study is exhibited to highlight the motivation of the work.
- **Chapter 3** Describes in detail how the project was implemented, introducing in chronological order each of the activities that were carried out for the specific and general goals to be achieved.
- **Chapter 4** Presents the *Reliability Enhanced EPS* architecture and describes in detail the four reliability-enhancing techniques that were incorporated. It also describes three power reduction strategies that were used not to compromise the overall efficiency of the design.

- **Chapter 5** Dives into the hardware design details of the EPS. Gives an overview of each building block of the architecture, describing their key features, functions, selection criteria, and how they were implemented.
- **Chapter 6** Describes the SPICE circuit simulations that were performed to validate the functionality and verify the performance of key circuits of the *Reliability Enhanced EPS*. Simulation results are presented through waveforms and tables.
- **Chapter 7** Proposes a three-metric system for evaluating and comparing different EPS architectures in terms of reliability. Based on this system, the EPS proposed herein is compared with its previous version and with the NanoPower P31U, which is made by GomSpace.
- **Chapter 8** Provides a brief recap of the entire manuscript and highlights the most important topics that were covered. The chapter's emphasis is placed on what has been done to achieve the work's goals, the results that were obtained, the opportunities that were enabled, and future works.

2 STATE OF THE ART

2.1 ELECTRICAL POWER SYSTEM

As well as in the human body the respiratory system is responsible for harvesting oxygen from the air and distributing it to all its cells, in a satellite, the electrical power system is responsible for harvesting energy from the Sun and distributing it to all its subsystems. This analogy gives an idea of the importance of the EPS and highlights the fact that if it stops working for any reason, all other subsystems will eventually stop working too, and the satellite mission will be doomed to fail.

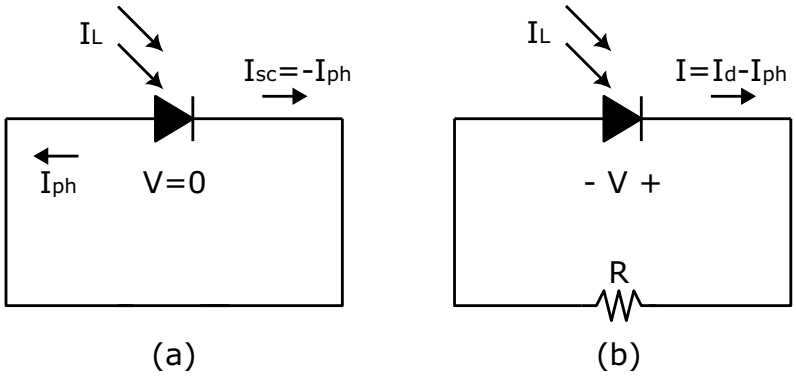
The description of the EPS specific functions may vary from one reference to another, but regardless of how they are worded, it is safe to say that it always encompasses these four activities: (1) power generation, (2) energy storage, (3) power conditioning, and (4) distribution (LASHAB et al., 2020; PATEL, 2004). In a nutshell, the energy is usually harvested by photovoltaic (PV) panels. In CubeSats, particularly, due to its high efficiency, the most adopted solar cell technology is the triple-junction gallium indium phosphide/gallium arsenide/germanium (GaInP/GaAs/Ge). After the energy is harvested, it is delivered both to the satellite loads and to the internal battery cells. The energy stored in the batteries is used to ensure the continuous operation of the satellite during eclipse or peak load conditions. Although it exhibits some disadvantages, Lithium-ion (Li-ion) remains the preferred energy storage technology, especially because it offers higher energy density, a higher number of charge/discharge cycles, and a lower self-discharge rate (WHITTINGHAM, 2012). The energy provided to the loads is pre-conditioned before being distributed and is usually made available in fixed output voltages of 3.3 V and 5.0 V (although other less common voltage rails may also be made available). Most of the time, switched-mode converters are used to provide regulated power to the loads but depending on the application, linear regulators can also be employed. In addition, the EPS may also implement monitoring and protection functions that are fundamental to prevent in-orbit circuit damage and to ensure the whole system is working as expected. These include voltage, current, and temperature sensors, overvoltage, overcurrent, latch-up protections, and others.

Although nowadays there are many different EPS architecture variations, they are usually categorized by their power generation method, either as a direct energy transfer (DET) architecture or as a peak power transfer (PPT) architecture (AGENCY, 2022). Before getting into the details of each architecture, to facilitate the understanding, it is first important lay out the basics of solar panel operation.

Solar panels are made up of photovoltaic cells that can be modeled as ideal *pn* junctions (KASAP; CAPPER, 2006). Figure 3 shows the equivalent PV cell circuit model under two different conditions (a) short-circuited and (b) connected to a load. When a cell is short-circuited (Figure 3-a), the short-circuit current (I_{sc}) is equal to the

module of the photocurrent (I_{ph}), which in its turn, is determined by the light intensity (I_L) multiplied by a constant (C) that depends on the photovoltaic characteristics of the cell, as given in equation (1).

Figure 3 – Ideal PV cell circuit model.



Source: Author, 2023

$$I_{sc} = -I_{ph} = I_L C \tag{1}$$

When a load is connected to the cell (Figure 3-b), the current I, which is given by equation (2), creates a voltage drop across the resistor R.

$$I = I_d - I_{ph} \tag{2}$$

The I_d portion of current I is a direct result of the *pn* junction characteristic of the cell and can be described by equation (3)

$$I_d = I_0 \left[exp\left(\frac{eV}{\eta k T} \right) \right] \tag{3}$$

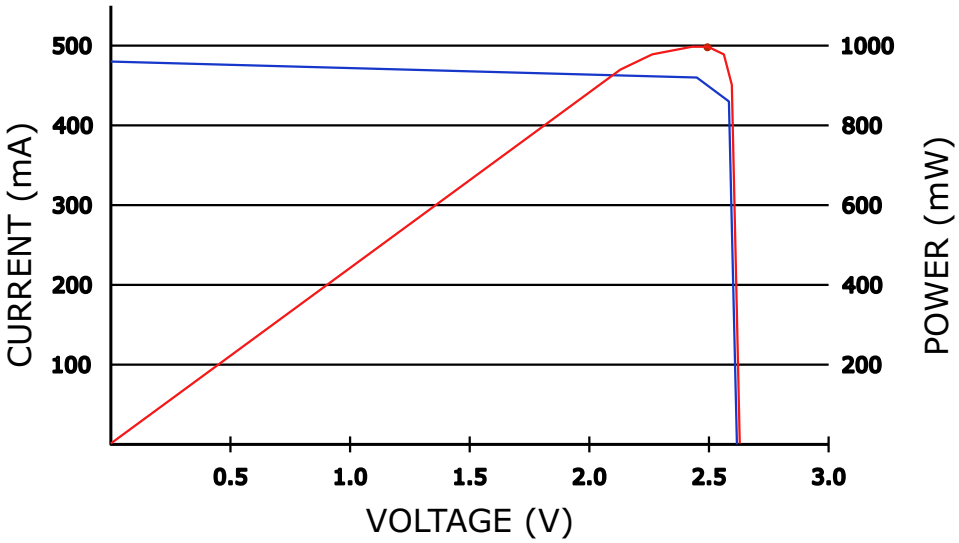
Where I_0 is the reverse saturation current, e is the electron charge, η is the emission coefficient (which varies between 1 and 2), k is the Boltzmann constant, T is the temperature in Kelvin, and V is the voltage across the resistor. Thus, as shown in equation (4), the current I can be described in terms of the voltage V by replacing I_d in equation (2)

$$I = I_0 \left[exp\left(\frac{eV}{\eta k T} \right) \right] - I_{ph} \tag{4}$$

From equation (4) it is possible to plot the I-V curves that define the electrical behavior of an ideal PV cell and, consequently, it is also possible to plot the power generated by the cell in terms of the voltage that is being applied to it. Figure 4 shows an example of a typical PV cell current-voltage curve. As it can be noted, there is a

specific voltage point at which the power generated by the panel is maximum, this point is usually referred to as the maximum power point voltage (V_{MPP}).

Figure 4 – Typical current-voltage characteristic.

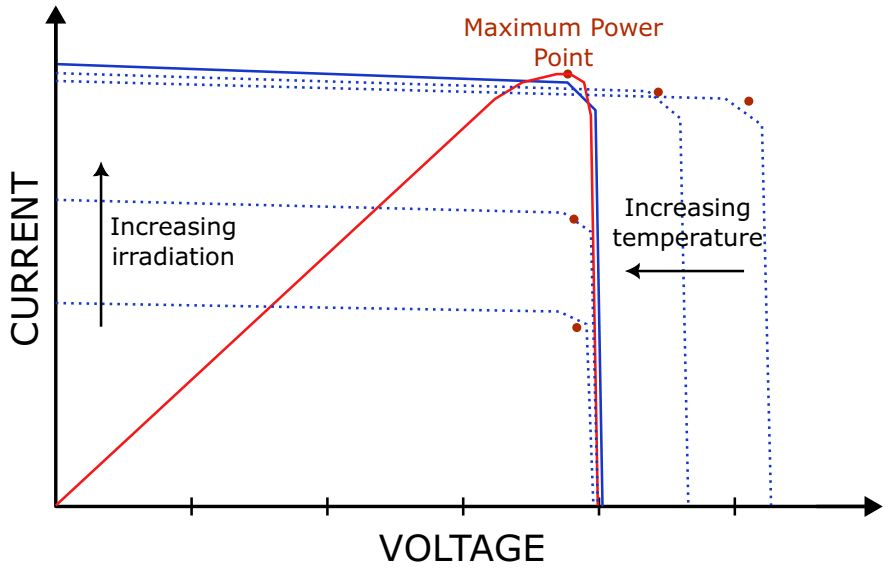


Source: Author, 2023

The caveat here, from the circuit design point of view, is that the V_{MPP} of a solar cell is not always the same. As clearly expressed in equation (4), the I-V curve of a solar cell is also dependent on its temperature and absolute light intensity. This means that for every change in temperature or irradiance, the solar cell will exhibit different electrical characteristics, and the voltage at which it must be operated to provide maximum power will no longer be the same. For this reason, throughout the years, several circuits have been proposed to maintain the solar panels operating as close as possible to their V_{MPP} regardless of I-V curve variations (SCHOEMAN; VAN WYK, 1982; LASHAB; SERA; GUERRERO, 2019). These are known as maximum power-point tracking (MPPT) circuits. Figure 5 shows how temperature and irradiance variations affect the I-V curve and the V_{MPP} voltage of a solar cell.

Going back to the difference between DET and PPT EPS architectures. As the name suggests, DET architectures are those that perform a direct transfer of energy from the PV panels to the battery, without applying any power shaping. This means that there is no solar panel voltage control and, therefore, no assurance that the panel will be operating at its V_{MPP}. As a consequence, DET architectures cannot extract the maximum power from the solar panels. A strategy widely adopted to mitigate this problem is to have a good matching between the battery voltage operating range and the solar panel V_{MPP} (RAGHUNATHAN et al., 2005). This way, the solar panel can be operated at a point that is at least close to its V_{MPP} while avoiding the use and overhead of a MPPT circuit. Yet still, for LEO mission applications, where nanosatellites

Figure 5 – Effect of temperature and irradiance variations on a PV cell current-voltage characteristic.



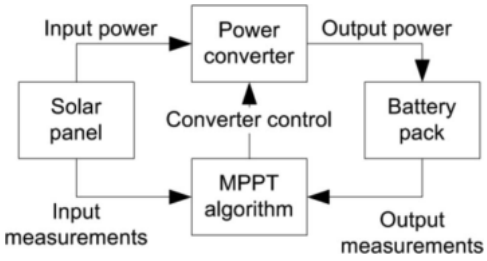
Source: Author, 2023

can spend up to 50% of their orbit in eclipse (SELCAN; KIRBIS; KRAMBERGER, 2016), and there is limited power generation and storage capabilities, it very challenging to employ a DET EPS architecture.

In response to this obstacle, various PPT architectures begun to emerge. In practice, the main difference, is that instead of connecting the PV panel directly to the battery, a DC-DC converter (also referred to as MPPT converter) is placed in between so that the power generated by the solar panel can be shaped. The converter is used to set the PV panel at its V_{MPP} voltage by matching the load to the panel's characteristic impedance. As shown in Figure 6, this is only possible because there is an auxiliary MPPT circuitry, which is usually implemented with a microcontroller, that gathers the input power and other EPS data to determine the DC-DC converter control. In addition, as DC-DC converters provide isolation between input and output, they make it possible to connect various PV panels to the same EPS bus while ensuring that all the panels can be operated as close as possible to their V_{MPP}. This characteristic is a key to maximize the power generated by the panels regardless of environmental condition variations, and that is why PPT architectures are most often the preferred choice for LEO nanosatellite applications.

The major drawback here is that the addition of DC-DC converters and micro-controllers (or other MPPT control strategy) have a direct impact on the complexity and reliability of the project. This is why it is still so challenging to find a viable EPS solution that is both reliable and capable of delivering the necessary power to its loads.

Figure 6 – Block diagram of a generic nanosatellite MPPT algorithm implementation.



Source: (SELCAN; KIRBIS; KRAMBERGER, 2016)

2.2 THE EPS RELIABILITY ISSUE

When it became internationally known that the EPS is responsible for most of the in-orbit CubeSat mission failures (GUO; MONAS; GILL, 2014; TAFAZOLI, 2009; SWARTWOUT, 2013; LANGER; BOUWMEESTER, 2016), more attention was directed to this subsystem and the topic began to gain traction in academic settings. Statistical studies were conducted to understand the underlying reasons for this EPS failure trend and scholars around the world started looking for different ways to improve the subsystem's reliability. As a starting point for further investigation into this issue, a study from 2017 dedicated itself only to analyzing the implementation and reliability aspects of the Cubesat electrical bus interfaces (BOUWMEESTER, Jasper; LANGER, Martin; GILL, 2017). Given the fact that data and power distribution lines impose requirements and constraints on all other subsystems, the authors understood that such an investigation was a milestone in the process of mapping the entire problem. The study was based on a literature survey and a questionnaire that included data from 104 CubeSats (60 launched and 44 to be launched). The questionnaire was sent out to people affiliated with the development of the CubeSats and was used to gather details on specific issues that were not disclosed in their flight results' publications. After analyzing all data, it has been concluded that most EPS failures cannot be attributed to electrical bus interface issues. Notwithstanding, it has been observed that some catastrophic satellite failures and a vast amount of bus lockups have been caused by the inter-integrated circuit (I^2C) data bus. Another fundamental observation made from this analysis is that 2 out of 5 CubeSats that did not have power distribution lines protection ended up failing after some days in orbit. Therefore, the study highly recommends protecting, both the central EPS unit as well as the local subsystems' power distribution lines against short circuits and over-currents (including those induced by radiation effects).

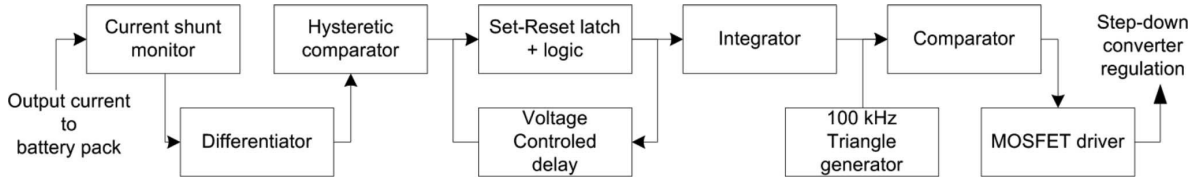
Similarly, an older study, from 2006, conducted a practical reliability analysis and used reliability modeling and prediction approaches to make sure an EPS architecture would meet its project requirements (ZAHRAN; TAWFIK; DYAKOV, 2006). First, the

authors sought to calculate the reliability of each internal component so that they could predict the overall system's reliability and only then propose an architecture that would meet the project's specifications. Through advanced Monte Carlo simulation techniques, the study demonstrated that the microcontroller is the most vulnerable component of the EPS architecture. The analysis shows that it contributes to about 23.9% of the failures and reduces the subsystem end-of-life (EOL) considerably. The use of redundant microcontrollers has been proposed by this and other authors as a solution to this problem (ZAHRAN; TAWFIK; DYAKOV, 2006; EDPUGANTI et al., 2020). However, as microcontrollers are usually the largest and most connected component of an EPS board, implementing redundancy becomes considerably inconvenient. In this case, the use of radiation-hardened microcontrollers seems to be the best solution, but as they are relatively expensive devices, they do not fit in the budget of a CubeSat project very often.

A great way for eliminating the microcontroller-related weakness from an EPS architecture without losing its high-energy harvesting capability is to implement an analog MPPT. On that wise, a study, from the University of Maribor, proposed an analog maximum power point tracking solution for LEO spacecraft applications. The proposed MPPT strategy is much similar to that of the ripple correlation control (RCC) method, where the solar panel's current and voltage outputs are measured and used in an analog multiplier to calculate the generated power. After this, the power signal is differentiated and used in conjunction with the current state of the MPPT algorithm to control the solar panel operating point. Figure 7 shows the block diagram of the proposed analog MPPT signal-processing chain. The principle of operation of this RCC variation method is the following: First, the power generated by the solar panels is calculated by measuring the output current of the MPPT power converter. The current measurement is directly translated into a power measurement because the converter's output voltage is fed into the battery, which keeps it almost constant. Then, the current signal is differentiated and its result is compared with a virtual zero, which will decide whether the output current (power) is increasing or decreasing. This data is used in a simple decision logic with a delay to drive an error amplifier circuit. The output of the integrator is then compared with the output of a triangle wave generator to create the pulse-width-modulated signal that is used to control the MPPT converter.

Additionally, to further improve the reliability of solar power generation systems in LEO environments, the study also suggests a careful selection of the analog components. The criterion defined by the authors was more focused on the latch-up tolerances, as they considered it to be the most aggressive radiation effect for this application. TID ratings were also checked, but due to the fact that their solution was targeted at LEO, they did not consider it necessary to place much emphasis on this. The use of transistors was limited to P-Channel MOSFET (PMOS) and NPN bipolar junctions (BJTs)

Figure 7 – Block diagram of the analog MPPT signal-processing chain.



Source: (SELCAN; KIRBIS; KRAMBERGER, 2016)

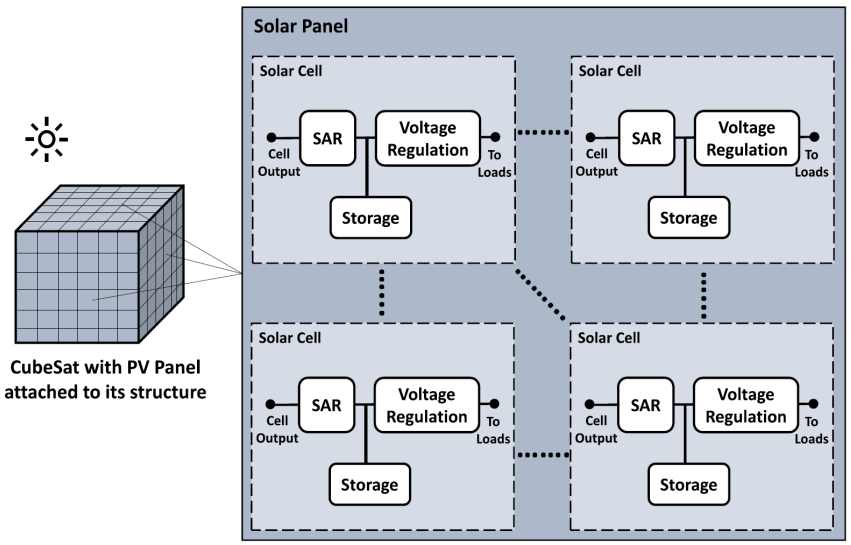
as these are more tolerant to latch-up than their counterparts. Passive components were simply presumed immune to TID up to 30 *krad* (SINCLAIR; DYER, 2013). For the remaining components in the architecture, a case-by-case approach was considered. Priority was given to silicon-on-insulator (SOI) technology, radiation-hardened, and radiation-tested devices. Although this study is innovative and could be used to address a critical EPS reliability issue, the downside is that the solution ended up becoming quite complex. Many components had to be added to implement the MPPT decision logic, which will have to be replicated for each panel. This has the potential to backfire and introduce other reliability and feasibility problems to a nanosatellite application. Furthermore, the efficiency of the MPPT converter was affected by the components' selection and should be further improved to better justify the implementation of the analog MPPT strategy.

The hardware architecture, which concerns the number of components and how they are connected to each other, is also a critical aspect of the EPS reliability. Depending on the components' arrangement, an EPS might be more reliable than another. Along these lines, a study published just last year proposed a module-integrated (MI) architecture to improve the EPS reliability (HUSSEIN; MASSOUD; KHATTAB, 2022). As shown in Figure 8, the idea is that the EPS should be divided into modules, so that each solar panel would have its own MPPT converter, storage system, and PoL converters integrated into its back.

Furthermore, the same study also proposed two different reliability metrics to compare the performance of the centralized, distributed, and module-integrated architectures. Altogether, 21 EPS architectures from these three categories were evaluated. The metrics were defined as follows:

- **Single point of failure (SPoF)**: Part of the subsystem (point/component) that, if it fails, will make the entire system fail. The lower the number of SPoF the better the EPS architecture reliability.
- **Series/parallel connection**: Assuming the reliability of two different components are R_{x1} and R_{x2}, the reliability of the subsystem (R_s) can be calculated based on their connection type. For series connections, the reliability can be

Figure 8 – Block diagram of a CubeSat module-integrated EPS.



Source: (HUSSEIN; MASSOUD; KHATTAB, 2022)

calculated as shown in (5):

$$R_s = R_{x1} R_{x2} \tag{5}$$

For parallel connections, the subsystem reliability can be calculated as shown in (6):

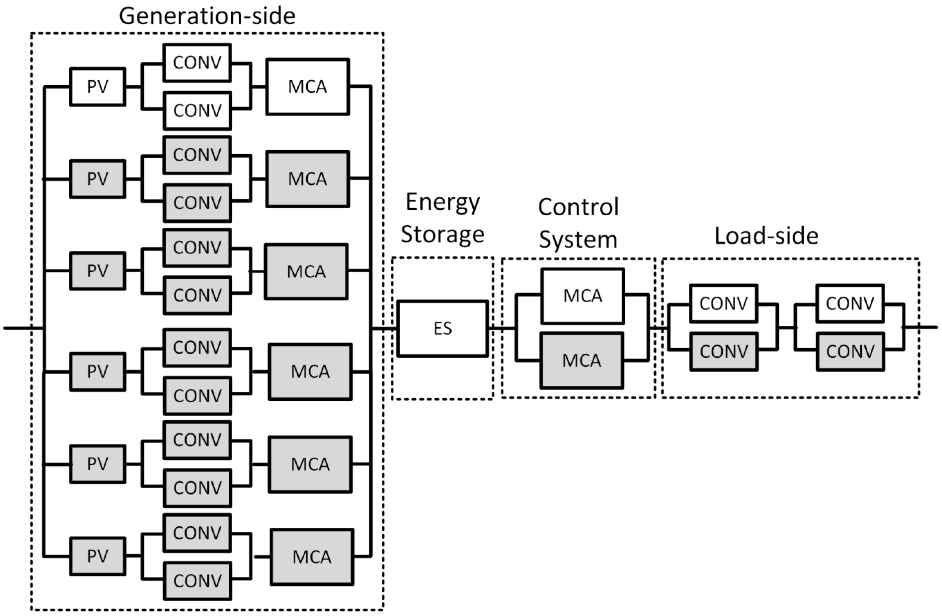
$$R_s = 1 - \left(1 - R_{x1}\right)\left(1 - R_{x2}\right) \tag{6}$$

The higher the R_s value, the higher the EPS architecture reliability.

After the comparison, the study concluded that module-integrated (MI) architectures are more reliable than distributed and centralized ones. To come to this conclusion, it was assumed that MI architectures do not have SPoF because there is an EPS integrated into each panel. However, this assumption is not always true because when one of the integrated EPSs fails the remaining ones are no longer capable of harvesting the same amount of energy. This means that the performance is degraded and the remaining modules become overwhelmed. In addition, as every integrated EPS has its own internal SPoF, when the first EPS fails, there is a great likelihood that the other ones are about to fail too. Although certain assumptions might have to be further verified, at least two great lessons can be learned from this study. The first is the ability to implement redundancy to eliminate SPoF, and the second is the importance of having an adequate reliability evaluation system to compare different EPS architectures.

Yet another aspect that can be detrimental to the reliability of an EPS and has been the focus of extensive research, is the electrical and thermal stress in the semiconductor devices, especially caused by the continuous operation of maximum power point tracking (MPPT) and point-of-load (PoL) converters (PECHT; DASGUPTA, 1995; WANG, H. et al., 2013). As a solution to this problem, a recent study proposed a distributed EPS architecture with power-down mode and dedicated MPPT converters (EDPUGANTI et al., 2021b). The authors' idea is that each solar panel should have its own power converter, gate driver, and microcontroller to provide higher maximum power point tracking accuracy and reduce electrical/thermal stress in semiconductor devices.

Figure 9 – Distributed EPS architecture with power-down mode for enhanced lifetime.



Source: (EDPUGANTI et al., 2021b)

As shown in Figure 9, except for the generation side, all other functionalities, such as system control, load conversion, and energy storage should be mutually shared by the system. The proposed power-down mode is based on the power generation and load consumption profiles of the EPS, and also reduces the stress by turning the converters' switching signals off during no or low power conditions. While the architecture proposed in this study delivers on what it promises, enhancing the EPS lifetime by reducing the stress of the semiconductor devices, it is extremely difficult to be implemented as it greatly increases the number of components, footprint area, cost, and current consumption of the subsystem.

In general terms, most reliability/lifetime enhancing techniques are associated with higher power consumption and/or with increased board area (CHANDRA; AITKEN,

2008; MESSER et al., 2001). For this reason, although many approaches for improving EPS reliability have been proposed in the past, most of them are impractical. Usually, papers only focus on the reliability aspects of the design, as an isolated issue, and do not consider how their techniques impact the whole system. As a consequence, it is difficult to find a reliable EPS architecture that while offering a greater likelihood of mission success also suits the other key nanosatellite/CubeSat project constraints. In agreement with this, a paper that presented an extensive and detailed review of all the conventional and emerging EPS architectures, also came to the conclusion that more researches have to be conducted to properly address this reliability issue (EDPUGANTI et al., 2021a). Therefore, this work is to propose a simple and viable EPS architecture, that incorporates state-of-the-art reliability-enhancing techniques without compromising the system's efficiency, area, and overall cost.

2.3 CASE STUDY

The study and the EPS architecture to be presented in this manuscript are not only conceptual, without practical application, but an integral part of a 2U CubeSat platform, which goes by the name of FloripaSat-2. A project envisioned for LEO missions of medium duration, that is being entirely developed by the Space Systems Research Laboratory (SpaceLab), from the Federal University of Santa Catarina.

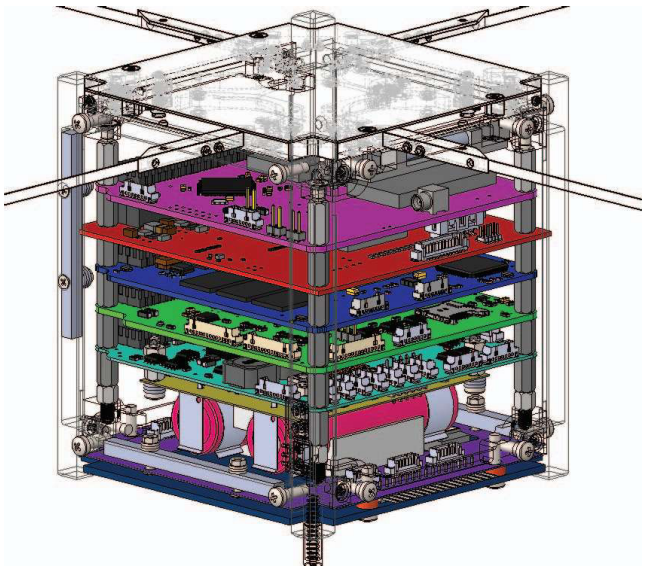
Besides the EPS, the platform comprises two other main subsystems, the onboard data handling (OBDH) and the telemetry tracking and command (TTC). In a nutshell, the OBDH is the satellite's brain, responsible for interpreting data, managing tasks, synchronizing actions, and controlling the data flow between the subsystems and the earth segment. The TTC in its turn, is the subsystem that establishes the communication between the satellite and the ground station. It features two radio modules and one microcontroller, which allows it to transmit and receive data on VHF and UHF bands. Furthermore, the FloripaSat-2 also includes a daughter board, four tape spring antennas, an attitude control system (ACS), an environmental data collector (EDC) payload, a mechanical structure, and several electrical connectors (MARCELINO et al., 2020a).

Environmental data collection is the primary and immediate application of the platform. Nevertheless, after testing the core spacecraft technologies in a high-radiation LEO environment, many other applications will naturally occur. Currently, there are already two missions planning to use the FloripaSat-2 platform. The first is known as GOLDS-UFSC and is intended for collecting environmental data, such as temperature, atmospheric pressure, and air humidity from different locations in Brazil. In general terms, the CubeSat will communicate with several data collector platforms (DCP), gather all their sensed data, and send it back to Earth. An activity that has always been performed by big satellites for weather forecasts and other purposes. The second mis-

sion is the Catarina Constellation, which is a program created by the Brazilian Ministry of Science, Technology, and Innovation, and consists in the use of nanosatellites for agricultural and national civil defense applications so as to contribute to the sustainable socioeconomic development of the country (MINISTÉRIO DA CIÊNCIA, 2021).

The FloripaSat-2 is meant to be an improved version of its predecessor FloripaSat-1. Figure 10 shows this 1U CubeSat platform that took about four years to be developed and made its launch in December 2019. During that period, SpaceLab made several contributions to the scientific community, publishing papers especially related to task scheduling algorithms (SEMAN et al., 2022; SLONGO et al., 2018; RIGO, Cezar Antônio et al., 2021; RIGO, Cezar Antonio et al., 2021), EPS architectures (KESSLER SLONGO et al., 2020), and thermal-electric battery models (VEGA MARTINEZ et al., 2021). The full review of the FloripaSat-1, including system architectures, components, functionalities, simulations, and initial test results was presented in (MARCELINO et al., 2020b) while its preliminary in-orbit results were presented in (MARCELINO et al., 2021).

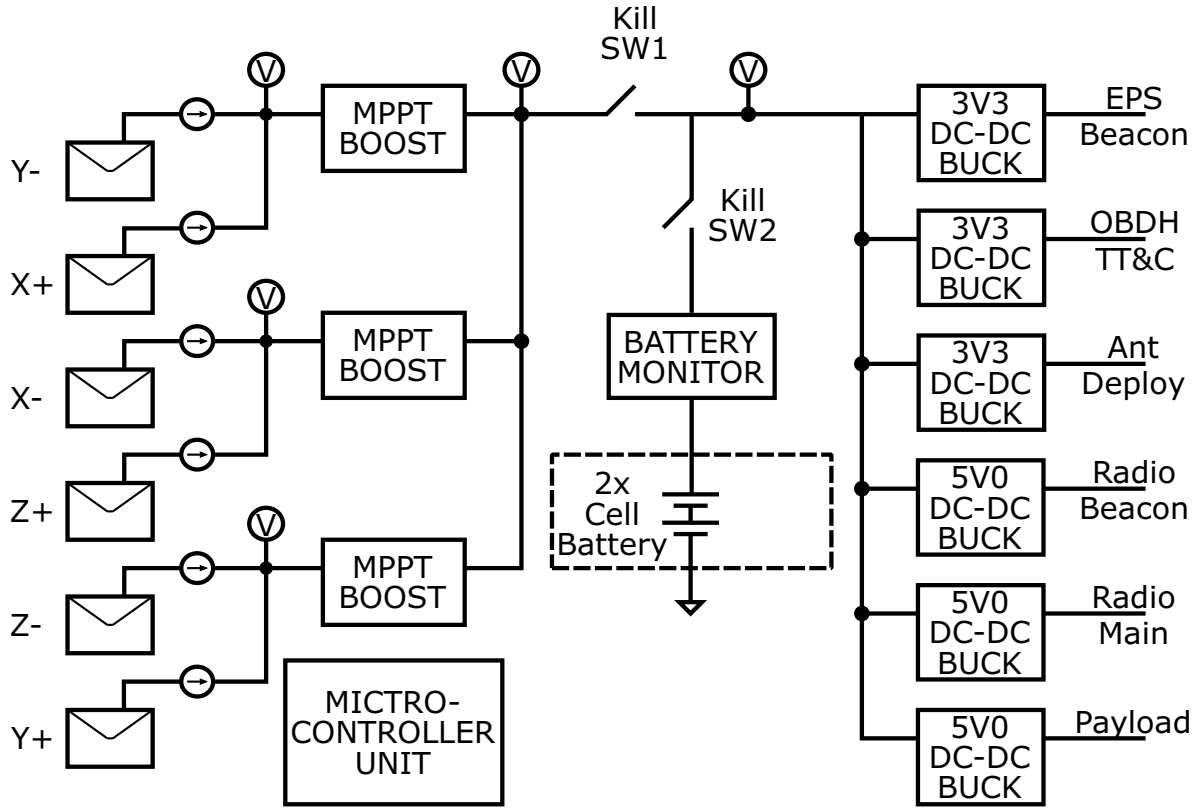
Figure 10 – Perspective view of the FloripaSat-1.



Source: (MARCELINO et al., 2020a)

As the forerunner was conceived for a short-duration technology demonstration LEO mission, reliability was not the main aspect of its design. None of the studies conducted at that time were focused on improving the system's reliability. Actually, the group's primary concern was to properly develop and integrate all the subsystems in time to test the technology in space. As shown in Figure 11, although functional and successful, the EPS architecture of FloripaSat-1 was not envisioned for medium/long-duration missions and, due to its 1U size, was limited only to small payloads.

Figure 11 – Block diagram of the FloripaSat-1 EPS.



Source: Author, 2023

The development of an improved version of the FloripaSat platform was prompted to fill this gap. It came out in response to different applications demanding better system reliability, longer lifetime, and higher payloads. The EPS proposed in this study is only one of the subsystems that are being improved and reformulated to meet new application requirements and address past mission issues.

3 METHODOLOGY

This chapter describes the procedures, activities, and materials used to develop the *Reliability Enhanced EPS* while ensuring that all the specific and general project goals are achieved.

1. **FloripaSat-1 EPS review:** Conduct a detailed review of the FloripaSat-1 EPS architecture. Read published articles, study the PCB schematic and layout, and analyze the bench-top tests and simulation results. This review is what is going to lay the foundations for this work. Architecture weaknesses, potential risks, and opportunities for improvement should be identified.
2. **FloripaSat-2 platform/mission requirements review:** Conduct a detailed review of the FloripaSat-2 platform specifications. Study the demands of the missions that have triggered this project development. This review should be used to define the *Reliability Enhanced EPS* design constraints and specifications.
3. **State of the art review:** Conduct an in-depth review of the state-of-the-art. The emphasis should be placed on relatively recent studies published in high-impact journals. The review topics should include the EPS subsystem, the EPS reliability issue, and high-reliability architectures. This review is not only meant to understand gaps in the literature but also to provide the ideas needed to conceive the *Reliability Enhanced EPS* design.
4. **Reliability Enhanced EPS proposal:** Incorporating state-of-the-art reliability-enhancing techniques propose a viable EPS architecture that meets the FloripaSat-2 platform demands
    - Draw the block diagram
    - Define the circuits' topologies
    - Select the components (supplier and part number)
5. **Reliability evaluation system proposal:** Based on the factors that impact the EPS reliability the most, define a system of metrics for evaluating and comparing different architectures
    - Describe the metrics ratings and weights
    - Demonstrate the evaluation system application
    - Find other well-consolidated CubeSat EPS architecture to use as a reference for comparison
6. **Circuit simulations:** Using the *LTSpice Simulator* from *Analog Devices* verify the functionality and the performance of the *Reliability Enhanced EPS* circuits
    - Download the SPICE models of all the necessary components

- Create the symbols of the components
- Set the appropriate boundary conditions and run the adequate simulations to verify, validate, and improve the proposed circuits

7. **PCB Schematic design:** Using the *Altium Designer Software* create a PCB project and make the schematic circuit design of the *Reliability Enhanced EPS*
    - Create a database library including the symbols and footprints of every component
    - Make the circuit schematic design
    - Provide directions for the PCB layout design
    - Generate the bill of materials (BOM)
8. **Paper submission:** Write a manuscript detailing what has been done in this master thesis and submit it to a high-impact factor journal/magazine

4 RELIABILITY ENHANCED EPS

As briefly presented in Chapter 2, several studies have been published approaching the EPS reliability issue in the past. Fundamentals have been established, weaknesses have been identified, reliability-enhancing and fault-tolerant techniques have been introduced, but it still remains a challenge to find a study that presents a reliable and viable EPS solution. The architecture proposed herein tries to bridge this gap in the literature by introducing a simple, low-cost, small-footprint design. The key reliability-enhancing techniques and power reduction strategies that were incorporated to enable such a design are described in this chapter.

4.1 ARCHITECTURE OVERVIEW

The architecture is targeted at a 2U CubeSat platform that uses 4 Li-ion battery cells to store the energy harvested by 10 PV solar panels. The battery cells are connected in a 2 series 2 parallel (2s2p) configuration and the solar panels are arranged in five groups of two, and then connected in series, in a 2x5 array. A MPPT battery charger circuit is used not only for controlling the charging of the batteries but also for establishing the maximum power harvesting voltage at the solar panels' outputs. Two DC-DC Buck converters are employed to provide regulated power at 3.3 V and 5.0 V to all the loads. Six high-side switches are implemented to connect the loads to the regulated power buses, guaranteeing isolation and providing better power management capabilities. As per standard, two separation switches are used to ensure that no active components of the nanosatellite are powered during the launch phase, avoiding interference with the ground station signals. Additionally, current and voltage sensing circuits are distributed throughout the board allowing for the monitoring and control of the EPS functionality. The measured signals are fed into a 16:1 analog multiplexer and sent to the OBDH microcontroller, which can keep track of all the values and take preventive actions on the fly. The high-level block diagram of the *Reliability Enhanced EPS* architecture is presented in Figure 12.

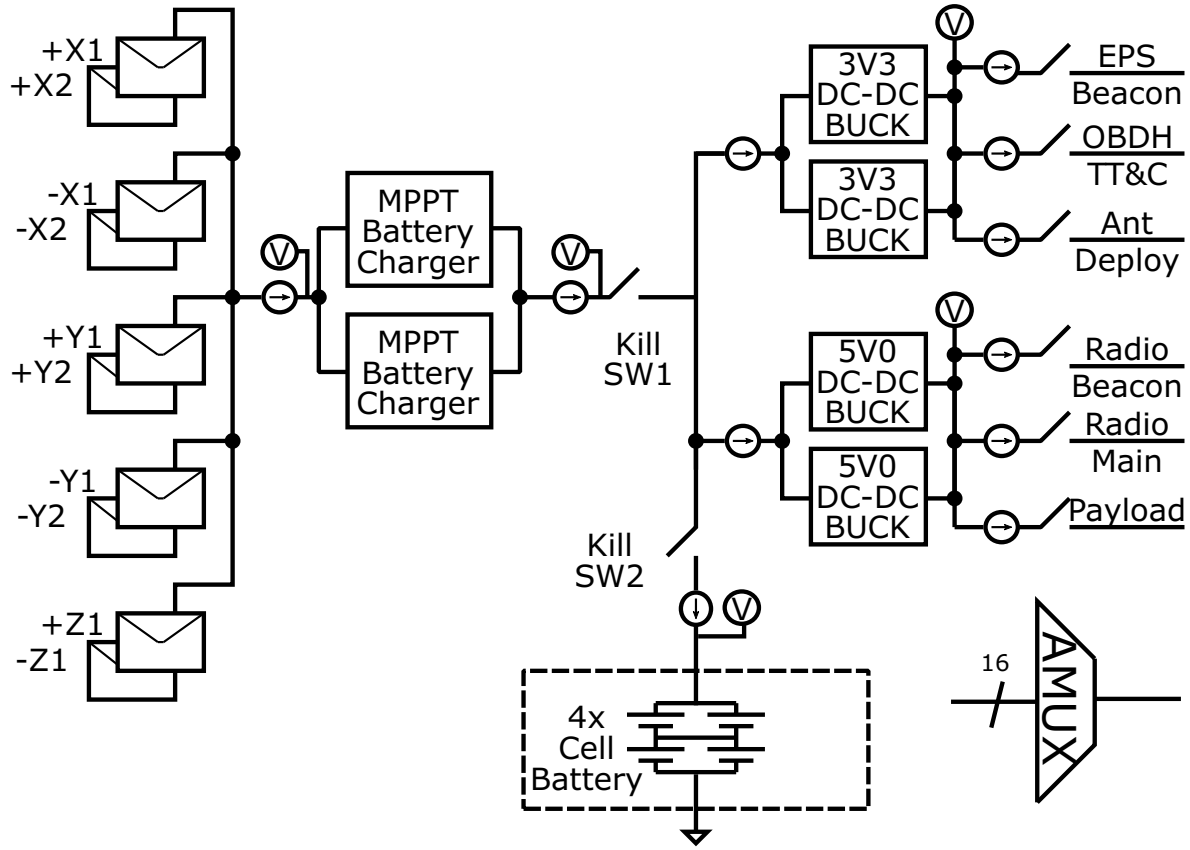
4.2 RELIABILITY ENHANCING TECHNIQUES

Based on the many studies that were already conducted on this topic, four key techniques were handpicked to enhance the EPS reliability without compromising other important project areas.

4.2.1 Methodical COTS selection

Circumstantial statistical analysis shows that picosatellites and nanosatellites exhibit higher failure rates and shorter lifetimes than microsatellites and minisatellites

Figure 12 – Block diagram of the reliability enhanced EPS.



Source: Author, 2023

(GUO; MONAS; GILL, 2014). Furthermore, the same study also reveals that university-class satellites exhibit lower reliability than satellites developed by non-university organizations, such as commercial companies, national defense, and space agencies. As most pico/nano/university satellites are based on the CubeSat standard, a correlation between low reliability and the use of COTS components can be established.

Table 1 – Small satellite mass categories.

Satellite category	**Mass range [kg]**
Picosatellite	0-1
Nanosatellite	1-10
Microsatellite	10-100
Minisatellite	100-500

Source: (GUO; MONAS; GILL, 2014)

To mitigate the risks associated with the poor quality of these components, especially related to their high radiation sensitivity, this EPS was designed using only COTS components with a considerable track record in the space industry. This means that only radiation-tested components (either from the NASA GSFC database or from IEEE

Radiation Effects Data Workshop articles) or components with recorded space flight heritage were employed in the project. In addition, all the transistors were selected based on the methodology presented in (SINCLAIR; DYER, 2013), which consists in applying the following criteria:

1. Where performance is not critical replace MOSFETs with bipolar junction transistors (BJTs);
2. When possible, replace N-Channel MOSFETs (NMOS) with PMOS as they have no single event burnout SEB mechanisms and total dose enhancement is seldom a problem;
3. When possible, use MOSFETs with a maximum gate voltage rating lower than the applied drain voltage ($V_{G(MAX)} < V_{DS}$) as it mitigates single-event gate rupture (SEGR). Additionally, limiting V_{GS} in circuit design will also reduce susceptibility to SEGR;
4. Massively derate the V_{DS} voltage rating for NMOS. 20% derating is appropriate. E.g. use a 40.0 V V_{DS} rated part for a 7.0 V nominal application.

Regarding the passive components, despite the fact that their failure rates are more than one order of magnitude lower than those of other semiconductor devices (SONG; WANG, B., 2012), in order to assume that they are radiation tolerant to least 30 krad, they must be operated in proper and derated biasing conditions (SINCLAIR; DYER, 2013). Therefore, every passive component was derated with margins higher than those suggested by the NASA GSFC part derating guidelines for space flight projects (SAHU; LEIDECKER; LAKINS, 2003). For example, a 0.6 voltage derating factor was attributed to ceramic capacitors, 0.6 voltage and 0.8 power derating factors were attributed to resistors, and a 0.5 voltage derating factor was attributed to all inductive devices.

4.2.2 Processor-less design

Besides reducing the cost, minimizing the required board area, and significantly lowering the power consumption, another key strategy implemented to strengthen the reliability of this EPS architecture is the use of no dedicated processor (microcontroller).

The processor-less concept was inspired by two fundamental observations. The first resides in the fact that EPS processors are usually responsible for implementing a minimal number of functions. For the most part of the architectures, they are only used to control the power switches of an MPPT converter, communicate with battery monitoring circuits, and monitor housekeeping data, such as temperature, voltage, and current. Considering that there are standalone alternatives for effectively implementing an MPPT converter (STAND-ALONE. . . , 2020) and that all housekeeping data monitoring and control is low speed and can be easily transferred to the OBDH microcontroller, it was understood that a topology without a dedicated processor could be seen fit.

The second observation concerns the fact that most EPS failures can be traced back to problems in their microcontroller. As mentioned in Chapter 2, a study has shown through advanced Monte Carlo simulation techniques that they are responsible for about 23.9% of the EPS failures (ZAHRAN; TAWFIK; DYAKOV, 2006). As it has already been proposed (ZAHRAN; TAWFIK; DYAKOV, 2006; EDPUGANTI et al., 2021b), implementing redundancy could be a plausible solution to the low-reliability characteristic of the COTS microcontrollers, however, such idea goes against what a CubeSat design stands for, raising costs, deepening the complexity, and increasing the required board area.

After carefully considering these two points, it was decided that for an enhanced reliability architecture, the benefits of removing the dedicated EPS microcontroller outweigh the drawbacks. Both processing functions related to MPPT control and battery monitoring are not necessary when using a standalone battery charge controller for solar panels. Although its MPPT method might not be the most accurate and there is not much room for optimizations there, removing a power-hungry component of the architecture while reducing the failure likelihood by 23.9% is a trade-off worth making. Housekeeping data and switch control functions were all transferred to the OBDH microcontroller and, to decrease the number of wires going out of the EPS board, an analog multiplexer was also added to the topology so that all the housekeeping signals could be monitored through a single wire.

One could argue that this strategy would not improve the reliability of the EPS as it is now dependent on the OBDH microcontroller reliability. The difference is that, as the OBDH microcontroller is a must for any satellite operation, designers usually implement redundancy strategies (BUSCH et al., 2015) or opt to invest in a rad-hard solution, which would not need to be duplicated in the EPS if it could be leveraged from the OBDH. In addition, as only secondary functions were transferred to the OBDH, even though its microcontroller happens to fail, it would not degrade the power efficiency of the EPS nor affect its default behavior.

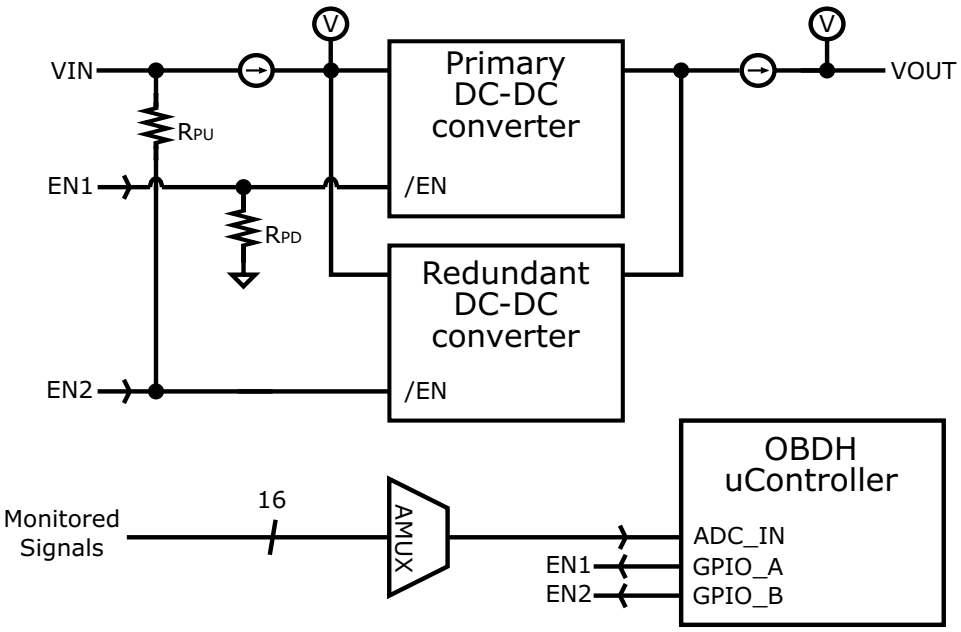
4.2.3 Partial standby redundancy

Hardware redundancy is one of the oldest and most effective reliability-enhancing techniques. It consists in duplicating the hardware design and incorporating a few extra circuits to detect any component/system failure and override its effects. Unfortunately, in nanosatellite applications, especially in CubeSats, it is neither cost-effective nor feasible (in terms of size and weight) to provide full hardware redundancy support. Therefore, to maximize the reliability of the EPS architecture, it was decided to implement a partial standby (passive) redundancy.

With the EPS microcontroller removal and considering that all components in the architecture have a significant track record in the space industry, it was only

deemed necessary to implement redundancy on components that experience high electrical/thermal stress or that represent a SPoF in the architecture, namely the battery charger and the PoL converters. The decision of using a standby type of redundancy was made based on two factors: to reduce the required power consumption and to preserve the reliability of the redundant units. This means that for every switched-mode converter of the architecture, there is a backup replica that is connected in parallel and remains powered off as long as it is not required (RAY, 2002a). The drawback of this type of redundancy, when compared to a hot standby type, is that it exhibits a greater downtime. This happens because when a failure takes place, the converter still has to be powered on and taken to a known state before it can take over the loads that were connected to the bus. To reduce this downtime, voltage and current monitoring circuits were added at the input and output of each converter so that the backup unit can be turned on as soon as the monitored signals go out of the user-set thresholds, way before their output capacitors get fully discharged.

Figure 13 – Block diagram of the standby PoL converters.



Source: Author, 2023

Figure 13 shows the standby redundancy high-level block diagram as implemented in the PoL and battery charger converters. Input and output currents and voltages are constantly monitored by the OBDH microcontroller, which can track their values and activate the redundant converter as the need arises at any given moment. Each converter features its individual enable signal so that they can be independently controlled by the microcontroller. Pull-up and pull-down resistors are used to ensure that even if the microcontroller signals are not available, the primary converter will be

enabled and the redundant one will be disabled. Simulation waveforms presented in Figure 23 demonstrate how the activation of the redundant converter plays out.

4.2.4 Load monitoring and control

The fourth key technique implemented to improve the reliability of the architecture is the use of load monitoring and control circuits. These mechanisms were brought into play to anticipate short circuits or misbehavior in the loads and disconnect them from the PoL converters before causing any damage to the EPS. Although the converters' controllers used in this architecture already have their overvoltage/overcurrent internal protections, the load monitoring and control circuits work as a second layer of protection, preventing the output of the converter to be brought down and automatically isolating a problematic load so that the rest of the circuits that are powered by the same rail are not affected by it.

The entire load monitoring and control strategy is depicted in the right corner of Fig. 12. For each PoL converter, an output voltage monitoring circuit was added to keep track of the regulated rail, three current monitoring circuits were added to keep track of the current that is being drawn by each specific load, and three high-side load switches that are enabled by three different signals were added so that the loads can be controlled independently. Like in the standby redundancy strategy, all the monitored signals are multiplexed and sent to the OBDH microcontroller, which can track these values and, given the need, connect/disconnect any load on the fly. A similar strategy was proposed in (CHEN et al., 2020), but the work's goal there was to be able to disconnect the loads to save up power during an eclipse and other low-power mode conditions. With the addition of the monitoring circuits, switches that were once only used to manage payloads' current consumption are now being used as a fault-tolerant strategy to increase EPS reliability. Detailed descriptions of the monitoring and high-side switch circuits are presented in Chapter 5.

4.3 POWER REDUCTION STRATEGIES

Besides removing the dedicated processor (which is usually a power-hungry component of an EPS) and reducing the number of active PoL converters from six (FloripaSat-1) to two, other power reduction techniques were implemented to ensure that the overall system efficiency would not be compromised.

4.3.1 Improved PoL converters efficiency

Apart from radiation immunity, the selection of the PoL converters' controllers was mainly driven by power efficiency and Gallium Nitride (GaN) power switch support. Unlike the previous FloripaSat version, which featured Buck converters with integrated

power switches and exhibited an average efficiency of 90%, this new architecture features Buck controllers with external power switches that, for the proposed operating range, exhibit an average efficiency of 96%. Furthermore, although in the previous version each load had its own dedicated converter, their designs were not customized, which made them operate out of their optimal load range and led to efficiency values as low as 70%. This issue was also solved by connecting three different loads to each PoL converter and optimizing the design to the expected average load.

GaN power switch support is another controller's feature that enabled higher power conversion efficiencies. As described in (COOK et al., 2018), GaN devices have a significantly wider band gap (3.4 eV) and a smaller physical depletion region, which allows them to operate at higher temperatures while maintaining a high breakdown voltage. The shorter depletion region width is the characteristic that makes their $R_{DS(on)}$ resistance lower and, depending on the operating frequency of the PoL converter, reduces the overall power loss. To make sure that all the design changes worked as expected, improving the converters' efficiency, the proposed topology, which is further described in the next section, was simulated for different load and input voltage scenarios. Simulation results and waveforms for both the 5.0 V and the 3.3 V Buck converters are presented in Chapter 6.

4.3.2 Low-power modes support

A simple but very effective way of reducing the architecture's power consumption is to provide support for different modes of operation (GONZALEZ-LLORENTE et al., 2015). Although a CubeSat takes about 96 minutes to complete an LEO orbit, its loads are not always active or required (EDPUGANTI et al., 2021b). Actually, most loads that are connected to the regulated bus outputs of an EPS, are only active for a short period of the orbit time, while tasks that were programmed in the OBDH microcontroller are being executed. After this period, loads might remain idle and the PoL converters might be operating aimlessly.

As the behavior of a nanosatellite is mostly cyclical, repeating the programmed tasks during every orbit, it is possible to predict its load profile to implement low-power modes of operation, where idle loads can be disconnected and PoL converters can be disabled as soon as they are no longer required. This feature is fully supported in this architecture through the use of high-side switches and individual enable signals, that were first incorporated for the activation of redundant converters, but that can also be used in conjunction with OBDH microcontroller commands to place the EPS in different low-power modes of operation. For various nanosatellite applications, this capability will be translated into keeping the PoL converters turned off for a great period of the orbit time, saving up a lot of energy and reducing the electrical/thermal stress of the power devices. Furthermore, if the energy harvesting/storing circuits happen to be

compromised during the mission, this hardware feature can also be leveraged by the OBDH microcontroller to prioritize the most important tasks over the secondary ones, cutting off the power supply of loads that are not critical to the conclusion of the mission.

4.3.3 Low-power components

After applying the methodical COTS selection technique that was presented earlier to establish a pool of components that could be used for each specific function of the EPS, power consumption ratings were also scrutinized to be used as second exclusion criteria, narrowing down the available component alternatives. Only then, other performance characteristics were evaluated/compared to make the final components selection.

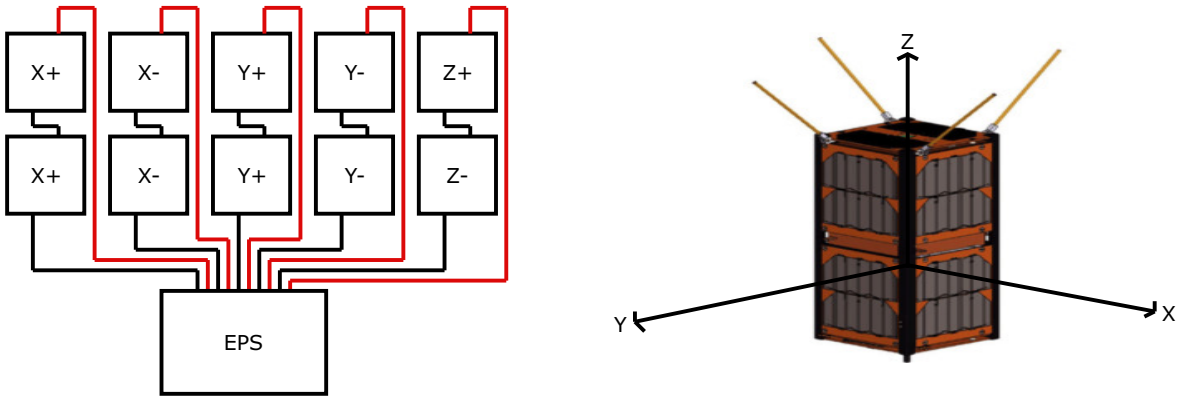
5 HARDWARE IMPLEMENTATION

Although the *Reliability Enhanced EPS* was entirely envisioned for the FloripaSat-2, which is a 2U CubeSat platform, the same block distributions, components, and techniques can be implemented in 3U and 6U CubeSat projects, depending on their PV panels and battery pack arrangements. This section presents an overview of each building block of the architecture, describing their key features, functions, selection criteria, and how they were implemented.

5.1 SOLAR PANEL ARRAY

The FloripaSat-2 features ten PV panels that are distributed in five groups of two. The solar panels of each group are connected in series and then connected to the input of the EPS board as shown in Figure. 14.

Figure 14 – Block diagram of the PV panels array.



Source: Author, 2023

Strategically, four of these groups were formed by panels from the same side of the CubeSat while the fifth was formed by the bottom (-Z) and the top (+Z) remaining panels. As both the temperature and the radiance incident on panels pertaining to the same side of a nanosatellite tend to be about the same, their maximum power point voltage MPPV will also be very much alike. Therefore, this panels' arrangement allows for the most accurate tracking of the mean MPPV of two different panels and consequently leads to the highest energy harvesting capability.

Although each panel group is composed of two series panels, each panel itself is composed of two series solar cells. Thus, each panel group is actually formed by four solar cells connected in series. Based on its space flight heritage, the CTJ30 triple junction solar cell was considered the best candidate for this application. The CESI photovoltaic unit is entirely envisioned for space applications and is fully qualified for

LEO and GEO orbits according to standard ECSS E ST20-08C. Table 2 shows the performance data of a single CTJ30 dollar cell.

Table 2 – Average electrical output parameters @AM0, 1367 W/m2 , T=25℃.

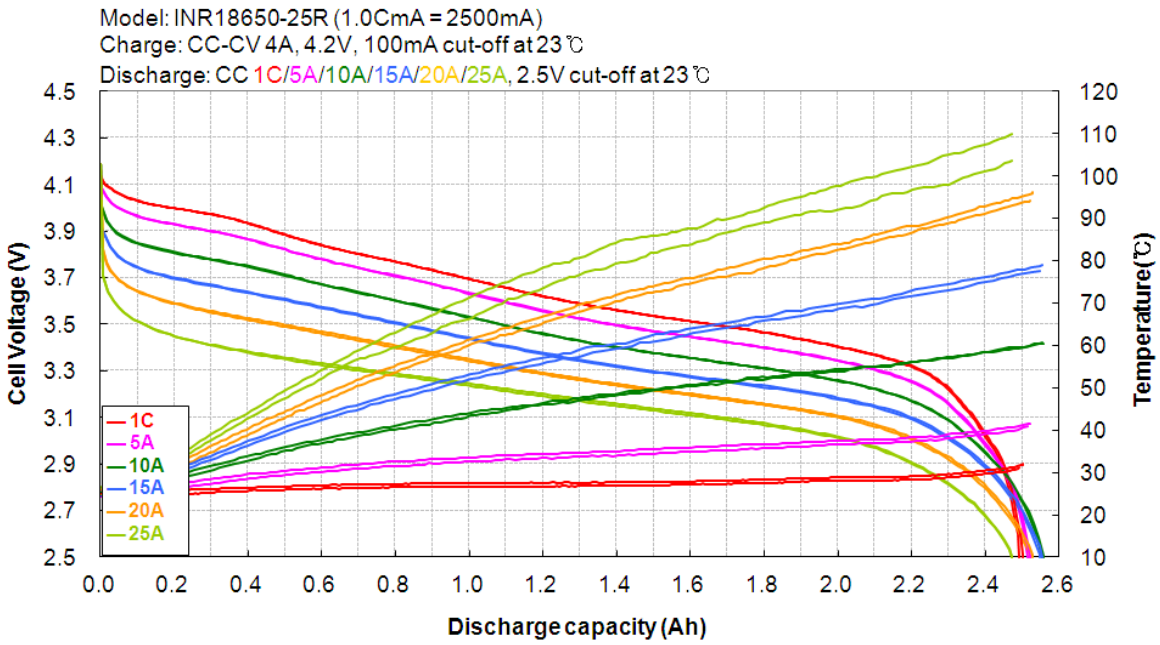
$Area[cm^2]$	$I_{SC}[mA]$	$V_{OC}[V]$	$I_m[mA]$	$V_m[V]$	$P_{max}[W]$	$Eff[\%]$
30.15	538	2.61	517	2.33	1.20	29.0

Source: (TRIPLE-JUNCTION. . . , 2020)

5.2 BATTERY PACK

The EPS battery pack comprises four Samsung INR18650-25R Li-Ion battery cells, which is one of the most widely adopted 18650 batteries on the market. The nominal charge capacity of each battery is 2500 mAh with a maximum continuous discharge current of 20 A. Its nominal voltage is 3.6 V, the maximum voltage is 4.2 V, and the cutoff voltage can be as low as 2.5 V. The battery pack was connected in a 2 series 2 parallel (2s2p) configuration for higher voltage and charge capacity ratings, 8.4V and 5000 mAh respectively.

Figure 15 – Single battery cell discharge characteristics.



Source: (INR18650-25R. . . , 2013)

As the depth of discharge (DoD) greatly impacts the life cycle of a Li-ion battery cell, it was decided never to discharge them to less than 55% of their full capacity.

This means a DoD of 0.45 and a charge capacity of 1.125 mAh. Considering the 10 A continuous discharge current of the cell voltage versus discharge capacity characteristic of the battery, which is shown in Figure 15, it was determined that the voltage of each battery cell could never be lower than 3.5 V. Consequently, for the given battery pack configuration, it was established that the range of the EPS bus voltage rail should be always between 7.0 V and 8.2 V.

It is important to mention, however, that different DoD values can be used depending on the mission-specific requirements.

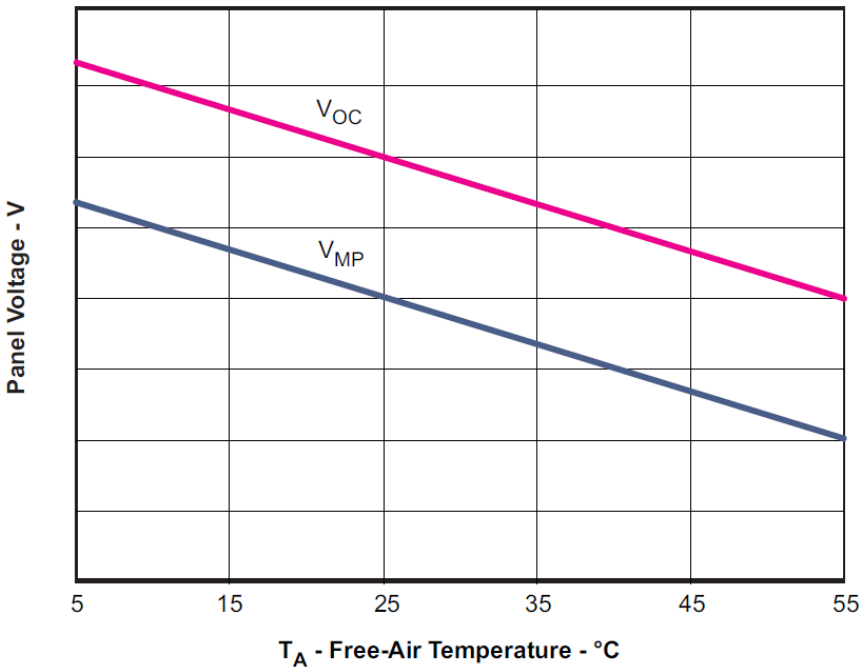
5.3 STANDALONE BATTERY CHARGER WITH MPPT

DET topologies can exhibit high reliability but they are not very commonly used because they suffer from low energy harvesting efficiency. Nowadays, most topologies employ some kind of MPPT strategy, which consists in tracking and adjusting the PV panel output voltage so that it harvests the most energy regardless of temperature and radiance variations. These techniques are usually implemented with the help of an algorithm that runs on a microcontroller and uses voltage/current/temperature readings to make the respective voltage adjustments.

Naturally, it is a lot more difficult to implement an MPPT algorithm without an EPS-dedicated microcontroller. Although it can be done using only analog parts, such an approach causes a significant increase in the number of components and complexity of the architecture. Therefore, after a careful benefit-risk assessment, it was decided to use a standalone, highly integrated, solar input, synchronous Buck battery charge controller, which implements a very simple MPPT method and exhibits an input voltage operating range of 5 V to 28 V.

The BQ24650RVAT is manufactured by Texas Instruments and uses a constant voltage MPPT strategy. This means that the battery charger automatically adjusts the charge current to maintain its converter input voltage at a resistor-programmed value, which guarantees the solar panels are operated at their maximum power point throughout the battery charging process. The caveat of this method is that the voltage of maximum power (V_{MP}) in a PV panel is greatly affected by temperature variations. For this reason, the battery charger also features an external MPPT temperature compensation circuit, which based on the temperature-independent relationship between the open-circuit voltage (V_{OC}) and V_{MP}, uses the V_{OC} variation rate as a reference to reprogram the battery charger input voltage value. In specific terms, as the temperature coefficient of a PV panel V_{OC} is similar to that of a common p-n diode ($\simeq -2mV/^{\circ}C$), an LM321 3-terminal current source is used to track this characteristic, creating a linear temperature-dependent current to compensate for the negative temperature coefficient of the solar panel (BQ24650. . . , 2020). Figure 16 exhibits how the difference between V_{OC} and V_{MP} is roughly constant throughout the battery's temperature operating range.

Figure 16 – Temperature-independent correlation between V_{OC} and V_{MP}.



Source: (BQ24650. . . , 2020)

Besides controlling the panels' output voltage for maximum solar energy harvesting, the BQ24650RVAT also implements all the functions expected from a conventional battery charger. It supports batteries from 2.1 *V* up to 26 *V* using a feedback voltage reference of 2.1 *V*. The charging process happens in three phases, namely, pre-charge, constant current, and constant voltage. The pre-charge is intended to revive deeply discharged cells. During this phase, the battery is charged with 1/10 of the fast charge current for 30 minutes. After this period the battery voltage level must be higher than a given threshold, otherwise, a fault is indicated in an external status signal. The constant current is the phase where the battery exhibits a lower resistance and, for this reason, is characterized by a fast charging current. An external sense resistor R_{SR} is used to define the fast-charging current level that should be set in accordance with the selected battery ratings. As the battery voltage increases, the constant voltage charging method is used to prevent the battery from overcharging. During the third phase, the charging current drops gradually from the fast charge level to the charge termination current level, which serves as a threshold to determine that the battery was fully charged. An open drain charge status output is used to indicate that the charge is complete. When the battery voltage falls below the recharge threshold, this charge cycle initiates again.

The integrated switch-mode battery charge controller is a synchronous 600 *kHz* constant-frequency Buck topology with high-accuracy current and voltage regulation. Depending on load demands, the controller can operate in either continuous conduction

mode (CCM) or discontinuous conduction mode (DCM). Associated with the pulse-width modulated (PWM) control logic, the highly integrated BQ24650RVAT features an internal level shifter, and two gate drivers, allowing for the use of external high-side and low-side N-Channel power switches. The choice of all the external components, including the inductor, input and output capacitors, compensations network, and power switches, was entirely based on the methodical COTS selection presented earlier. The selected N-Channel transistor was the Vishay Si7414DN-T1-E3, which is a 60 V PWM optimized trench FET of 25 $m\Omega$ $R_{DS(ON)}$ resistance, 8.7 A continuous drain current, and 800 pF input gate capacitance.

Besides the aforementioned advantages, the most determining factor for the selection of the BQ24650RVAT was its relevant track record in the aerospace industry. In a nutshell, the battery charger exhibits good radiation test data for LEO missions (FAIRBANKS et al., 2013) and has recently been selected by NASA for use in its 6U CubeSat project, PACE-2 (NGUYEN, 2022).

5.4 POL BUCK CONVERTERS

Both the 5.0 V, and the 3.3 V PoL Buck converters were designed using the Linear Technology LTC3833 step-down controller. Two key characteristics drove the controller's selection: high radiation tolerance and GaN high-electron mobility transistor (HEMT) support. In terms of radiation tolerance, in the Large Hadron Collider at CERN, the controller demonstrated great resistance to SEEs, total ionizing dose (TID), and strong magnetic field (ABBATE et al., 2014). Full support to GaN transistors was also considered an important aspect in this selection because the technology has long been considered an extraordinary promise for LEO space applications. When compared to ordinary MOSFETs, GaN transistors exhibit lower $R_{DS(ON)}$ resistance and are able to operate at much higher frequencies. This characteristic can potentially increase the converter's efficiency and reduce its footprint (DE SANTI et al., 2018; LI et al., 2016). Furthermore, due to their structure and material properties, GaN devices are inherently resistant to radiation. Recent tests conducted at NASA Jet Propulsion Laboratory JPL have shown that they are resistant to both radiation-induced TID and SEEs (TSAO et al., 2018; SCHEICK, 2014).

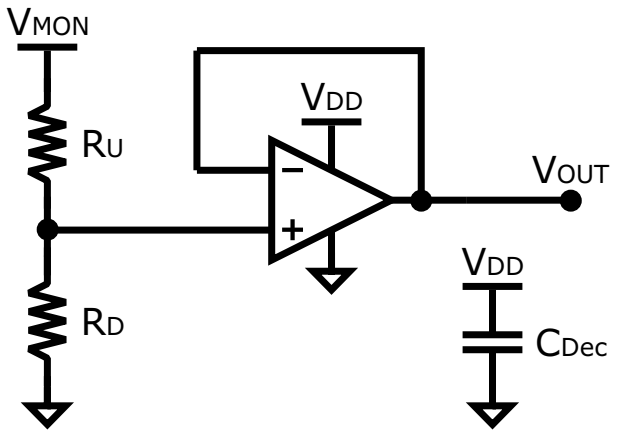
Regarding its electrical characteristics, the controller exhibits a wide input voltage range of 4.5 V up to 38 V. Its switching frequency is externally programmable and can be set at any given value between 200 kHz and 2 MHz. The output voltage can be easily configured to both 3.3 V and 5.0 V, with an accuracy of $\pm$ 0.67% over the entire temperature range of operation. Furthermore, the LTC3833 features over-voltage/overcurrent protections to prevent damage from voltage surges/current spikes. Power good output and enable input signals are also available, facilitating the implementation of redundancy. The low-side and high-side power switches of the Buck converters

are two EPC2016C enhanced-mode GaN transistors. A 10 A, 100 V device that features a $R_{DS(on)}$ resistance of 12 mΩ and is especially recommended for high-speed DC-DC conversion.

5.5 VOLTAGE MONITORING CIRCUITS

As shown in Figure 17, the voltage monitoring circuits are composed of a resistive voltage divider, an operational amplifier in a voltage follower configuration, and a decoupling capacitor. The circuit operation is very straightforward, the resistive divider takes a sample of the monitored voltage, and the amplifier buffers the signal, which is then sent to the OBDH micro-controller after passing through the multiplexer. The resistors values were calculated in such a way that when the monitored voltage is at its expected level, the output is equal to 2 V. This gives room for the OBDH to detect any unexpected voltage behavior, either going up or down.

Figure 17 – Circuit diagram of the voltage monitors.



Source: Author, 2023

In addition, a lower boundary was established for the resistor values, so that they never drain more than 150 μA of current.

$$V_{OUT} = \frac{V_{MON} R_D}{R_D R_U} \tag{7}$$

$$R_D + R_U > \frac{V_{MON(MAX)}}{150 \mu A} \tag{8}$$

The operational amplifier is the LMV321RIYLT, which is manufactured by Texas Instruments and was selected based on previous radiation test data (DAVIS et al., n.d.). The record shows that when three samples of this part were submitted to heavy ions and protons tests for SEEs, none of them failed. Furthermore, this opamp features an

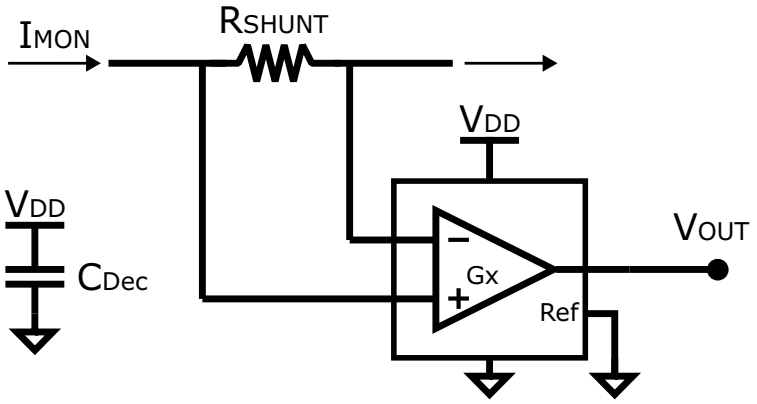
extended input voltage common mode range, rail-to-rail input and output, 1 *MHz* gain bandwidth product, and a supply current as low as 145 μA. The resistors used in the voltage divider are both from the Vishay CRCW-HP series, feature a 1% tolerance, a 100 *ppm*/*C* temperature coefficient, a 75 *V* voltage rating, and are AEC-Q200 qualified.

Altogether, five units of this monitoring circuit were strategically positioned in the architecture to make sure all voltage buses are behaving properly. Based on the readings of these circuits, the OBDH microcontroller can take preventive actions, such as disconnecting loads and activating redundant circuits.

5.6 CURRENT MONITORING CIRCUITS

As shown in Figure 18, the current monitoring circuits are composed of a high-precision shunt resistor, a current-sense amplifier, and a decoupling capacitor. In simple terms, the circuit behaves as a current-to-voltage converter. The current that passes through the shunt resistor creates a voltage drop that is read by the amplifier and multiplied by its internal gain.

Figure 18 – Circuit diagram of the current monitors.



Source: Author, 2023

Equation (9) depicts how the shunt resistor values were calculated. To solve the equation it was attributed that the output voltage V_{OUT} should be equal to 2 *V* when the monitored current is at its maximum level.

$$R_{SHUNT} = \frac{V_{OUT}}{I_{MON} G_{AIN}} \tag{9}$$

This gives room for the OBDH to detect any unexpected current behavior, either going up or down. The current sense amplifier is the INA199C3DCKR, which is manufactured by Texas Instruments, and was selected based on its radiation tests data (DAVIS et al., 2019). The records show that this part has been submitted to SEEs tests

using heavy ions and protons and did not present any failure condition. In terms of features, the amplifier offers a wide common-mode voltage range, which allows it to sense both low-side and high-side currents. Its maximum gain error is lower than $\pm 1\%$, its quiescent current does not exceed 100 μA and, to facilitate the selection of the shunt resistor, three different fixed voltage gains are available: 50 V/V, 100 V/V, and 200 V/V.

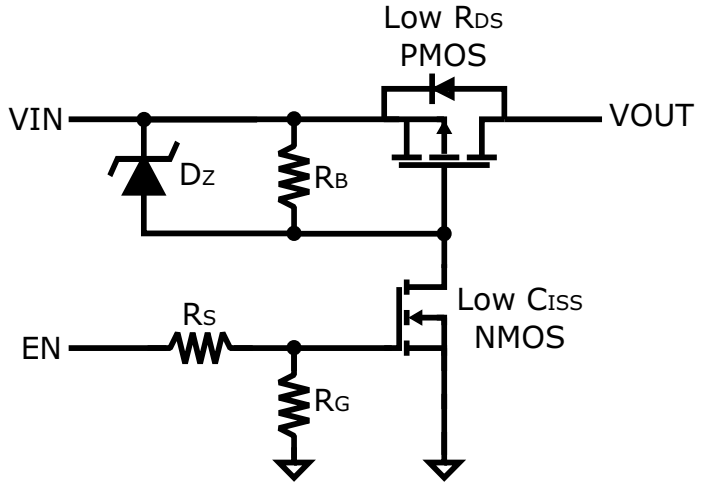
All the high-precision shunt resistors are from the Vishay WSL series, feature a 1% tolerance, a 75 ppm/℃ temperature coefficient, a 0.5 W power rating, and are AEC-Q200 qualified. As shown in Figure 12, eleven current monitoring circuits were conscientiously distributed in the architecture to ensure the proper operation of the EPS. Lastly, as in the voltage monitoring circuits, the amplifier's output is sent to a multiplexer and then to the OBDH microcontroller, which keeps track of all these readings and can take preventive actions on the fly.

5.7 HIGH-SIDE SWITCHES

The high-side switches are low $R_{DS(on)}$ PMOS transistors that are used to connect/disconnect loads to the PoL converters. As their input voltage rail is not the same as the rail of their enable signals, which should come from the OBDH microcontroller, a low gate capacitance NMOS is used in association with a resistor and a Zener diode to ensure the proper biasing and control of the PMOS switch. As shown in Figure 19, two more resistors were added to the topology at the gate of the NMOS. R_S is a series resistor that is used to limit the current sourced from the microcontroller when the NMOS is being turned on, and R_G is a pull-down resistor that is used to discharge the gate capacitance and to ensure that all loads will be connected when there is no enable signal available to control the switch.

The NVTFS5116PLTAG vertical trench-gate style, manufactured by Onsemi, was deemed the best PMOS COTS candidate for the high-side switches application. Besides being included in the GSFC database, its radiation test results show that, for VDS voltages not lower than –30 V, it can be safely used in the majority of the space radiation environments (LAUENSTEIN et al., 2017). In addition, this automotive-grade transistor is AEC-Q101 qualified, supports –14 A of continuous drain current, and exhibits a $R_{DS(on)}$ resistance of 52 $m\Omega$. For the gate control role, based on its good radiation test data (BOLEY, 2008), it was decided to use the SI2302DDS NMOS transistor. A device that is manufactured by Vishay, exhibits 320 pF of input gate capacitance, and 0.6 V of threshold voltage. Both characteristics that are essential to implement the respective function.

Figure 19 – Circuit diagram of the high-side load switch.



Source: Author, 2023

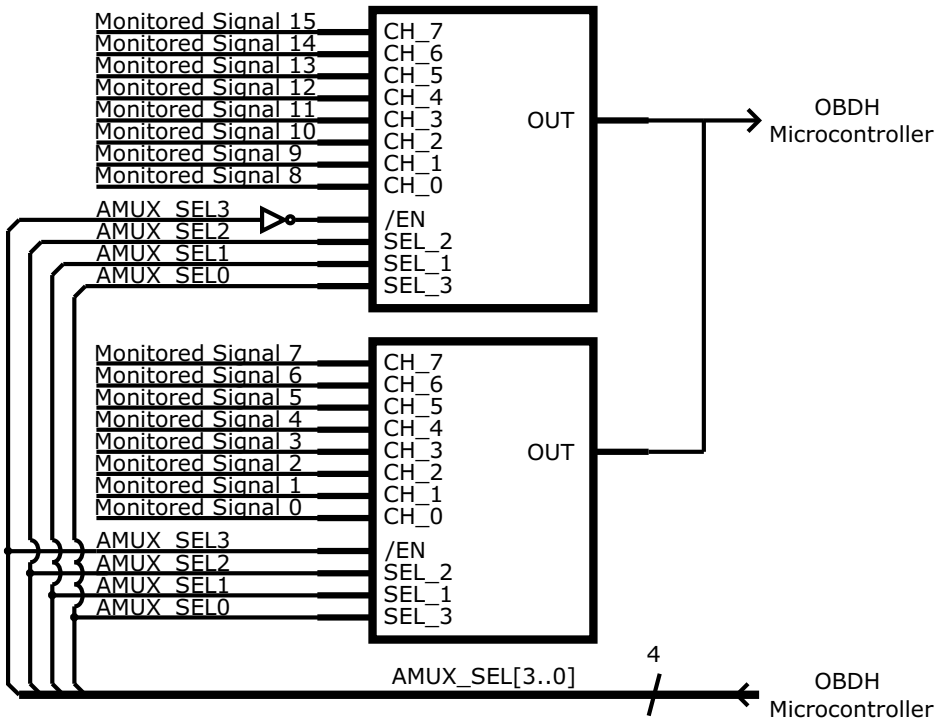
5.8 ANALOG MULTIPLEXER

To reduce the number of wires going out of the EPS and facilitate the interface with the OBDH microcontroller, it was determined that all the monitored signals should be made available through a 16:1 digitally controlled analog multiplexer. Given the lack of a candidate that would satisfy the COTS selection criteria of this project, it was considered to use an association of two 8:1 analog multiplexers instead. After a throughout research, the selected part was the CD4051BPWR, an 8-channel analog multiplexer made by Texas Instruments. The selection decision was predominantly made based on the part's high radiation tolerance. In recent tests, two samples of this part were submitted to heavy ions and protons and did not present any destructive failure or degradation in their performance (DAVIS et al., 2019). The second reason for choosing the CD4051BPWR is that it features a disable pin which, with the addition of an inverter, can be used as a fourth input control pin, making it possible to easily transform two 8-channel multiplexers into a 16-channel multiplexer. Figure 20 depicts in detail how the two multiplexers were connected. Lastly, it is also important to highlight that the CD4051BPWR consumes an extremely low quiescent current, that can be as low as 40 *nA* at ambient temperature.

5.9 SEPARATION SWITCHES

To prevent unintentional activation, the EPS architecture features two remove-before-flight (RBF) pins, two deployment switches, and two separation switches. Each separation switch consists of two PMOS transistors, that are connected in parallel to

Figure 20 – Circuit diagram of the 16:1 analog multiplexer.



Source: Author, 2023

reduce their $R_{DS(on)}$ resistance and lower their conduction power losses. For the same reasons exposed in the high-side switches section, the NVTFS5116PLTAG was deemed the best PMOS COTS device for this application.

For more detailed information on hardware implementation, circuit topologies, and components values, please refer to the PCB schematic diagram presented in Appendix A. The PCB layout will follow guidelines and rules to reduce risks associated with both electromagnetic compatibility (EMC) and electromagnetic interference (EMI), which were already developed and validated by the SpaceLab research group (RIGO, Cezar Antonio et al., 2020) and (D. J. BHATT ARUN BINDAL, 2019).

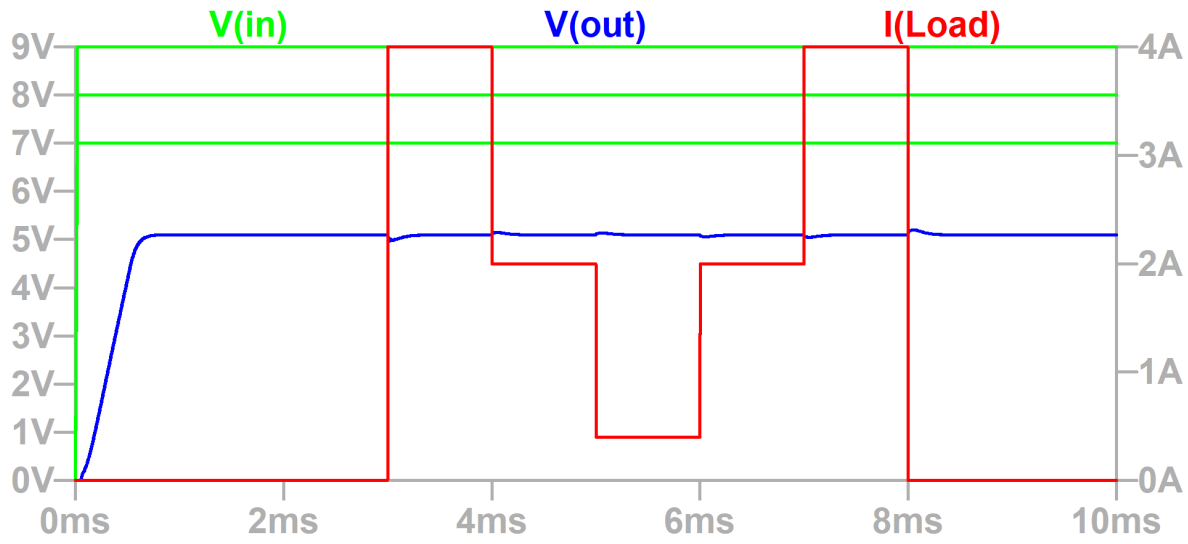
6 CIRCUIT SIMULATIONS

This section presents the main SPICE circuit simulations that were carried out to validate the functionality and verify the performance of the enhanced reliability EPS.

6.1 5.0 V POL CONVERTER

The efficiency and stability of the 5.0 V Buck converter were verified through parametric time domain simulations. To check the control loop stability, fast load steps of rise/fall time much lower than the inverse of the converter's unity gain frequency ($T_r = T_f << 1/F_c$) were applied to the converter's output. In this way, the control loops could be excited over a sufficiently wide frequency range, highlighting not only loop stability problems, but also slope compensation and load regulation issues. As shown in Figure 21, after the power-up period, six load steps (0-100%, 100%-50%, 50%-10%, 10%-50%, 50%-100%, and 100% to 0% of the maximum load) of 1 *ns* rise/fall time were applied to emulate the worst-case load scenarios. The average efficiency of the converter was calculated for each of the loads. In addition, the input voltage was parameterized to cover the entire EPS bus voltage range, as defined in accordance with the battery cell specifications. Therefore, the same simulation was run for input voltages of 7.0 *V*, 8.0 *V*, and 9.0 *V*.

Figure 21 – Transient simulation waveform of the 5.0 V Buck converter.



Source: Author, 2023

Table 3 shows the converter's efficiency for each simulated input voltage and load condition.

Table 3 – 5.0 V Buck converter efficiency.

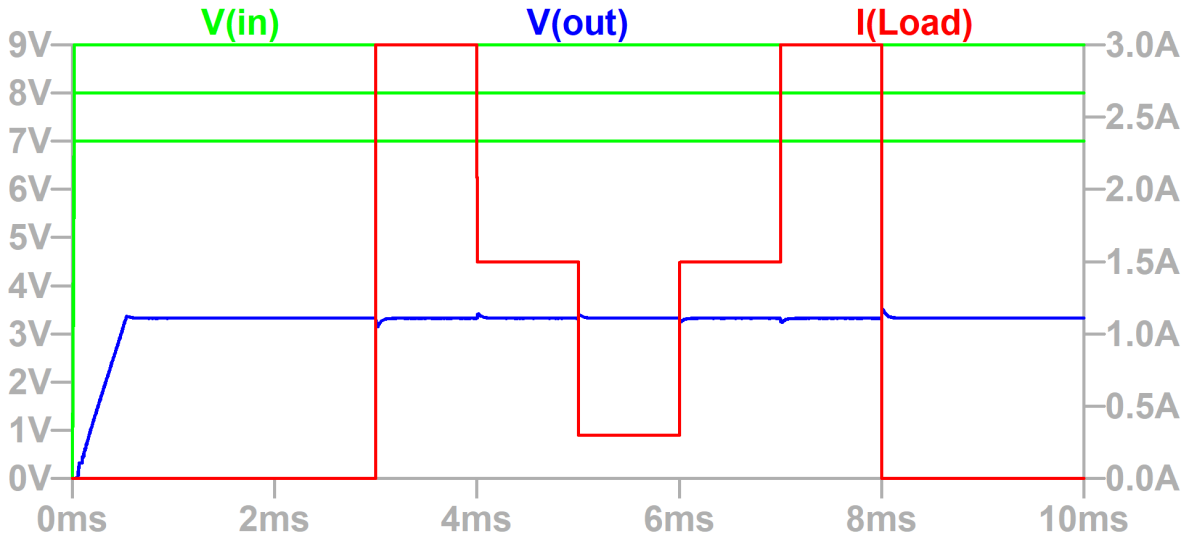
Input voltage [V]	**Output current [A]**	**Efficiency [%]**
7.0	0.4	98.2
	2.0	98.1
	4.0	97.1
8.0	0.4	98.5
	2.0	97.9
	4.0	97.2
9.0	0.4	98.5
	2.0	97.8
	4.0	97.3

Source: Author, 2023

6.2 3.3 V POL CONVERTER

The 3.3 V Buck converter performance was evaluated using the same simulation procedure that was used for the 5.0 V Buck converter. The only difference is that its maximum output current is 3.0 *A* instead of 4.0 *A*, as per specifications. Load step rates and rise/fall times were kept the same. Figure 22 shows the 3.3 V PoL converter simulation waveforms and Table 4 shows its efficiency for each simulated input voltage and load condition.

Figure 22 – Transient simulation waveform of the 3.3 V Buck converter.



Source: Author, 2023

Table 4 – 3.3 V Buck converter efficiency.

Input voltage [V]	Output current [A]	Efficiency [%]
7.0	0.3	96.2
	1.5	97.0
	3.0	95.9
8.0	0.3	96.3
	1.5	96.4
	3.0	96.0
9.0	0.3	95.4
	1.5	96.3
	3.0	96.0

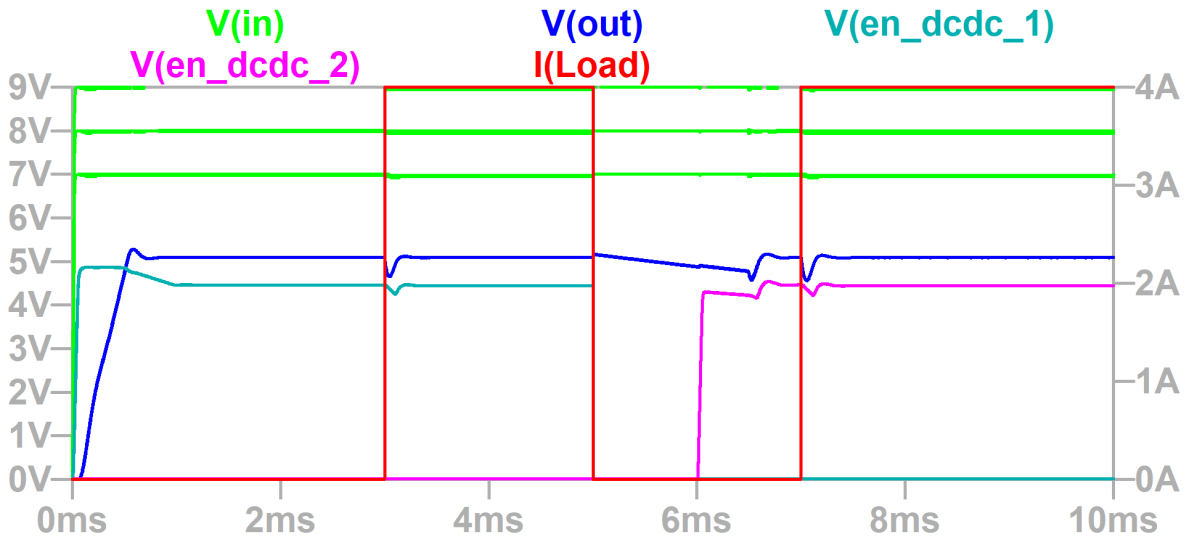
Source: Author, 2023

6.3 STANDBY REDUNDANCY ACTIVATION

Time-domain simulations were also performed to validate the activation mechanism of the standby redundant 5.0 V Buck converter. The simulation sequence intended to emulate a real scenario and consisted in the following steps: a) Primary converter is powered-on; b) 4.0 *A* load current is connected; c) Assuming a disturbance is detected, the load is disconnected; d) Primary converter is disabled; e) Secondary converter is enabled; f) 4.0 *A* load current is reconnected.

The same simulation was run for input voltages of 7.0 *V*, 8.0 *V*, and 9.0 *V*. Figure 23 shows the simulations waveforms.

Figure 23 – Transient simulation waveform of the 5.0 V standby Buck converter activation method.



Source: Author, 2023

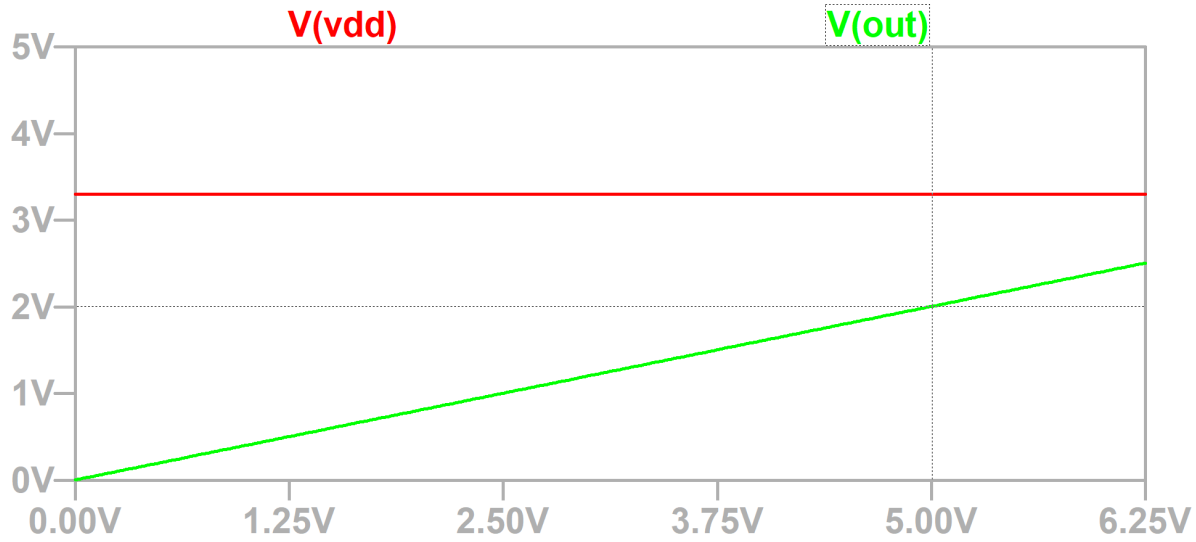
It is important to mention that the firmware required for the OBDH microcontroller

to implement the standby redundancy is not within the scope of this study. The simulation presented above aims to demonstrate how the mechanism is supported from the hardware point of view. The exact same activation mechanisms are used for both the redundant 3.3 V Buck converter and the MPPT battery charger.

6.4 VOLTAGE MONITORING CIRCUITS

DC and time-domain simulations were performed to validate the functionality of the voltage monitoring circuit topology. The DC analysis was used to verify the resistive voltage divider ratio and the opamp rail-to-rail input/output capabilities. Basically, it consisted in performing an input voltage sweep (voltage to be monitored) from zero to its maximum value, so that the buffer output could be examined. Figure 24, shows the DC simulation waveform of the 5.0 V voltage monitoring circuit, which is used to measure the 5.0 V Buck converter output. As it can be observed, the circuit was designed in such a way that when the monitored voltage is at 5.0 V the output voltage is at 2.0 V. The DC sweep was run from 0 to 6.25 V using a voltage step of 25 mV.

Figure 24 – DC simulation waveform of the 5.0 V voltage monitoring circuit.

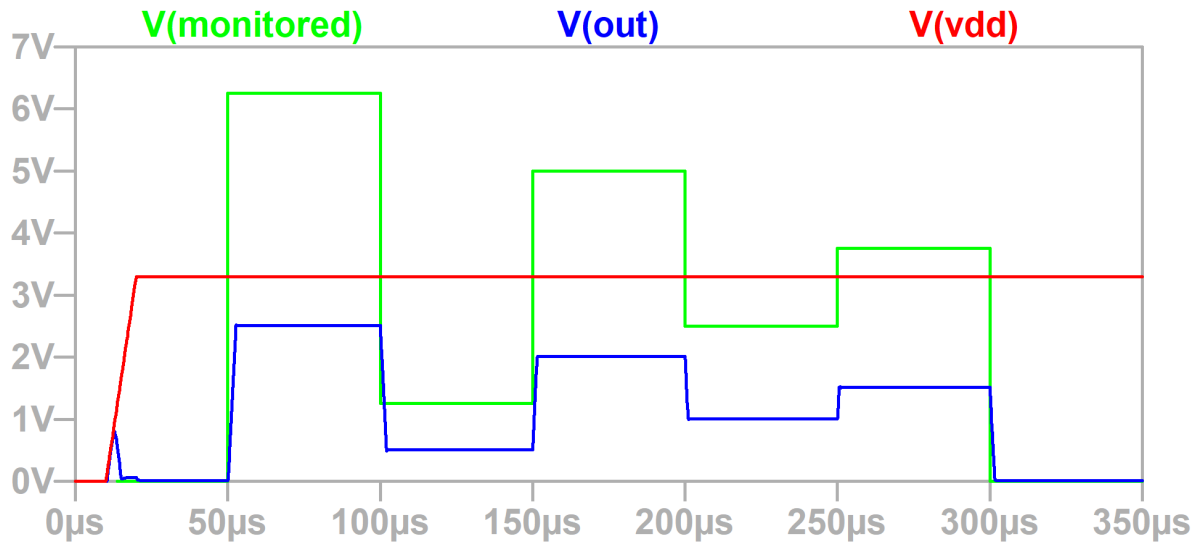


Source: Author, 2023

The time-domain analysis was used to verify the power-on process and the slew rate of the voltage monitoring circuit. The simulation consisted in initializing the circuit and then applying six sudden voltage steps to the monitored rail. Each voltage step was 50 μs long with a rise/fall time of 1 ns. Thus, it was possible to examine how fast the output buffer responds to voltage disturbances. As shown in Figure 25, the voltage steps were applied in the following sequence: 0 – 6.25 V, 6.25 – 1.25 V, 1.25 – 5 V, 5 – 2.5 V, 2.5 – 3.75 V, and finally 3.75 – 0.0 V.

As all other voltage monitoring circuits use the same topology, for the sake of brevity, it was not considered necessary to include their simulation results.

Figure 25 – Transient simulation waveform of the 5.0 V voltage monitoring circuit.



Source: Author, 2023

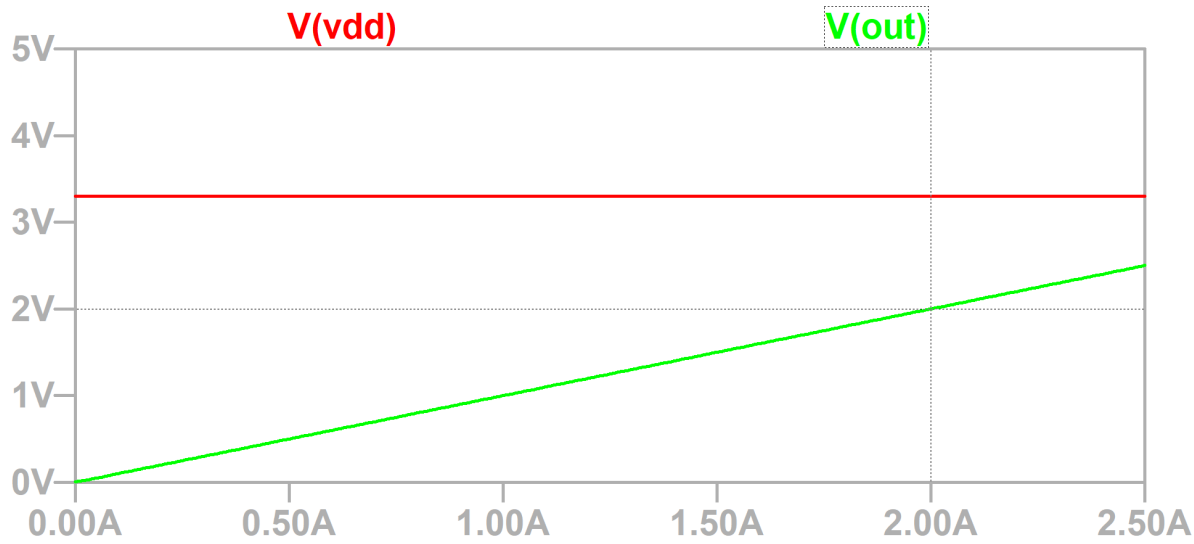
6.5 CURRENT MONITORING CIRCUITS

DC and time-domain simulations were also performed to validate the functionality of the current monitoring circuit topology. The DC analysis was mainly used to verify the gain and the common-mode input range capabilities. Essentially, it consisted in performing a current sweep (current to be monitored) from zero to its maximum value, so that the current sense amplifier could be examined.

Figure 26, shows the DC simulation waveform of the 2.0 A current monitoring circuit, which is used to measure the nanosatellite payload current. As can be observed, the circuit was designed in such a way that when the monitored current is at 2.0 A the output voltage is at 2.0 V. The DC sweep was run from 0 to 2.5 A using a current step of 25 mA.

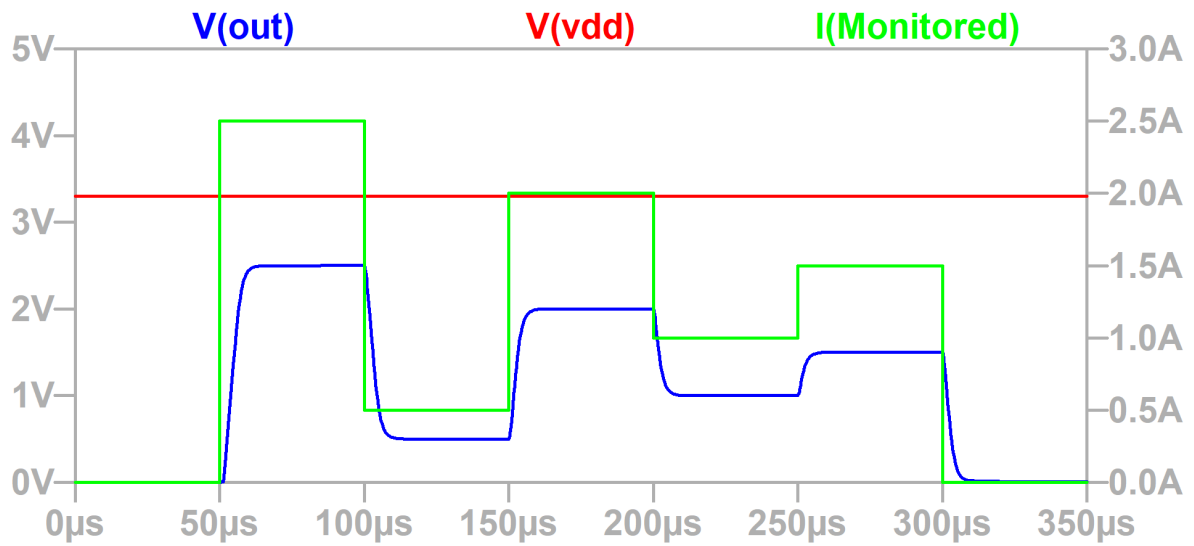
The time-domain analysis was used to verify the power-on process and the slew rate of the current sense amplifier. The simulation consisted in initializing the circuit and then applying six sudden current steps to the monitored load. Each load step was 50 us long with a rise/fall time of 1 ns. Thus, it was possible to examine how fast the amplifier responds to current disturbances. As shown in Figure 27, the current steps were applied in the following sequence: $0-2.5\,A$, $2.5-0.5\,A$, $0.5-2.0\,A$, $2.0-1.0\,A$, $1.0-1.5\,A$. and finally $1.5-0.0\,A$. As all other current monitoring circuits use the same topology, for the sake of brevity, it was not considered necessary to include their simulation results.

Figure 26 – DC simulation waveform of the 2.0 A current monitoring circuit.



Source: Author, 2023

Figure 27 – Transient simulation wavefrm of the 2.0 A current monitoring circuit.



Source: Author, 2023

7 RELIABILITY EVALUATION AND COMPARISON

7.1 RELIABILITY METRICS

To quantify the reliability of the EPS architecture and establish a method for comparing it with other topologies, a three-metric evaluation system is proposed. In this system, each metric is equally weighted using a zero (0) to three (3) rating scale and the final reliability rating is calculated by summing the ratings obtained in each of the metrics. As might be expected, zero (0) represents the lowest reliability level and nine (9) represents the highest.

The three metrics along with their (0) to (3) rating scales are described in detail in the subsections below.

7.1.1 Dedicated Processor

As detailed in Chapter 2, the microcontroller is the component that most affects the reliability of an EPS. For this reason, it is pertinent to use it as a reliability metric. The *dedicated processor* 0 to 3 rating scale is defined as follows: (0) ordinary COTS processor, (1) COTS processor with radiation test data or space flight heritage, (2) radiation-hardened processor, and (3) no dedicated processor.

7.1.2 Single points of failure - SPoF

A SPoF is an individual fault/malfunction that leads the entire system to fail. It is usually characterized by a point/component of the design that is vital to the subsystem operation and has no redundancy or circuit support to outweigh its failure effects. Every SPoF poses a potential risk to an EPS architecture and, for this reason, it can be used as a reliability metric. Passive components, such as current sensing resistors and decoupling capacitors do not need to be taken into account because their failure rates are not significant when operated under proper and derated biasing conditions (SINCLAIR; DYER, 2013). Power bus interfaces also do not need to be considered because most EPS failures cannot be attributed to them (BOUWMEESTER, Jasper; LANGER, Martin; GILL, 2017). The *SPoF* 0 to 3 rating scale is defined as follows: (0) more than five SPoF, (1) five to three SPoF, (2) two or one SPoF, and (3) no SPoF.

7.1.3 Hardware Architecture

Although the series/parallel connection metric introduced in (HUSSEIN; MASSOUD; KHATTAB, 2022) and briefly described in Chapter 2 can be helpful in some cases, it is not always applicable because it does not define a way for calculating the reliability of a system that features standby redundant components. A more in-depth study on this subject (RAY, 2002b), used the same mathematical principles to define

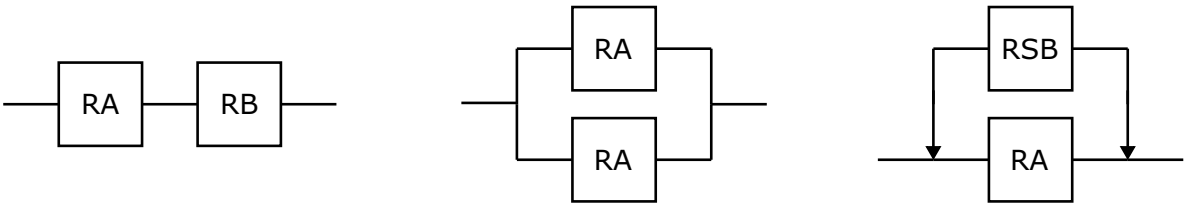
not only the probability of success (reliability) of systems featuring series and parallel components but also of those featuring active and standby redundant components. Initially, the work defines the reliability (R_X) of a given component in terms of failure rate and operation time, making a distinction between non-continuous and continuous operation components, as shown in equations (10) and (11) respectively.

$$R_X(t) = e^{-\lambda_1 t} \tag{10}$$

$$R_X(t) = e^{-\left[\lambda_1 td + \lambda_2 t(1-d)\right]} \tag{11}$$

Where λ_1 is the failure rate during the operation, λ_2 is the failure rate during non-operation, and d is the duty cycle factor, which is the ratio between operation time and total mission time.

Figure 28 – Basic reliability block diagrams.



a) Series components

b) Active redundancy components

b) Standby redundancy components

Source: Author, 2023

Building on this, the work defines the reliability of a system (R_S) based on how its components are connected. Figure 28 shows the most commonly encountered reliability block diagrams (RBD), including series components, active redundant components, and standby redundant components (which is a particular case of the parallel connection). The reliability of each system RBD (a, b, c, depicted in Figure 28) is then given by equations (12), (13), and (14), respectively.

$$R_S = R_A R_B \tag{12}$$

$$R_S = 2R_A - R_A^2 \tag{13}$$

$$R_S = R_A \left[1 + \frac{1-(R_A)^Q}{Q}\right] \tag{14}$$

Where Q is a constant defined by the failure rate of the standby component (λ_S) divided by the failure rate of the active component (λ_A).

$$Q = \frac{\lambda_{SB}}{\lambda_A} \tag{15}$$

It is essential to clarify, however, that an RBD is not the same thing as an electrical circuit block diagram. Actually, it is a visual representation of how the components of a system are reliability-wise related, regardless of how they are electrically connected or positioned in the design. For example, when the failure of a single component leads the entire system to fail, this component must be represented by a series connection, on the other hand, when the system is operating if at least one of *n* components is operating, these components must be represented by a parallel connection. Therefore, once the RBD of an EPS architecture is drawn, it is possible to calculate its reliability using the three aforementioned equations.

Another important aspect of this metric is that in order to differentiate between the reliability of the architecture (which concerns the number of components and how they are connected) and the reliability of the components themselves, it must be considered that all components exhibit the same individual failure rate at the same time. Otherwise, the high individual-component reliability of given components could potentially mask the weaknesses of an architecture, giving the false impression that one architecture is better than the other when this is not the case. The *hardware architecture* 0 to 3 rating scale is defined as follows: (0) probability of success lower than 70% (1) probability of success between 70% and 80%, (2) probability of success between 80% and 90%, and (3) probability of success higher than 90%.

Additionally, to ensure the reliability of a given design, it is important to calculate its absolute reliability, using the different individual reliability of each component to solve the RBD equation. These values can be obtained from statistical analysis of component-level failure tests and are usually provided by the component manufacturers. Otherwise, a high-reliability EPS architecture could potentially yield a low-reliability solution due to the overlooked low-reliability of its individual components. Such analysis is out of the scope of this work as it would require obtaining reliability data on all the components of each architecture, which in many cases are not easily accessible or disclosed.

7.2 METRICS APPLICATION

The application of the three-metric evaluation system is demonstrated using different architectures. Specifically, the *Reliability Enhanced EPS* (hereinafter referred to as FloripaSat-2), the FloripaSat-1, and the NanoPower P31U. The rating of the EPSs according to each of the three metrics is demonstrated below.

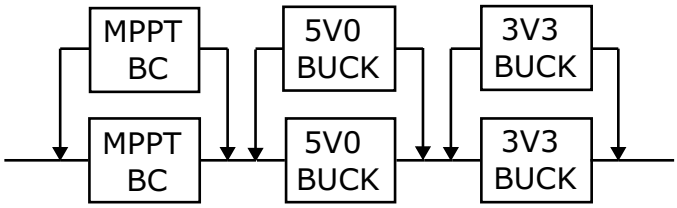
Dedicated processor: Preliminary project reviews and part number inspections were required to perform the *dedicated processor* rating.

- FloripaSat-1: Features the Texas Instruments MSP430F6659IPZR, which is a 16-bit ordinary COTS microcontroller
- FloripaSat-2: Features no dedicated microcontroller
- NanoPower: Features a COTS microcontroller with space flight heritage

Single points of failure - SPoF: A detailed electric circuit block diagram review was required to identify the SPoF of each architecture and rate them in accordance with this metric. Besides passive components and power bus interfaces, separation switches were also not taken into account as they are featured in all three architectures. With these assumptions in place, it was found that the FloripaSat-2 EPS exhibits no SPoF, the FloripaSat-1 EPS exhibits three SPoF, and the NanoPower EPS exhibits three SPoF.

Hardware architecture: To calculate the reliability and rate each EPS in accordance with the *hardware architecture* metric it was first necessary to draw their RBDs. To solve the RBD equations and ensure they would be effective in determining the most reliable hardware architecture, ruling out any unique component reliability biases, the same individual-component reliability of 0.95 was attributed to every internal components

Figure 29 – Reliability block diagram of the proposed FloripaSat-2 EPS.



Source: Author, 2023

Then, using the RBD shown in Figure 29, the reliability of the FloripaSat-2 was calculated as follows:

$$R_{S(FSat2)} = \left(2R_{BC} - R_{BC}^2\right)\left(2R_{5V0} - R_{5V0}^2\right)\left(2R_{3V3} - R_{3V3}^2\right) \tag{16}$$

Where,

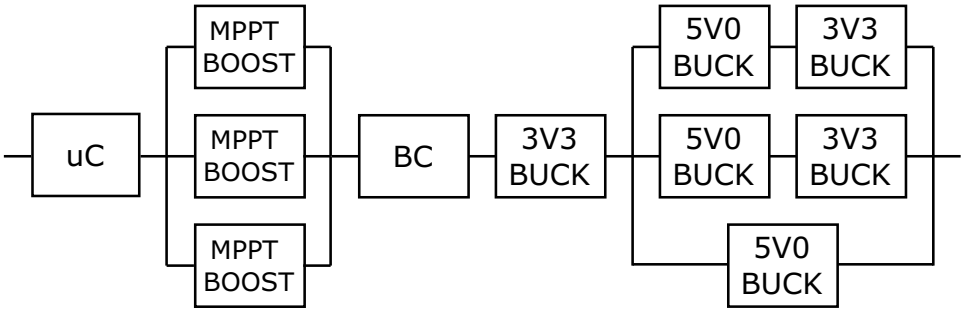
$$R_{BC} = R_{5V0} = R_{3V3} = R_A = 0.95 \tag{17}$$

Then,

$$R_{S(FSat2)} = \left(2R_A - R_A^2\right)^3 = 0.9925 \tag{18}$$

Similarly, using the RBD shown in Figure 30, the reliability of the previous FloripaSat EPS platform was calculated as follows:

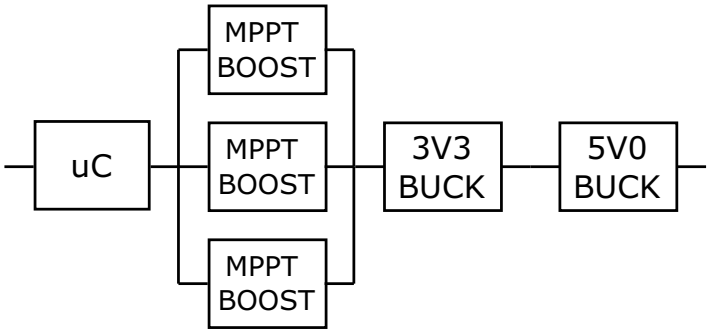
Figure 30 – Reliability block diagram of the FloripaSat-1 EPS.



Source: Author, 2023

$$R_{S(FSat1)} = R_A^3\left[1-\left(1-R_A\right)^3\right]\left\{1-\left[\left(1-R_A\right)\left(1-R_A^2\right)^2\right]\right\} = 0.8568 \tag{19}$$

Figure 31 – Reliability block diagram of the GomSpace NanoPower EPS.



Source: Author, 2023

Lastly, using the RBD shown in Figure 31, the reliability of the NanoPower EPS was calculated as follows:

$$R_{S(nPower)} = R_A^3\left[1-\left(1-R_A\right)^3\right] = 0.8572 \tag{20}$$

7.3 COMPARISON SUMMARY

Table 5 shows how each EPS was rated according to the three-metric reliability evaluation system. As it can be noted, this is a very effective method for spotting the weaknesses and strengths of any given architecture. For example, the FloripaSat-1 was found to be the least reliable architecture, primarily because it features a COTS microcontroller that has no recorded space flight heritage or radiation test data available.

Therefore, if someone intends to improve this architecture's reliability, upgrading its processing solution is certainly a head start. The ratings also revealed another significant point for improvement in the FloripaSat-1 and NanoPower EPSs. Both architectures exhibit three SPoF, which can potentially undermine their reliability. An effective way of reducing the risks associated with the SPoF without making major design changes is to ensure that only high-reliability components are featured at these points. Regarding the hardware architecture metric, all the EPSs were rated relatively well, however, depending on the reliability of their individual components and on the mission requirements, adjustments might have to be made to improve the RBD of the FloripaSat-1 and NanoPower architectures. Instead of reformulating the whole design, implementing redundancy could be a great alternative to reduce the number of series components and increase their system's probability of success.

Table 5 – EPS architectures reliability comparison.

Platform	**Hardware Architecture**	**SPOF**	**Dedicated Processor**	**Total**
FloripaSat-2	3	3	3	9
NanoPower	2	1	1	4
FloripaSat-1	2	1	0	3

Source: Author, 2023

Lastly, the summary of results clearly indicates that the techniques that were incorporated into the *Reliability Enhanced EPS* have made a major impact on its reliability level.

8 CONCLUSION

8.1 FINAL CONSIDERATIONS

This work presents an overview of the EPS reliability issue and of the EPS reliability-enhancing techniques that have been proposed in the past years. In view of the critical need for more practical and viable design alternatives, especially to be used in the FloripaSat-2 platform, a *Reliability Enhanced EPS* architecture was proposed. Four major techniques were incorporated into this architecture to improve its reliability. Namely, methodical COTS selection, processor-less design, passive redundancy, and load monitoring and control. Each of these techniques was thoughtfully chosen to improve reliability without compromising other design aspects, such as power consumption, cost, and board area. In addition, to ensure the viability of the project, three power reduction design strategies were also put in place. The entire proposal was supported by block diagrams, theoretical analysis, design equations, SPICE circuit simulations, and PCB schematic. Furthermore, given the significant role the EPS subsystem plays in the high number of nanosatellite mission failures, another relevant observation made from the state-of-the-art analysis, was the scarcity of well-established methodologies for evaluating and comparing the reliability of EPS architectures. In this regard, the study contributes to the literature by proposing a three-metric evaluation system, which is based on the most critical reliability aspects of an EPS. The applicability of the method was demonstrated by evaluating and comparing three different architectures: the one proposed herein, its previous version, and the NanoPower P31U, designed by GOMSpace. Comparison results confirmed the effectiveness of the reliability-enhancing techniques that were implemented. According to the three-metric evaluation system ratings, the proposed EPS features the most reliable architecture among the three candidates that were considered for this analysis. The standby redundancies, the removal of the dedicated microcontroller, and the elimination of SPoF yielded the *Reliability Enhanced EPS* a grade of 9 out of 9. While the NanoPower received a grade of 4, and the FloripaSat-1, a grade of 3. In terms of PoL converter's efficiency, this architecture also exhibits significant improvements when compared to its previous version. Circuit simulations have shown that the average efficiency of 5.0 V and the 3.3 V PoL converters are 98% and 96%, respectively. The innovative character of this study was demonstrated through its submission to the **IEEE Aerospace and Electronic Systems Magazine**, which is a high-impact factor journal in the subject area. In terms of relevance and application, the Brazilian's National Council for Scientific and Technological Development (CNPq), has recently approved an R$ 1 million funding, under Grant **407174/2022-2**, for the Federal University of Santa Catarina to develop and manufacture an entire nanosatellite to test and validate the *Reliability Enhanced EPS* in-orbit.

8.2 FUTURE WORK

The *reliability enhanced EPS* presented in this master thesis is an integral part of a CubeSat platform and for this reason, it has created opportunities for many future works. The layout, manufacturing, and assembly of the EPS board will be the immediate next steps, which will be followed by benchtop tests, radiation tests, and a throughout analysis of the obtained results. Other subsystems of this platform will also be redesigned for improved reliability and better performance, including the OBDH, the TTC, and others. Then, the focus will shift to the proper integration of the subsystems and preparation for launch. After this, in-orbit test results will be evaluated and a compilation of the lessons learned through this process will be made.

In terms of upgrades for the next versions, the proposed EPS architecture features a standalone battery charge controller that implements a constant voltage MPPT algorithm. Although this chip is extremely versatile, and the method is proven to work, it does not offer the best-known tracking accuracy, which can reduce the PV panels harvesting capabilities. Bearing this in mind, it is suggested that more research should be conducted and efforts should be made to implement a higher accuracy analog MPPT control. To reduce the complexity of the implementation, it is suggested that some functionalities should be leveraged from the OBDH microcontroller.

Now, building on what has been presented and on the knowledge that has been gained through this master thesis, the author might also propose a reliability enhanced nanosatellite design for interplanetary missions, which would be developed in the pursuit of a doctorate degree. The key difference in this case is that instead of orbiting around the earth, interplanetary trajectories are usually whole or partial orbits around the Sun (AGENCY, 2022), which brings many different radiation effects and reliability issues into play. The emphasis of such research would be on the entire nanosatellite design instead of on the EPS only.

Lastly, it is worth mentioning that the reliability-enhancing techniques, the power reduction strategies, and the three-metric evaluation system presented in this work can be used by other universities and research centers around the world to expedite the design, improve the reliability, and facilitate the evaluation of their nanosatellite EPS architectures.

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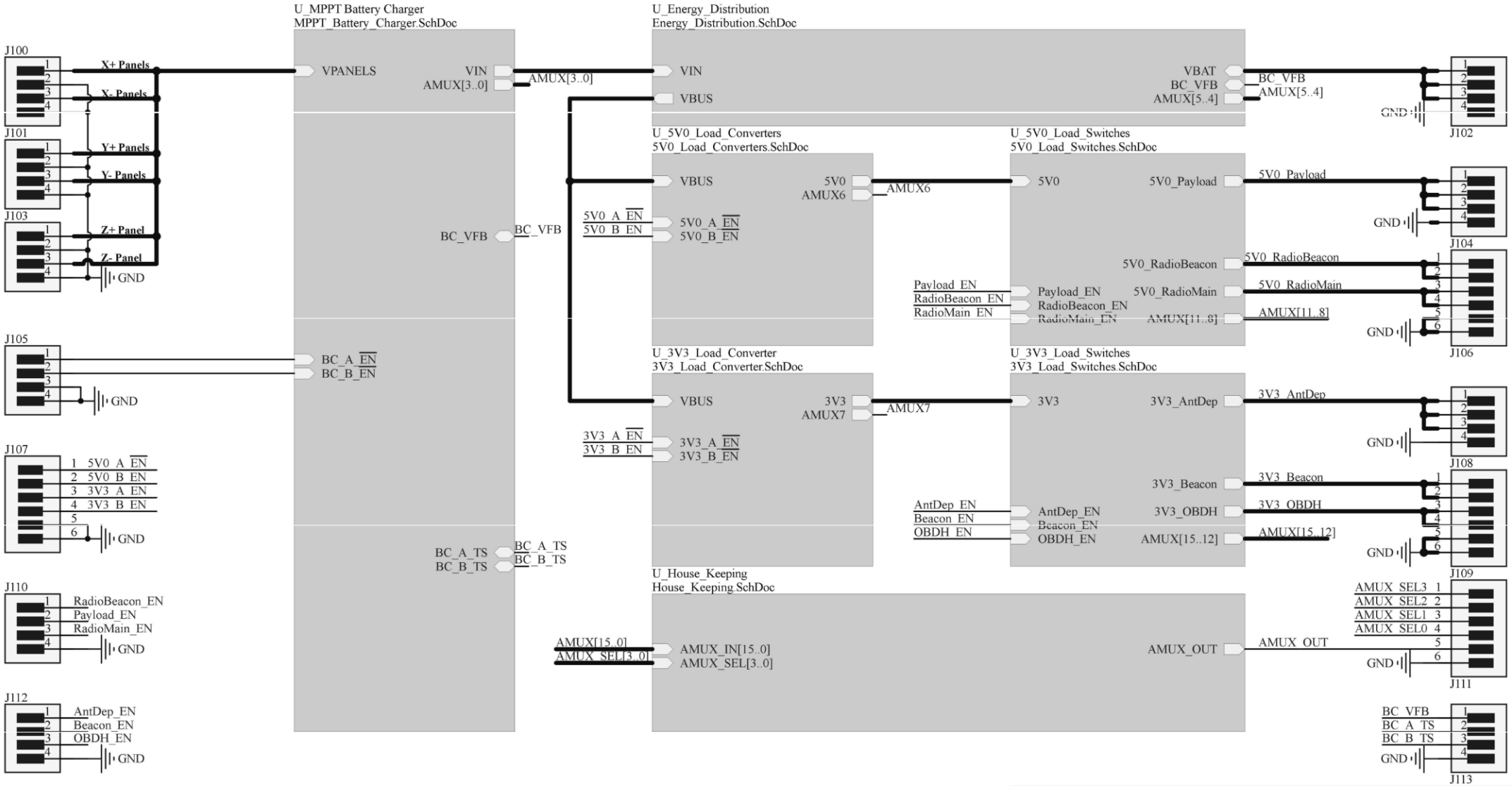
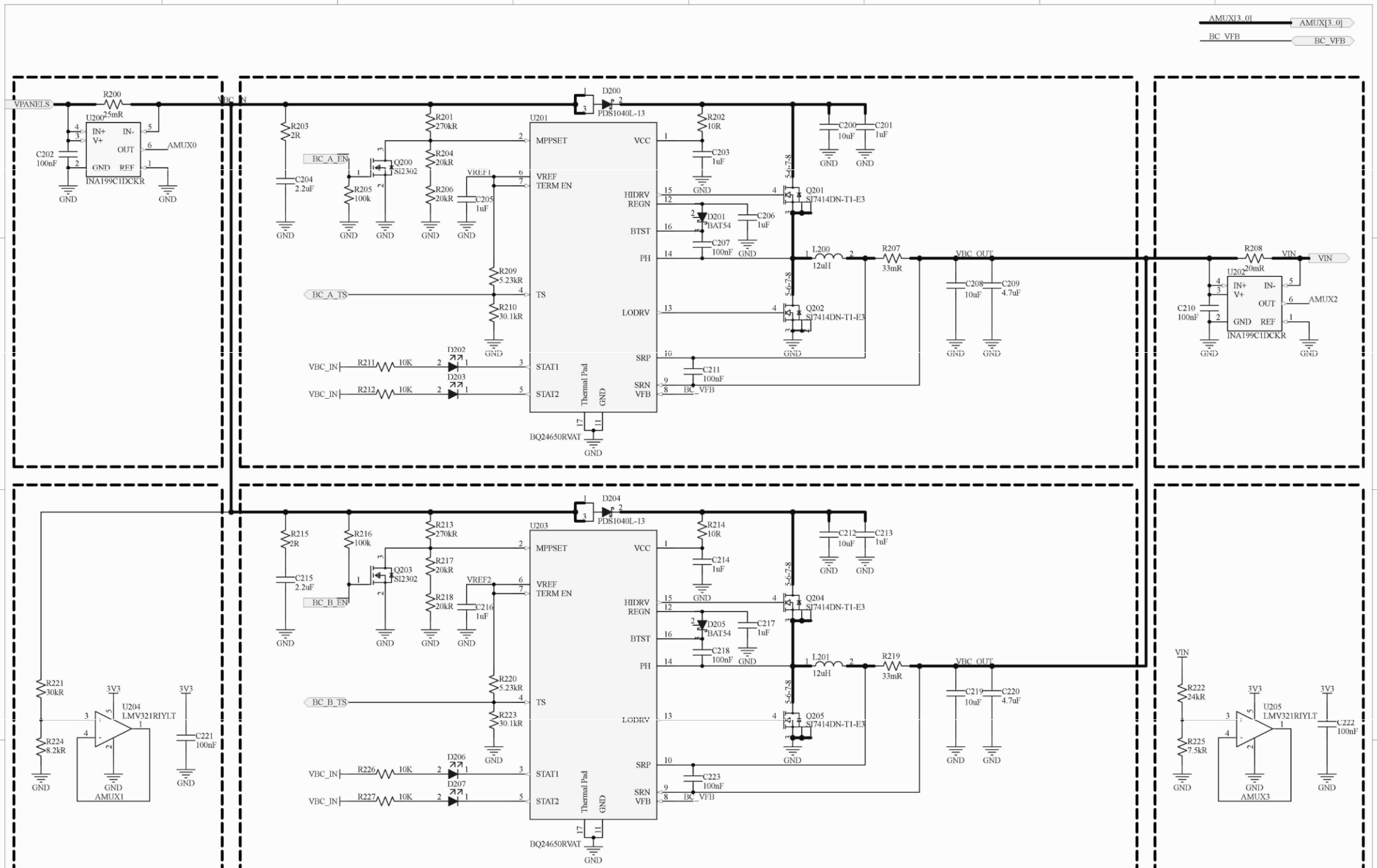
APPENDIX A – PCB SCHEMATICS

Reliability Enhanced Electrical Power System

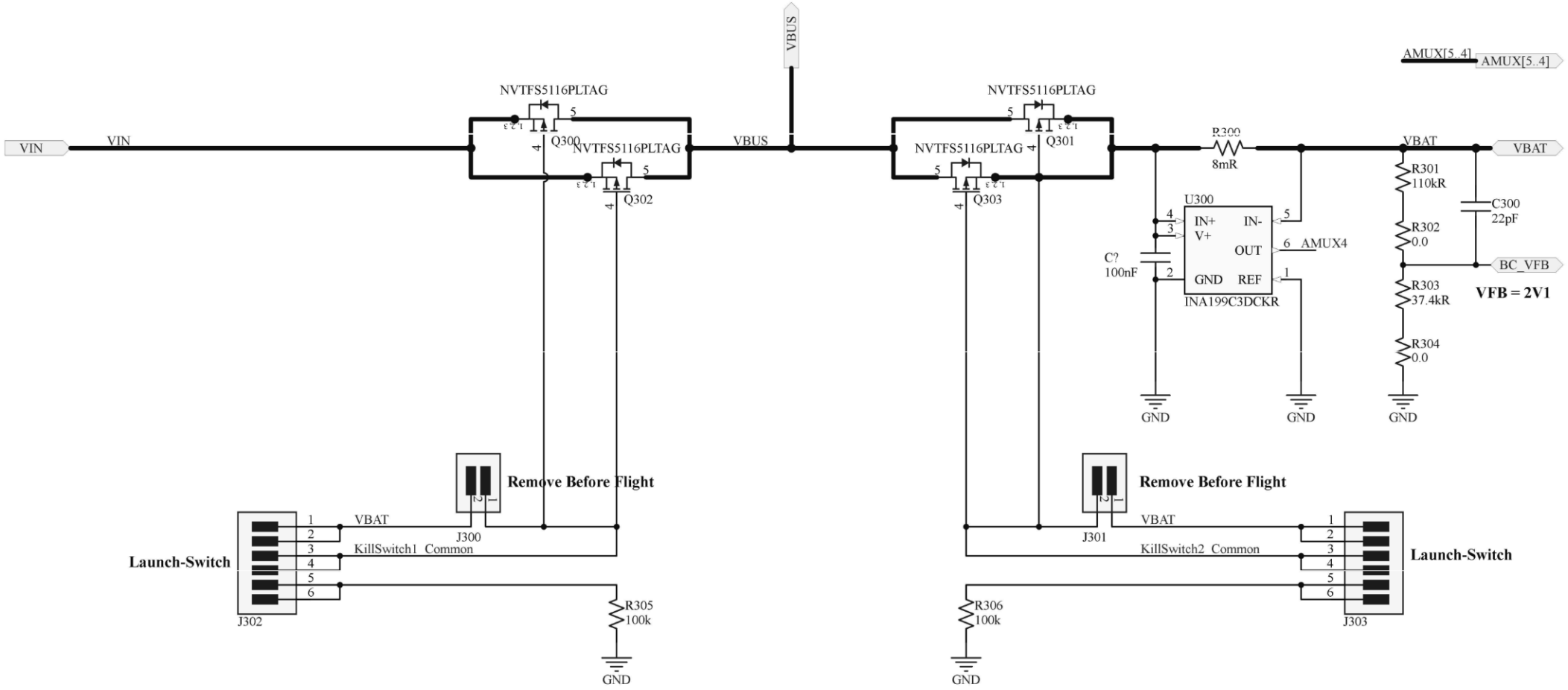


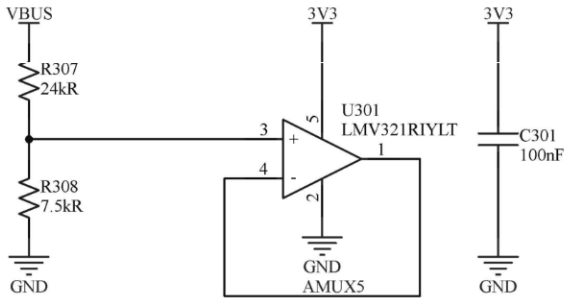
SpaceLab - Federal University of Santa Catarina			
Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS Top*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *1* of *8*	Size: A4



VPANELS Current Monitoring Lookup Table	VPANELS Voltage Monitoring Lookup Table	VIN Voltage Monitoring Lookup Table	I_VIN Current Monitoring Lookup Table	Battery Charger Data
I_Panels = 0.4A -> AMUX0 = 0.5V I_Panels = 0.8A -> AMUX0 = 1.0V I_Panels = 1.2A -> AMUX0 = 1.5V I_Panels = 1.6A -> AMUX0 = 2.0V I_Panels = 2.0A -> AMUX0 = 2.5V	VPANELS = 2.4V -> AMUX1 = 0.5V VPANELS = 4.7V -> AMUX1 = 1.0V VPANELS = 7V -> AMUX1 = 1.5V VPANELS = 9.3V -> AMUX1 = 2.0V VPANELS = 11.6V -> AMUX1 = 2.5V	VIN= 2.1V -> AMUX3 = 0.5V VIN= 4.2V -> AMUX3 = 1.0V VIN= 6.3V -> AMUX3 = 1.5V VIN= 8.4V -> AMUX3 = 2.0V VIN= 10.5V -> AMUX3 = 2.5V	I_VIN = 0.5A -> AMUX2 = 0.5V I_VIN = 1.0A -> AMUX2 = 1.0V I_VIN = 1.5A -> AMUX2 = 1.5V I_VIN = 2.0A -> AMUX2 = 2.0V I_VIN = 2.5A -> AMUX2 = 2.5V	MPPSET = 1.2*(1+270k/40k) = 9.3V VOUT = 2.1*(1+ 110K/37.4K) = 8.3V Rsens = 0.04/Ichg= 0.04/1.2 = 33mOhm

SpaceLab - Federal University of Santa Catarina			
Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS MPPT Converters*			
Engineer: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision:	Sheet *2* of *8*	Size: A3





VBAT Input Current Monitoring Lookup Table
I_VBAT = 0.32A -> AMUX4 = 0.5V
I_VBAT = 0.64A -> AMUX4 = 1.0V
I_VBAT = 0.96A -> AMUX4 = 1.5V
I_VBAT = 1.2A -> AMUX4 = 2.0V
I_VBAT = 1.6A -> AMUX4 = 2.5V

VBUS Voltage Monitoring Lookup Table
VBUS = 2.1V -> AMUX4 = 0.5V
VBUS = 4.2V -> AMUX4 = 1.0V
VBUS = 6.3V -> AMUX4 = 1.5V
VBUS = 8.4V -> AMUX4 = 2.0V
VBUS = 10.5V -> AMUX4 = 2.5V

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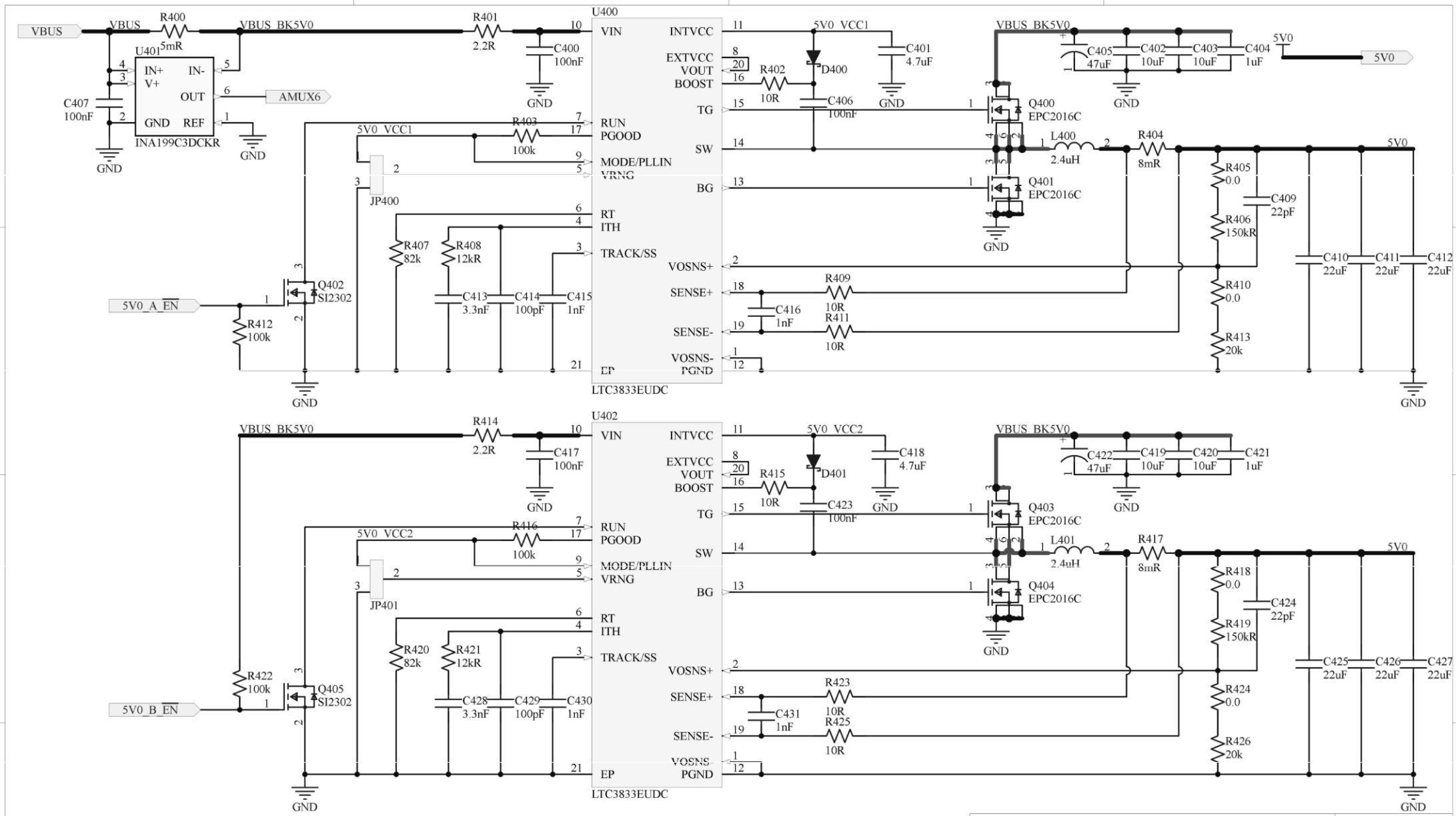
Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS Energy Distribution*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *3* of *8*	Size: A4



DESIGN EQUATIONS [1]

- Vout = 0.6(1+RFB2/RFB1)
- RFB2 = RFB1(Vo/0.6 - 1) if RFB1=3k and Vo=5V, then
- RFB2 = 3000*(5/0.6 - 1) = 22kOhm

DESIGN EQUATIONS [2]

- tss = 0.6(Css/1u) if tss = 600us, then

Css=1u(600u/0.6) = 1nF

- Rsense = Vsense_max/(Iout_max-dIL_max/2)

DESIGN EQUATIONS [3]

- Rt[kOhm] = (41550/Fsw[kHz] -2)

if Fsw = 500kHz, then

- Rt = 41550/500 -2 = 81.1kOhm

DESIGN EQUATIONS [4]

0.75 < Run < 1.2:
- TG and BG off

Run<0.75:
- Shutdown mode

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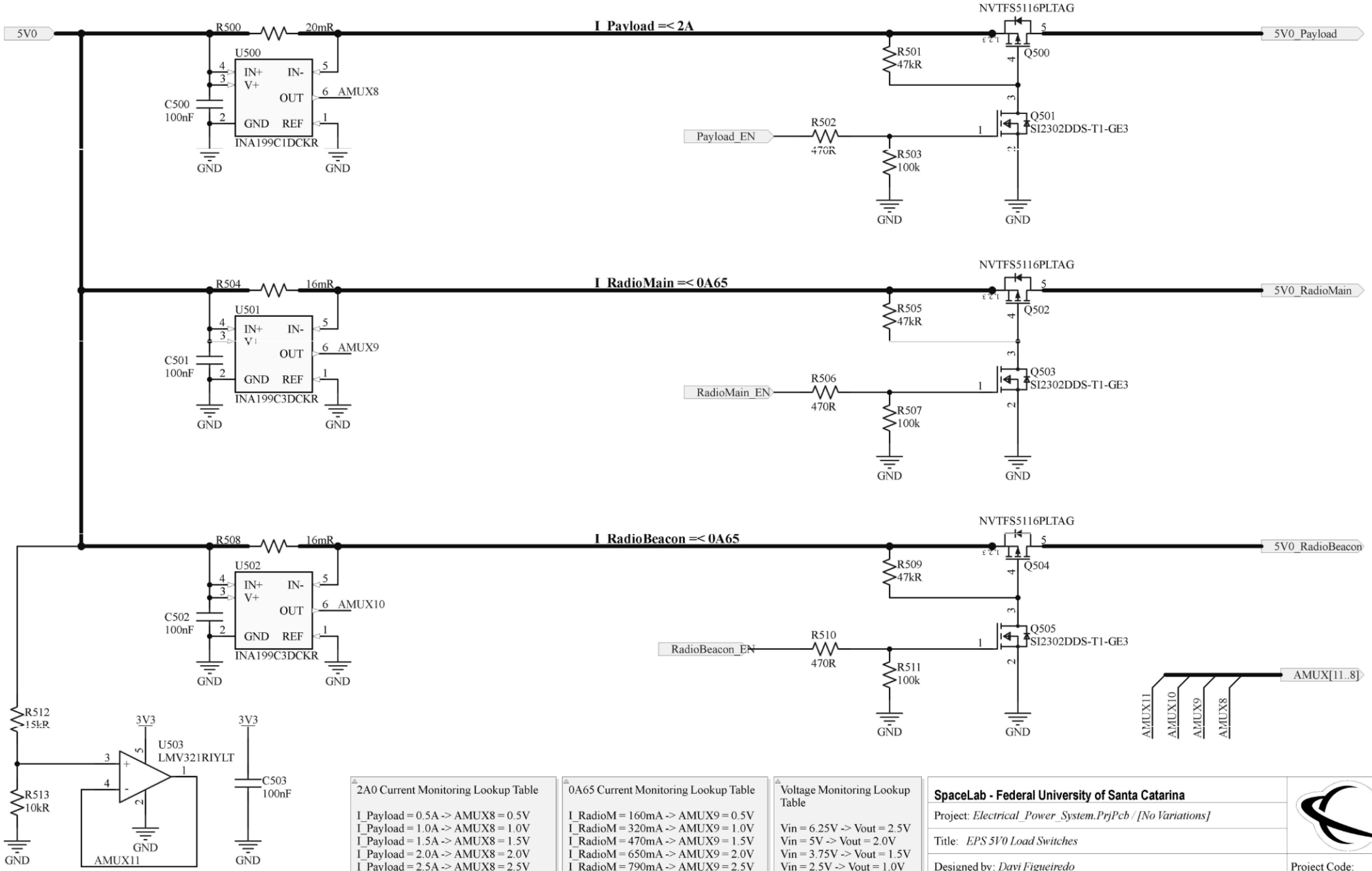
Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS 5V0 Load Converters*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *4* of *8*	Size: A4



2A0 Current Monitoring Lookup Table
I_Payload = 0.5A -> AMUX8 = 0.5V
I_Payload = 1.0A -> AMUX8 = 1.0V
I_Payload = 1.5A -> AMUX8 = 1.5V
I_Payload = 2.0A -> AMUX8 = 2.0V
I_Payload = 2.5A -> AMUX8 = 2.5V

0A65 Current Monitoring Lookup Table
I_RadioM = 160mA -> AMUX9 = 0.5V
I_RadioM = 320mA -> AMUX9 = 1.0V
I_RadioM = 470mA -> AMUX9 = 1.5V
I_RadioM = 650mA -> AMUX9 = 2.0V
I_RadioM = 790mA -> AMUX9 = 2.5V

Voltage Monitoring Lookup Table
Vin = 6.25V -> Vout = 2.5V
Vin = 5V -> Vout = 2.0V
Vin = 3.75V -> Vout = 1.5V
Vin = 2.5V -> Vout = 1.0V
Vin = 1.25V -> Vout = 0.5V

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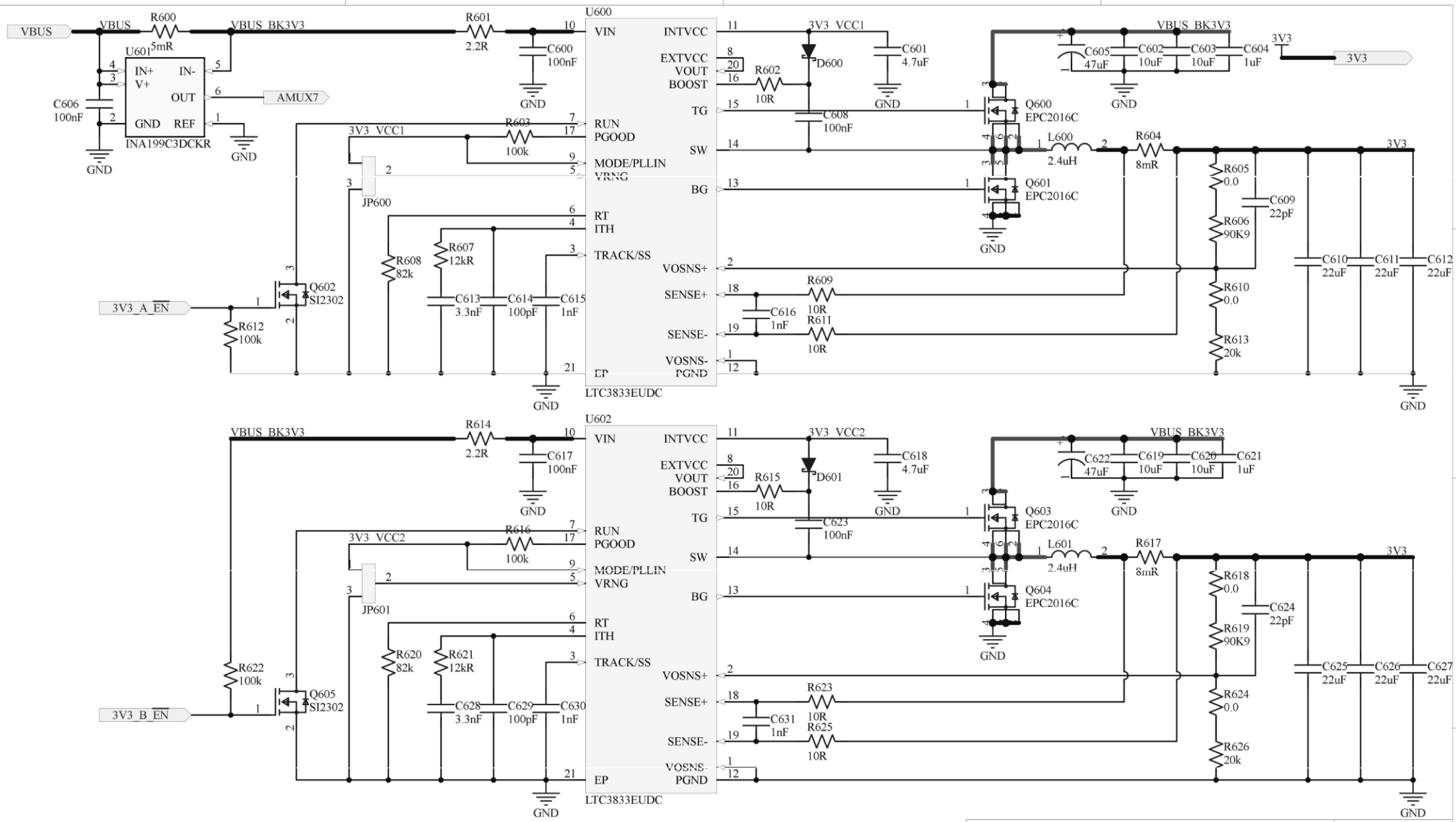
Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS 5V0 Load Switches*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *5* of *8*	Size: A4



DESIGN EQUATIONS [1]

- Vout = 0.6(1+RFB2/RFB1)

- RFB2 = RFB1(Vo/0.6 - 1) if RFB1=20k and Vo=3.3V, then

- RFB2 = 20000*(5/0.6 - 1) = 90kOhm

DESIGN EQUATIONS [2]

- tss = 0.6(Css/1u) if tss = 600us, then

Css=1u(600u/0.6) = 1nF

- Rsense = Vsense_max/(Iout_max-dIL_max/2)

DESIGN EQUATIONS [3]

- Rt[kOhm] = (41550/Fsw[kHz] -2)

if Fsw = 500kHz, then

- Rt = 41550/500 -2 = 81.1kOhm

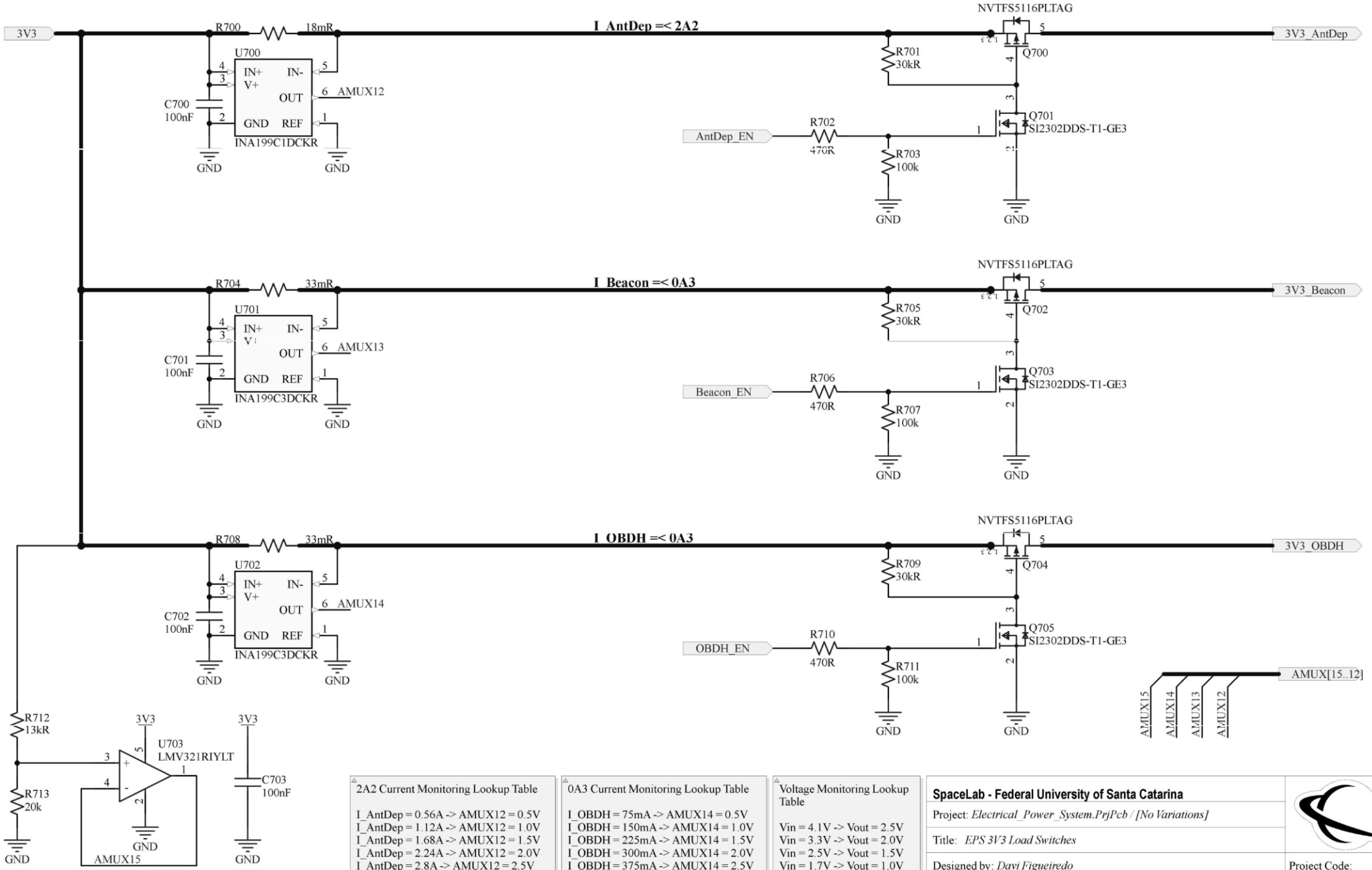
DESIGN EQUATIONS [4]

0.75 < Run < 1.2:
- TG and BG off

Run<0.75:
- Shutdown mode

SpaceLab - Federal University of Santa Catarina

Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS 3V3 Load Converters*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *6* of *8*	Size: A4



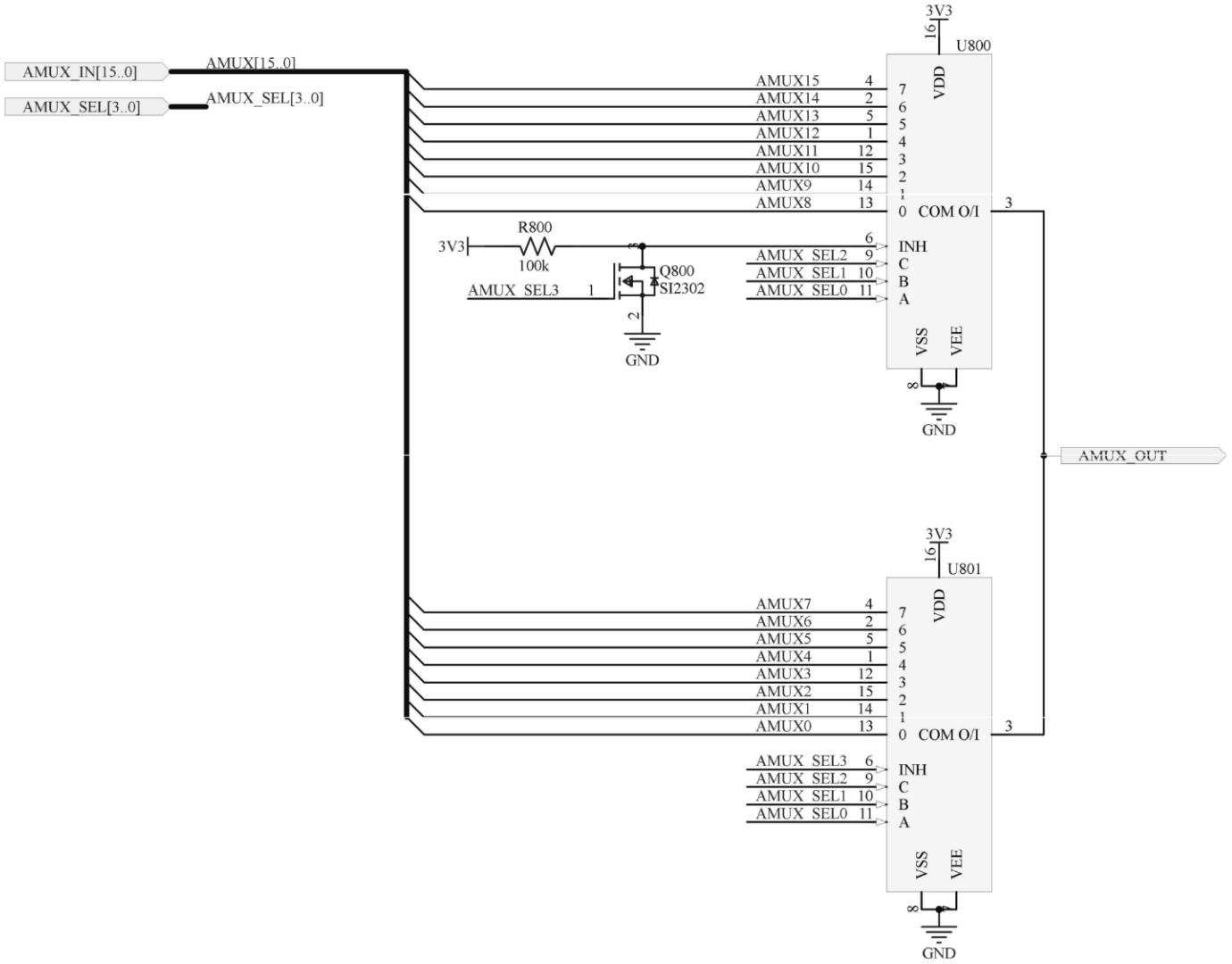
2A2 Current Monitoring Lookup Table
I_AntDep = 0.56A -> AMUX12 = 0.5V
I_AntDep = 1.12A -> AMUX12 = 1.0V
I_AntDep = 1.68A -> AMUX12 = 1.5V
I_AntDep = 2.24A -> AMUX12 = 2.0V
I_AntDep = 2.8A -> AMUX12 = 2.5V

0A3 Current Monitoring Lookup Table
I_OBDH = 75mA -> AMUX14 = 0.5V
I_OBDH = 150mA -> AMUX14 = 1.0V
I_OBDH = 225mA -> AMUX14 = 1.5V
I_OBDH = 300mA -> AMUX14 = 2.0V
I_OBDH = 375mA -> AMUX14 = 2.5V

Voltage Monitoring Lookup Table
Vin = 4.1V -> Vout = 2.5V
Vin = 3.3V -> Vout = 2.0V
Vin = 2.5V -> Vout = 1.5V
Vin = 1.7V -> Vout = 1.0V
Vin = 0.9V -> Vout = 0.5V

SpaceLab - Federal University of Santa Catarina

Project: *Electrical_Power_System.PrjPcb / [No Variations]*			
Title: *EPS 3V3 Load Switches*			
Designed by: *Davi Figueiredo*			Project Code:
Date: 1/6/2023	Revision: *	Sheet *7* of *8*	Size: A4



LOOK-UP TABLE

AMUX_SEL [3]	[2]	[1]	[0]	AMUX_OUT	Parameter
0	0	0	0	AMUX0	VPANELS Input Current
0	0	0	1	AMUX1	VPANELS Input Voltage
0	0	1	0	AMUX2	
0	0	1	1	AMUX3	
0	1	0	0	AMUX4	
0	1	0	1	AMUX5	
0	1	1	0	AMUX6	
0	1	1	1	AMUX7	
1	0	0	0	AMUX8	
1	0	0	1	AMUX9	
1	0	1	0	AMUX10	
1	0	1	1	AMUX11	
1	1	0	0	AMUX12	
1	1	0	1	AMUX13	
1	1	1	0	AMUX14	
1	1	1	1	AMUX15	

SpaceLab - Federal University of Santa Catarina

Project: *Electrical_Power_System.PrjPcb / [No Variations]*

Title: *EPS House Keeping Signals*

Designed by: *Davi Figueiredo*

Project Code:

Date: 1/6/2023 | Revision: * | Sheet *8* of *8* | Size: A4