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Julio Cesar Dias

UNIDIRECTIONAL CONVERTERS WITH SWITCHED-CAPACITORS AND MULTISTATE SWITCHING CELLS

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À minha família, que me apoiou durante todo o processo de desenvolvimento acadêmico e pessoal.

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Perfection itself is imperfection.

(Vladimir Horowitz)

ABSTRACT

This work proposes new rectifier topologies with high voltage gain, low input harmonic content and reduced voltage and current stress in the semiconductor devices. The structures proposed in this work integrate switched-capacitor cells and multistate switching cells to achieve higher voltage gains and higher output power. Switched-capacitor cells use switches to associate capacitors in series and parallel in different stages, providing high voltage gain, modularity, divided voltage across the capacitors and switches and self-balanced capacitor voltages. Multistate switching cells use intercell transformers to divide the total input current between the converter legs, thus reducing the current stress across the switches. They also have a multilevel input characteristic, which reduces the input current harmonic content and the size of input filters. The use of these techniques can increase the power levels without affecting the control complexity of the system. They also allow the use of devices with lower costs by dividing the voltage and current in the components and providing a multilevel voltage characteristic in the input. This work presents a dc-dc converter to introduce the concept and then expands it into single-phase and three-phase converters that integrate multistate switching cells with switched-capacitor cells. The steady-state and dynamic analysis of the three topologies are performed and supported by simulation results and experimental results performed on converters that use the integration of three-state switching cells and symmetrical ladder switched-capacitor cells. The converters were experimentally validated with modular prototypes. The dc-dc module was build in a way that made it possible to add more modules to test the ac-dc single-phase and the three-phase prototype. In the dc-dc converter it was possible to convert 100 V to 1200 V with a 1 kW output power. It was possible to test the ac-dc topology by adding a diode bridge in the module input and electrolytic capacitors in its output. The single-phase rectifier converted a 127 V input to a 1200 V output with a 1.3 kW output power. By replacing the boost diodes in the modules by MOSFETs and associating the modules in parallel, it was possible to test the three-phase rectifier with a 220 V input voltage, 1200 V output and 4 kW. All prototypes achieved a 1200 V output with reduced voltage stress on the devices and shared currents in the intercell transformer windings. The dc-dc and the three-phase converters achieved efficiency levels in the range of 97%, whereas the single-phase efficiency was lower than 96% due to the power losses on the diode bridge. In the dc-dc and three-phase converter, most of the losses were MOSFET switching losses. The proposed concept was validated by the experiments, but the experiments also show in which aspects the proposed concept can be improved in future works. The proposed concept can be suitable for high-voltage gain applications, such as renewable energy systems due to its gain profile and shared voltage and current in the devices.

Keywords: High voltage gain. Switched capacitor. Multistate switching cell. Power factor correction. Unidirectional converters.

RESUMO

Este trabalho propõe novas topologias de retificadores com elevado ganho em tensão, corrente de entrada com baixo conteúdo harmônico e esforços de tensão e corrente reduzidos nos dispositivos semicondutores. As estruturas propostas neste trabalho integram células de capacitor chaveado e células de comutação multiestados com o fim de obter maiores ganhos de tensão e capacidade de potência. Células de capacitor chaveado usam interruptores para associar capacitores em série e em paralelo em diferentes estágios, assim fornecendo elevado ganho em tensão, modularidade, divisão da tensão nos capacitores e interruptores e, por fim, capacitores com tensões naturalmente equilibradas. Células de comutação multiestados usam um transformador de interfase para dividir a corrente total de entrada entre os braços do conversor, assim reduzindo os esforços de corrente nos interruptores. Também apresentam uma característica de entrada multinível, que reduz o conteúdo harmônico da corrente de entrada e o tamanho dos filtros. Este trabalho propõe topologias geradas a partir desses princípios e realiza a análise de um conversor CC-CC, um retificador monofásico e um trifásico propostos baseados no conceito introduzido. As análises estática e dinâmica das três topologias são realizadas e resultados de simulação e experimentais são usados para validar o estudo teórico. Os conversores foram validados experimentalmente com protótipos modulares. O módulo CC-CC foi construído de forma que possibilitou a adição de mósulos para realizar os testes como conversor CA-CC monofásico e trifásico. No conversor CC-CC foi possível converter uma entrada de 100 V em 1200 V processando 1 kW. Foi prossível testar o retificador monofásico ao adicionar uma ponte de diodos na entrada do módulo e capacitores eletrolíticos na saída. O retificador monofásico foi projetado para uma entrada de 127 V e uma saída de 1200 V, processando 1.3 kW. Ao trocar os diodos do boost por interruptores ativos e associando os módulos em paralelo, foi possível testar o retificador trifásico com uma entrada de 220 V, saída de 1200 V e 4 kW. Todos os protótipos atingiram o valor de 1200 V de tensão de saída com esforços de tensão reduzidos nos dispositivos e correntes divididas nos enrolamentos do transformador intercélulas. Os conversores CC-CC e o trifásico atingiram rendimentos na faixa de 97%, enquanto o rendimento do monofásico foi abaixo de 96% devido às perdas na ponte de diodos. Nos conversores CC-CC e trifásico a maior parte das perdas é na comutação dos MOSFETs. O conceito proposto foi validado nos experimentos, mas esses experimentos também serviram para mostrar pontos de aprimoramento para trabalhos futuros. O conceito proposto demonstra possibilidade de uso em aplicações renováveis devido à sua característica de ganho com possibilidade de compartilhamento de tensão e corrente nos dispositivos.

Palavras-chave: Alto ganho em tensão. Capacitor chaveado. Célula de comutação multiestados. Correção de fator de potência. Conversores unidirecionais.

RESUMO EXPANDIDO

Introdução

Diversas aplicações cotidianas requerem o uso de conversores de elevado ganho, como acionamento de máquinas, aplicações renováveis, armazenamento de energia, entre outros. A conversão de energia em alto ganho possui diversos desafios relacionados a limitações existentes na tecnologia de componentes eletrônicos. Dispositivos semicondutores dimensionados para valores de tensão ou corrente elevados tendem a ser caros e possuem elementos parasitas que prejudicam o rendimento e volume dos conversores. As elevadas impedâncias parasitas de dispositivos semicondutores de alta potência aumentam as perdas no circuito, o que influencia não somente no seu rendimento, mas também no volume e custo por muitas vezes necessitar de sistemas de arrefecimento mais robustos. As características dinâmicas lentas de dispositivos para elevados valores de tensão também prejudicam o rendimento com o aumento das perdas de comutação, e influenciam no volume devido à necessidade de filtros maiores para atenuar o conteúdo harmônico de baixa frequência. Tendo em vista esses problemas, este trabalho propõe como alternativa a integração de células de capacitor chaveado em conversores com células de comutação multiestados. Células de comutação multiestados utilizam transformadores intercélulas para dividir corrente entre dispositivos e multiplicar a frequência que será filtrada a partir de pulsos defasados nos dispositivos da célula de comutação. Essa célula reduz o tamanho dos filtros e também reduz as perdas nos dispositivos semicondutores ao dividir a corrente entre eles. A célula de capacitor chaveado é utilizada para dividir o nível de tensão de saída entre os dispositivos e dividir a tensão entre os capacitores de saída de forma equilibrada, além da possibilidade de modularização para aumentar o ganho de tensão do circuito sem afetar os níveis de tensão nos dispositivos semicondutores. Foram propostas três topologias para a validação da proposta, um conversor CC-CC, um CA-CC monofásico e um CA-CC trifásico.

Objetivos

Este trabalho tem como objetivo propor novas topologias de conversores com ganho de tensão elevado, potência elevada e redução de esforços de tensão e corrente nos dispositivos semicondutores.

Metodologia

Foi realizada uma revisão bibliográfica para analisar o estado da arte de topologias de alto ganho em tensão e potência, e também realizado um estudo em células de capacitor chaveado e células de comutação multiestados. A partir desse estudo, foram propostas formas de integrar esses dois conceitos para gerar novas topologias. Esses dois conceitos foram aplicados na topologia *boost* para a concepção de topologias CC-CC e CA-CC com correção de fator de potência. Foi realizada a análise teórica dessas topologias a fim de realizar os cálculos de dimensionamento dos dispositivos e estratégia de controle. Após a análise teórica

estática e dinâmica dos conversores, foram realizadas simulações para validar os resultados teóricos e, por fim, foram confeccionados módulos de potência para a validação experimental das topologias propostas.

Resultados e Discussão

Para validar o conceito, implementou-se na prática três conversores, um conversor CC-CC com 100 V de entrada, 1200 V de saída e potência de saída de 1 kW; um retificador monofásico com 127 V de entrada, 1200 V de saída e 1300 W de potência de saída; e um retificador trifásico com 220 V de entrada, 1200 V de saída e 4 kW. Todos eles foram implementados com células de comutação de três estados e duas células *ladder* em cada braço da célula de comutação. Todos os conversores realizaram a conversão com a tensão nos capacitores equilibrada, assim conseguindo dividir a tensão nos interruptores e alcançando uma saída de 1200 V com 400 V em cada dispositivo semicondutor. A célula de comutação multiestados foi capaz de multiplicar a componente da frequência de comutação, além de dividir a corrente de entrada no transformador de interfase. O equilíbrio das correntes foi obtido de forma natural, sem técnicas ativas de controle, ao utilizar *gate drivers* com características muito similares no projeto. Os retificadores operaram com fator de potência acima de 0.99 e apresentaram conteúdo harmônico condizente com os limites da norma IEC 61000-3-2 e IEC 61000-3-4. O conversor CC-CC atingiu rendimento de 97%, mas ao aumentar a tensão de entrada e potência de saída foi possível atingir rendimento na faixa de 98%. O rendimento no retificador monofásico caiu abaixo de 96% devido à inserção de uma ponte de diodos na entrada. No retificador trifásico foi possível obter rendimento na faixa de 97%.

Considerações Finais

Foi proposta a integração de células de capacitor chaveado com células de comutação multiestados a fim de conceber topologias de conversores estáticos com ganho de tensão elevado e elevado processamento de corrente, mas mantendo esforços baixos de tensão e corrente nos dispositivos semicondutores. Os conversores utilizados para validar a proposta foram capazes de realizar o processamento de potência de acordo com a proposta, apresentaram esforços reduzidos de tensão e corrente nos dispositivos e regulação na tensão de saída e corrente de entrada. Ainda é possível em trabalhos futuros aprimorar o desempenho dos conversores a partir de otimização no dimensionamento de componentes, uso de ponte síncrona no retificador monofásico e utilização de técnicas para redução das perdas de comutação nos conversores, entre outros.

Palavras-chave: Alto ganho em tensão. Capacitor chaveado. Célula de comutação multiestados. Correção de fator de potência. Conversores unidirecionais.

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1 INTRODUCTION

1.1 CONTEXTUALIZATION

High voltage levels can be beneficial and necessary for several uses, since it is used to reduce the power losses and volume of conductors due to the current level reduction. Some applications, such as X-ray, air filters and plasma sources need high voltages to operate properly, and to generate these higher voltage levels there is a need for power supplies capable to withstand the high voltages on their semiconductor devices. There are several other applications today that require these supplies, such as pulsed lasers, telecommunication supplies, electric vehicles and machine drives [1–6].

Step-up ac-dc converters are usually required in these types of applications, which aim to rectify and increase the voltage levels from the utility grid or to lift the voltage levels from sources with even lower voltage outputs (e.g., wind energy conversion systems, photovoltaic modules, fuel cells. The voltage from these types of sources can be increased to inject the extracted energy into the grid or to supply equipment [7–11]. However, there are many limitations regarding the voltage and current stress in the devices used in these power supplies.

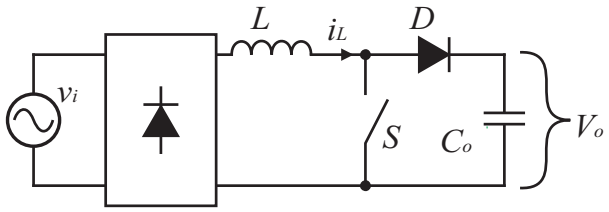
Although the power electronics field has evolved substantially over the last decades, more studies are yet needed to improve the efficiency, cost, weight and volume and to overcome current limitations of energy conversion systems. Power electronics is an important component in many applications and its research is necessary due to the rising demand of consumer electronics, automation, and new problems that have arised in the last years with the rise of blockchain technology, cryptocurrency mining, electromobility and the increased teleworking rates during the COVID-19 pandemic. All of these factors have caused a higher demand of electrical energy, which requires more efficient conversion systems to reduce costs, environmental impact and improve power quality [12–14].

As new semiconductor devices become available with the emergence of wide band gap technologies, the research for new structures can help solving issues in power conversion. In applications that require high voltage rates, there are still several issues with conventional conversion techniques, such as maximum voltage restrictions of electronic devices and parasitic elements, which limit the conversion ratio of power converters and reduce their efficiency as the power and voltage rates increase. These restrictions call for the research of new structures that do not need to rely on semiconductors devices with high breakdown voltages, which are expensive devices with slow dynamics and are not commercially available at a large scale. The slow dynamics of these devices require bulkier passive filters, which increase the costs of the converters. Furthermore, these devices have high conduction losses that decrease the conversion ratio and efficiency of high voltage gain converters [1, 11, 15].

Power converters supplied by the grid or energy sources should have input currents with low harmonic distortion in order to avoid electromagnetic disturbances, reduce the non-active power content and avoid causing voltage distortions that may damage equipment that is connected to the same point of power delivery [point of common coupling (PCC)] [16–18]. Several systems are supplied by the utility grid or ac generators and, making it necessary to regulate the input current of the equipment in order to achieve near-unit power factor. Furthermore, it is essential that the converters input harmonic currents meet the requirements for harmonic control and recommended practices that are

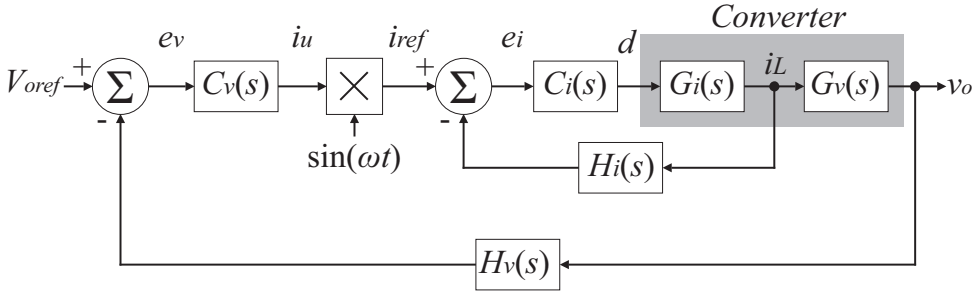
established by international standards and guidelines [19–21].

Fig. 1 – Boost PFC rectifier.



The input power factor of an equipment can be improved by using passive or active solutions. Although passive solutions are more robust, they require bulky and heavy passive devices for filtering the harmonic content. Besides, passive filters may be more expensive compared to active solutions due to the rising cost of copper and magnetic core material. One alternative is the boost converter with active power factor correction (PFC), shown in Fig. 1, which is a widespread active technique to achieve near-unit power factor. The main advantage of the boost rectifier compared to other basic converter topologies (buck, buck-boost) is its input inductor, which is designed to attenuate the switching frequency harmonic component from the input current. PFC rectifiers that operate in continuous conduction mode (CCM) are typically controlled with two cascaded loops, one inner input current loop with faster dynamics and an outer output voltage loop with slower dynamics (See Fig. 2). The outer loop generates a peak current reference which is multiplied by the phase of the input voltage, thus providing a rectified sinusoidal input current reference to the inner loop. The inner loop controls the input current according to the outer loop reference. Because the inner loop is designed with a much faster dynamic response than the outer loop, the dynamics of the inner loop can be ideally viewed by the outer loop as a static gain, thus the two loops can be controlled independently and the system transfer functions for each loop have a first order equivalent response. Since the PFC boost rectifier has a current-fed input, regulated output voltage, high input power factor and it can be controlled by linear methods, it is a very widespread topology that is suitable for several applications. However, due to its parasitic components and the voltage stress across the switches, it has limitations for high-gain applications. It is also not suitable for high-power applications, since they require power switches that are more expensive and have slower dynamics. Due to the switches slow dynamics, the switching frequency must be decreased in higher voltage or higher power applications, increasing the size and weight of the input filters [22–26].

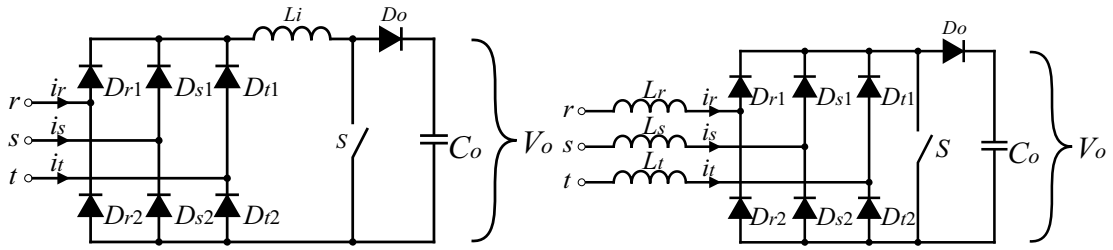
Fig. 2 – Typical control strategy of PFC rectifiers.



For higher power levels, three-phase inputs are more adequate, since the current is shared between the phases. There are several configurations of the three-phase boost

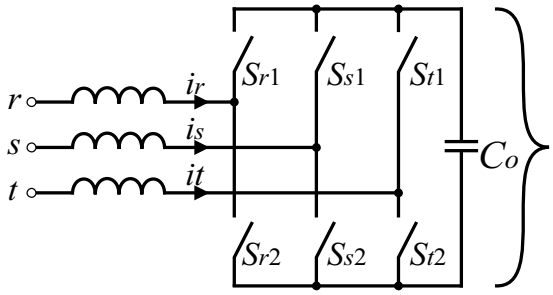
rectifier suitable for different input configurations. A simple solution is the three-phase extension of the single-phase boost rectifier, which is conceived by changing the input diode bridge (See Fig. 3). The input current in this converter is divided in the three-phase diode bridge. However, the boost converter switch and diode process all the output energy. Besides, the input currents presents low-frequency harmonic content, since the phase currents cannot be controlled individually [27–29].

Fig. 3 – Three-phase boost rectifiers with diode bridge [29]: (a) inductor on the dc side, (b) inductors on the ac side.



An alternative for reducing the current stress on the switches of the boost converter and controlling the input phase currents is the three-phase bidirectional boost rectifier, shown in Fig. 4. This converter enables the control of the input current within a sinusoidal shape in the three phases and divides the current stress in the switches. The control strategy of three-phase rectifiers is more complex than the single-phase, since the three phase currents cannot be controlled individually due to their coupling [29–32]. The three-phase rectifier analysis will be addressed with more details in later chapters, since the new structures presented in this thesis are derived from this rectifier and the design methodology of the proposed rectifier is very similar to the conventional bidirectional boost rectifier.

Fig. 4 – Three-phase bidirectional boost rectifier [29].



The three-phase bidirectional rectifier has a higher voltage gain than the single-phase PFC boost converter and it can process higher current values, since the input power is divided between the three phases. However, there are still limitations due to the voltage stress on the devices (equal to the output voltage), which requires more expensive switches for higher output voltages. These switches are also slower and have higher conduction losses than switches designed for lower current levels. There are also limitations regarding the voltage gain due to parasitic elements, which require lower modulation index and affects the converter voltage regulation. As the voltage and power levels increase,the use of slower switches result in bulkier and heavier input passive filters [26, 33].

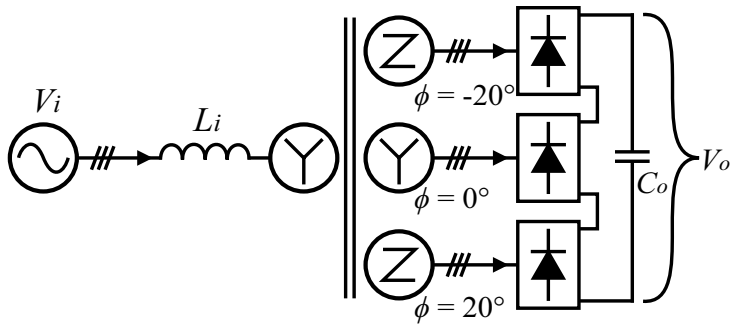
In cases where the switching frequency of the semiconductor devices is too low, the input current filter must also be designed for lower cutoff frequencies, which can result in phase-shifted currents due to the inductive reactance, therefore affecting the input power factor. There are some solutions to prevent this issue, which can be implemented in a passive or active way. A passive solution is the use of higher order filters with a higher cutoff frequency, which present faster dynamics and a higher high-frequency attenuation. However, these filters require more components and the higher order transfer function might increase the control complexity. Furthermore, in cases that the switching frequency is too low, the high-frequency attenuation might not be enough to meet the requirements of harmonic control guidelines [19–21].

Improvements in the input power factor in applications that require higher voltage or power levels can be achieved with other more suitable topologies. An alternative is the use of multipulse rectifiers, which can be implemented with diode or SCR bridges (See Fig. 5). These rectifiers use transformers in configurations to phase-shift the voltage on the secondary windings, which result in an input current in the primary coil with lower harmonic content than the conventional six-pulse rectifier. The secondary windings of the transformers are connected to six-pulse rectifiers, which can be connected in a series association, thus providing a high voltage gain and reducing the voltage stress across the semiconductor. This solution is robust and capable of processing higher power levels, since it uses only diodes or SCRs as switching devices. However, the gain of the rectifier depends on the turn ratio of the transformer and the number of modules. A higher turn ratio affects the voltage stress on the switches and might require gate drivers with high voltage isolation for applications with SCR. The increased number of modules requires additional transformers and diodes or SCRs, which affects the size, cost and complexity of the converter. Other disadvantage is the use of low-frequency transformers, which must be designed in non-conventional configurations for phase-shifting the voltages on the secondary windings in applications were multiple pulses are used. Besides, the use of low frequency transformers increase significantly the weight and volume of the conversion system.

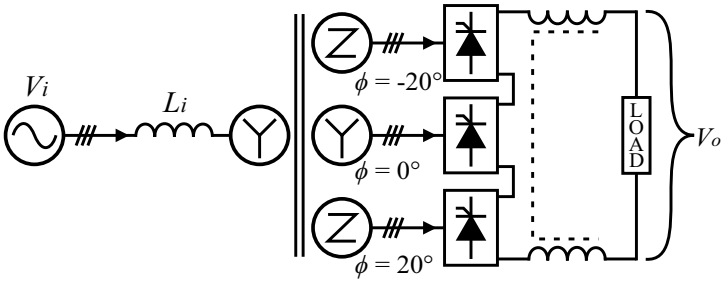
Low frequency input filters can be avoided by using different structures of switched-mode power supplies able of reducing the voltage stress on the switches, such as multilevel and multistage converters [1,34–37]. Multilevel rectifiers use multiple switch combinations to provide different voltage levels on the converter input, thus shaping the switched voltage after the input filter into a sinusoidal shape with lower harmonic content than the conventional two-level rectifiers. These rectifiers also allow the use lower voltage switches, which are less expensive and faster, thus reducing even more the size and weight of input filters. A major advantage of multilevel topologies is the voltage stress on the switches, which can be lower than the grid peak voltage, being useful structures for high and medium voltage applications. The main disadvantage of the multilevel converters is their complexity. These converters have a high number of controlled switches and require many isolated gate drivers. Furthermore, complex modulation schemes are required in some structures to balance the capacitor voltages, thus increasing computational effort and including elements that can fail and reduce the robustness of the converter [34–38]. Fig. 6 illustrates some multilevel rectifier topologies.

In this thesis a new alternative for higher voltage gain and power levels is proposed, which is a family of dc-dc and ac-dc converters based on the integration between switched-capacitor (SC) and multistate switching cells (MSSC). Because these techniques are the main study subjects of this thesis, a more thorough literature review is presented with an

Fig. 5 – 18-pulse series-type rectifiers [34]: (a) diode bridge, (b) SCR bridge.



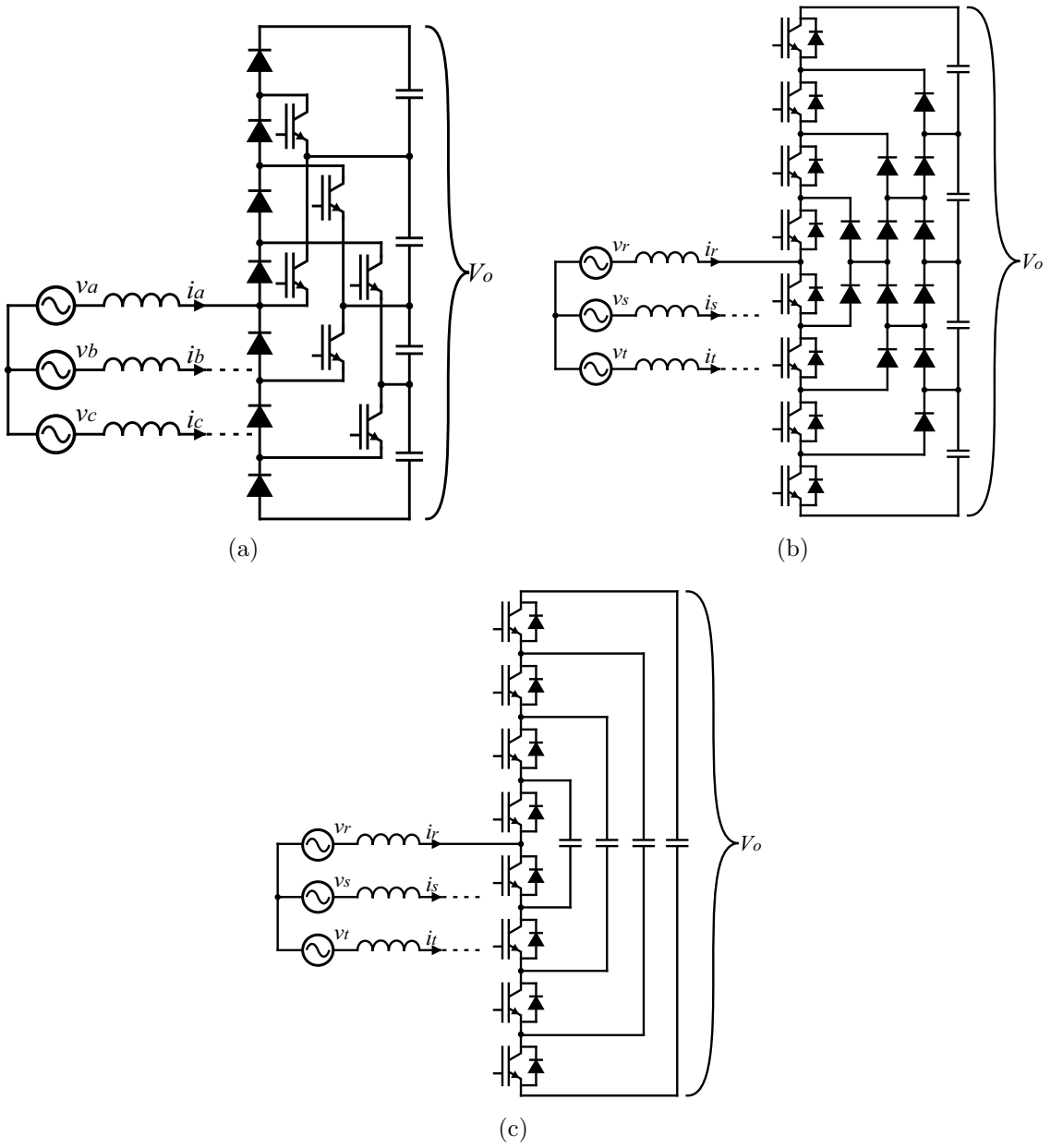
(a)



(b)

individual section for each one of them.

Fig. 6 – Multilevel three-phase rectifier topologies [36]: (a) Unidirectional five-level rectifier, (b) Five-level diode clamped rectifier, (c) Five-level flying-capacitor rectifier.

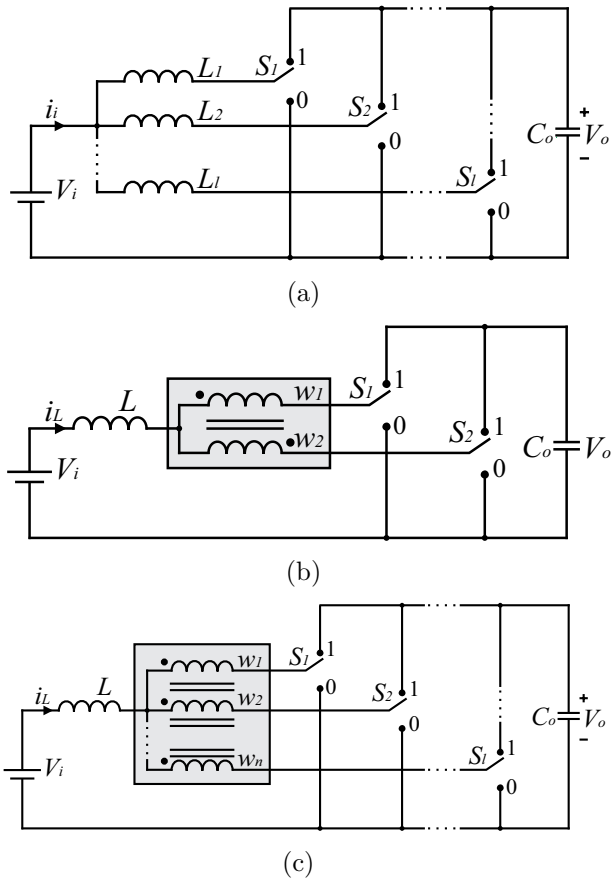


1.2 LITERATURE REVIEW: MULTISTATE SWITCHING CELLS

As mentioned previously, some common issues related to high power conversion are the current stress in the switches and low switching frequency, which can require bulky input filters. However, it is possible to process more power with a higher frequency by dividing the power between more converters or by dividing the current between more switches. Two techniques that have been often used in literature for this purpose are the interleaved converters and the MSSC, shown in Fig. 7.

In this thesis the MSSC will be studied due to the possibility of reducing the number of magnetic cores and increasing the number of voltage levels in the filter point of connection. This study, however, can be expanded into future works to cover interleaved

Fig. 7 – Current sharing techniques: (a) interleaved converter, (b) 3SSC, (c) MSSC.



topologies without major differences or increased complexity issues. The main purpose of this thesis is to introduce the concept of integrating MSSC with SC cells in ac-dc conversion.

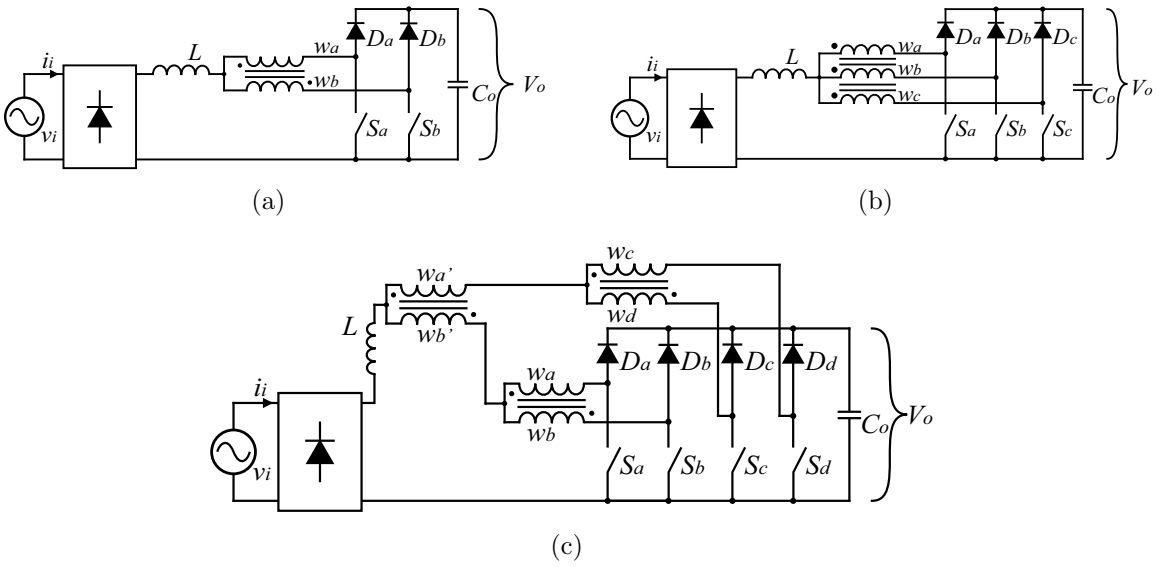
Either the interleaved cell and the MSSC are controlled by phase-shifted PWM signals. The input current of the converter is the sum of the phase shifted currents of each winding, which results in a total input current with a fundamental frequency that is the switching frequency multiplied by the number of phase-shifted carrier waves. The operation principle of the MSSC will be described in chapter 3.

The use of the MSSC for dc-dc conversion was first presented in Brazilian literature by [39, 40], where variations of the three-state switching cell (3SSC) were integrated to the basic converter topologies. The 3SSC is based on the current-fed push-pull converter, which uses an isolated transformer with a center-tapped input. By removing the secondary winding of the push-pull transformer and connecting the windings to the output, the input current can be shared between the switches and the converter can operate as a conventional boost [41]. The use of integrated magnetics had been first proposed before in [42] for buck converters with MSSC and interphase transformers have also been used for harmonic current reduction in low frequency applications [43, 44]. The study of the interphase transformer for the 3SSC boost converter with two input sources had also been performed before in [45]. In [46] the work was extended for a generalization of the MSSC converters based on the study of the four-state cell basic topologies.

In [47] the use of the 3SSC in PFC rectifiers was proposed. The study was expanded in [48], covering 4SSC and 5SSC and proposing different methods for implementing the

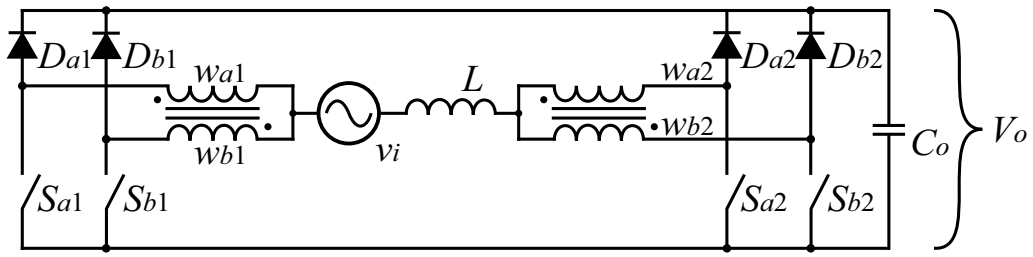
MSSC, as shown in Fig. 8. The circuit shown in Fig. 8 (c) suggests a different configuration that cascades the interphase transformers for more states. However, the use of cascaded coupled inductors for MSSC was proposed by [49] for ac-dc conversion. This configuration is practical for more states due to the constructive aspects of the interphase transformer, however, it lacks experimental verification.

Fig. 8 – Single-phase PFC rectifiers with MSC [48]: (a) 3SSC, (b) 4SSC, (c) 5SSC with cascaded interphase transformers.



A bridgeless version of the 3SSC boost rectifier was proposed in [50]. The bridgeless version of the structure requires more semiconductor devices and magnetic elements than the conventional structure, as can be seen in Fig. 9. However, the current in the devices of the bridgeless version is divided between the legs, whereas in the bridged converter the input diode bridge must be designed for the total input current.

Fig. 9 – Single-phase bridgeless boost rectifier with 3SSC [50].



In [51] a T-Type 3SSC converter with high voltage gain was proposed. The converter provides high power factor, current sharing in the switches, low voltage stress and high voltage gain. However, it uses an isolated transformer to provide the high voltage gain.

The MSSC can also be implemented in multilevel topologies, thus reducing the voltage stress on the switches and reducing the size of the input filters. A generalized study of multilevel MSSC rectifiers was presented in [52]. In this work, a 3-level 3SSC converter was implemented to evaluate the analysis. Fig. 11 (a) shows the generalized structure and Fig. 11 (b) shows the converter that was implemented in [52].

Fig. 10 – Single-phase T-type rectifier with 3SSC [51].

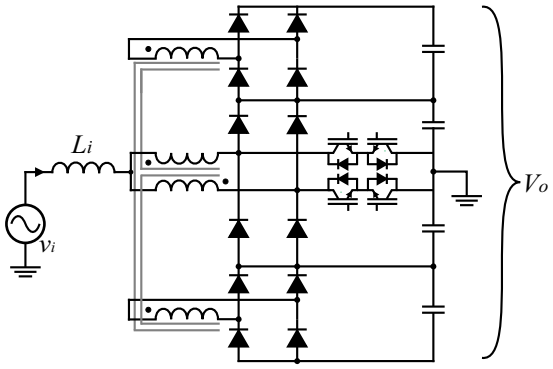
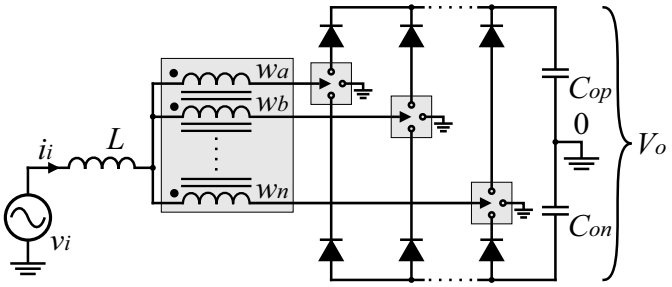
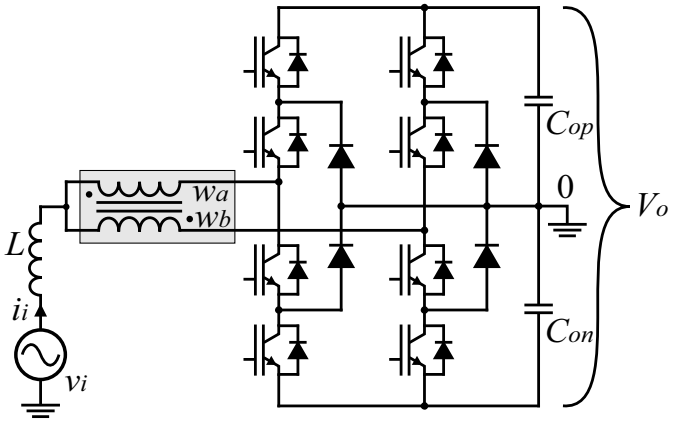


Fig. 11 – Three-level MSSC rectifiers [52].



Another variation of the multilevel MSSC rectifier is the neutral-point-clamped (NPC) converter, which was proposed by [49] and expanded into a three-phase version by [53] for an inverter application and in [54] as a rectifier, as shown in Fig. 12. The rectifier proposed in [54] is a 5-level NPC rectifier that can be expanded into more levels to divide the voltage stress on the switches and reducing the input harmonic content. However, by adding more levels, the complexity of the circuit increases significantly, since more controlled switches are added.

Fig. 12 – Single-phase boost NPC rectifier with 3SSC [54].



For higher power applications, three-phase structures are more often used. In multi-phase structures the phases are usually coupled, except in some specific applications, such as generators with open-ended windings [55–57]. In cases where the phases are coupled, the unidirectional switching-cell that is used in two-level single-phase structures cannot control the input current adequately and provide high power factor [58]. This issue can be

worked around by using complementary converters for different loads, multilevel topologies or by using synchronous switching cells that are capable of controlling the input currents in different directions [53, 59–61].

The three-phase dc-ac converter with MSSC was introduced by [53, 62]. The proposed topology is a bidirectional converter with the capability of dividing the current stress on the switches. Because it is a bidirectional topology, the converter can be controlled as an inverter or a rectifier by changing the reference current signal in the current controller to change the converter power flow. The three-phase inverter with 4SSC is shown in Fig. 13. An NPC version of the 4SSC inverter was also proposed in [53] (See Fig. 14). It provides low voltage stress on the switches and can also change its power flow in order to work as a rectifier. However, it uses more active switches and requires more isolated gate drivers.

Fig. 13 – Three-phase inverter with 4SSC [53].

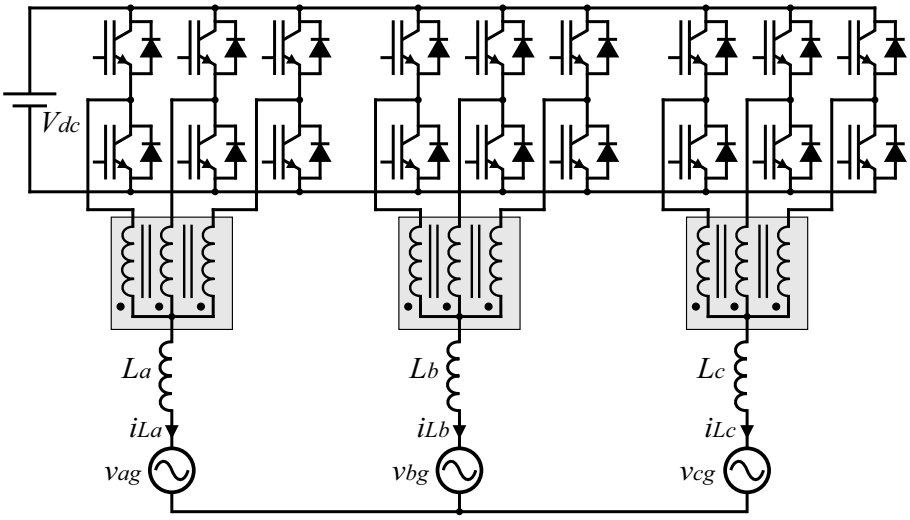
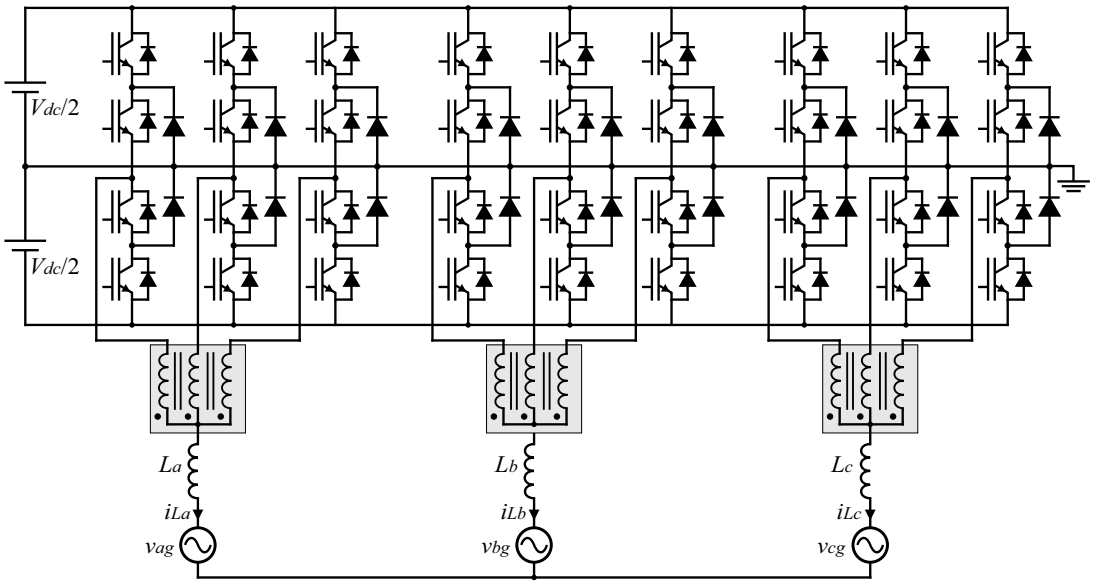


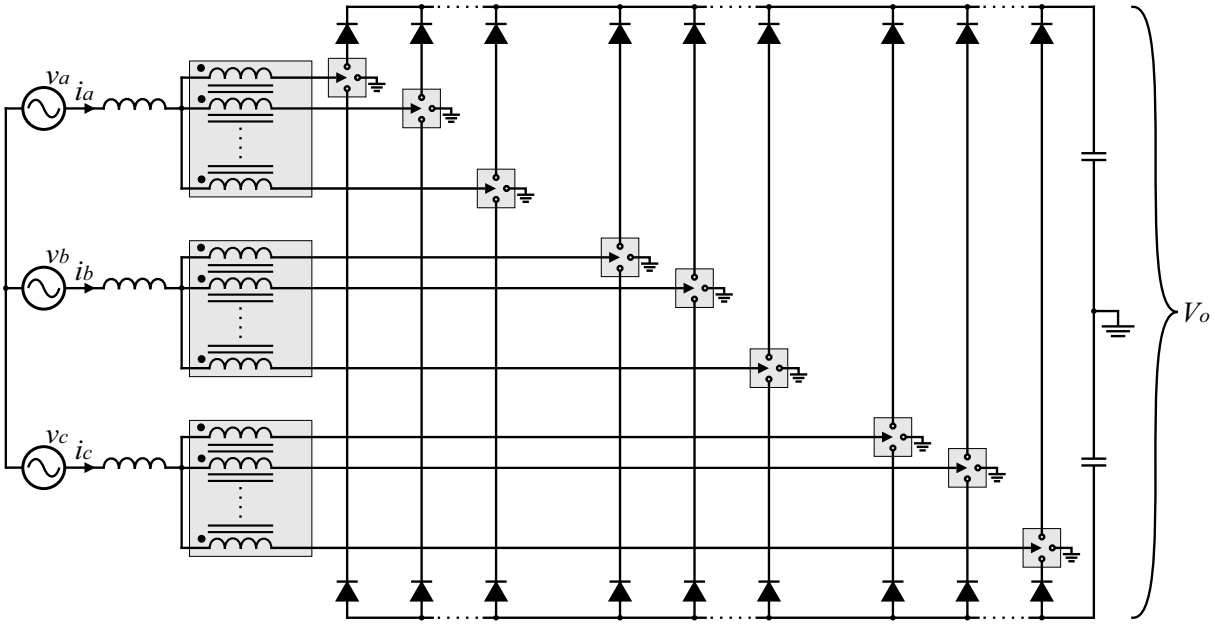
Fig. 14 – Three-phase NPC inverter with 4SSC [53].



The unidirectional three-phase rectifier with MSSC was proposed by [60, 63], where a generalized topology of multilevel three-phase rectifiers was presented with different

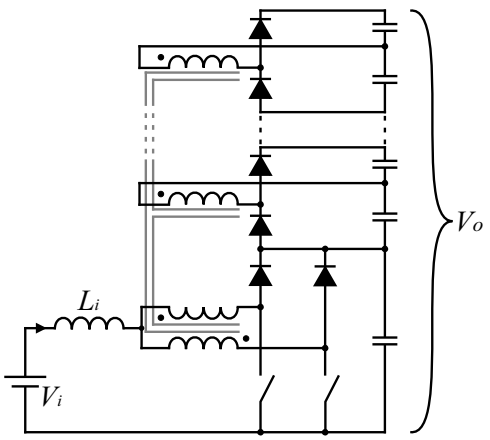
methods for implementing the commutation cell of the structure, as shown in Fig. 15. The voltage stress on the switches is the output voltage divided by two in this structure. This topology has a more simple switching strategy than the NPC structure and requires less gate drivers, but there are voltage balance issues when expanding it into more levels such as the NPC.

Fig. 15 – Three-phase unidirectional multilevel rectifier with MSSC [60].



The presented topologies are suitable for high input current, however they present limitations for higher voltage gains. Some of the topologies can achieve higher voltage gain by increasing the number of levels, but they increase in complexity and may require more switches that demand isolated gate drivers. There are dc-dc topologies in literature that can achieve higher voltage gain, such as the converter presented in [64] (See Fig. 16), which inserts secondary windings on in the interphase transformer connected to Delon circuits in their outputs to multiply the voltage gain. This converter presents limitations in higher voltage gains due to the transformer isolation. Also, this structure does not operate appropriately for duty cycle values lower than 0.5.

Fig. 16 – Boost converter with 3SSC and voltage multiplier [64].



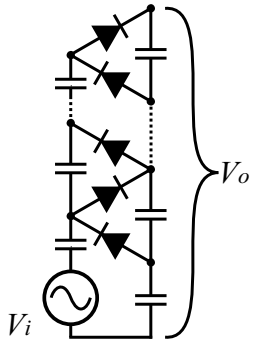
Some alternatives presented in the literature suggest the use of SC voltage multipliers for achieving higher voltage-levels. However, there are not ac-dc structures in literature integrating SC cells to multistate switching cells. A literature review on SC based converters will be performed in the next section, in which these other topologies will be presented.

1.3 LITERATURE REVIEW: SWITCHED CAPACITOR CONVERTERS

The popularity of SC converters has increased in power electronics recently, possibly due to the improvement of capacitors for high frequency applications and advances semiconductor materials. These converters can provide high voltage gain, reduce the voltage stress across the switches and do not require inductive elements, thus avoiding voltage spikes that may occur due to leakage inductance in magnetic elements. Besides, they present good stability, modularity and their voltage gain can be increased by cascading more cells [65, 66].

The SC concept was first described by Maxwell [67] and introduced first for voltage doubling by Villard [68]. This concept was expanded in [69], where the Villard circuit was cascaded into more levels, thus conceiving the SC cell that today is known as the Greinacher or Cockcroft-Walton (CW) voltage multiplier [70], illustrated in Fig. 17.

Fig. 17 – Greinacher/CW voltage multiplier [71].

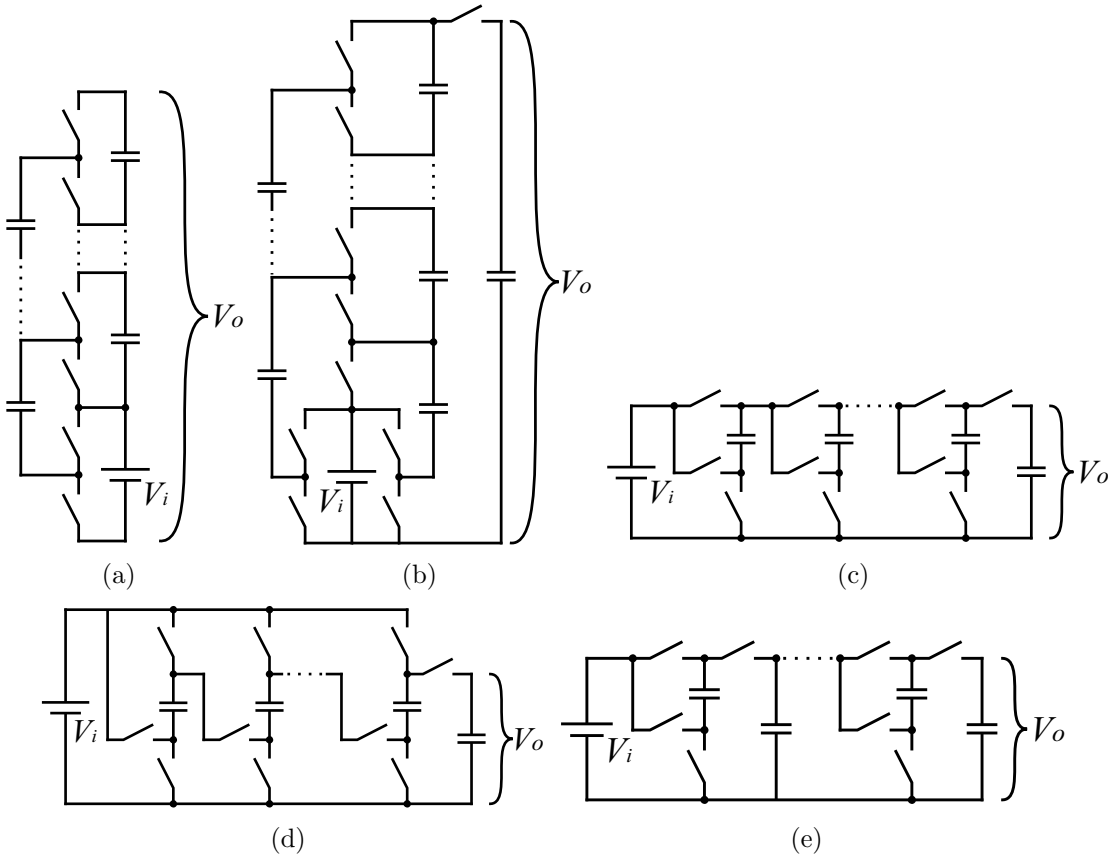


The operation principle of the SC converters is based on the energy transfer of capacitors that are associated in parallel in different operational stages. At the moment that two capacitors are connected in parallel, the capacitor with the lowest voltage ideally acts as a short-circuit connected to a voltage source equivalent to the difference of the voltages between the two connected capacitors [72]. The only elements that limit the charging current of the capacitors are the parasitic resistances and inductances in the current path, although these elements can also be inserted in the circuit in order to limit the capacitor charge current or to use the resonance caused by the inductive elements to achieve soft-switching [73]. It is also important to design the capacitors properly, so that they maintain the charge between two operational stages, resulting in a lower difference in the voltages when two capacitors are connected in parallel, thus reducing the peak and RMS charge and discharge currents [74, 75].

Due to their operation principle, SC cells have discrete voltage gains which are defined by the topological configuration and by the number of cascaded cells. Some of the most common SC voltage multiplier topologies are the Ladder, Dickson, Fibonacci, Series-Parallel and Doubler topologies, shown in Fig. 18. The main drawbacks of SC cells are the

voltage regulation and number of active switches. The voltage gain of SC converters can be regulated by changing the duty cycle or switching frequency [76], but doing so is not recommended. One of the reasons is the non-linear static gain that is significantly affected by parasitic elements. Besides, SC converters behave as linear sources when the output voltage is controlled and the converter efficiency is equivalent to the difference between the output voltage and input voltage divided by the ideal gain. This occurs because the voltage drop in the output is due to the power dissipated on parasitic elements of the circuit [77].

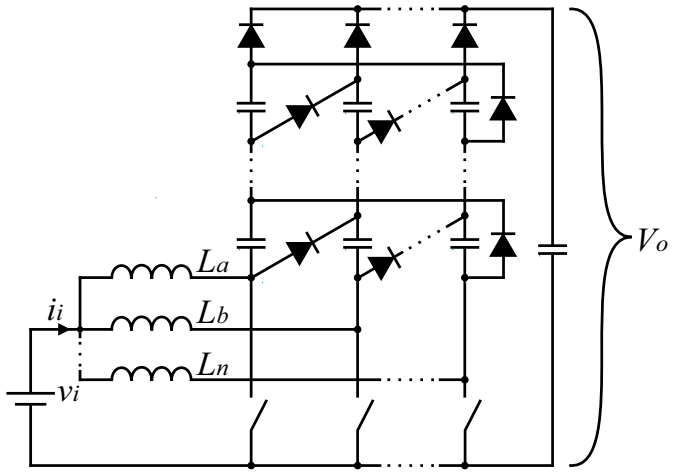
Fig. 18 – SC cells [78]: (a) Ladder, (b) Dickson, (c) Fibonacci, (d) Series-Parallel, (e) Doubler.



One alternative to overcome these disadvantages by integrating these converters in basic topologies with inductive accumulation. By proposing hybrid topologies, it is possible to obtain non-isolated structures with high voltage gain and low voltage stress on the switches.

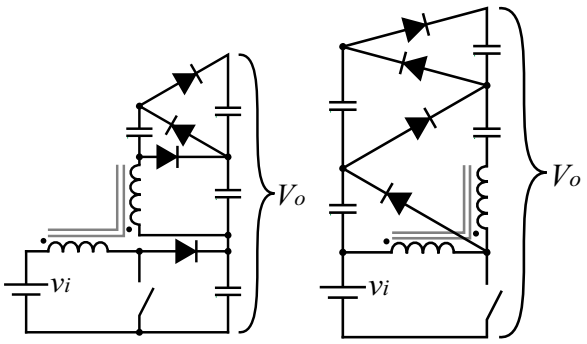
The use of hybrid SC topologies was proposed by [79] for achieving high convertion ratios with the Ćuk converter. In [80], a high step-up hybrid converter based in this concept was proposed by inserting a voltage multiplier cell into an interleaved boost converter, as shown in Fig. 19. This structure multiplies the voltage gain of the boost converter, divides the current stress on the switches and can be expanded into more levels in order to increase the voltage gain. The topology can also replace the inductors for a MSSC, use active switches for bidirectionality and be associated with other basic topologies [81]. The main drawback of this converter is the voltage stress of the SC diodes, that is twice the voltage across the capacitors of the voltage multiplier cell. Therefore, this topology is more suitable for applications with low input voltage.

Fig. 19 – Generalization of interleaved boost converter with voltage multiplier cells [80].



In [82] the integration between the CW cell and the boost-flyback converter was proposed, as well as the integration of the CW with other basic topologies with a coupled inductor, as shown in Fig. 20. In this topology the diodes and capacitors can operate with a lower voltage stress by adjusting the turns ratio of the coupled inductor. However, this topology requires requires more components than the previous converter.

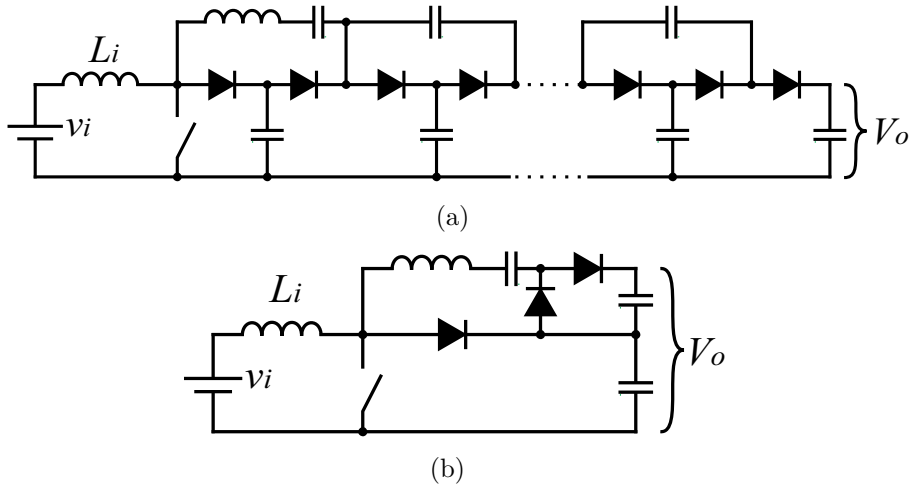
Fig. 20 – Boost-flyback converter with CW SC cell [82]: (a) Conventional boost-flyback structure, (b) Input power sharing.



To reduce the number of components of the CW cell and achieve high voltage gain with low voltage stress, one alternative is to integrate the ladder SC cell to the boost converter, as proposed in [83]. This topology can be implemented with a single output capacitor [Fig. 21 (a)] or integrate the voltage multiplier capacitor with the output [Fig. 21 (b)]. The inductor inserted in series with the capacitors of the voltage multiplier is optional. The capacitor current is limited by parasitic resistances in the circuit, but an auxiliary inductor can be added to reduce the peak current in the capacitor at the start of an operational stage, which can reduce the capacitor size and can be used to achieve soft-switching [73, 84, 85].

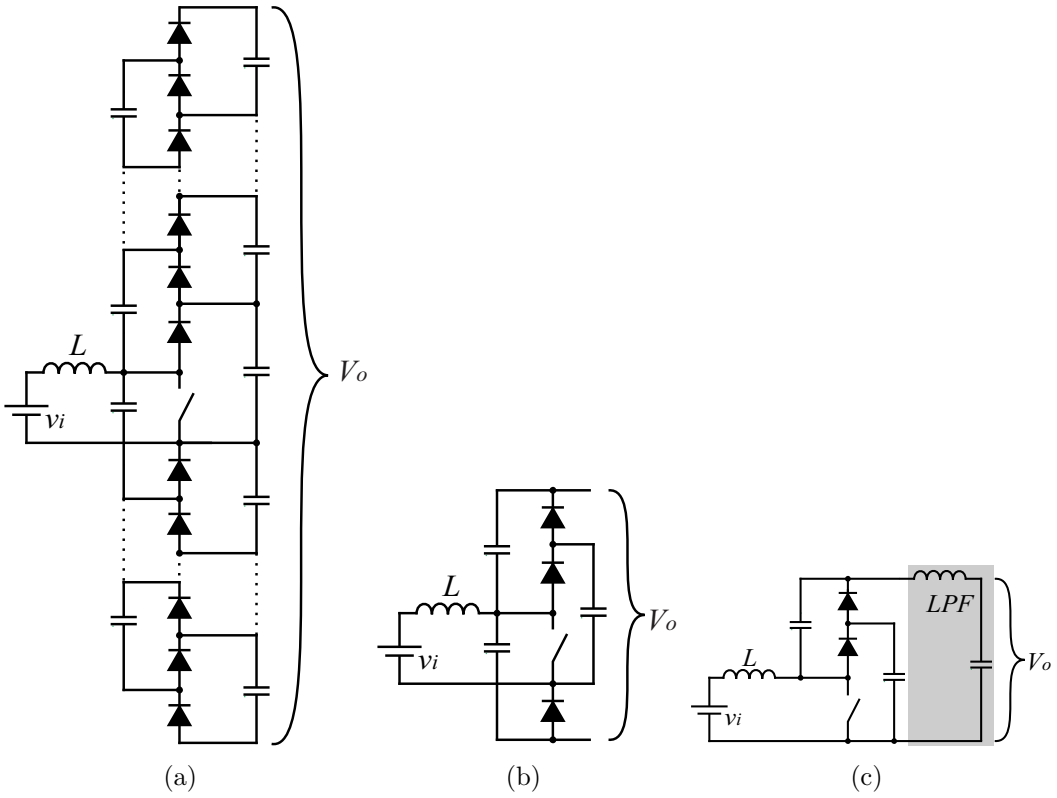
The study of the hybrid boost converter (HBC) with the ladder SC cell integrated to the output capacitor was expanded in [86, 87] and generalized in [88], in which new topologies were derived based on the association of the ladder SC cell and basic converter topologies. In this study, a generalized structure of the hybrid boost converter was proposed, as illustrated in Fig. 22 (a). Fig. 22 (b) and (c) show other ways of implementing

Fig. 21 – Hybrid boost converter with ladder SC cell [83]: (a) 'M' voltage multiplier cells, (b) Output capacitor integration into the cell.



the cell by using a symmetric configuration and using low-pass filters in the converter output.

Fig. 22 – HBC [87]: (a) Generalization, (b) Symmetric configuration, (c) Output with low-pass filter.

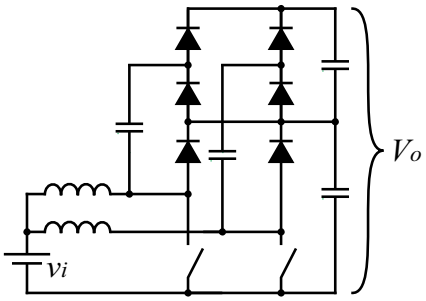


The study performed in [88] had also proposed the integration of the ladder SC cell with the interleaved boost converter (See Fig. 23) in order to reduce the current stress in the components. The converter uses more switches than the topology proposed in [80], but it can be advantageous in some applications with higher input voltage due

to the lower voltage stress across the diodes, since diodes with lower breakdown voltage value are usually less expensive and present faster dynamics. The fast dynamics of these devices also allow the switching frequency to be increased, thus reducing the size of passive components.

Other dc-dc topologies have been proposed in the literature to integrate SC cells with interleaving techniques, such as [89], which uses a variation of the topology presented by [80] with a differential connection in the SC cell, but does not present a generalized approach. In [90] an interleaved converter that uses SC cells has also been proposed. The topology has a lower device count compared to the HBC for some configurations, but it requires a number of SC cells equivalent to the number of interleaved inputs.

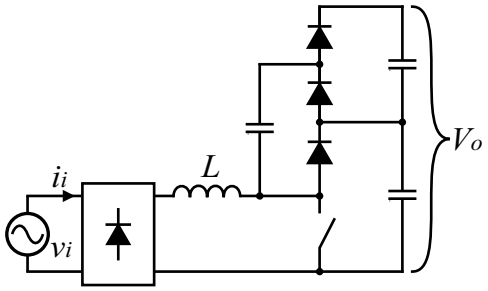
Fig. 23 – Hybrid interleaved boost converter with ladder SC cell [88].



The HBC is going to be one of the main subjects of study of this thesis because it provides high voltage gain with low voltage stress on the switches and has a common source for all switches. Furthermore, since this work focuses on the study of rectifiers, that are usually supplied by the grid and can achieve high capacitance voltages, the ladder SC cell is more suitable for this study than other SC cells due to the voltage across the devices. The variation of the topology shown in Fig. 23 is going to serve as the base for the proposed rectifiers in this thesis, because one of the objectives is also to reduce the current stress on the devices of hybrid SC converters.

Several dc-dc, ac-dc, dc-ac and ac-ac topologies were proposed after the ladder SC cell [91–98]. The integration of the ladder SC cell with the boost PFC rectifier was proposed in [99, 100]. The rectifier provides high voltage gain with low stress on the switches and high power factor without adding active switches or increasing the complexity significantly, compared to the conventional boost PFC rectifier. The hybrid boost rectifier (HBR) is shown in Fig. 24.

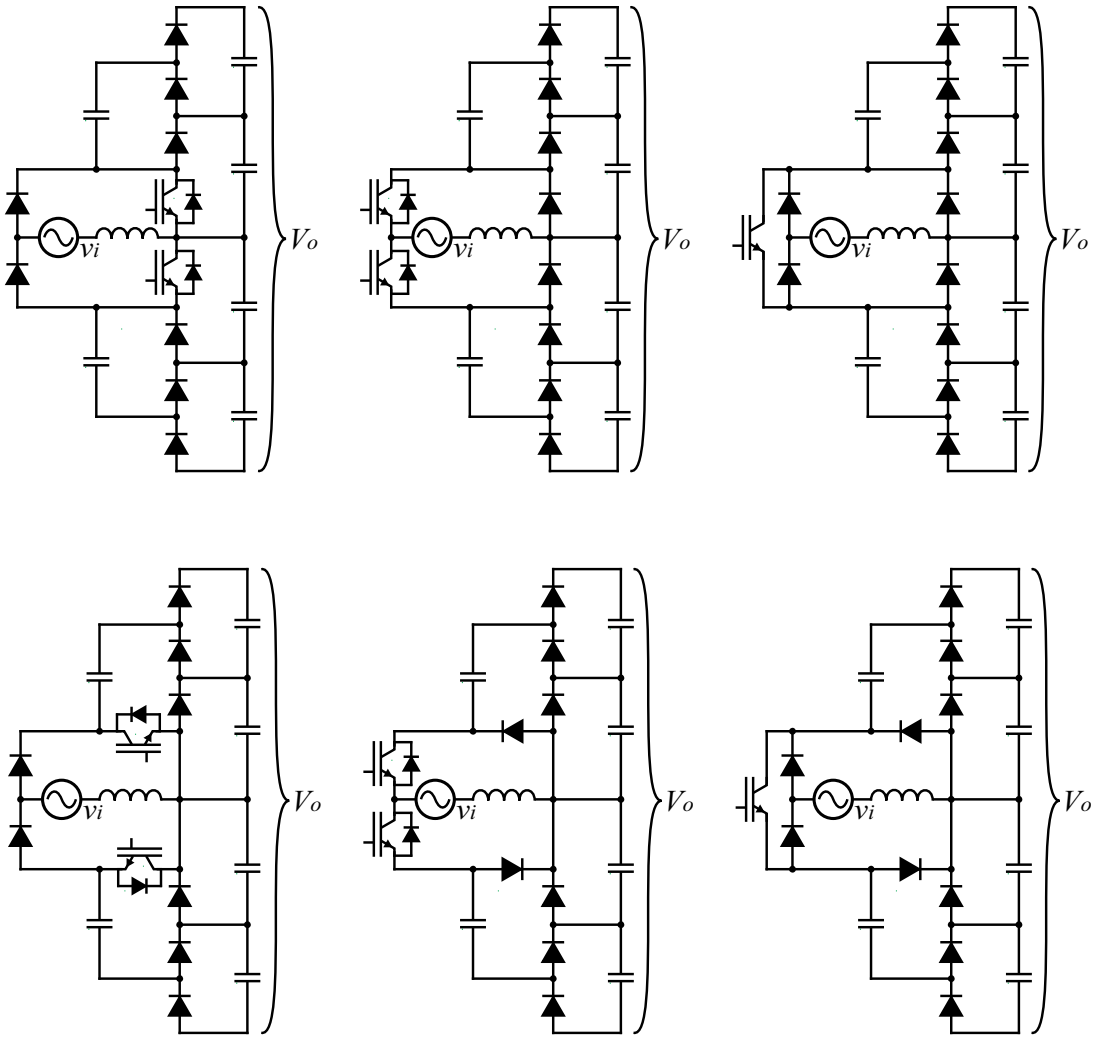
Fig. 24 – HBR [99].



A family of three-level rectifiers based on the HBR was proposed in [33, 101]. These rectifiers provide lower harmonic content in the input inductor current and use less

switches than the conventional HBR for the same voltage gain, since some topological variations are bridgeless versions of the converter. However, like in conventional doubler rectifiers, they require an additional control loop for the output capacitors voltage balancing and the topologies are more suitable for an even number of cascaded SC cells and a multiplication factor above four. The three-level HBR converters are shown in Fig. 25.

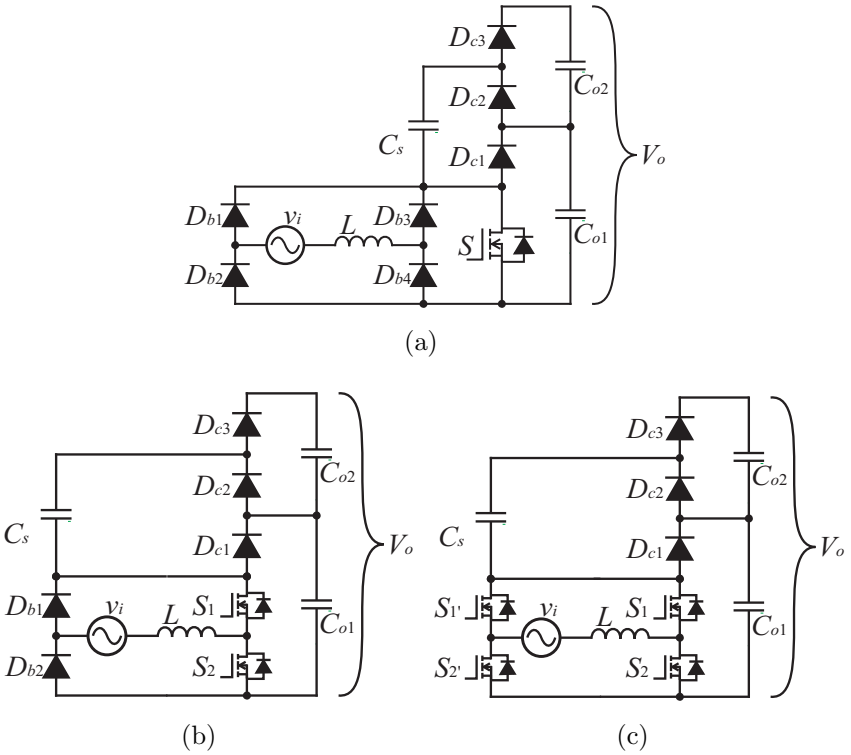
Fig. 25 – Three-level single-phase HBR with different switching cells [101].



Two two-level bridgeless variations of the HBR were proposed in [102, 103] by the author, where the input inductor of the HBR was transferred to the AC side an the commutation cell was modified. The proposed topologies use less switches and present better efficiency than the conventional HBR. Another advantage is the use of a single gate signal for all switches, typical of unidirectional bridgeless boost topologies. The major drawback is the additional active switches compared to the conventional HBR. The bridgeless variations of the HBR are illustrated in Fig. 26.

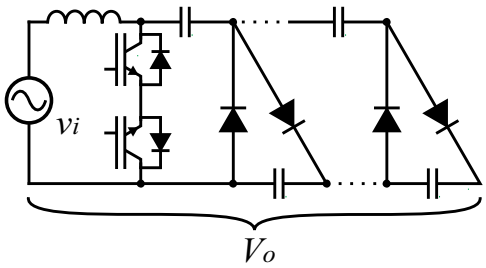
Other rectifier topologies can also be derived from the integration between different basic topologies and SC cells, such as the topology presented in [104], that uses a matrix input with bidirectional switches associated with the CW cell, which is not advantageous compared to the other topologies mentioned. This converter was modified into a simpler version using a single four-quadrant switch (typically composed of an association of two or more switches) and uses less semiconductor devices than the HBR with a ladder cell.

Fig. 26 – HBR with inductor on AC side [102]: (a) HBR with diode bridge, (b) Bridgeless HBR with two switches, (c) Bridgeless HBR with four switches.



However, this topology requires more capacitors than the ladder based HBR. The HBR with a CW cell is illustrated in Fig. 27 [105].

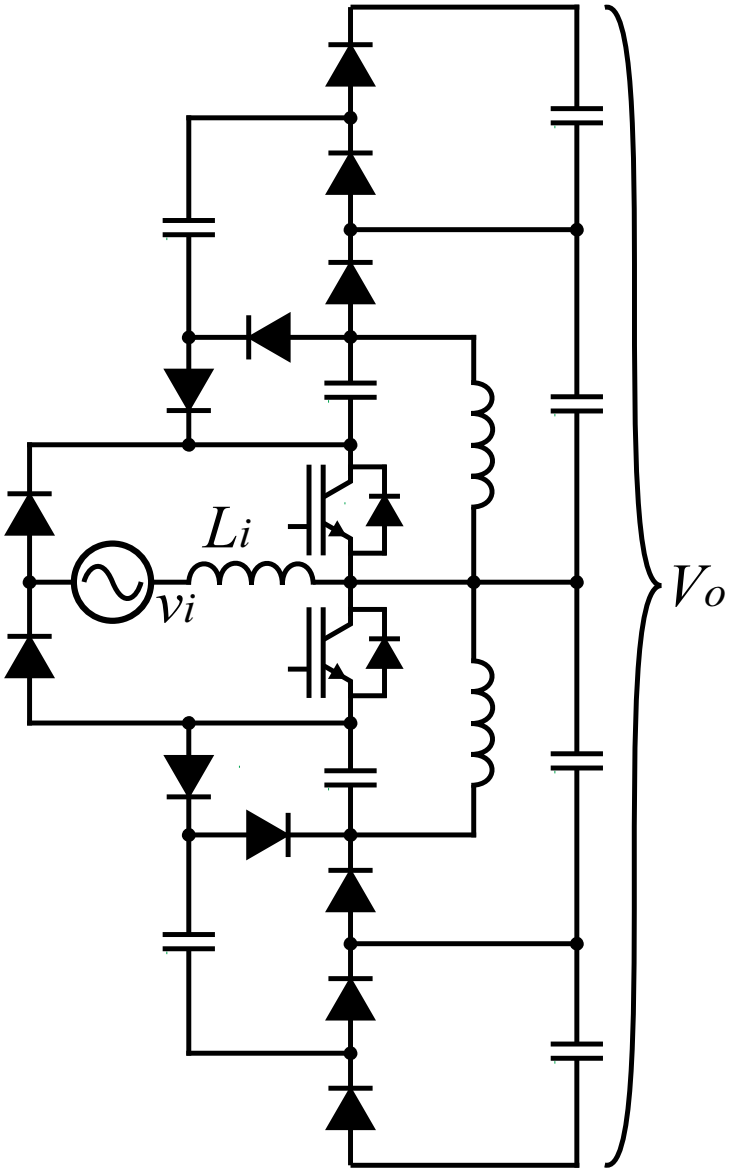
Fig. 27 – Bridgeless HBR with CW cell [105].



SC cells can also be associated with other rectifier topologies as long as they have voltage-fed stage, such as the boost output or the buck input stages. It can also be integrated to the coupling capacitor of indirect converters, as proposed in [106], in which the ladder SC cell is integrated with a SEPIC converter, shown in Fig. 28. The SEPIC rectifier uses more passive and active devices than the other hybrid topologies presented, but it offers an advantage regarding the control complexity. When operating in DCM, the converter can be controlled by a constant duty cycle reference to control the output voltage. There is no need for an input current control loop, since the input inductor average current naturally follows the input voltage shape. This increases the robustness of the converter, reduces the control complexity and removes the input sensors required in CCM converters.

For applications with higher power levels with higher voltage, SC cells can be in-

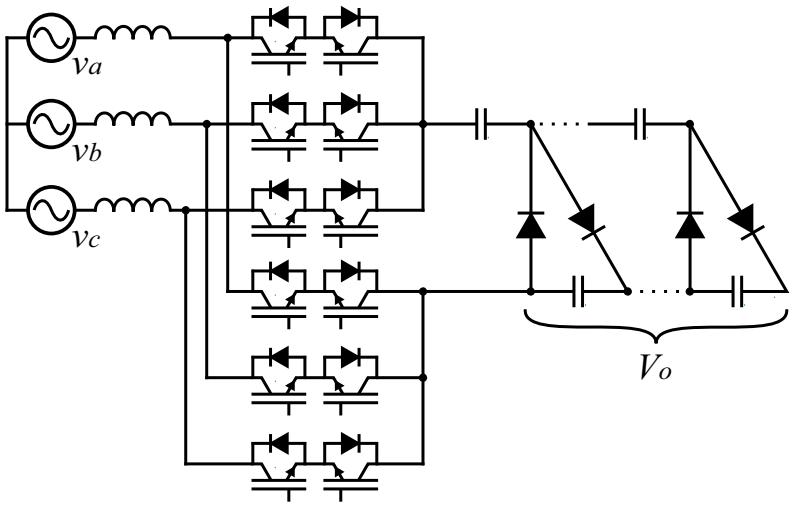
Fig. 28 – Hybrid SEPIC rectifier [106].



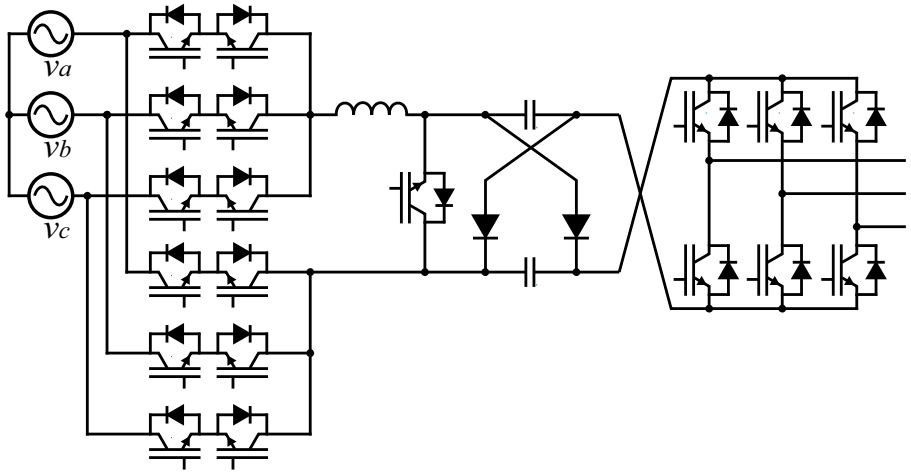
tegrated with three-phase converters. In [107] a three-phase rectifier was conceived by integrating the CW cell with a current-fed three-phase-to-single-phase matrix converter, which is used to generate the single-phase alternate signal for the CW multiplier. The major disadvantages of this topology are the complexity, use of bidirectional switches and the power processed by the CW multiplier, which is the sum of the input power in the three phases. Another matrix converter based on hybrid SC converter was proposed in [94], where an HBC was used to boost the intermediary stage. In the same way as the CW based topology, the converter also has the disadvantage of using a single-phase stage to process all the power. The CW rectifier with a three-phase-to-single-phase matrix input is illustrated in Fig. 29 (a) [107], and the indirect matrix converter is illustrated in Fig. 29 (b) [94].

In [108] a hybrid multilevel three-phase rectifier was proposed. Although it uses more components than the matrix topologies, it has several advantages, such as a control strategy with lower complexity, less active switches and the output power divided by three legs with SC voltage multipliers connected to each one of them, whereas in the matrix

Fig. 29 – Hybrid matrix converters: (a) CW rectifier with a three-phase-to-single-phase matrix input [107], (b) HBC in the intermediary stage of an indirect matrix converter [94].



(a)



(b)

topologies a single voltage multiplier has to process the entire output power. The hybrid multilevel three-phase rectifier is shown in Fig. 30 [108].

A bidirectional three-phase inverter using the SC concept was proposed in [109]. This structure is a high step-down converter that can change its power flow from the AC to the DC side and perform as a high step-up rectifier. The structure has the disadvantage of using many switches and requiring many isolated gate drivers. The three-phase hybrid inverter is shown in Fig. 31 [109].

Other three-phase structures can also integrate SC cells to achieve high gain, such as the SEPIC rectifier, proposed in [110]. Like the single-phase version, the three-phase rectifier does not need an input control loop, which is a significant advantage in three-phase systems. The major disadvantage is the high number of components of the SEPIC converter. The three-phase SEPIC rectifier is shown in Fig. 32 [110].

Hybrid three-phase rectifiers integrated with SC cells are still new technologies and there are few works related in the scientific literature, since the use of SC cells in power electronics is recent. One of the main objectives of this work is to propose a solution to

Fig. 30 – Hybrid multilevel three-phase rectifier [108].

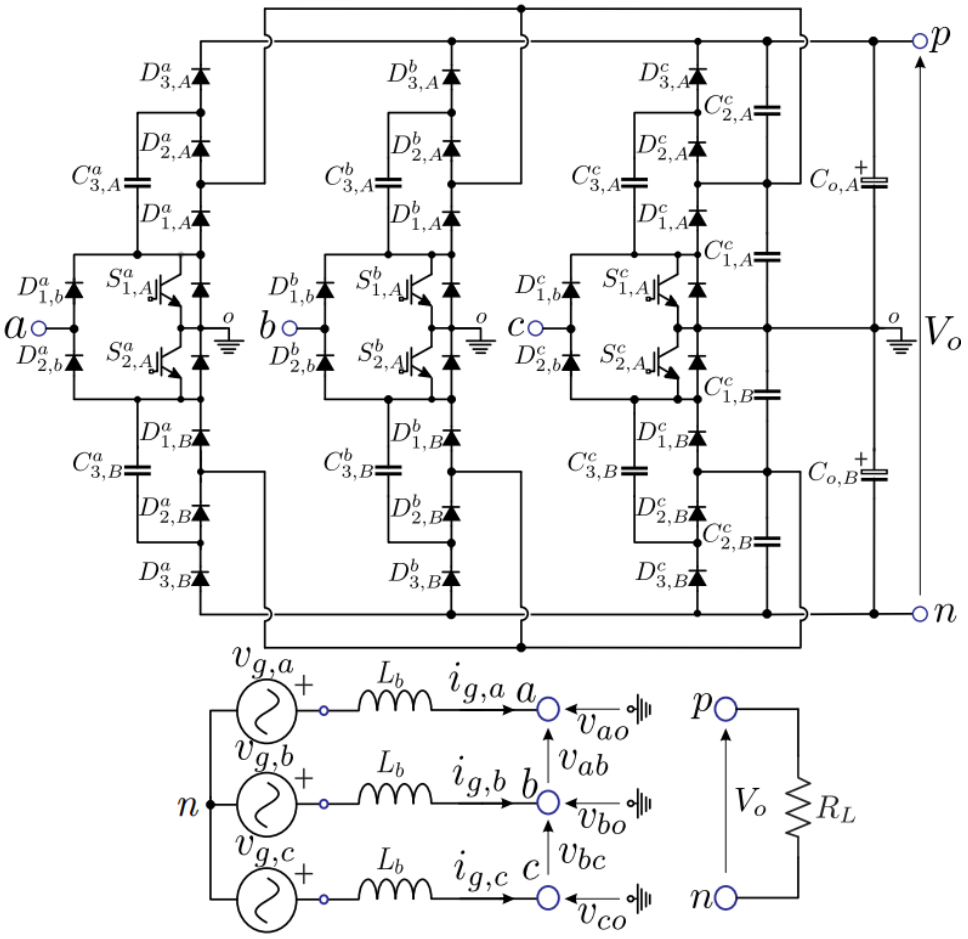


Fig. 31 – Hybrid three-phase inverter [109].

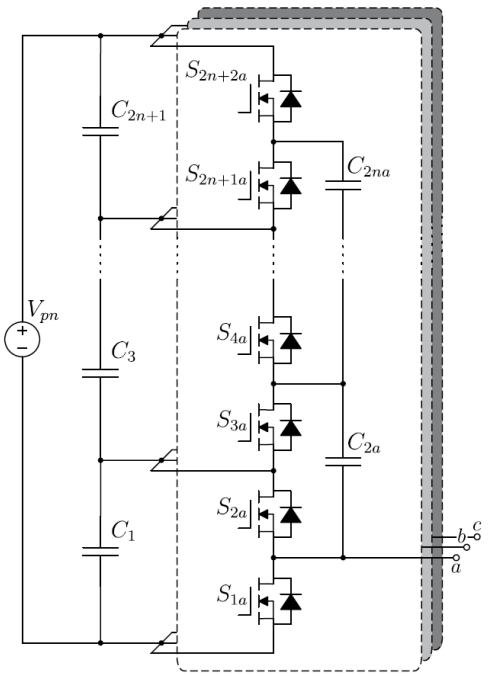
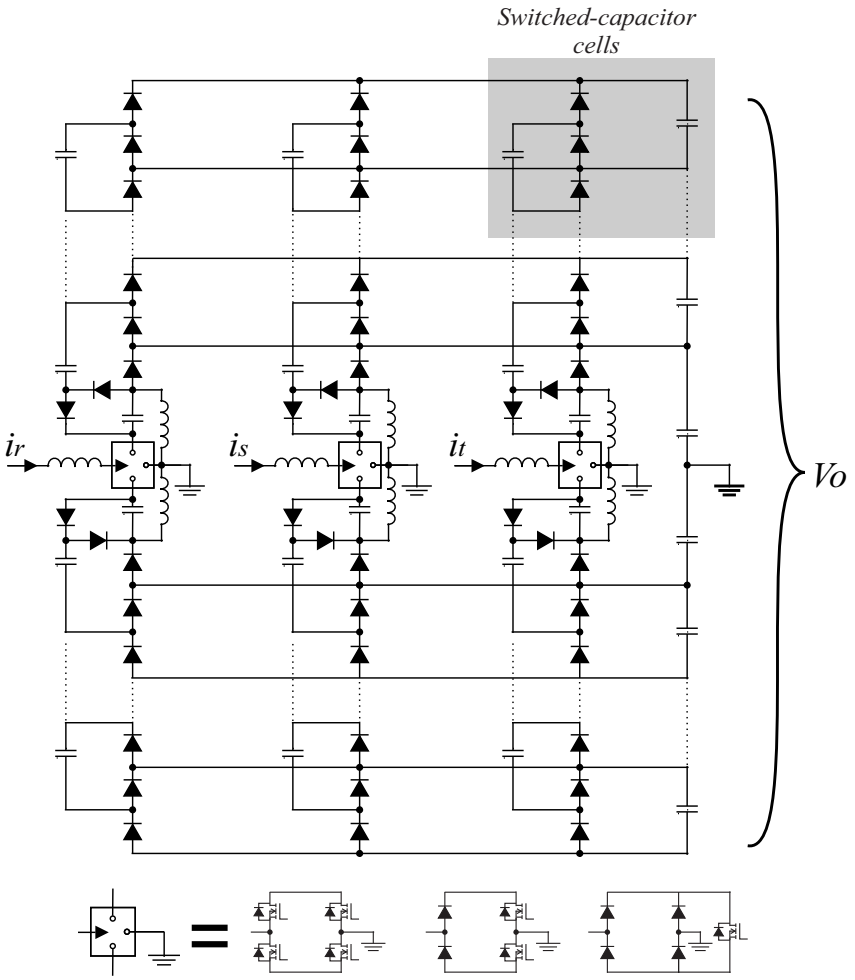


Fig. 32 – Hybrid three-phase SEPIC rectifier [110].



reduce the current stress in hybrid SC rectifiers, that is possibly the main reason why SC structures are not yet widely studied for higher power applications.

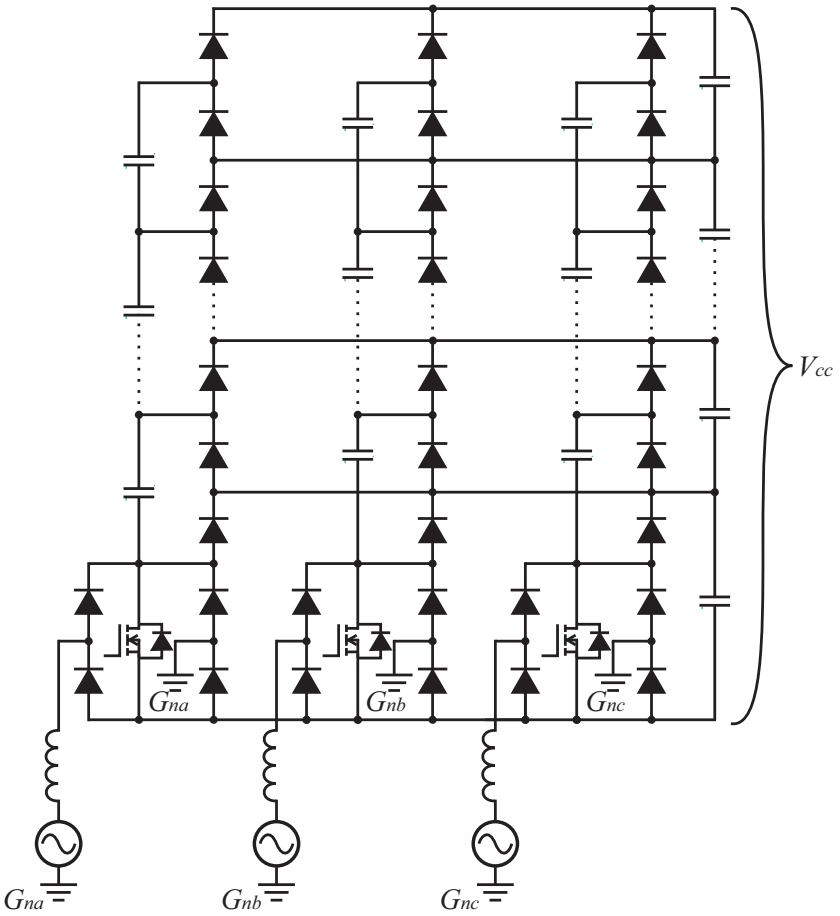
1.4 PROPOSED TOPOLOGIES

This work is a continuation of the master's dissertation [103]. In that work the topologies shown in Fig. 26 have been proposed. One of the main issues with the HBR topologies is the limited power levels they can operate, because the SC cells cause an increase in the current stress in the switches. Besides, the capacitors are subjected to high current levels as well, hence it is necessary to increase the size of the capacitors to handle the current.

One alternative to increase the power levels would be to develop a three-phase version of the HBR. As stated before, two-level three-phase PWM rectifiers usually require bidirectional commutation cells due do the coupling of the phases, otherwise they cannot provide high input power factor, unless they operate in a six-wire configuration. The first structure proposed in this thesis is a modular configuration of the topology, that was published in [57]. The structure is capable of achieving high voltage gain and dividing the voltage stress across the switches. Its main disadvantage is the limited range of applications, since it can only be used with generators with open-ended windings. The

topology also has limitations concerning the current levels, like the single-phase versions. The proposed topology is illustrated in Fig. 33.

Fig. 33 – Hybrid modular three-phase boost rectifier.

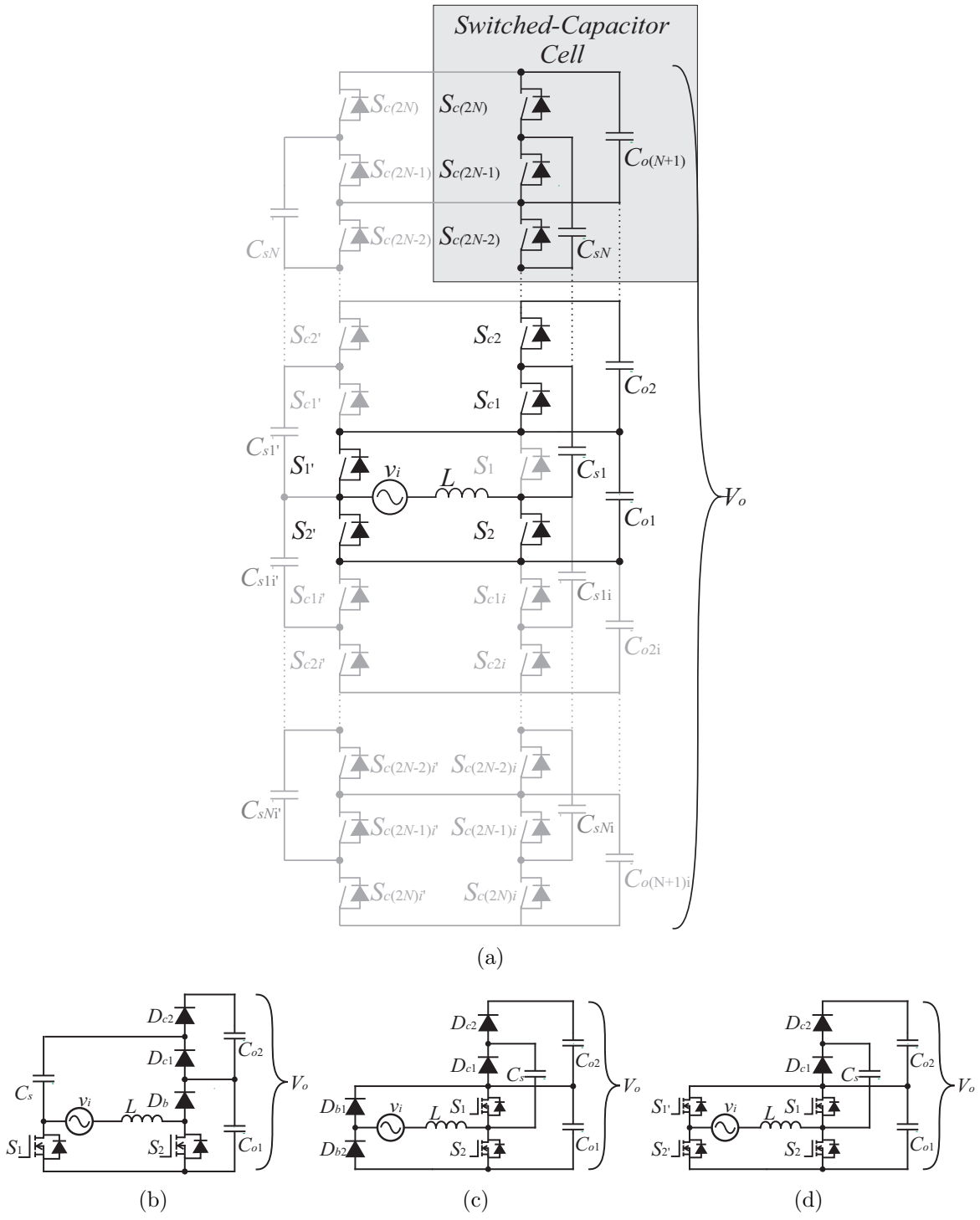


In order to reduce the topology into a 3-wire input rectifier, some changes had to be made in the commutation cell. The proposed alternative was to connect the capacitor C_s to the center of one leg. This change modifies the control strategy of the converter and the operation principle, since the HBR topologies proposed in [103] had the same control strategy for both grid half cycles and the new topologies have complementary gate signals. On the other hand, the topologies reduce the number of switches and can be implemented in different configurations. They are advantageous due to the total number of devices and number of devices switching in high and low frequencies. The proposed topologies are shown in Fig. 34 and were published in [111].

The generalized structure shows that there are several methods of implementing the converter. The SC cells can be added to one or both legs. Whether it is added in one leg, the converter requires less components. In this case, the output capacitors are only charged in one grid half-cycle. Besides, one leg must process more power than the other in a single-leg SC cell configuration.

The converter can be expanded by cascading more cells in a symmetrical or asymmetrical configuration. Adding cells alternately is preferable, because each cell receives the energy of the cell before, and the increase in the number of cascaded cells result in more power processed by the cells near the input to compensate the power losses that occur when cascading them.

Fig. 34 – Single-phase rectifiers and configurations: (a) Generalized structure, (b) Common-source, (c) Totem-pole, (d) Full-bridge.



The common-source and totem-pole topology were evaluated experimentally and achieved efficiency values of 97.9% and 97.1%, respectively. The main advantage of the common-source topology is the low number of components. The main disadvantage compared to the other configurations is that all switches are switched in high frequency, whereas in the totem-pole topology the bridge diodes switch in low frequency.

The full-bridge topology uses more active switches, which slightly increases the

complexity of the structure, but it makes the topology more flexible, since it can be controlled in different ways. The switches in the full-bridge configuration can be controlled by a two-level or three-level modulation scheme or as a synchronous totem-pole rectifier. By choosing a three-level modulation, the switching frequency component in the input inductor is doubled, reducing its size. The synchronous totem-pole configuration is also advantageous, since two switches switch in low frequency, which improves the converter efficiency.

The diodes in the proposed structure can be replaced by active switches. By doing so, the converter becomes bidirectional and can operate as a high-step-down inverter. The bidirectional topology operating as an inverter already exists in literature and was presented in [95].

Although the unidirectional topologies that were proposed are significant contributions of this thesis, they do not overcome the limitations of the hybrid SC converters that this thesis proposes to explore, the current stress on the switches. Therefore, these topologies will not be presented in more details in this document, but they will serve as the basis for conceiving the main structures that are proposed in this work. Some of these structures were experimentally evaluated and published in conference and journal papers.

One method to improve the converter capability to process more power is to expand the topology into a three-phase configuration. The three-phase variation of the proposed HBR, shown in Fig. 35, has a similar operation principle to the conventional three-phase boost bidirectional rectifier. The structure can be implemented with SC cells in one or more legs and be configured symmetrically or asymmetrically, like the single-phase variation. Compared to the multilevel topology shown in Fig. 30, it has advantages of using less components and does not need a control loop to regulate the voltage balance across the output capacitors. However, it presents as disadvantage being a two-level topology, which requires bulkier input filters and has a minimum capacitor voltage equivalent to the line-to-line peak input voltage.

The three-phase HBR is also advantageous compared to the modular HBR due to its voltage gain, which is related to the line voltage, such as conventional boost rectifiers. It also uses less components than the modular rectifier. Besides, the use of a 3-wire configuration makes it viable for a wider range of applications. The major disadvantages of the topology compared to the modular HBR are the modelling and control complexity.

By increasing the number of phases, the converter increases its capability of processing more power, but it still has the current stress issues of SC converters. A new solution is proposed in this thesis to overcome the current limitation of SC converters, which is the integration of MSSC cell in hybrid SC converters. Fig. 36 shows a block diagram that illustrates the proposed concept. In this thesis three topologies will be studied with more depth, a dc-dc and a single-phase and a three-phase ac-dc converter. However, the concept can be expanded to more topology variations and load profiles. One advantage of using SC cells at the output is the self-balanced voltage on the capacitors, which can be used to supply loads connected in series, such as half-bridge based converters and multilevel inverters with series input voltage supplies.

Based on the concept presented in Fig. 36, the first proposed topology is a variation and generalization of the interleaved dc-dc converter proposed in [88]. The variation proposed in this thesis uses MSSC cells instead of the interleaved commutation cell. The reason to introduce a dc-dc converter before presenting the rectifier circuits is because the high frequency analysis of the rectifiers is based in the dc-dc converter. The generalized structure is shown in Fig. 37.

Fig. 35 – Three-phase HBR - Generalized structure.

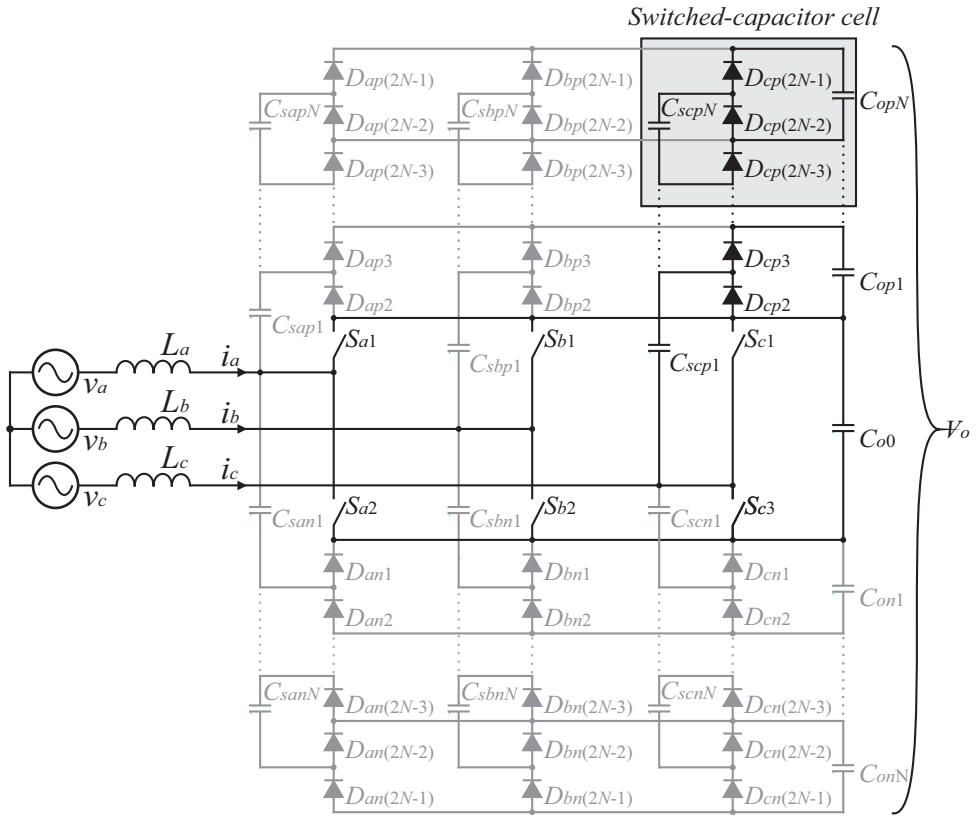
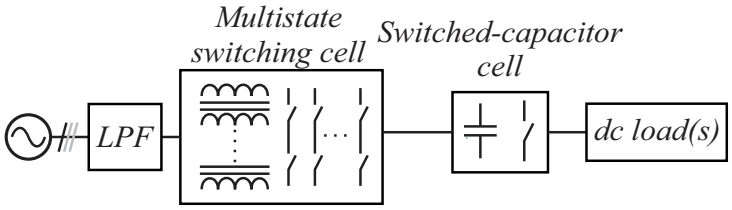


Fig. 36 – Generalization of the proposed concept.



From this converter are derived the ac-dc versions the topologies proposed in this thesis. The first topology, shown in Fig. 38, is the single-phase rectifier that is going to be studied with more details in this thesis. The converter can also be implemented in a bridgeles version, as shown Fig. 39, or a multilevel version, shown in Fig. 40. However, these versions will not be approached with more details herein, their study is suggested as a future work for this thesis.

Finally, the three-phase version of the rectifier was conceived, which is suitable for applications with higher power levels. The converter is capable of multiplying the voltage, as well as dividing the current in the switches and multiplying the switching frequency viewed by the input filter. The three-phase topology that will be studied in this thesis is shown in Fig. 41. One limitation of the structures studied in this thesis is that the minimum voltage across the switches cannot be lower than the input line-to-line voltage. Similar to the single-phase versions, this limitation can be overcome by into a multilevel topology, thus resulting on the topology shown in Fig. 42, which increases the complexity, but reduces the voltage on the switches by half and also reduces the input current harmonic content. This topology is also suggested for future works due to time

Fig. 37 – HBC with MSSC and SC cell - Generalized structure.

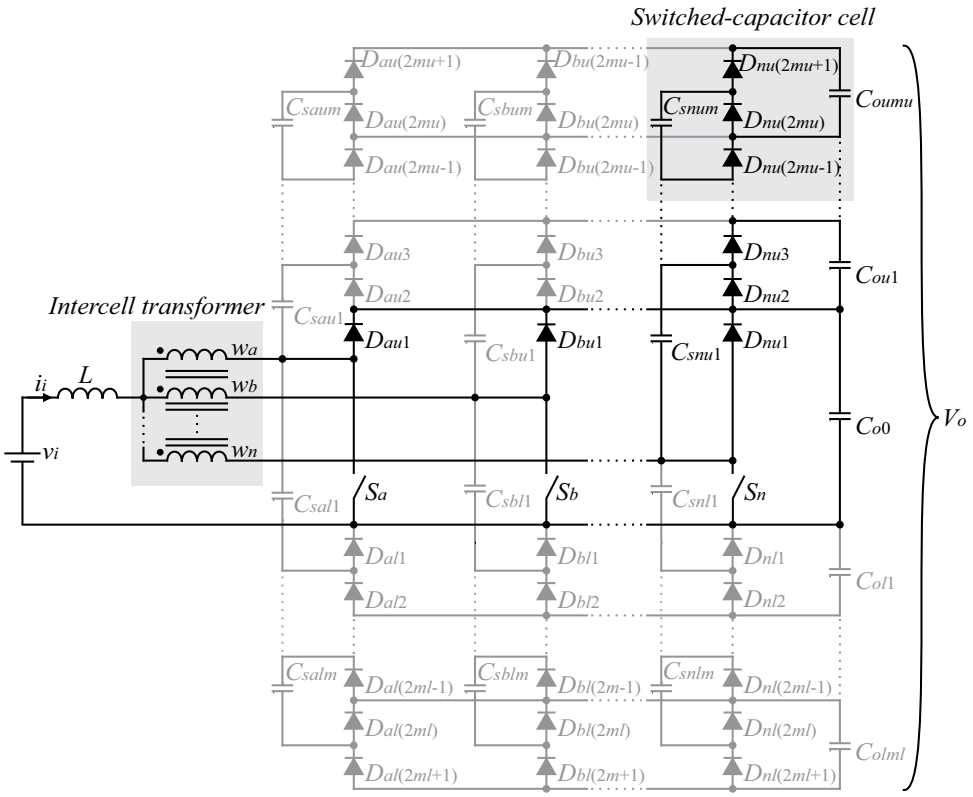
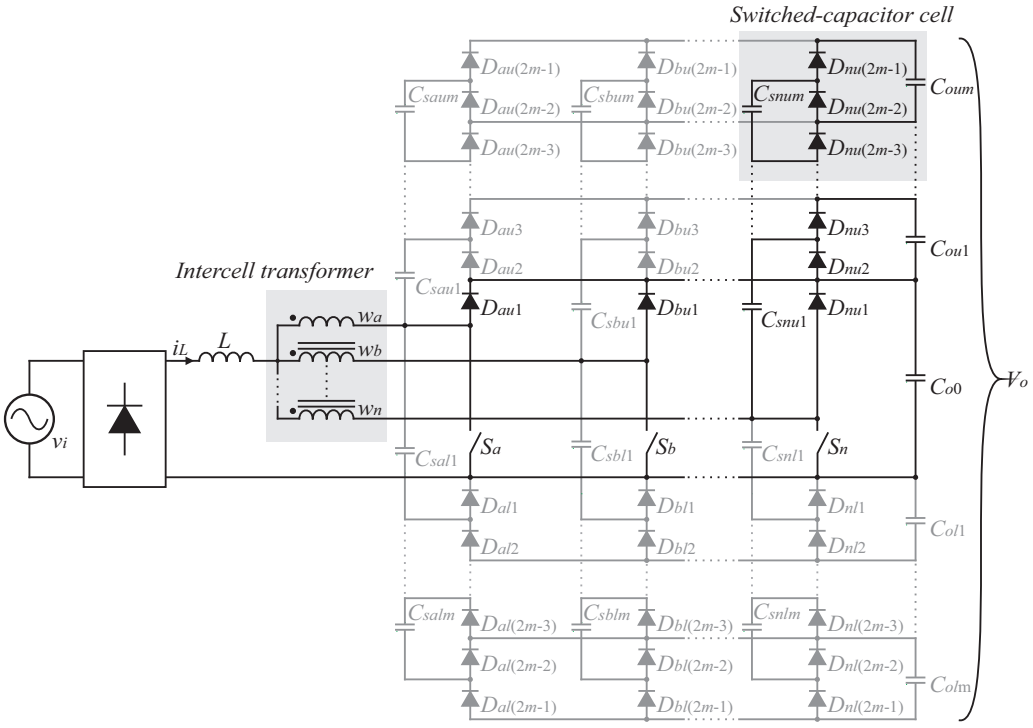


Fig. 38 – Single-phase HBR with MSSC and SC cell - Generalized structure.



limitations and for not being necessary for presenting the concept that is proposed in this thesis.

All topologies with MSSC and SC cells presented in this work can work as bidi-

rectional converters by changing the diodes for active switches, so that they operate as high-step-down inverters. The topologies that will be approached with more details in this work are the dc-dc converter shown in Fig. 37, the single-phase rectifier shown in Fig. 38 and the three-phase rectifier shown in Fig. 41.

Fig. 39 – Bridgeless HBR with MSSC and SC cell - Generalized structure.

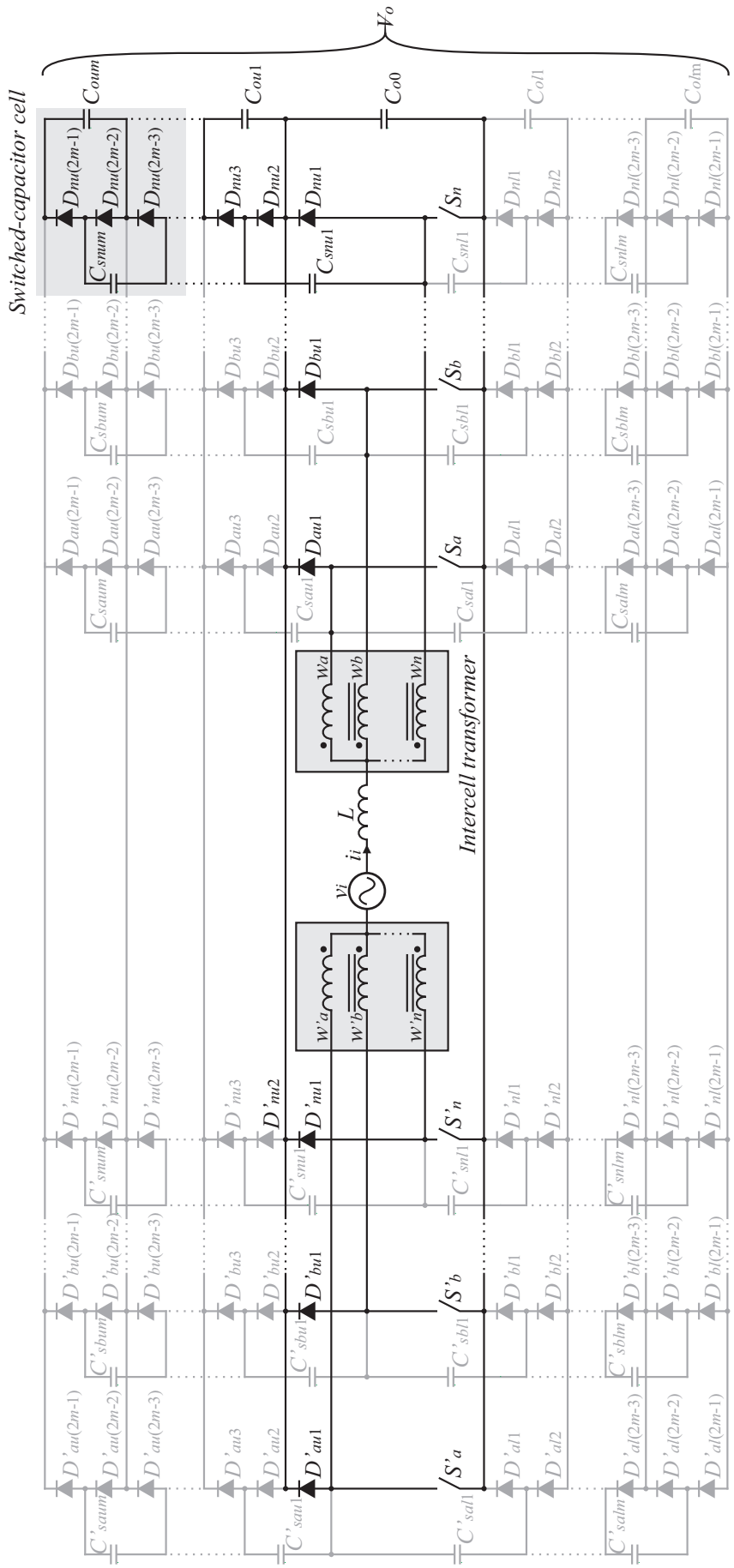
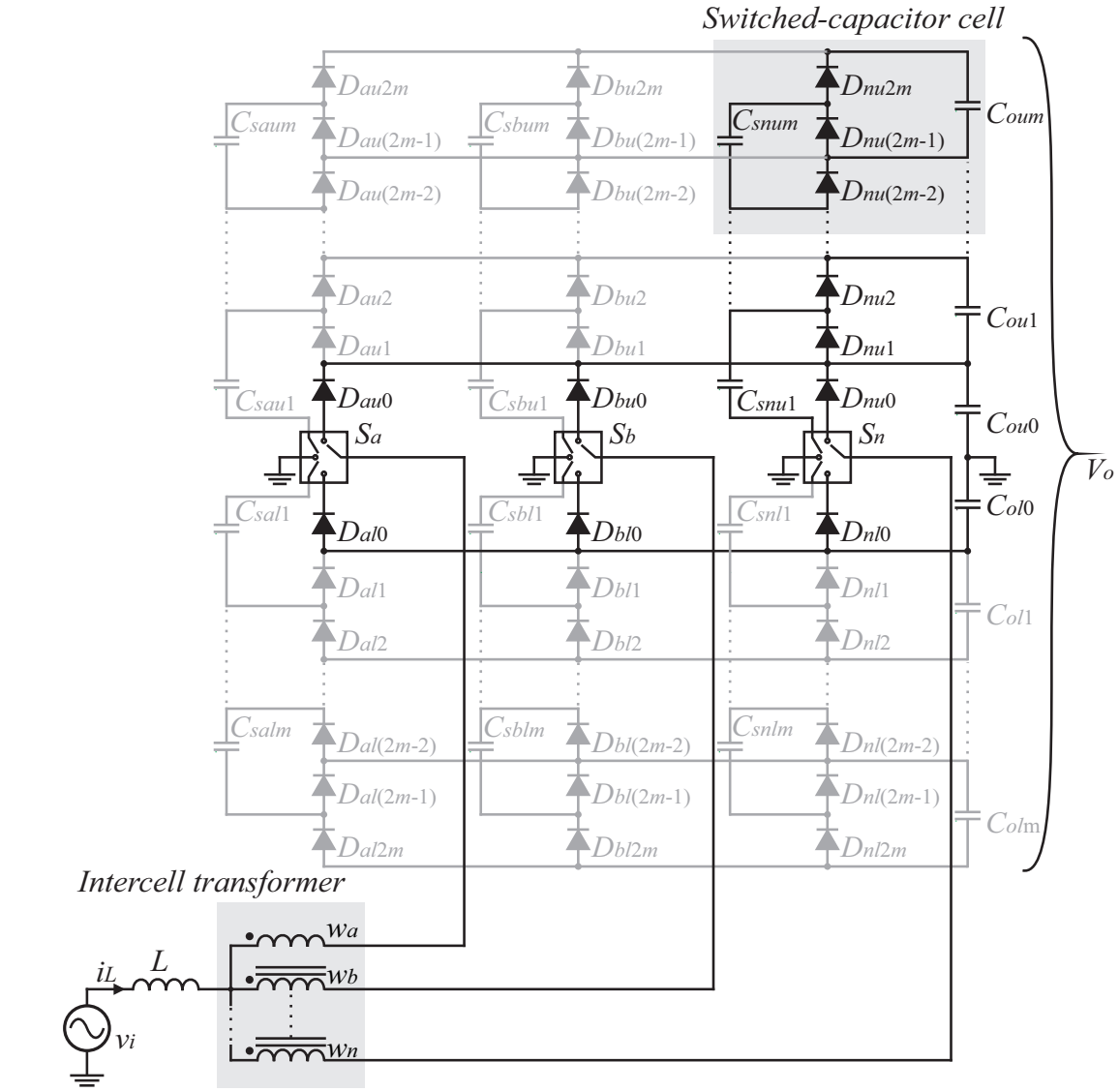


Fig. 40 – Multilevel HBR with MSSC and SC cell: (a) Generalized structure, (b) Switching-cell configurations.



(a)

(b)

Fig. 41 – Three-phase HBR with MSSC and SC cell - Generalized structure.

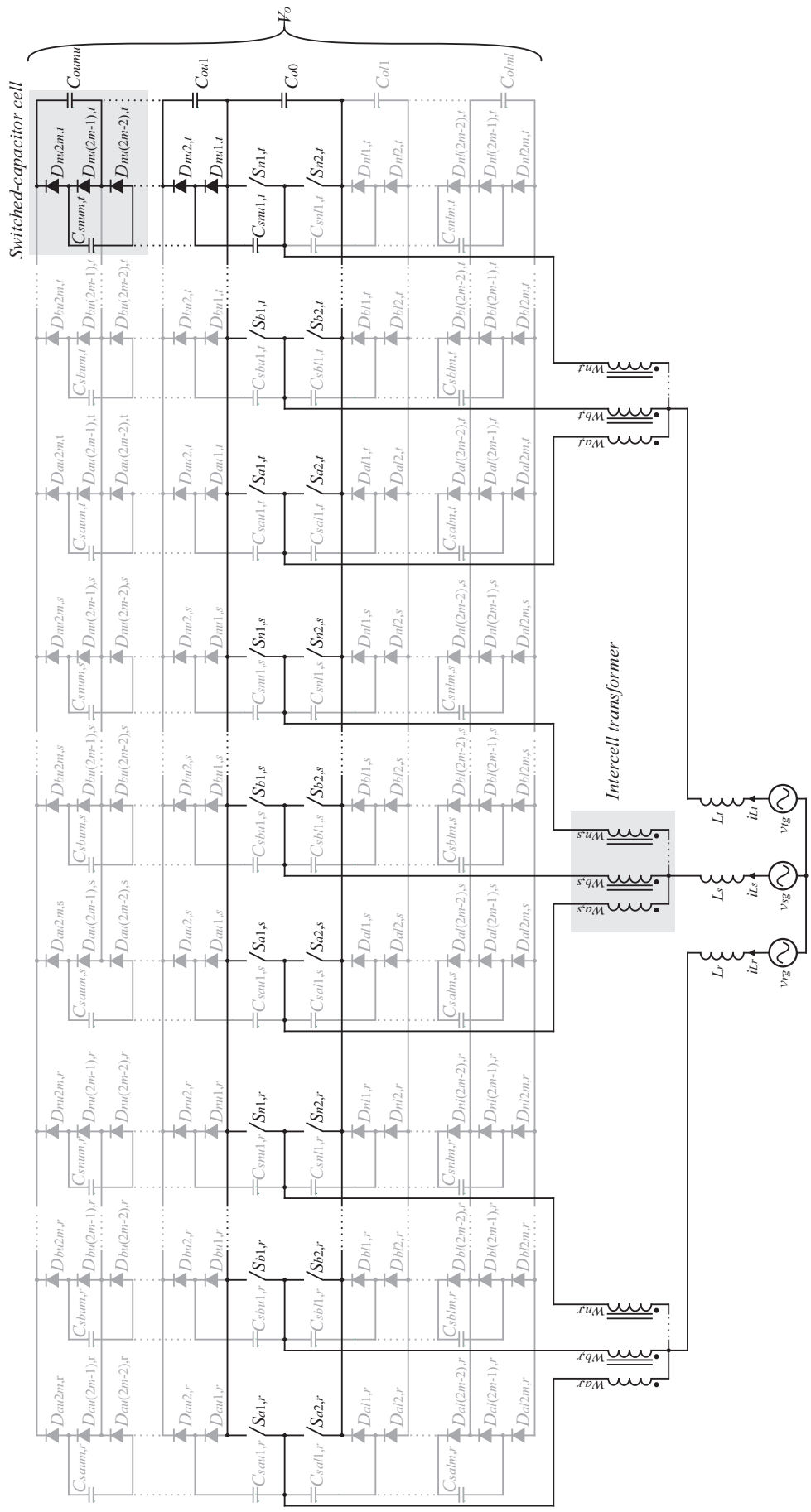
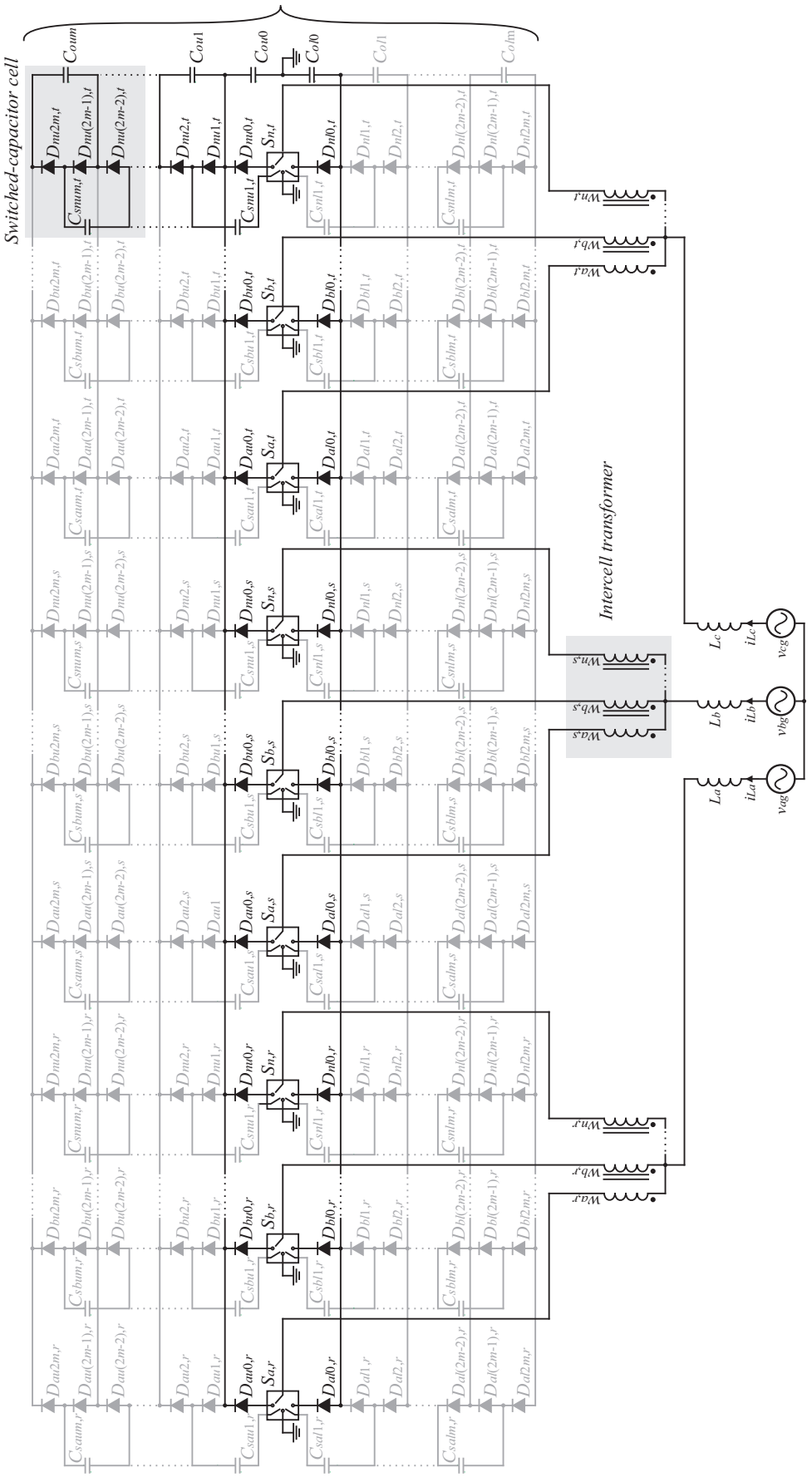


Fig. 42 – Multilevel Three-phase HBR with MSSC and SC cell - Generalized structure.



1.5 STRUCTURE OF THE THESIS

This document is organized in six chapters. In this introductory chapter the state of the art topologies related to high voltage gain was presented and the novel structures proposed in this thesis were introduced.

Chapter 2 introduces the operation principle of SC cells and the modeling strategies that are used for simplifying the analysis of hybrid structures.

Chapter 3 shows the analysis of the boost converter with MSSC and SC cells. The operation principle and modeling strategy of the converter shown in Fig. 37 will be presented for a 100 V input to 1200 V output converter design that operates with a 1 kW output power. The theoretical analysis, simulation and experimental results will be presented for a 3SSC converter with the proposed concept.

Chapter 4 shows the analysis of the single-phase boost rectifier with MSSC and SC cells shown in Fig. 38. Theoretical analysis, simulation and experimental results will be presented for a 127 V input to 1200 V output design example.

Chapter 5 shows the analysis of the three-phase rectifier with MSSC and SC cells shown in Fig. 38. Theoretical analysis, simulation and experimental results will be presented for a 220 V line-to-line input to 1200 V output, 4 kW design example.

Finally, chapter 6 summarizes the contributions of the study, presents the conclusions and suggests future works that could contribute to this research field.

2 SWITCHED CAPACITOR CELLS

2.1 OPERATION PRINCIPLE

SC converters have a different operating principle from conventional converters, since they do not have any current-fed stage. Basic converters with voltage-fed input and output (e.g. buck-boost, flyback) are called indirect converters, because although their input and output are not current-fed there is a current stage, since they have an intermediate inductor that stores energy from the input and transfers it to the output in different operational stages.

SC converters are structures that are based on the direct transfer of energy between the capacitors, which is performed by using different switching combinations to associate capacitors in series and parallel in each switching stage. This affects the voltage regulation of these structures and causes them to have integer discrete gains.

The analysis of SC circuits is different from conventional structures. In basic converters, the parasitic elements of the circuit are often neglected because the influence of the capacitors and inductors on the voltage and current ripple is much more significant than the influence of parasitic elements. In SC converters this simplification cannot be made to choose the components and verify its steady-state characteristic. When a capacitor is connected to another capacitor or voltage source with a different voltage level they behave as short-circuits at that instant, whereas in conventional converters the capacitor is always connected to an inductor or resistor, which provides a soft charge or discharge of the capacitor [72].

The lack of inductive elements added to the circuit also affects the voltage gain, since the gain is not determined by an inductor volt-second or a capacitor current-second relation as in basic topologies, but by the way the capacitors are associated in each switching stage. Therefore, the ideal voltage gain of SC converters is determined only by the topological configuration and number of cascaded SC cells.

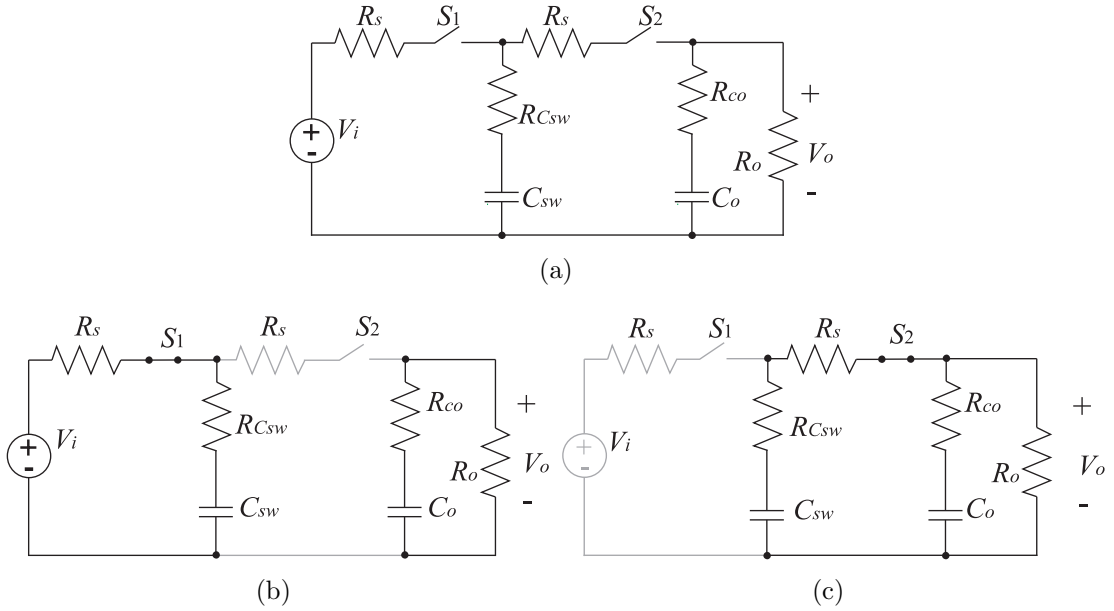
For a better understanding of the operation principle of SC cells, a unity gain SC cell can be used as an example. This structure is widely used in literature to understand steady-state models for SC structures, although there is no advantage in using this structure in practical applications, since its voltage gain is non-linear, depends on parasitic aspects and is directly proportional to the converter efficiency [74, 75, 112–114]. Fig. 40 (a) shows the unity gain SC converter.

The converter operates in two stages. In the first stage, shown in Fig. 40 (b), the capacitor C_s is charged by the input voltage source V_i. The charging current of the capacitor is limited by the series parasitic resistances in the switch and capacitor. The series parasitic elements in the circuit determine the capacitor charging and discharging time constants. Therefore, parasitic elements need to be considered in order to choose the right capacitance value.

In the second operational stage, shown in Fig. 40 (c), the capacitor C_s transfers the energy to the output capacitor C_o and, in the same way as the first stage, the current is limited by parasitic elements. The efficiency of this structure is given by V_o/V_i, since the voltage drop is due to the parasitic resistances and the possibility that the intermediary capacitors cannot store enough energy to transfer to the output in the chosen switching frequency. The efficiency of SC converters can be improved by increasing the capacitance values. A larger capacitance value reduces the voltage ripple and the voltage difference

between the capacitors, thus reducing the voltage across the parasitic resistances and the charging and discharging currents.

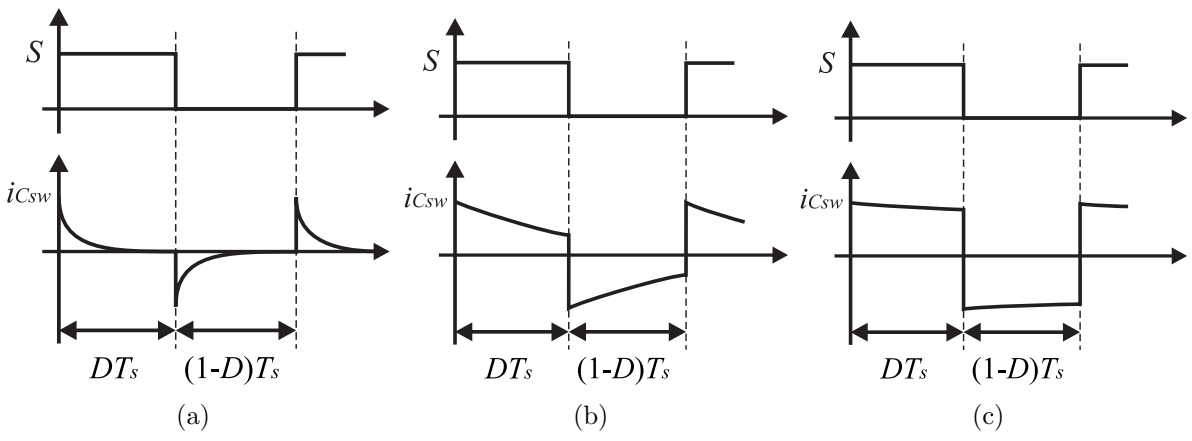
Fig. 43 – Unity gain SC converter: (a) topology, (b) capacitor charging, (c) capacitor discharging.



2.2 CHARGE MODES

The capacitance and resistance values in a SC circuit determine the way the capacitors will charge and discharge. There are three different modes that a SC cell can operate that are related to the charging and discharging times of the circuit. The charging modes are described in Fig. 44.

Fig. 44 – SC charge modes: (a) complete charge (CC), (b) partial charge (PC), (c) no charge (NC).



The CC mode, shown in Fig. 44 (a), occurs when the time constants of the circuit are low and the capacitors charge and discharge completely during one operational stage.

This charge mode can be used to reduce the capacitor size in low power applications that do not require high efficiency and prioritize energy density. The main drawbacks of this mode are the high RMS current values and the voltage drop on the capacitor. In applications with higher power values this mode might be disadvantageous, since the reduction of the capacitor size might result on larger heatsinks to compensate for the power losses. In applications with many cascaded cells it is also undesirable due to the increasing voltage drop between stages and loss on efficiency.

The PC mode, shown in Fig. 44 (b), is an intermediary mode that is used in most applications. It requires higher capacitance values than the CC mode, but it improves the converter efficiency and reduces the voltage drop across the capacitors. In this mode there is a balance between size and efficiency.

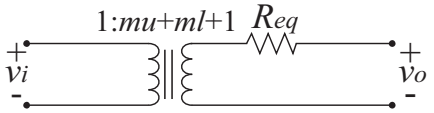
Finally, the NC mode, shown in Fig. 44 (c), occurs when the capacitors are oversized. This mode is the most efficient, since it has the lowest current ripple, thus the lowest RMS current values. It can be used in applications where efficiency is prioritized and there must not be a significant voltage drop between stages, such as applications that require too many cascaded cells. This mode, however, requires high capacitance values, which might increase the cost and volume of the converter.

Other ways of changing the charge mode of the SC structures is by changing the resistances and inductances of the current path (this can be done by adding passive elements or selecting switches with higher parasitic elements), or by changing the switching frequency of the converter. A higher switching frequency allows the capacitors to charge with lower time constants, which reduces the conduction losses of the cell at the expense of the switching losses.

2.3 DESIGN METHODOLOGY

Defining the right capacitance values for the SC converter is important to reduce losses and not oversize the circuit. For that reason, it is important to have a steady-state model of the converter considering the main losses of the circuit. Several works in literature do that by obtaining an equivalent circuit of the SC cells, shown in Fig. 45. The circuit is composed of an ideal transformer and a series resistance that represents the conduction losses [74, 75, 78, 112–117].

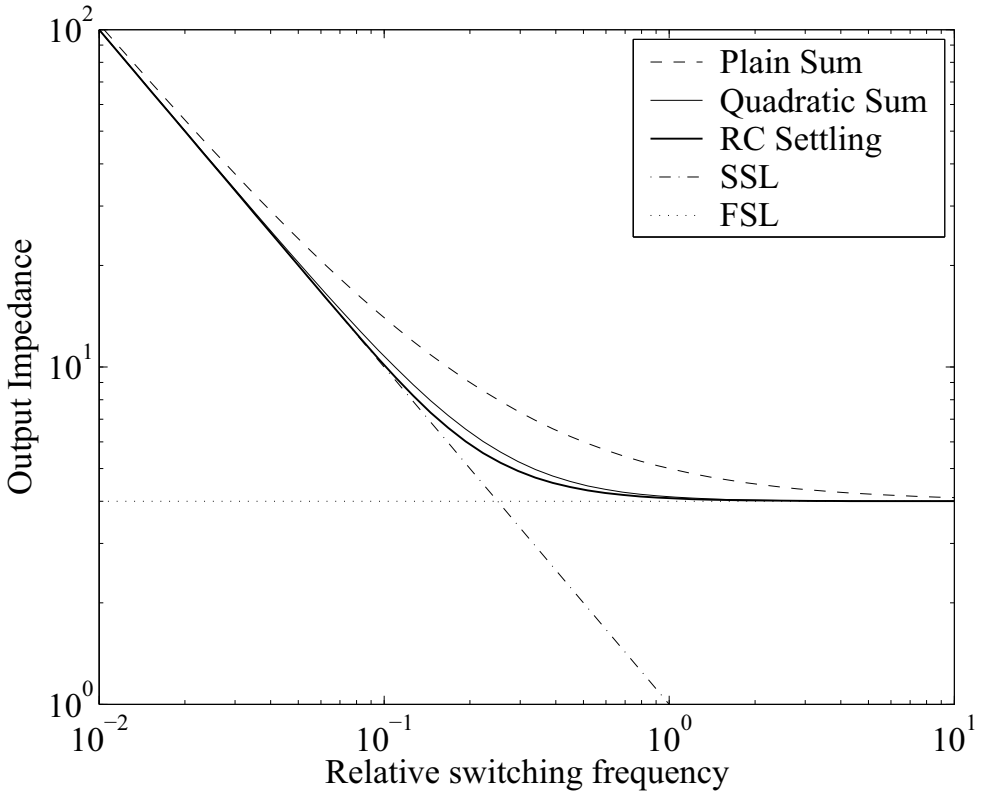
Fig. 45 – Equivalent circuit of SC converters



In this study, the method proposed by [78, 117] is applied, it consists in deriving the output impedance of SC converters by obtaining the charge multiplier vectors of the circuit in each topological state and estimating the equivalent resistance, that is obtained by calculating the asymptotic limits of the output impedance curve related to the switching frequency, as shown in Fig. 46. The slow switching limit (SSL) and fast switching limit (FSL) asymptotes are calculated based on the predominant non-idealities of each condition. The total output impedance is then be estimated through the quadratic sum of the asymptotic resistances.

This method is not the most precise in literature, since it is an estimation based on

Fig. 46 – Equivalent resistance and asymptotic limits [78].

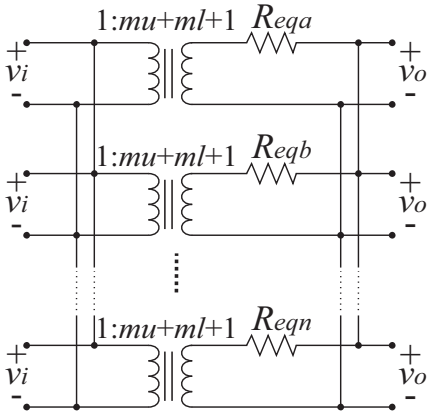


two limit conditions and it does not calculate R_{eq} directly at its operation point, but it is a more practical approach for systems that can be expanded into more levels, since it does not require complex differential equations. The simplicity of the equations obtained in this method allows it to be more easily generalized. The steady-state model of SC systems can become very complex due to the number of capacitors, which may result in high order differential equations. Because the parasitic resistances cannot be neglected in the SC steady-state models, they also contribute for the mathematical complexity of the system. By using this method, the system can be generalized and expanded without significant increase in complexity. Furthermore, this method has not shown large divergences with simulation results and it is one of the most cited methods in the scientific literature [117].

The topologies proposed in this thesis use interleaved SC cells connected to a single output. The complete system with all the cells could be analyzed to obtain its R_{eq}, but it is an impractical way to approach it, not only because of the number of components, but because the number of operational stages. Furthermore, more complex R_{eq} derivation methods should be used for this analysis, since the charge vector based analysis is only suitable for converters with two operational stages. A more practical method to analyze the converter is by analyzing a single leg and expanding the converter into multiple parallel connected equivalent circuits [118], as shown in Fig. 47.

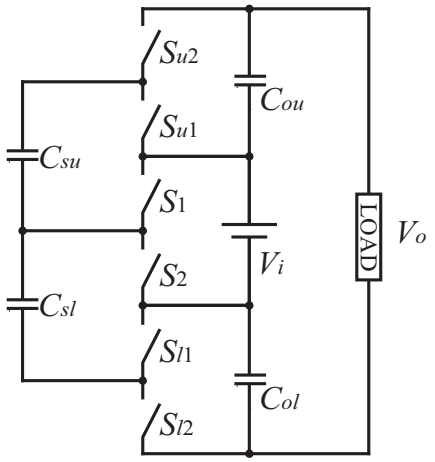
The converters studied experimentally in this thesis have 3SSCs and two cascaded SC cells that are configured symmetrically. For the SC analysis, the output capacitance is calculated for a single leg, that is shown in Fig. 48. The diodes are replaced by active switches and the capacitor C_{o0} is replaced by a voltage source V_i for didactic purposes. In the hybrid topology, the output capacitor C_{o0} works as an input source that is supplied by the input boost converter. In hybrid converters, the switches of the basic converter can be shared with the SC cell in order to reduce the number of components of the circuit,

Fig. 47 – Equivalent circuit of parallel connected SC converters



instead of adding an independent ladder cell to the converter output.

Fig. 48 – Symmetrical ladder SC cell for one converter leg.



In the charge multiplier vector analysis, the charge flow of the ladder converter in the two operational stages is analyzed. For this analysis, all the charges are presented relative to the output charge q_{out} and the steady-state operation is considered, therefore:

$$q_C^{st1} + q_C^{st2} = 0 \tag{2.1}$$

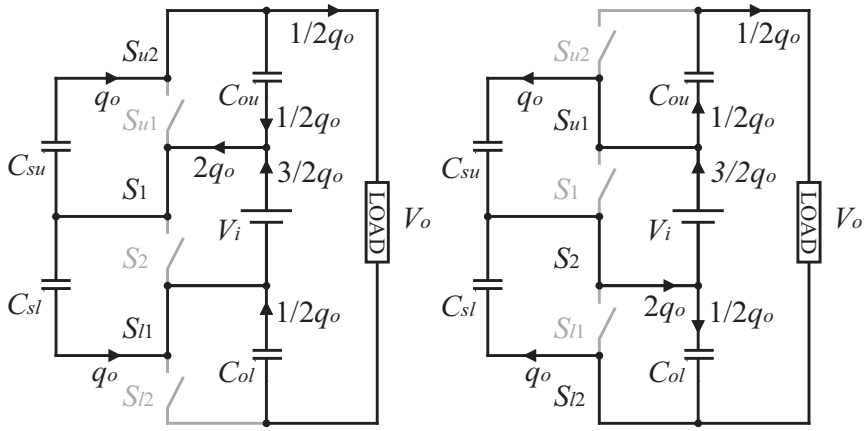
where q_C^{st1} and q_C^{st2} are, respectively, the capacitor charges in the first and second operational stages.

The ladder SC cell has two operational stages that are presented in Fig. 49. In the first stage, described by Fig. 49 (a), the switch S_1 is switched ON and the cell diodes represented by S_{u2} and S_{l1} also start conducting. The input source V_i transfers energy energy to the lower SC cell capacitor C_{sl} and the upper capacitor C_{su} transfers energy to the upper output capacitor C_{ou} and the output.

In the second stage, described by Fig. 49 (b), the switch S_2 and the cell diodes represented by the switches S_{u1} and S_{l2} are switched ON. In this stage, the source V_i transfers energy to the capacitor C_{su} and the capacitor C_{sl} transfers energy to the capacitor C_{ol} and the output. In both stages the output capacitors and input source transfer energy to the output.

By analyzing the topological states of the ladder SC cell, the charge multiplier

Fig. 49 – Ladder SC cell topological states and charge flow: (a) upper SC storage and lower SC transfer stage, (b) uper SC transfer and lower SC storage stage.



vectors can be obtained to calculate the asymptotic limits of the converter. First, SSL is calculated by neglecting the switches effect on the converter losses, and then the FSL is calculated by neglecting the capacitors effect.

This method can be used to analyze any SC cell with two operational stages, but in this work the ladder cell is used as an example since it is the cell used for the proposed structures.

2.3.1 Slow switching limit (SSL)

The charge value in the capacitors in one stage are obtained with the KVL and KCL and then organized in a multiplier charge vector as a function of the output charge q_o, described by:

$$a_C = \begin{bmatrix} q_{Csu} & q_{Csl} & q_{Cou} & q_{Col} \end{bmatrix} . q_o \tag{2.2}$$

where q_{Cj} are the charge values of each capacitor C_j . Because $q_C^{st1} = -q_C^{st2}$, the capacitor charge vectors for each stage are described by a_C and $-a_C$.

The Tellegen theorem [119] states that

> *It is proved that in a network configuration, for branch currents i satisfying the node equations and branch voltages v satisfying the mesh equations, Σiv summed over all branches is zero.*

By applying the Tellegen's theorem to the topological states and considering the linear relations between the current and charge, the sum of the power across the devices is given by

$$-V_i(q_i^{st1} + q_i^{st2}) + V_o(q_o^{st1} + q_o^{st2}) + \sum_{capacitors} (q_{Cj} v_{Cj}^{st1} - q_{Cj} v_{Cj}^{st2}) = 0 \tag{2.3}$$

where q_i^{st1} and q_i^{st2} are the input charge in the first and second topological states, respectively, and v_{Cj}^{st1} and v_{Cj}^{st2} are the capacitor voltage values for each topological state.

Since the proposed topology uses a symmetrical configuration, q_i and q_o are equal in both stages. Therefore, (2.3) can be rewritten as

$$-2V_i q_i^{st1,2} + V_o q_o + \sum_{capacitors} q_{Cj} \Delta v_{Cj} = 0. \tag{2.4}$$

Considering that

$$\Delta v_{Cj} = \frac{q_{Cj}}{C_j} \tag{2.5}$$

(2.4) is rewritten in a way that the voltage ripple values of each capacitor do not need to be known variables, thus resulting in

$$-2V_i q_i^{st1,2} + V_o q_o + \sum_{capacitors} \frac{q_{Cj}^2}{C_j} = 0. \tag{2.6}$$

The resulting equation is then rewritten as a function of q_o and the sum of capacitor charges is replaced by the multiplier charge vector, resulting in

$$-3V_i q_o + V_o q_o + a_C^{\circ 2} \cdot C_{lsc}^{\circ -1} q_o^2 = 0 \tag{2.7}$$

where the notation $a_C^{\circ 2}$ represents the Hadamard power of the vector and C_{lsc} is a vector with the capacitances of the ladder SC cell, described by

$$C_{lsc} = \begin{bmatrix} C_{su} & C_{sl} & C_{ou} & C_{ol} \end{bmatrix}^T. \tag{2.8}$$

By considering a resistive load and neglecting the output voltage ripple, it is known that $q_o = I_o T_s$. By isolating the output voltage from (2.7), the output characteristic of the SC circuit can be obtained with known parameters of the converter, as described by

$$V_{o,SSL} = 3V_i - \frac{I_o}{f_s} a_C^{\circ 2} \cdot C_{lsc}^{\circ -1} \tag{2.9}$$

where I_o is the output voltage of the SC converter and f_s is the converter switching frequency.

By comparing the output characteristic equation with the equivalent circuit shown in Fig. 45, the SSL equivalent resistance $R_{eq,SSL}$ is given by

$$R_{eq,SSL} = \frac{a_C^{\circ 2} \cdot C_{lsc}^{\circ -1}}{f_s}. \tag{2.10}$$

The resulting equation is inversely proportional to the switching frequency and the capacitances, as expected in the asymptotic SSL.

2.3.2 Fast switching limit (FSL)

To obtain the FSL resistance, the capacitance charge vector is neglected, since the converter operates in the NC mode and the voltage ripple null, thus the capacitance charge in each stage is neglectable.

In the FSL the resistive losses are predominant, therefore a multiplier charge vector of the parasitic resistances must be obtained. In most works the resistance vector is obtained by analyzing the charge only in the active switches. However, since the topology in this work uses diodes and the rectifiers might use larger capacitors in the output, the equivalent series resistance (ESR) of these capacitors may be relevant in the analysis,

including the input source ESR. For better organizing the variables, the resistance vector will be separated into a switch and a capacitance resistance vector, given by

$$\begin{cases} a_{Rs} = \begin{bmatrix} q_{Su1} & q_{Su2} & q_{S1} & q_{S2} & q_{Sl1} & q_{Sl2} \end{bmatrix} \\ = \begin{bmatrix} 1 & 1 & 2 & 2 & 1 & 1 \end{bmatrix} q_o \\ a_{Rc} = \begin{bmatrix} q_{Rco0} & q_{Rcou} & q_{Rcol} & q_{Rcsu} & q_{Rcsl} \end{bmatrix} \\ = \begin{bmatrix} 3/2 & 1/2 & 1/2 & 1 & 1 \end{bmatrix} q_o \end{cases} \tag{2.11}$$

Like in the SSL analysis, the Tellegen's theorem is applied by considering that sum of the average power dissipated in every branch is zero, resulting in

$$-3V_i q_o + V_o q_o + \sum_{resis\,\tan ces} (q_{Rs} v_{Rs} + q_{Rc} v_{Rc}) = 0. \tag{2.12}$$

Considering that

$$v_R = i_R^2 R = R \frac{q_R}{DT_s} \tag{2.13}$$

the equation is rewritten as

$$-3V_i q_o + V_o q_o + \sum_{resis\,\tan ces} \left(\frac{R_s q_{Rs}^2 f_s}{D} + \frac{R_c q_{Rc}^2 f_s}{D} \right) = 0 \tag{2.14}$$

where D is the duty cycle related to the stage the switch is turned ON.
The expression (2.14) can be rewritten in function of q_o, resulting in

$$-3V_i q_o + V_o q_o + a_{Rs}^{\circ 2} \cdot R_{slsc} \cdot D_{slsc}^{\circ -1} q_o^2 f_s + a_{Rc}^{\circ 2} \cdot R_{slsc} q_o^2 f_s = 0 \tag{2.15}$$

where R_{slsc} and R_{clsc} are the vectors with the switches and capacitor resistances, respectively, given by

$$\begin{cases} R_{slsc} = \begin{bmatrix} R_{Su1} & R_{Su2} & R_{S1} & R_{S2} & R_{Sl1} & R_{Sl2} \end{bmatrix} \\ R_{clsc} = \begin{bmatrix} R_{Co0} & R_{Cou} & R_{Col} & R_{Csu} & R_{Csl} \end{bmatrix}^T \end{cases} \tag{2.16}$$

where D_{slsc} is a vector that contains the duty cycle of each switch, given by

$$D_{slsc} = \begin{bmatrix} (1-D) & D & D & (1-D) & D & (1-D) \end{bmatrix}. \tag{2.17}$$

By replacing q_o for I_o/f_s in (2.15), the equation is rewritten with known variables, resulting in

$$-3V_i + V_o + a_{Rs}^{\circ 2} R_{slsc} \cdot D_{slsc}^{\circ -1} I_o + a_{Rc}^{\circ 2} \cdot R_{clsc} I_o = 0. \tag{2.18}$$

The output voltage is then isolated to obtain the output characteristic, described by

$$V_o = 3V_i - I_o \left(a_{Rs}^{\circ 2} \circ R_{slsc} \cdot D_{slsc}^{\circ -1} + a_{Rc}^{\circ 2} \cdot R_{clsc} \right) \tag{2.19}$$

The FSL equivalent resistance R_{eqFSL} is derived by comparing the equation to the equivalent circuit, where the R_{eqFSL} is described by

$$R_{eqFSL} = a_{Rs}^{\circ 2} \circ R_{slsc} \cdot D_{slsc}^{\circ -1} + a_{Rsc}^{\circ 2} \cdot R_{clsc} \tag{2.20}$$

The FSL asymptote depends only on the resistance values and the converter duty cycle, since the switching frequency does not affect the current ripple in the FSL assumption.

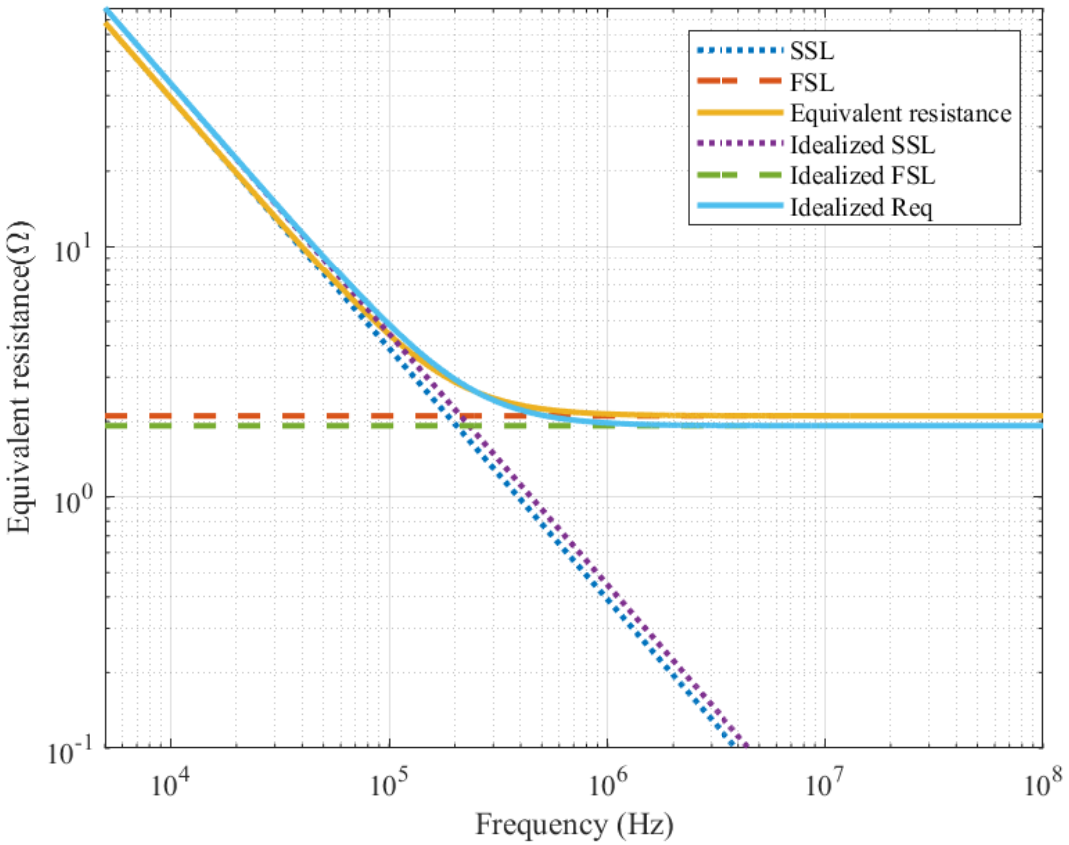
2.3.3 Total equivalent resistance

After calculating the equivalent resistances for SSL and FSL, it is possible to estimate the total equivalent resistance by performing the quadratic sum of both equivalent resistances, described by

$$R_{eq} = \sqrt{R_{eqSSL}^2 + R_{eqFSL}^2}. \tag{2.21}$$

By plotting the calculated equivalent resistance in relation to the frequency with real parameters, it can be seen in Fig. 50 that $R_{eq,FSL}$ determines the minimum possible R_{eq}, and then choose the most suitable operation point for the converter in regards to the conduction losses. Fig. 50 also shows the equivalent resistance value for two cases, one idealized case where all capacitors have the same capacitance value and only the switch resistance is considered, and another that is closer to the practical case, where the output capacitors are larger, the ESRs of the capacitors are considered and the diode resistances are different from the switch resistances.

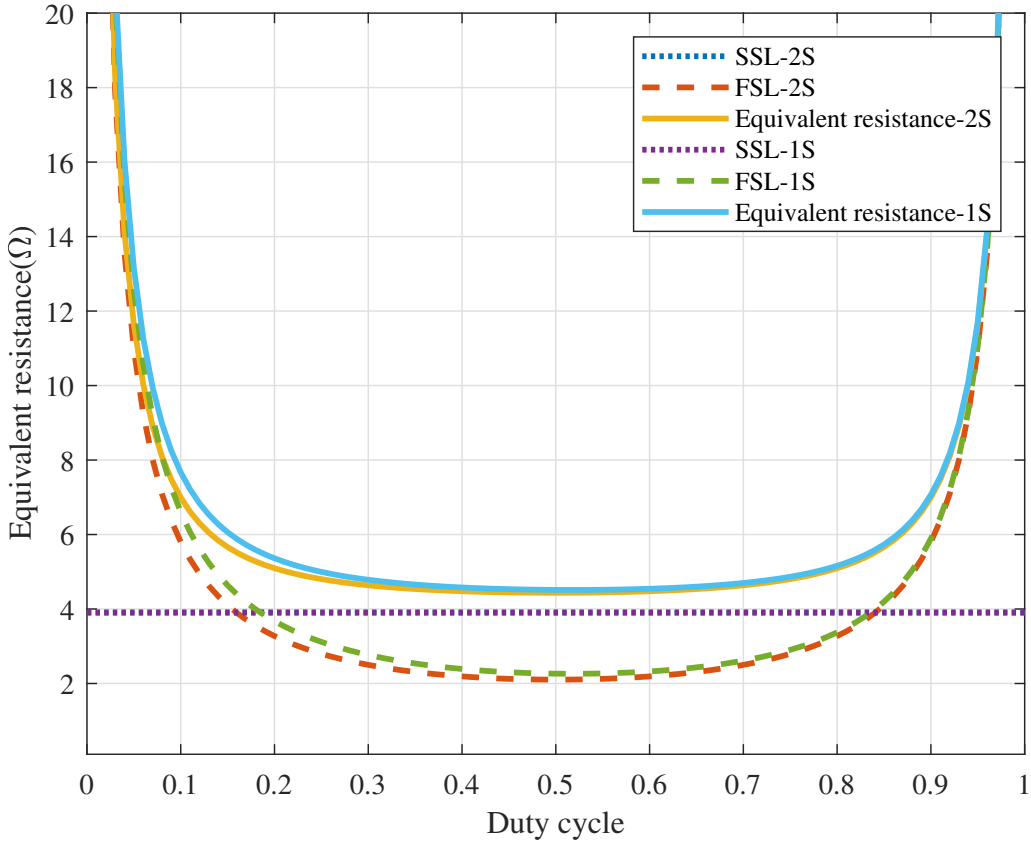
Fig. 50 – Equivalent resistance as a function of the switching frequency.



By plotting the equivalent resistance as a function of the duty cycle (See Fig. 51) it can be noticed that, although the SSL curve is highly influenced by the switching

frequency, the converter resistances are predominant in the losses due to high or low duty-cycles, since it has a high influence on the FSL curve, that is constant related to the frequency. This graphic shows the equivalent resistance for two cases, one where the boost converter stage has one switch and one diode, as in the dc-dc and the single-phase ac-dc converter, and the other case where there are two active switches in the bridge, like in the three-phase rectifier. In this example the MOSFET resistance is lower than the diode resistance to show that the lowest equivalent resistance in this case does not occur when $D = 0.5$, but varies according to the path with lower resistance.

Fig. 51 – Equivalent resistance as a function of the duty cycle.



The equivalent resistance calculation can be used to determine the most suitable capacitance value for the application. By tracing R_{eq} in function of the capacitance C_s, it is possible to choose a capacitor that is not oversized and does not compromise the efficiency. The output capacitor can be chosen based on the desired output ripple, dynamic aspects, hold-up time or can be equal to the capacitor C_s and be chosen based on the R_{eq} criterion. In the single-phase AC-DC converter it must be chosen based on the low-frequency ripple, but in the DC-DC and three-phase AC-DC converters, other criteria might be more adequate, since there is no significant low-frequency components in the output voltage.

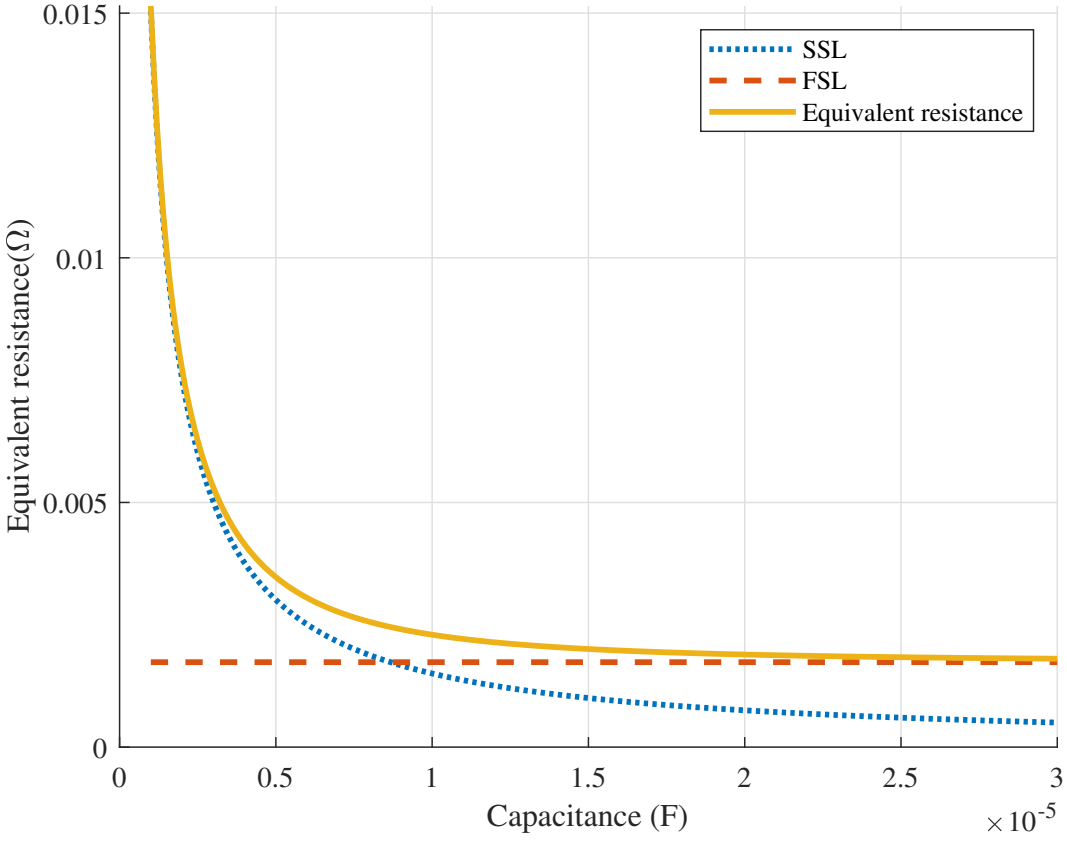
As can be seen in Fig. 52, a higher capacitance value results in lower conduction losses. The work [77] took the assumption that the most adequate capacitance value should be based on the region that the curvature is more accentuated, the "knee" of the curve. However, it may in some cases be more useful to operate nearer to the part of

the curve with a higher R_{eq} value and choose an operation point that is based on other aspects of the circuit. By operating with a higher R_{eq}, a lower capacitance value can be used and reduce the volume of the system. A too high R_{eq} can increase the size of the converter, since it may require large heatsinks to compensate the losses. A lower R_{eq} requires a larger capacitance, but it can help achieving a higher efficiency. The efficiency of a switched capacitor is described by

$$\eta_{SC} = \frac{V_o}{V_i} = \frac{V_o}{V_o + I_o R_{eq}} = \frac{R_o}{R_o + R_{eq}}. \tag{2.22}$$

By choosing the desired efficiency of the cell based on R_{eq}, it is possible to select the capacitor value that is most adequate for each application through Fig. 52.

Fig. 52 – Equivalent resistance as a function of the capacitance C_s.



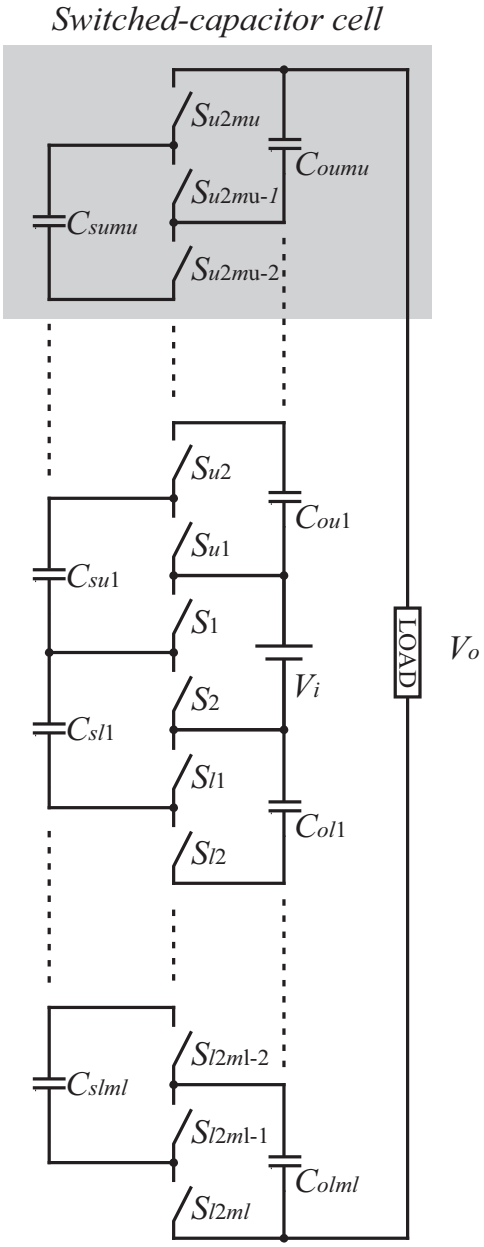
In ac-dc applications, since the duty cycle varies and the equivalent resistance varies with it, it should be more adequate to design the capacitor for the condition where there is more power transfer between the input and output for each phase. This can be performed by calculating the equivalent resistance for a duty cycle value where the phase current is at its peak value.

2.3.4 Generalization

The main advantage of the methodology presented in this chapter is the possibility of expanding the analysis to more cascaded SC cells. For this analysis, a generalized sym-

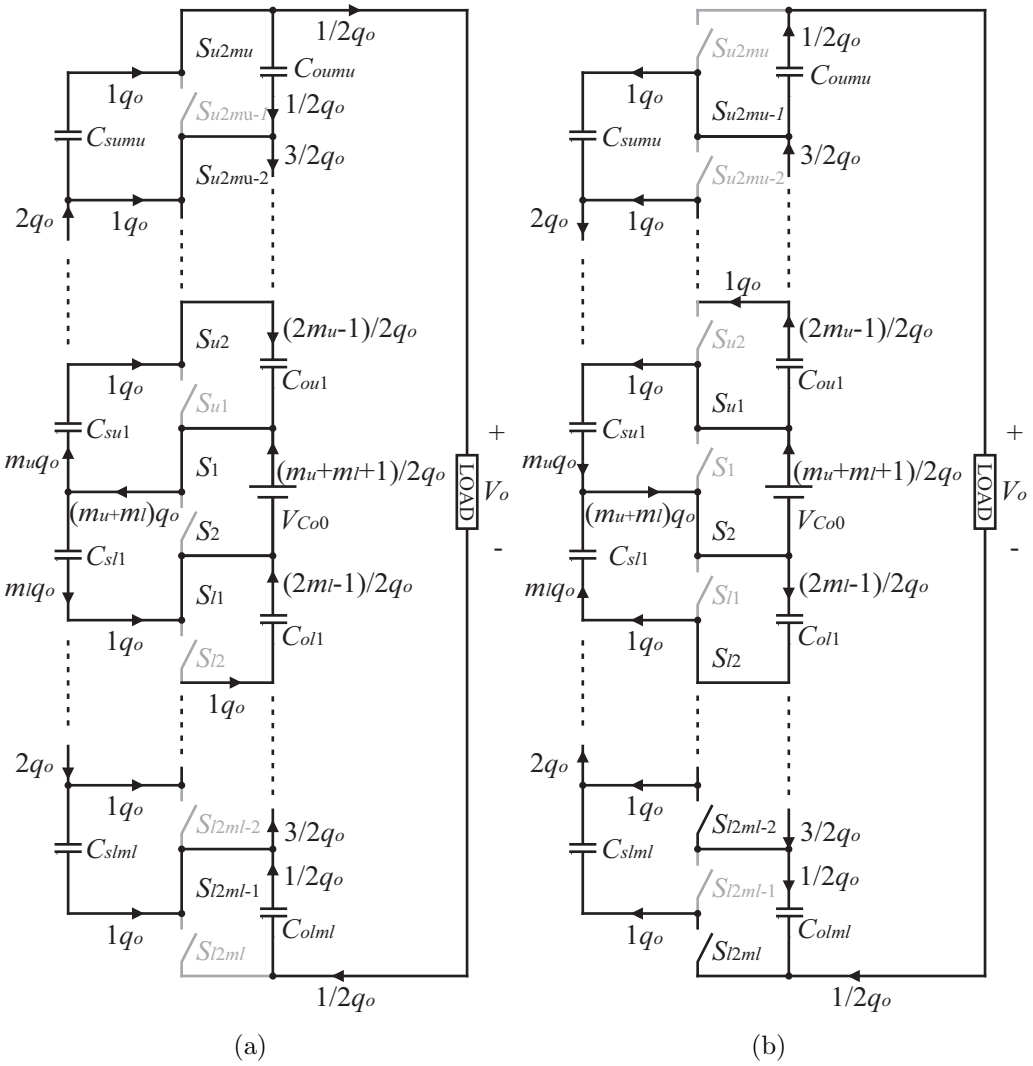
metrical ladder SC cell with m_u upper and m_l lower cells is considered. The generalized ladder structure is shown in Fig. 53.

Fig. 53 – Generalization of the symmetrical ladder SC cell.



The topological states of the generalized SC cell are described in Fig. 54. In the first stage, S_1, the even numbered S_{pj} and the odd numbered S_{nj} switches are switched ON. In this stage all upper C_{spj} capacitors transfer energy to the C_{opj} capacitors and the lower C_{onj} capacitors transfer energy to the C_{snj} capacitors. In the second stage S_2, the odd numbered S_{pj} and even numbered S_{nj} switches are switched ON. The capacitors that stored energy in the first stage transfer energy in the second stage, as well as the capacitors that transfer energy in the first stage store energy in the second stage, and their charge flow directions are inverted.

Fig. 54 – Generalized symmetrical SC cell topological states and charge flow: (a) upper SC storage and lower SC transfer stage, (b) upper SC transfer and lower SC storage stage.



The same methodology that was applied to the $m = 1$ symmetrical ladder cell can be applied to the m cells by only changing the charge vectors of the generalized structure. The vectors of the generalized topology are obtained from the analysis the charge flow of

each topological state. The generalized capacitor charge multiplier vector is described by

$$a_C = \begin{bmatrix} q_{Csu1} \\ q_{Csu2} \\ \vdots \\ q_{Csum} \\ q_{Csl1} \\ q_{Csl2} \\ \vdots \\ q_{Cslm} \\ q_{Cou1} \\ q_{Cou2} \\ \vdots \\ q_{Coum} \\ q_{Col1} \\ q_{Col2} \\ \vdots \\ q_{Colm} \end{bmatrix}^T = \begin{bmatrix} m_u \\ m_u - 1 \\ \vdots \\ 1 \\ m_l \\ m_l - 1 \\ \vdots \\ 1 \\ (2m_u - 1)/2 \\ (2m_u - 3)/2 \\ \vdots \\ 1/2 \\ (2m_l - 1)/2 \\ (2m_l - 3)/2 \\ \vdots \\ 1/2 \end{bmatrix}^T . \tag{2.23}$$

The charge multiplier vector of the switches resistances is described by

$$a_{Rs} = \begin{bmatrix} R_{Su1} \\ \vdots \\ R_{Sum} \\ R_{S1} \\ R_{S2} \\ R_{Sl1} \\ \vdots \\ R_{Slm} \end{bmatrix}^T = \begin{bmatrix} 1 \\ \vdots \\ 1 \\ m_l + m_u \\ m_l + m_u \\ 1 \\ \vdots \\ 1 \end{bmatrix}^T q_o. \tag{2.24}$$

In the switch resistance vector, the bridge switches have a charge value that is equivalent to twice the number of cells, whereas all the other switches have the same charge as the output. This occurs because the output average current equals the average current in those switches, since the average capacitor current values are zero and only the cell switches contribute to the total average output current value.

Finally, the capacitor resistance vector is described by

$$a_{Rc} = \begin{bmatrix} R_{Co0} \\ R_{Cou1} \\ \vdots \\ R_{Coum} \\ R_{Col1} \\ \vdots \\ R_{Colm} \\ R_{Csu1} \\ \vdots \\ R_{Csum} \\ R_{Csl1} \\ \vdots \\ R_{Cslm} \end{bmatrix}^T = \begin{bmatrix} (m_u + m_l + 1)/2 \\ (2m_u - 1)/2 \\ \vdots \\ 1/2 \\ (2m_l - 1)/2 \\ \vdots \\ 1/2 \\ m \\ \vdots \\ 1 \\ m \\ \vdots \\ 1 \end{bmatrix}^T q_o. \tag{2.25}$$

The equivalent resistance of the generalized converter is obtained through the expressions (2.10), (2.20) and (2.3.3). Like the case where $m_i = 1$, the capacitance of the generalized case can be varied to estimate the most adequate capacitance value for the circuit. The parameters were chosen based on the components used in the practical case. Furthermore, the capacitance values for this example were chosen to have the same voltage ripple in all capacitors, therefore, the capacitance values are a proportion of their charges, given by

$$\begin{cases} C_{omi} = C_{smi} \frac{2}{2m_i - 1} \\ C_{smi} = \frac{C_{s1}}{m_i} \end{cases} \tag{2.26}$$

By tracing the curve relating C_s to R_{eq} and using the proportionality relation from (2.26), it is possible to determine an adequate capacitance value for the SC cell. Fig. 55 shows the R_{eq} variation for different capacitance values according to the proportionality relation and compares it to simulated results with symmetrical ladder cells, where $m = m_u + m_l$. The simulations used the parameters shown in 1. The values are based on real components that will be used in the experiments. In the output, a 1 A current source was connected, but a resistor or any current value in the output would result in the same R_{eq} value. There are some divergences between the theoretical and simulation values, since the curves are the quadratic sum of two asymptotes. However, the shapes of the curves are similar to the simulation results and the method did not require complex differential equations, even for more cells. Therefore, the method is adequate for the purposes of this project, since it is used to estimate a range of capacitance values, so that a commercial capacitor can be chosen.

The equivalent resistance calculation is a method that helps choosing the capacitor. However, it is also essential that the capacitor design attends other criteria according the necessities of each design. The capacitance value is not only important for estimating the losses, but it may be designed to limit to the voltage ripple or calculated based on the hold-up time criterion. The right capacitor should also be selected according to its maximum current capability. Thus, the equivalent resistance is a starting point to choose the right capacitor for the project.

Fig. 55 – Theoretically estimated and simulated equivalent resistance.

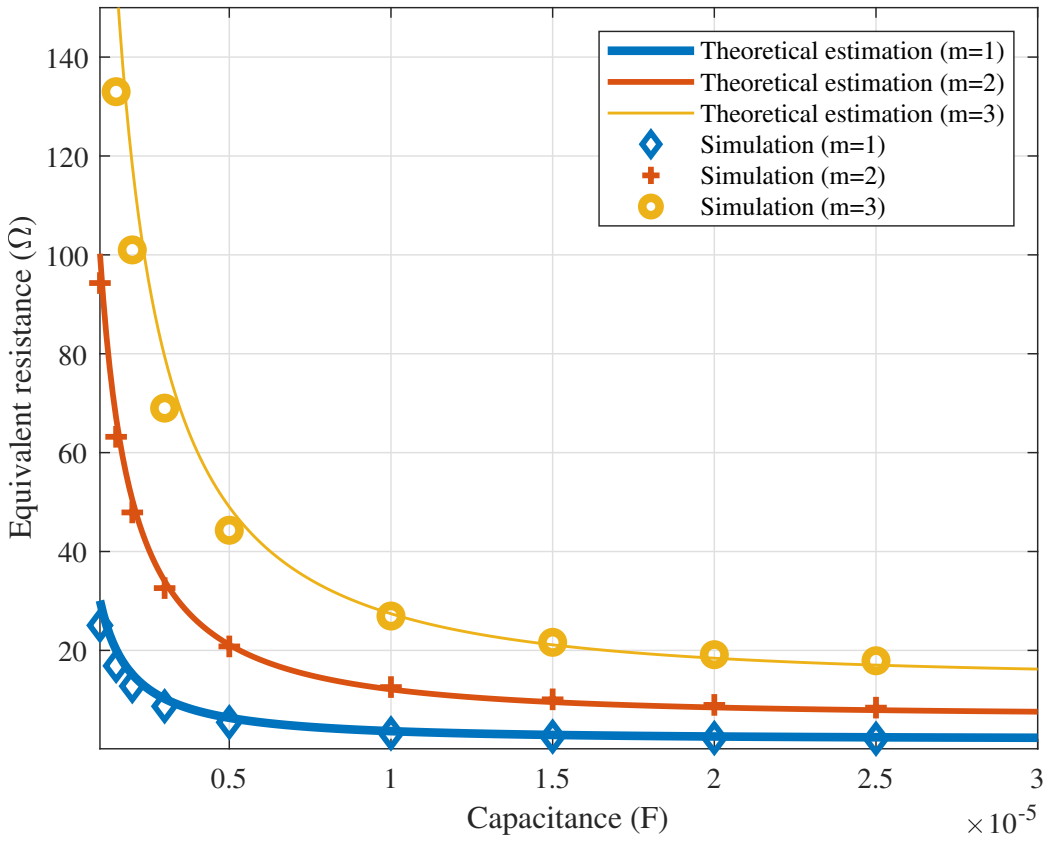


Table 1 – Specifications of the ladder simulated circuits

Suecification	**Value**
Input voltage	400 V
Switching frequency (f_s)	100 kHz
Duty cycle	0.5
S_1 and S_2 ON resistances	80 mΩ
S_l and S_u ON resistances	100 mΩ
C_o and C_s ESR	0.005 mΩ

2.4 SUMMARY

This section presented an introduction to SC cells. The operation principle and the possible modes of operation were presented.

A design methodology was chosen for the ladder SC cell based on the calculation of the equivalent resistance value. The chosen method was the charge multiplier based method, that does not result in complex differential equations and can be generalized into multiple levels. The method consists in finding two asymptotic limits for the equivalent resistance and then estimating the total equivalent resistance by performing the the quadratic sum of the asymptotes.

The design methodology was applied for the symmetrical ladder SC cell, where the equivalent resistance was obtained for one leg of the converter. The method was generalized into more cascaded SC cells and then compared to simulations, that presented results similar to the calculated values.

3 HYBRID BOOST DC-DC CONVERTER WITH MSSC AND SC CELLS

3.1 MULTISTATE SWITCHING CELL

The main objective of this thesis is to propose the integration of MSSC and SC cells for dc-dc converters and shows how the concept can be expanded to PFC ac-dc converters. This chapter presents the analysis, simulation and experimental results of the proposed dc-dc converter.

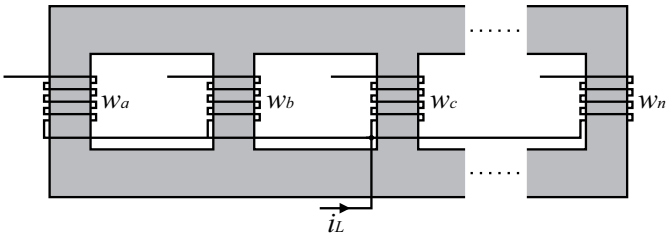
Multistate switching cells (MSSC) can be used to reduce the size and the cost of circuit devices by reducing the current on the switches and multiplying the current switching frequency component that goes through the filter. The MSSC uses phase-shifted signals that control the legs of the converter. Each leg is connected to a winding of an Intercell transformer (ICT) that processes a fraction of the total input current.

The ICT must be implemented in a way that the magnetic flux of each leg of the core is equally divided between the other legs. Therefore, the relation between mutual inductances between two phases and self inductance values of the interphase transformer, the coupling factor, is given by

$$k_{ICT} = -\frac{M_{ij}}{n-1}\sqrt{L_i L_j}. \tag{3.1}$$

where M_{ij} is the mutual inductance between phases i and j, $L_{i,j}$ is the self inductance of a phase and k is the number of phases in the ICT. To obtain this relation, the ICT of the MSSC converter is implemented as shown in Fig. 56.

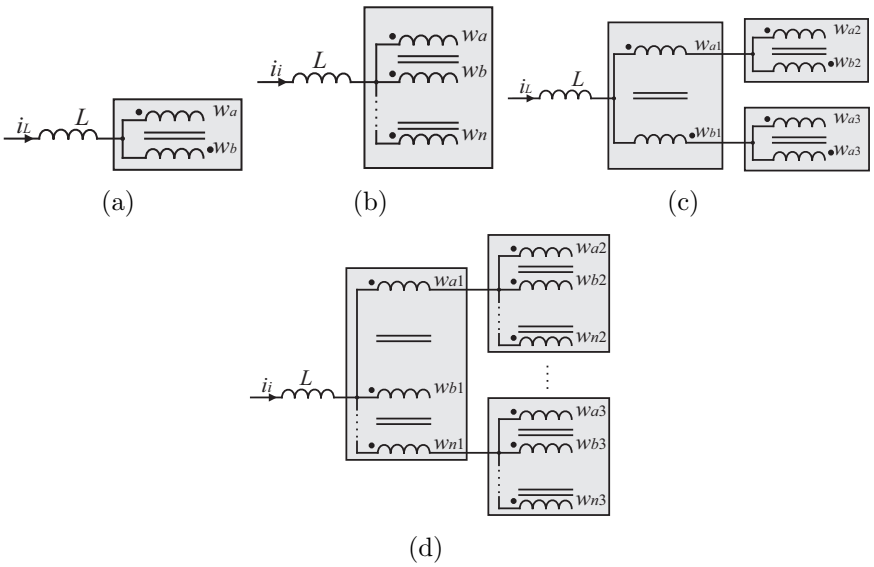
Fig. 56 – Implementation of the multiphase ICT.



The MSSC can be implemented in different ways depending on the number of states required for the application. For three-state applications, since the coupling factor is -1, a regular transformer with two windings at the same core leg can be used, achieving a good coupling. Four-state applications can use three-phase transformers with one winding in each leg to equally divide the magnetic flux in the transformer core. For applications that divide the current into more levels it can be difficult to implement the transformer with a single core, thus some associations can be made with more cascaded transformers. Fig. 57 shows different configurations to implement the ICT.

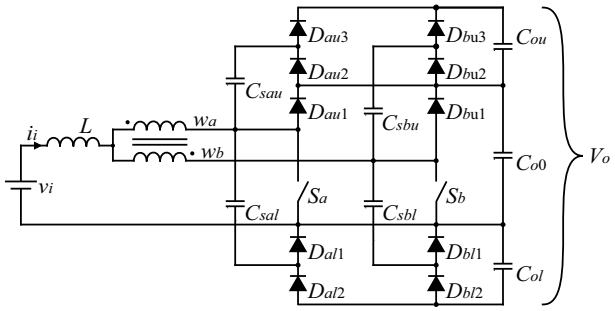
One of the main advantages of the MSSC is the possibility of adjust the number of levels to suit its application. In this thesis the three-state switching cell (3SSC) is used to validate the proposed concept. Additionally, some studies and experiments where performed with the 4SSC. The converter presented a high efficiency (above 98%), however there are some implementation issues that makes this topology impractical due to the

Fig. 57 – MSSC configurations: (a) 3SSC, (b) single transformer MSSC, (c) MSSC single-phase transformers and (d) MSSC with multiphase transformers



ICT implementation with commercial cores. Most commercial magnetic cores available are asymmetrical and there are some methods to implement 4SSCs with asymmetrical cores, but there are disadvantages using these methods, approached in Appendix A with more details. A more extended analysis and experimental results of the 4SSC converter was submitted to a journal paper. The proposed boost dc-dc converter with SC cells and 3SSC is shown in Fig. 57.

Fig. 58 – Boost converter with 3SSC and SC cells.



The number of legs of the converter, or phases in the ICT determine the the number of states in the MSSC. Each state is defined by the number of topological combinations with the same characteristic as viewed by the transformer and the input. Knowing that the legs of the converter are controlled with three carrier signals that are phase-shifted in 180°, the states are described by Table 2.

The combination of topological states of the MSSC depends on the converter duty cycle. Since this dc-dc converter study is expanded into a single-phase and a three-phase rectifier, either operating in CCM, it is important to understand the converter in a wide duty cycle range. Therefore, the converter analysis is performed for two operating regions, that are referred to as region A ($0 < d < 1/2$) and B ($1/2 < d < 1/2$), where d is the duty cycle of one switch. The number of operating regions in the converter depends on the total number of legs. It is important to analyze each region because there are different

Table 2 – Topological states of the 3SSC

State	S_1	S_2	D_1	D_2
State 1 (0 Switches ON)	-	-	X	X
State 2 (1 Switch ON)	-	X	X	-
	X	-	-	X
State 3 (2 Switches ON)	X	X	-	-
Neutral State (DCM only)	-	-	-	-

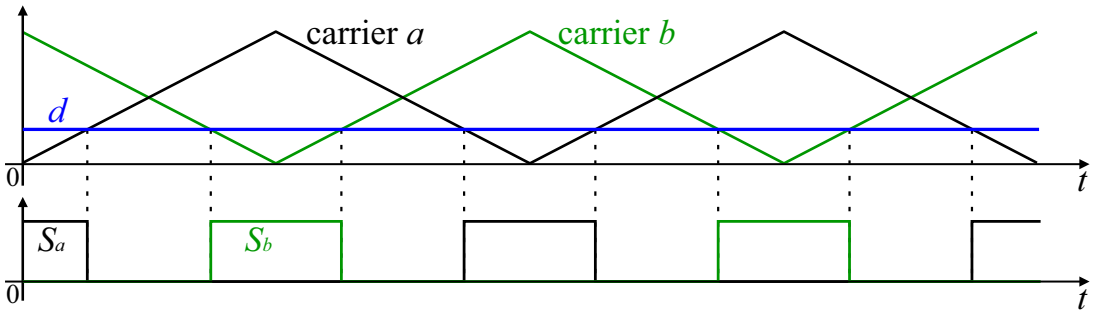
topological states associated to each one of them. region A always operates at the states 1 and 2, whereas region B always operates between the states 2 and 3.

3.2 REGION A ($D < 1/2$)

3.2.1 Operation principle

The region A operation occurs when the converter operates with a duty cycle lower than 1/2. The converter operates in state 1 and 2 and there is no overlap between the gate signals of different legs, as can be seen in the modulation scheme shown in Fig. 59.

Fig. 59 – Modulation scheme in region A.



There are four operational stages in region A, shown in Fig. 60. These stages alternate between the states 1 and 2, since the gate control signals do not overlap. Thus, there is either one or no switch turned ON in each topological state.

In the first operational stage [See Fig. 60 (a)], the switch S_a is turned ON and the diodes D_{au2} and D_{al2} are forward biased. In the other leg the switch S_b is turned OFF and the complementary diodes D_{bu1}, D_{bu3} and D_{bl1} are forward biased. The input current is divided between the windings of the ICT. The current in the winding w_a flows through S_a, and the current in w_b flows through the diode D_{bu1}. In the leg a, the capacitor C_{sau} stores energy and C_{sal} transfers energy to the output capacitor C_{ol}, whereas in the leg b the upper cell capacitor C_{sbu} transfers energy to the output capacitor C_{ou} and the lower capacitor C_{sbl} receives energy from the output capacitor C_{o0}.

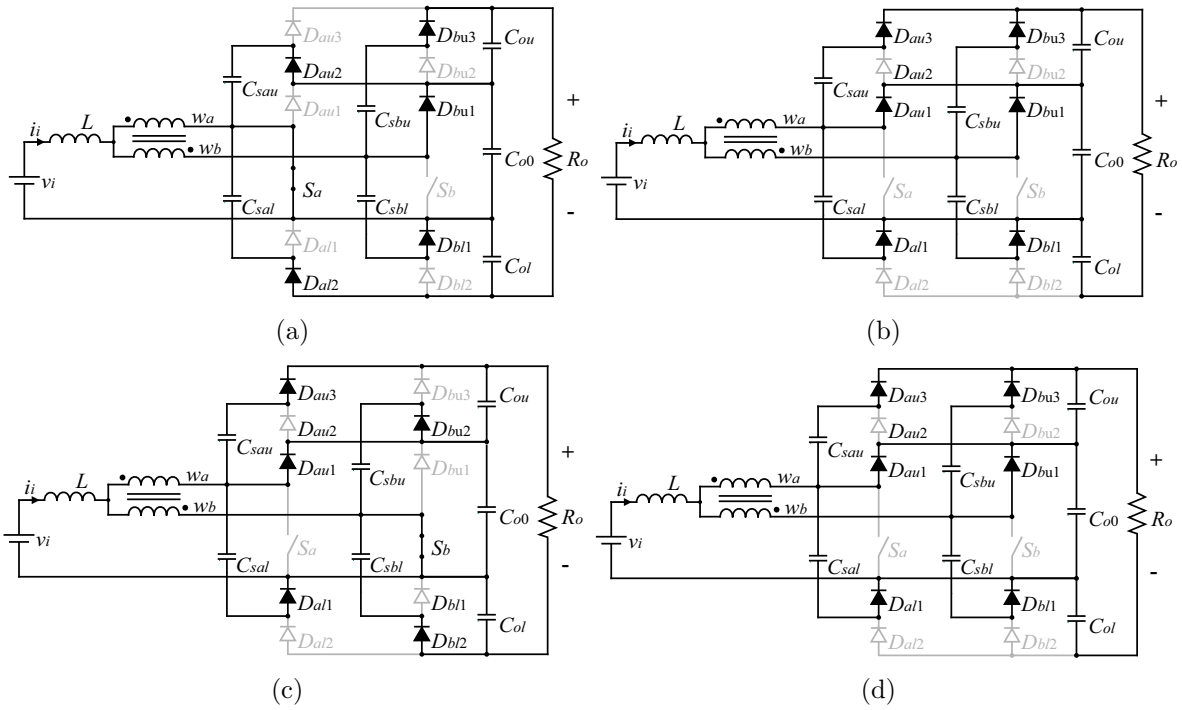
In the second stage [See Fig. 60 (b)] all switches are turned OFF and all odd numbered diodes are forward biased, connecting the ICT windings to the output capacitor C_{o0}. Since these diodes are forward biased through to the currents in the ICT windings, the capacitor C_{o0} is connected in parallel with the lower cell capacitors C_{sal} and C_{sbl}, which

store energy during this stage. The upper cell capacitors C_{sau} and C_{sbu} are connected in parallel with the upper output capacitor C_{ou} and the lower output capacitor C_{ol} does not receive or transfer energy to any other capacitor during this stage, but it transfers energy to the output.

The third stage [See Fig. 60 (c)] [Fig. 60 (e)] has a principle of operation that is similar to that of the first stage, but S_b is turned ON, S_a OFF and the operation principle of leg a is reflected to the leg b. Either stages 1 and 3 operate in state 2 from the input inductor's perspective.

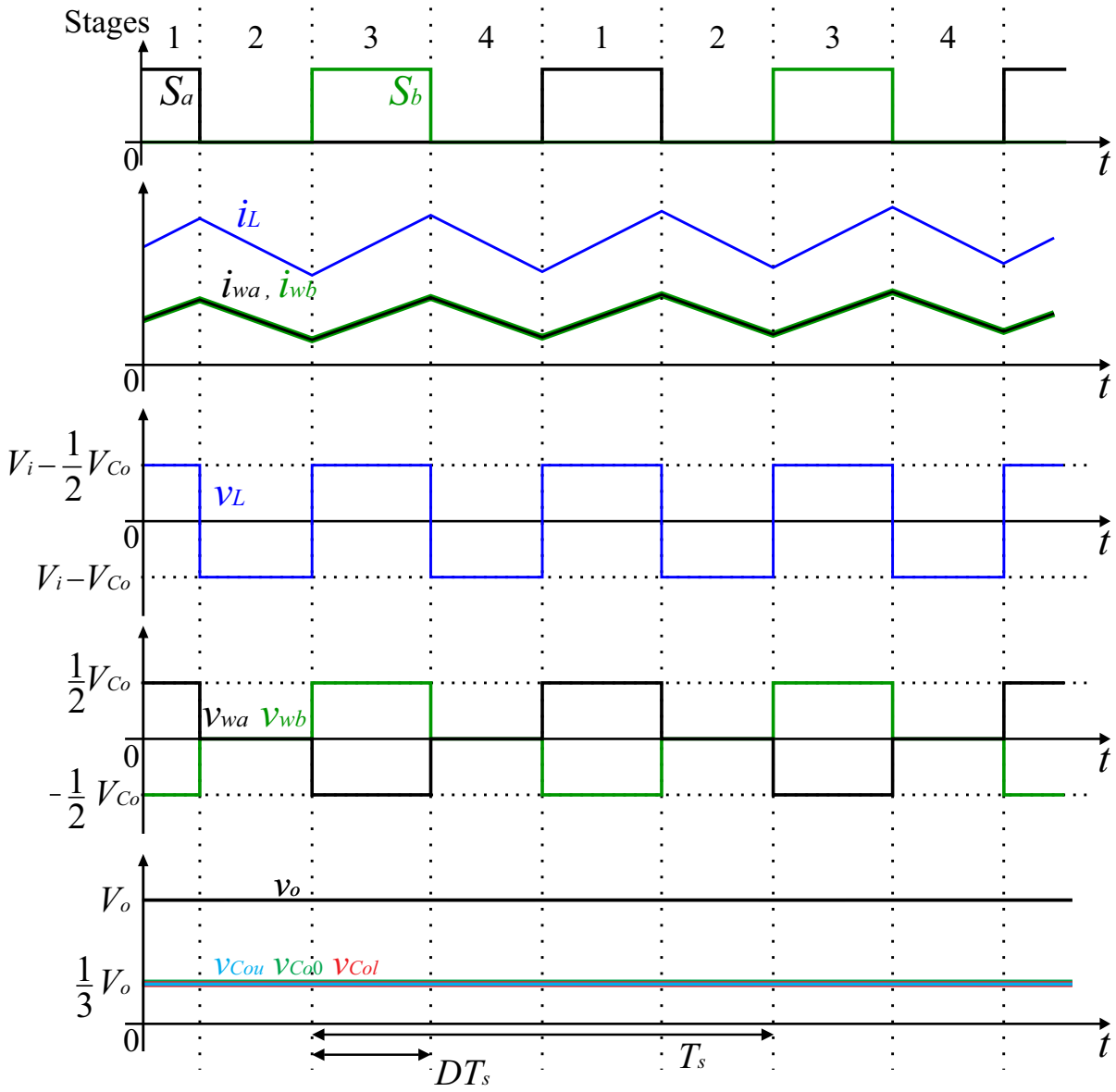
The fourth [Fig. 60 (d)] stage presents the same operation principle and topological state as the second stage, because no switch is commanded to turn ON. Either stage 2 and 4 operate in state 3.

Fig. 60 – Hybrid boost converter with MSSC and SC - Operational states in region A: (a) to (d) represent the stages 1 to 4



The main waveforms of the converter for region A are shown in Fig. 61. Since all of the output capacitors have the same voltage value, their voltage are described as V_{Co}. It should be noted that the voltages across the capacitors are one third of the total output voltage and the average current in the ICT windings are half the total input inductor current. Other advantages shown in the waveforms are the ripple frequency in the inductor (twice the switching frequency), and the inductor voltage, which is lower than the typical boost converter, resulting in a lower current ripple as well.

Fig. 61 – Main waveforms of the boost converter with 3SSC and SC in region A.

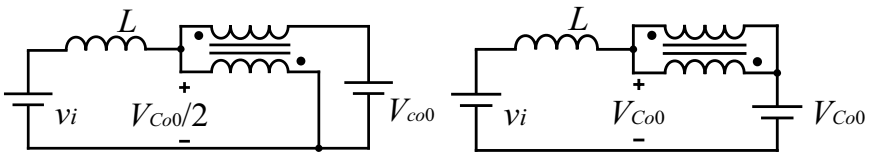


3.2.2 Static gain

The static gain is derived through the inductor volts-second relation to obtain the relation between the voltage on C_{o0} and the input voltage, then the multiplication factor of the SC cell is applied to obtain the total converter static gain. The analysis of the converter in this region can be performed by knowing that the voltage value across the inductor is the same for every equivalent circuit topology regarding each state. Therefore, the volts-second analysis can be performed during half the switching period, because the voltage across the inductor is the same for the stages 1 and 3, and it is also the same in stages 2 and 6. The equivalent circuit of the converter for states 2 and 1 are described by Fig. 62 (a) and (b), respectively. In these circuits the windings of the transformer were not specified, since it makes no difference in the inductor's perspective.

In the operational stages 1 and 3 (state 2), one switch conducts and the output capacitor voltage is equally divided between the transformer windings and the voltage

Fig. 62 – Equivalent circuits in region A: (a) stages 1 and 3, (b) stages 2 and 4.



across the winding that is connected to the input inductor is $V_{Co0}/2$. In the stages 2 and 4 (state 1), the windings are short-circuited, thus the voltage across them is zero. The voltage values across all capacitors is ideally the same, since they are connected in parallel to each other at different operational stages. Since the output capacitors are connected in series and their voltages are self-balanced, the voltage across each capacitor is given by

$$V_C = \frac{V_o}{m_u + m_l + 1} \tag{3.2}$$

where m_u and m_l are the number of, respectively, upper and lower cascaded SC cells in at least one leg of the converter. The number of legs with SC cells connected to them do not affect the relation between the capacitors and output voltage, they only affect the power loss distribution in the devices.

By knowing the voltage across the winding that is connected to the switch that is turned ON, the static gain can be obtained through the volts-second relation within $T_s/2$. The average voltage across the inductor in region A is described by

$$\langle v_L \rangle_{\frac{T_s}{2}} = \frac{2}{T_s}\left[\int_0^{DT_s}\left(V_i - \frac{1}{2}V_{Co0}\right)dt + \int_{DT_s}^{\frac{T_s}{2}}\left(V_i - V_{Co0}\right)dt\right] = 0. \tag{3.3}$$

By solving the integrals, the equation is rewritten as

$$\langle v_L \rangle_{\frac{T_s}{2}} = 2\left[V_i D - \frac{1}{2}V_{Co0}D + V_i\left(\frac{1}{2} - D\right) - V_{Co0}\left(\frac{1}{2} - D\right)\right] = 0. \tag{3.4}$$

Knowing that the inductor average voltage is zero and by isolating the terms V_{Co0} and V_i, the relation between the capacitor voltages and the input voltage in region A is described by

$$\frac{V_{Co0}}{V_i} = \frac{1}{1 - D}. \tag{3.5}$$

To obtain the static gain, (3.2) is applied to (3.5), resulting in

$$\frac{V_o}{V_i} = \frac{m_u + m_l + 1}{1 - D}. \tag{3.6}$$

3.2.3 Inductor current ripple

By analysing the voltage across the input inductor in one stage it is possible to obtain the current ripple of the inductor. In the stages that one switch is ON, the

inductor voltage is described by

$$V_L = V_i - \frac{1}{2}V_{Co0} = L\frac{di_L}{dt} = \frac{L\Delta i_L}{DT_s} \tag{3.7}$$

where Δi_L is the inductor current ripple.

By developing the equation and writing it as a function of V_o, (3.7) is rewritten as

$$\Delta i_L = \frac{V_o\left(1-2D\right)D}{2Lf_s\left(m_u+m_l+1\right)}. \tag{3.8}$$

The current ripple is normalized to assess the influence of the duty cycle on the current ripple. The normalized current ripple is described by

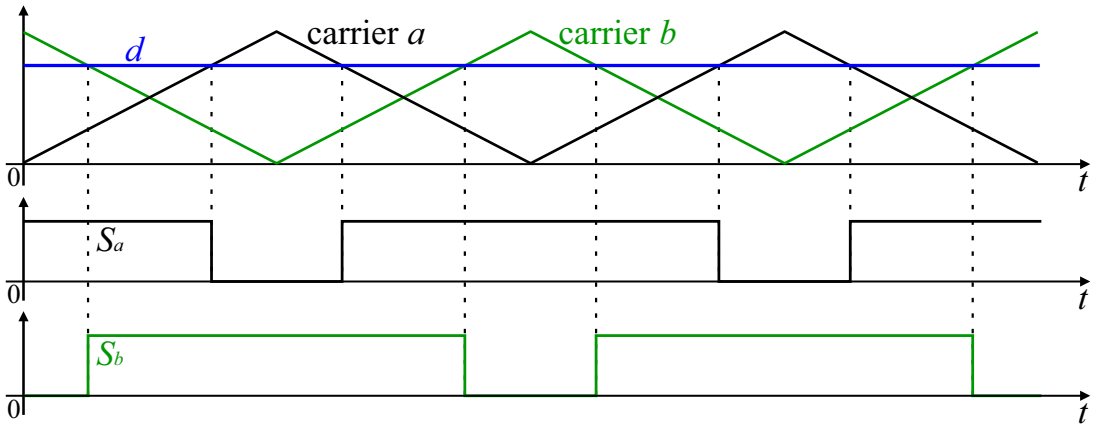
$$\overline{\Delta i_L} = \left(1-2D\right)D. \tag{3.9}$$

3.3 REGION B ($D > 1/2$)

3.3.1 Operation principle

Region B occurs when the converter operates with a duty cycle above 1/2. Thus, the operation of the converter alternates between in states 2 and 3. The switching signals overlap; therefore, there is always one or two switches turned ON at the same time. The modulation scheme for region B is illustrated in Fig. 63.

Fig. 63 – Modulation scheme for region B.



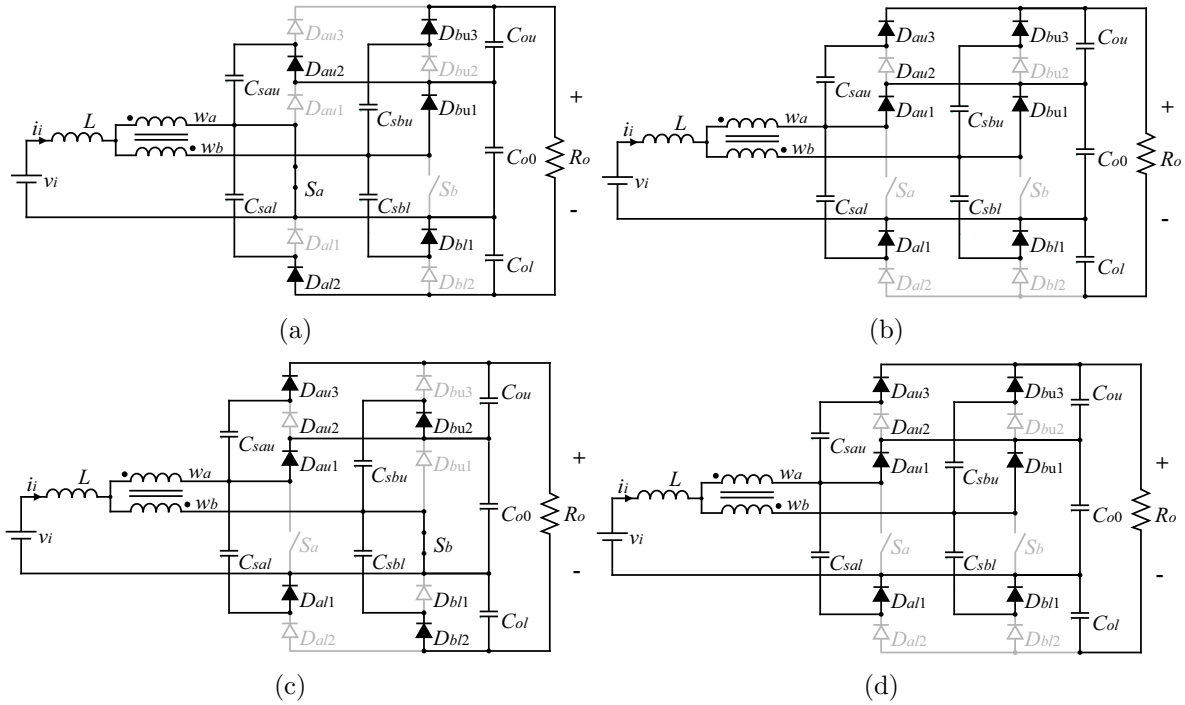
There are four operational stages in region B, which are illustrated in Fig. 64. In the first stage [See Fig. 64 (a)] the switch S_a is turned ON, the even numbered diodes conduct in leg a and the odd numbered diodes conduct in leg b. This stage in region B presents the same operation principle as in region A, since the topological state is the same. The current in the winding w_a flows through S_a and the current in w_b flows through the diodes connected to them. The capacitor C_{sau} stores energy and C_{sal} delivers energy to C_{ol}. In the leg b the capacitor C_{sbl} stores energy, since D_{bu1} is forward biased due to the current in the winding w_b. The upper cell capacitor C_{sbu} transfers energy to C_{ou}.

In the second stage [See Fig. 64 (b)] the switches S_a and S_b are turned ON and all even numbered diodes are forward biased. Since the switch command signals overlap

in this stage, the windings w_a and w_b are connected in parallel by S_a and S_b and the voltage across the transformer windings is zero. The upper cell capacitors C_{sau} and C_{sbu} store energy and the lower cell capacitors C_{sal} and C_{sbl} deliver energy to the lower output capacitor C_{ol}.

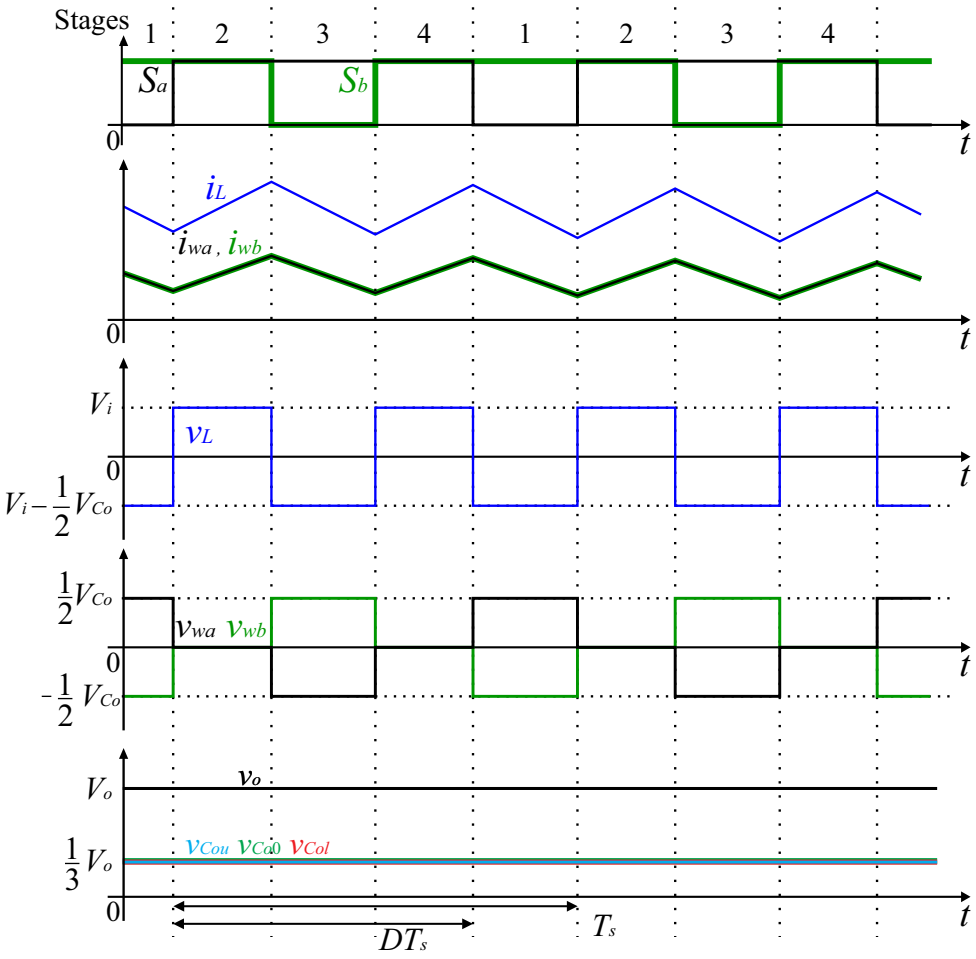
The third operational stage is similar to the first stage, but with S_b turned ON instead of S_a. The fourth operational stage has the same principle as the second stage, since both switches are turned ON.

Fig. 64 – Hybrid boost converter with MSSC and SC - Operational states in region B: (a) to (d) refer to stages 1 to 4.



The main waveforms in region B are illustrated in Fig. 64. The voltage across the capacitors have the same relation with the output as in region A, since the SC cell associate two capacitors in parallel in each stage. Therefore, the voltage across the capacitors are, ideally, the same. The current ripple in the input inductor is similar to region A as well. The input current ripple presents a frequency component that is twice the switching frequency, since the inductor voltage is the same for stages 1 and 3 and the same for stages 2 and four.

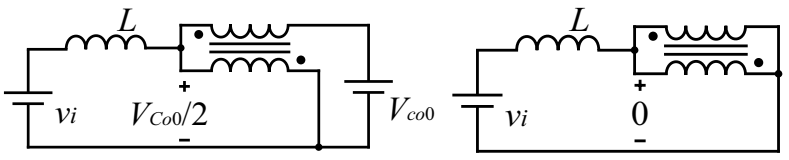
Fig. 65 – Main waveforms of the boost converter with 3SSC and SC in region B.



3.3.2 Static gain

The inductor volts-second relation is used to obtain the static gain of the converter. For every topological state that corresponds to each state described in Table 2 the inductor voltage has the same value, thus this analysis can be performed in half of the switching period. The stages 1 and 3 can be described by the equivalent circuit shown in Fig. 66 (a), that represents the state 2, and the stages 2 and 4 are described by the equivalent circuit shown in Fig. 66 (b), that represents the state 3.

Fig. 66 – Equivalent circuits in region B: (a) stages 1 and 3, (b) stages 2 and 4.



(a) (b)

In the stages 1 and 3 one switch is turned ON and the voltage across C_{o0} is divided between the windings. the stages 2 and 4 the windings of the ICT are connected in parallel and their voltages is zero. By analyzing the equivalent circuits, the average voltage across

the inductor in half switching period is given by

$$\langle v_L \rangle_{\frac{T_s}{2}} = \frac{2}{T_s}\left(\int_0^{\frac{(2D-1)T_s}{2}} V_i dt + \int_0^{(1-D)T_s} V_i - \frac{1}{2}V_{Co0}dt\right) = 0 \tag{3.10}$$

By solving the expression the relation between V_{Co0} and V_i is obtained, as given by

$$\frac{V_{Co0}}{V_i} = \frac{1}{1-D}. \tag{3.11}$$

The static gain is obtained by replacing (3.2) in (3.11) and rewritting it as a function of m, as described by

$$\frac{V_o}{V_i} = \frac{m_u + m_l + 1}{1-D}. \tag{3.12}$$

Although the voltage levels in the inductor in the second stage are different in region A and region B, the static gain is yet the same for both regions, as also occurs in the conventional boost converter with MSSC.

3.3.3 Inductor current ripple

The inductor current ripple is obtained by analysing the voltage across the inductor in one of the operational stages. The inductor voltage in the state 3 is described by

$$V_L = V_i = L\frac{di_L}{dt} = \frac{2L\Delta i_L}{(2D-1)T_s}. \tag{3.13}$$

The current ripple is then isolated in the expression, resulting in

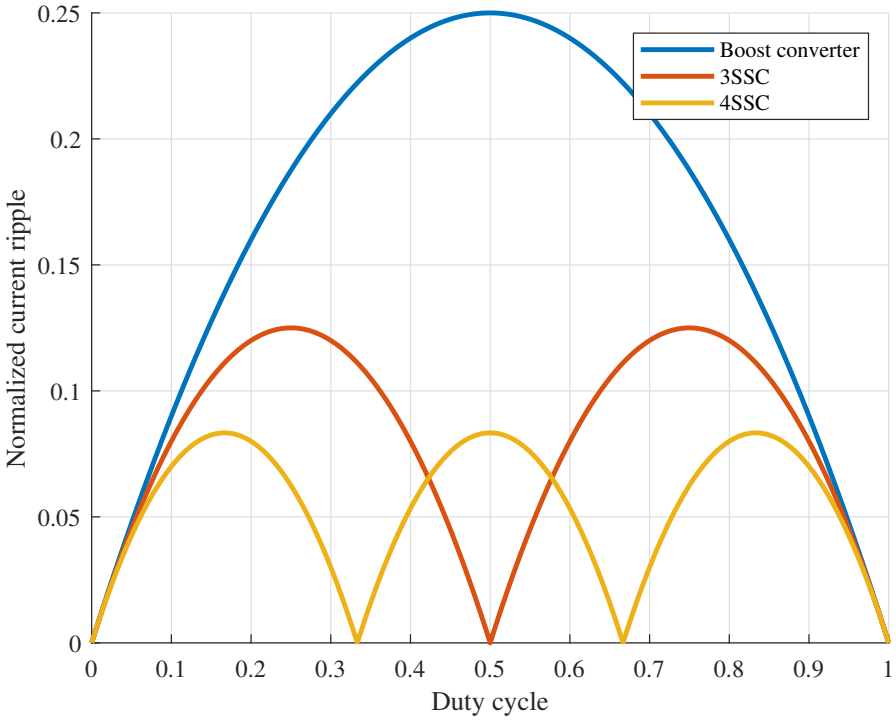
$$\Delta i_L = \frac{V_o(-2D^2 + 3D - 1)}{2Lf_s\left(m_u + m_l + 1\right)} \tag{3.14}$$

The relative normalized current ripple is then obtained, so that it can be compared to the normalized ripple in the other regions, as described by

$$\overline{\Delta i_L} = -2D^2 + 3D - 1. \tag{3.15}$$

The relative normalized current ripple is plotted versus the duty cycle and compared to the region A, as shown in 67. This figure also shows the normalized current of the conventional boost converter and the proposed topology with 3SSC to assess the main of using MSSC and the advantage of using a switching cell with more stages. Although there are still drawbacks regarding the increased complexity of the system with more cells and implementation issues regarding the geometry of commercial cores.

Fig. 67 – Normalized current ripple.



3.4 VOLTAGE STRESS

In each switching state, the converter connects capacitors in parallel, therefore the capacitor voltage values are the same, assuming that they were correctly designed for the switching frequency. When the switch of a leg is turned ON, the even numbered diodes of that leg are forward biased and the odd numbered are reverse biased, thus associating the OFF semiconductor devices in parallel with one of the output capacitors and cell capacitors. When the switch is turned OFF, the odd numbered diodes conduct and the even numbered ones block current, thus associating them in parallel with one output capacitor and cell capacitors. Thus, the voltage stress across the semiconductor devices is given by

$$V_S = V_D = V_C = \frac{V_o}{m_u + m_l + 1}. \tag{3.16}$$

3.5 CURRENT STRESS

Assuming that the legs share the power equally, and that the average current across the capacitors is zero, the average current across the diodes is described by

$$I_D = \frac{I_o}{n}. \tag{3.17}$$

where n is the number of legs in the converter.

By knowing the average current value and the time the diodes conduct, the average

current through the diode when it conducts is given by

$$\begin{cases} \langle i^{st1}_{Dieven} \rangle_{DT_s} = \frac{I_o}{nD} \\ \langle i^{st2}_{Diodd} \rangle_{(1-D)T_s} = \frac{I_o}{n(1-D)} \end{cases} \tag{3.18}$$

knowing that

$$I_L = I_o \frac{n(m_u + m_l + 1)}{1 - d} \tag{3.19}$$

the current in the odd numbered diodes can be written as

$$\left\langle i^{st2}_{Diodd} \right\rangle_{(1-D)T_s} = \frac{I_L}{(m_u + m_l + 1)n}. \tag{3.20}$$

The current values are presented as local average values during the ON period for simplifying, since the charge and discharge currents of the capacitors depend on many parasitic values to be calculated. Some idealizations are considered to estimate the current stress on devices, so that the equation does not become too complex and analytical solutions become impractical.

Knowing the average current through the even numbered diodes during their conduction, the switch average current during the ON period is estimated, given by

$$\left\langle i^{st1}_{Si} \right\rangle_{T_s} = i_{wi} + (m_u + m_l) \left\langle i^{st1}_{Dieven} \right\rangle_{T_s} = \frac{i_L}{n} + (m_u + m_l) \left\langle i^{st1}_{Dkeven} \right\rangle_{T_s} = \frac{1}{n} \left[i_L + (m_u + m_l)\, I_o \right]. \tag{3.21}$$

The switch and diode RMS currents are derived, as described by

$$\begin{cases} I^{RMS}_{Si} = \sqrt{\frac{1}{T_s} \int_0^{DT_s} \left(\frac{i_L}{n} + (m_u + m_l)\, \frac{I_o}{nD} \right)^2 dt} = \frac{\sqrt{D}}{n} \left(i_L + (m_u + m_l)\, \frac{I_o}{D} \right) \\ I^{RMS}_{Dieven} = \sqrt{\frac{1}{T_s} \int_0^{DT_s} \left(\frac{I_o}{nD} \right)^2 dt} = \frac{I_o \sqrt{D}}{nD} \\ I^{RMS}_{Dkodd} = \sqrt{\frac{1}{T_s} \int_{DT_s}^{T_s} \left(\frac{I_L}{n(m_u + m_l + 1)} \right)^2 dt} = \frac{I_L \sqrt{1-D}}{n(m_u + m_l + 1)} \end{cases} \tag{3.22}$$

3.6 MSSC DYNAMIC ANALYSIS

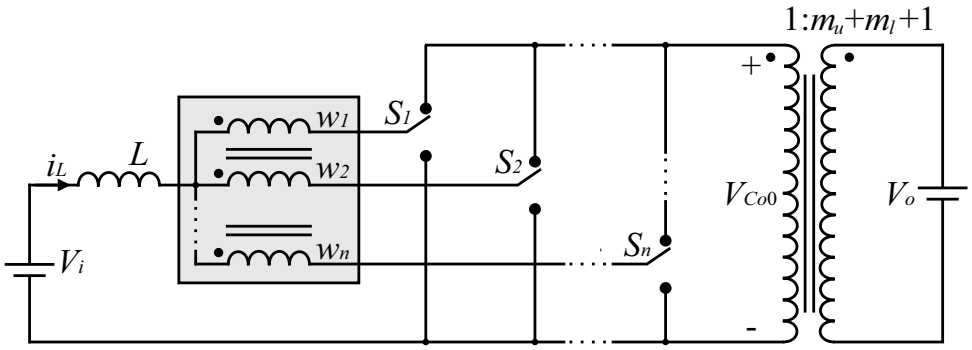
The equivalent circuit of the DC-DC converter shown in Fig. 68 is used. The ideal dc and ac transformer represents the SC cell voltage gain, and there is an ideal switch in each leg to represent the switching state of the converter. The switches and windings notation in this example are given in numbers, instead of letters, because it fits better the mathematical notation for a generalized analysis of the MSSC. In the 3SSC analysis, letters are used to make clearer if the number in the name of the component refers to a leg, or to a component in the SC cell.

The voltage across the switches is given by

$$v_{Si}(t) = V_{Co0} u_i \tag{3.23}$$

where u_i is the switch function referred to S_i and can be either 0 or 1.

Fig. 68 – Equivalent circuit for dynamic analysis.



The sliding average value of the switch function is described by

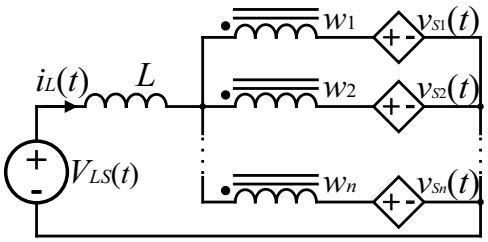
$$d_i(t) = \langle u_i \rangle = f_s \int_0^{Ts} u_k(t)dt = f_s \left(\int_0^{t_{on}} 1dt + \int_0^{t_{off}} 0dt \right) = t_{on} f_s. \tag{3.24}$$

(3.24) is replaced in (3.23) to obtain the sliding average voltage across the switches, given by

$$v_{Si}(t) = V_{Co0} d_i(t). \tag{3.25}$$

The equivalent circuit is then redrawn by replacing the switches by dependent sources with their average voltage values, illustrated in Fig. 69.

Fig. 69 – Averaged equivalent circuit.



The voltage across the windings of the ICT are described by

$$v_{wi}(t) = L_{ii} \frac{di_{wi}(t)}{dt} + \sum_{j=1 \wedge j \neq i}^{n} M_{ij} \frac{di_{wj}(t)}{dt} \tag{3.26}$$

where L_{ii} is the self inductance of winding w_i and M_{ij} are the mutual inductances. (3.26) is expanded to all the windings and rewritten in matrix notation as

$$V_{wICT} = M_{ICT} \cdot \frac{d}{dt} I_{wICT}. \tag{3.27}$$

where V_{wICT} is the ICT windings voltage vector, M_{ICT} the inductance matrix and I_{wICT}

the current vector, described by

$$\begin{cases} V_{wICT} = \begin{bmatrix} v_{w1}(t) & v_{w2}(t) & \cdots & v_{wu}(t) \end{bmatrix}^T \\ M_{ICT} = \begin{bmatrix} L_{11} & M_{12} & \cdots & M_{1n} \\ M_{21} & L_{22} & \cdots & M_{2n} \\ \vdots & \vdots & \ddots & \cdots \\ M_{n1} & M_{n2} & \cdots & L_{nn} \end{bmatrix} \\ I_{wICT} = \begin{bmatrix} i_{w1}(t) & i_{w2}(t) & \cdots & i_{wn}(t) \end{bmatrix}^T \end{cases}. \tag{3.28}$$

The voltage across the windings of the ICT an also be described by analysing the diagram shown in (69), obtaining

$$v_{wn}(t) = V_i - v_{Si}(t) - L\frac{di_L(t)}{dt}. \tag{3.29}$$

Since the inductor current is the sum of the current in all windings, (3.27) is replaced in (3.29) and rewritten as

$$M_{ICT} \cdot \frac{d}{dt} I_{wICT} = V_i \cdot I_n - V_{Co0} \cdot D_{MSSC} - L \cdot J_k \cdot \frac{d}{dt} I_{wICT} \tag{3.30}$$

where J_k is a $k \times k$ matrix of ones, I_n is a $n \times n$ identity matrix and D_{MSSC} is the MSSC duty cycle vector, described by

$$D_{MSSC} = \begin{bmatrix} d_{w1}(t) & d_{w2}(t) & \cdots & d_{wi}(t) \end{bmatrix}^T. \tag{3.31}$$

The terms related to i_{wk} are isolated and (3.30) is rewritten as

$$(L \cdot J_n + M_{wICT}) \cdot \frac{d}{dt} I_{wICT} = V_i \cdot I_n - V_{Co0} \cdot D_{MSSC}. \tag{3.32}$$

The expression is simplified by assuming that the duty cycle value is the same for every leg and the magnetic core is symmetric (i.e. the legs have the same reluctance value). Since the self inductances in all legs are considered the same, as well as the duty cycle, the current value in each winding and their dynamic characteristics are the same. The only difference between the legs is a delay that occurs due to the phase-shift during a fraction of the switching period. However, since this analysis considers the CCM with low current ripple and the sliding average values during T_s, the converter dynamics during a fraction of the switching period can be neglected, since they do not add dominant poles or zeros to the converter small-signal model. Therefore

$$\begin{cases} L_{ii} = L_{11} = L_{22} = \ldots = L_{nn} \\ d(t) = d_1(t) = d_2(t) = \ldots = d_n(t) \\ M_{ij} = -\frac{1}{n-1}\sqrt{L_{ii}L_{jj}} \\ i_{wa}(t) = i_{w2}(t) = \ldots = i_{wn}(t) = \frac{i_L(t)}{n} \end{cases}. \tag{3.33}$$

(3.33) is replaced in (3.32), resulting in

$$(L \cdot J_k + M_{wsym}) \cdot \frac{d}{dt} \begin{bmatrix} \frac{i_L(t)}{n} \\ \frac{i_L(t)}{n} \\ \vdots \\ \frac{i_L(t)}{n} \end{bmatrix} = V_i \cdot I_k - V_{Co0} \cdot D_{MSSC} \tag{3.34}$$

where M_{wsym} is the ideal inductance matrix of a ICT with a symmetrical core, given by

$$M_{wsym} = \begin{bmatrix} L_{ii} & -\frac{L_{ii}}{n-1} & \cdots & -\frac{L_{ii}}{n-1} \\ -\frac{L_{ii}}{n-1} & L_{ii} & \cdots & -\frac{L_{ii}}{n-1} \\ \vdots & \vdots & \ddots & \vdots \\ -\frac{L_{ii}}{n-1} & -\frac{L_{ii}}{n-1} & \cdots & L_{ii} \end{bmatrix}. \tag{3.35}$$

Assuming the idealizations proposed in (3.33), the sum of transformer self and mutual inductances in each row of the matrix $M_{wsym}$is zero and (3.34) is rewritten as

$$L\frac{di_L(t)}{dt} = V_i + V_{Co0}d(t). \tag{3.36}$$

The expression is decomposed in large and small signal terms, resulting in

$$L\frac{d\widetilde{i}_L(t)}{dt} = V_i + V_{Co0}D + V_{Co0}\widetilde{d}(t). \tag{3.37}$$

By neglecting the large-signal variables, applying the Laplace transform and rewritting it in function of the output voltage, the input current transfer function is described by

$$\frac{\widetilde{i}_L(s)}{\widetilde{d}(s)} = \frac{V_{Co0}}{sL} = \frac{V_o}{sL(m_u + m_l + 1)}. \tag{3.38}$$

The resulting transfer function is the same as the conventional boost converter transfer function, which implies that, for a symmetrical core topology, the transformer dynamics can be neglected. The main difference in the converter dynamics between the conventional boost converter and the converter with an MSSC is the inductor size, which results in faster dynamics for the MSSC boost converter.

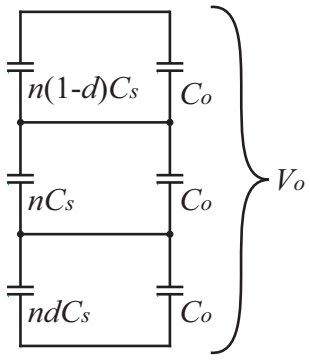
3.7 OUTPUT VOLTAGE DYNAMIC ANALYSIS

Due to the complexity of SC converters and number of operational stages in the proposed topology, equivalent circuits are useful tools to obtain the dynamic characteristic of the converter. Since the ICT does not affect the converter static gain or the dynamics of the converter, the circuit can be represented as a conventional boost converter with an ideal transformer that represents the SC-cell. However, to analyze the output dynamics, the SC cell must be considered.

An equivalent capacitance value is obtained from the SC cell to represent how it affects the total output dynamics. For that, an equivalent capacitance is obtained for each output capacitor by analysing the capacitors associated in parallel in each stage, as performed in [120]. Because each cell capacitor is connected to an output capacitor

during the times dT_s and $(1-d)T_s$, the output can be viewed as an average equivalent capacitance, as shown in Fig. 70.

Fig. 70 – Equivalent output capacitance.



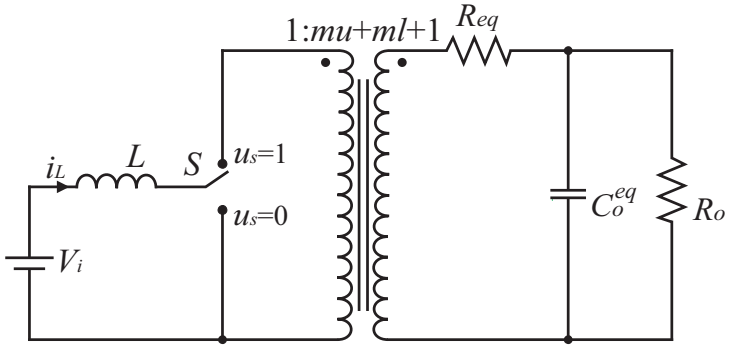
By calculating the equivalent capacitance as viewed by the output, based on the association shown in Fig. 70, the equivalent capacitance for the proposed topology with one upper and one lower SC in each leg is described by

$$C_o^{eq} = \frac{(C_o + C_s n)\,(C_o + C_s dn)\,(C_o + C_s n - C_s dn)}{3{C_o}^2 + 4C_o C_s n - {C_s}^2 d^2 n^2 + {C_s}^2 dn^2 + {C_s}^2 n^2} \tag{3.39}$$

In the previous analysis it was shown that the effect of the ICT can be neglected in the dynamic analysis. The dynamic effect of the SC-cell in the output can also be represented by an equivalent capacitor [120–122]. Therefore, the converter can be simplified for the dynamic analysis as the circuit shown in Fig. 71, where R_{eq} is the equivalent resistance of one leg divided by the total number of legs.

Although it has only one switch and one capacitor, it presents the same dynamic characteristics as the circuit with MSSC and SC cells, since the steady-state characteristics are the same and the previous section showed that the ICT influence on the input dynamics is negligible when the self inductances of the ICT are very similar. For obtaining the transfer functions of the system, a state space averaging analysis is performed, as presented in [122].

Fig. 71 – Equivalent DC-DC converter.



The state equation system is given by

$$\begin{cases} \dot{x} = A \cdot x + B \cdot u \\ y = E \cdot x + F \cdot u \end{cases} \tag{3.40}$$

where the state vector and the input vector are described by

$$\begin{cases} x = \begin{bmatrix} i_L & v_{C_o^{eq}} \end{bmatrix}^T \\ u = V_i \end{cases} . \tag{3.41}$$

By solving the circuit for the two topological states $u_s = 0$ and $u_s = 1$, the state and input matrices are obtained, given by

$$\begin{cases} A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_o C_o^{eq}} \end{bmatrix}, \quad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\ A_2 = \begin{bmatrix} -\frac{R_{eq}}{(m_u+m_l+1)^2 L} & \frac{1}{(m_u+m_l+1)L} \\ \frac{1}{(m_u+m_l+1)C_o^{eq}} & -\frac{1}{R_o C_o^{eq}} \end{bmatrix}, \quad B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \end{cases} . \tag{3.42}$$

The feedforward matrix value is zero, since the input does not affect the output directly, and the matrix E for obtaining the input current and output voltage in function of the duty cycle is given by

$$\begin{cases} E_i = \begin{bmatrix} 1 & 0 \end{bmatrix} \\ E_v = \begin{bmatrix} 0 & 1 \end{bmatrix} \end{cases} . \tag{3.43}$$

By linearising the matrices and applying the Laplace transform, the transfer function is described by

$$G(s) = E(sI_2 - A)^{-1} \cdot [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U] \tag{3.44}$$

where

$$A = A_1 D + A_2(1 - D). \tag{3.45}$$

In expression (3.44), I_2 is a 2×2 identity matrix and the matrix E can be replaced by E_v or E_i, whether the output voltage or input current transfer function must be obtained.

3.8 SIMULATION RESULTS

Simulations were performed to assess the theoretical analysis of the proposed topologies. The software PSIM was used to simulate the circuit. The simulations results were exported to a .csv format and plotted with the software MATLAB for better presenting them. The main specifications of the circuit are presented in Table 3. The parasitic elements of the circuit are based on commercial components that were used for experimental validation.

First, the converter was simulated in the rated power operation point. The duty cycle was set as 0.75 to achieve the specified gain of 12, as can be seen in Fig. 72. The average output voltage achieved was 1188 V due to the parasitic elements, which cannot be neglected in the simulation due to the natural characteristic of the SC cells. In this simulation it is possible to see the first advantage of the proposed structure, that is the high voltage gain. With a duty cycle of 0.75, the converter achieved a gain of approximately 12, which is three times higher than the conventional boost converter.

The inductor and ICT currents were simulated at the rated operation point. The inductor was designed for a current ripple of 10% of the input current, that is ideally 10 A. The average input current value in the simulation is 9.9 A and the current ripple is 0.96 A.

Table 3 – Specifications of the proposed DC-DC converter

Specification	**Value**
Input voltage V_i	100 V
Output voltage V_o	1200 V
Output power P_o	1 kW
Switching frequency f_s	100 kHz
Switched capacitors C_s	5.6 μF
Output capacitors C_o	2 x 5.6 μF
Input inductor L_i	250 μH
ICT self inductances L_i	4800 μH
Switch resistances (Rohm SCT2080AL) R_s	80 mΩ
Diode resistances (Cree C3D04065A) R_d	100 mΩ
Diode forward voltage V_d	0.9 V

The inductor and ICT currents are shown in Fig. 73. This figure presents two advantages of the proposed topology: 1 - the multiplied switching frequency in the inductor and 2 - the current share between the windings of the ICT, that present an average current of 4.95 A each.

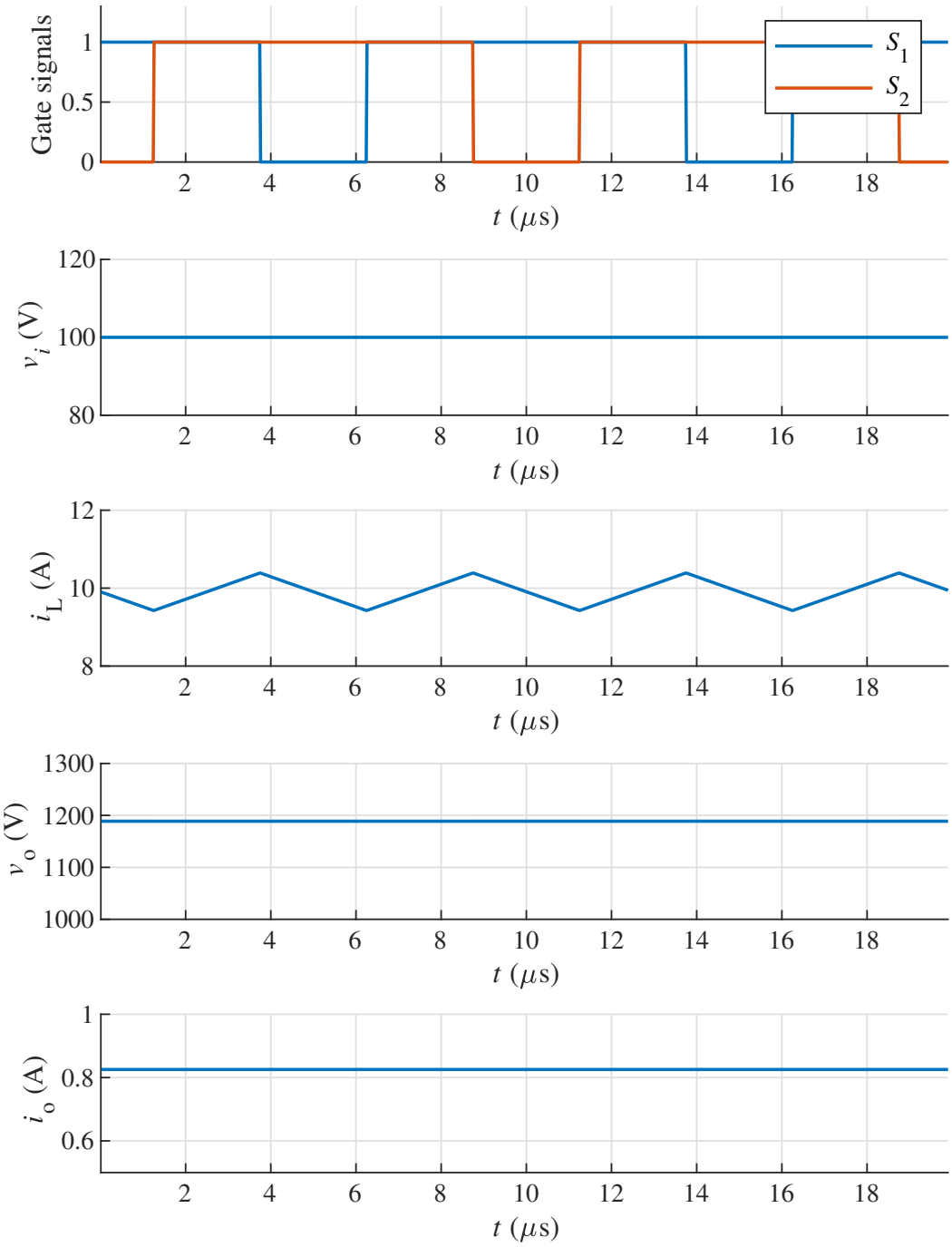
Another advantage of this topology is the divided voltage stress across the components. For this analysis, the voltage across the switch, diodes and capacitors are shown in Fig. 74 for one leg, since the voltage across the other legs have the same shape phase-shifted. In this study, the diode reverse voltages are shown, instead of the forward voltages for aesthetic purposes. The maximum voltage on each semiconductor device is around 400 V, that is one third of the output voltage. The voltage difference across the capacitors is due to the losses in the circuit. The voltage value across the switched capacitors V_{Cau} and V_{Cal} is different due to the parasitic elements in the current path of each stage, that is different in the dc-dc and single-phase ac-dc topology because of the diode D_{au1}, which causes an asymmetry in the upper and lower SC cells.

The current in the switches, diodes and cell capacitors were also obtained, as shown in Fig. 75. The calculated RMS current across S_1 is around 5.29 A and the simulated current is around 5.35 A, which is an acceptable deviation, assuming that the high frequency ripple was neglected in the theoretical analysis. The calculated average current across the diodes is 8.33 A and the simulated values were around 0.417 A and 0.412 A. The difference between the calculated and simulated values is mainly due to the static gain, that is slightly lower in the simulated circuit due to the converter losses. Due to the many operational stages and the fact that in some stage two cell capacitors deliver current at the same time to the output, the capacitor currents become non-linear. Knowing the output voltage and the voltage across C_{o0} and assuming that the average output current of the SC cell is the average current in D_{au3} or D_{al2}, the equivalent resistance of a single cell can be estimated. The calculated R_{eq} for the rated power conditions is 5.7 Ω and the simulated equivalent resistance is 5.9 Ω.

To validate the transfer function of the converter, a duty cycle step of 0.01 was applied and the simulated signals were compared to the step response of the transfer function in the software MATLAB. This comparison is shown in Fig. 76, where it is shown that the simulation response is very similar to the calculated transfer function.

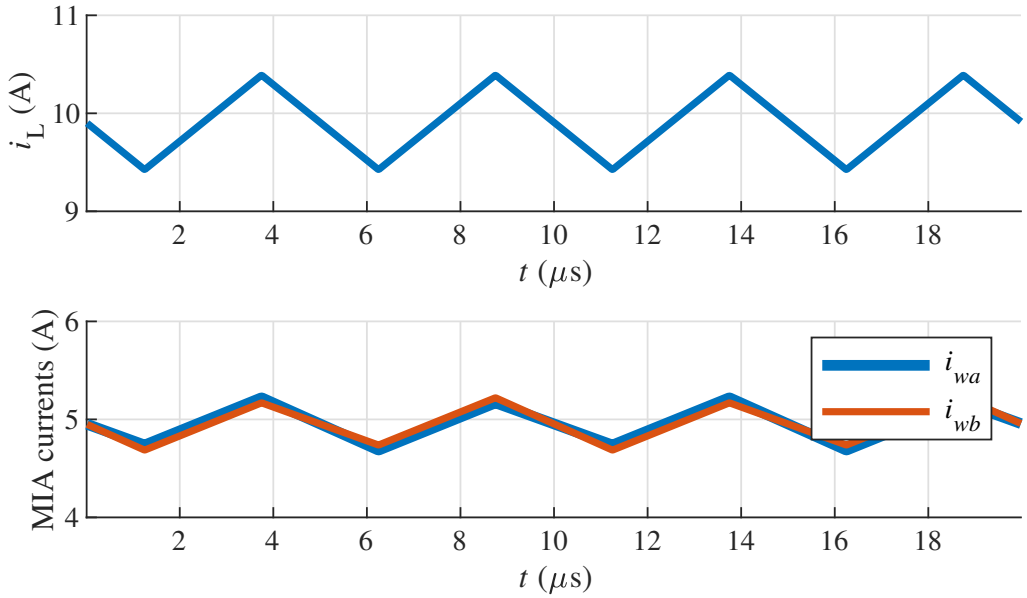
After validating the transfer functions, a controller was designed for practical applications. The block diagram of the controlled system is shown in Fig. 77. The control

Fig. 72 – Simulation of the DC-DC topology - Rated power.



system consists of two cascaded control loops, an outer voltage control loop and an inner current control loop. The outer control loop was designed with a 200 Hz crossover frequency and a 90° phase margin, and the faster inner loop was designed with a 2 kHz

Fig. 73 – Simulation of the DC-DC topology - Current in the inductor and ICT.



crossover frequency and a 60° phase margin. The controller was implemented digitally with the C-block with a 25 kHz sample frequency to simulate the actual controller that was used for the experimental verification.

Finally, to evaluate the controller, a load step was applied from 50% to 100% of the rated load value, and then a 100% to 50% load step was applied after the system was settled. Fig. 78 shows the output voltage and current and the capacitor voltages during the transient. The capacitors in an SC cell transfer enough energy to one another in a switching period, so that the transient does not affect their voltage balance. Because of that, the cell dynamic can be neglected in the analysis and no additional control loop is necessary to guarantee the capacitors voltage balance. This aspect is also important because an imbalance during the load transient could provoke high voltage peaks across other devices, which could be destructive. Due to the SC cell natural behavior, this cannot occur in the proposed topology, unless the controller or the capacitors are not properly designed.

Fig. 74 – Simulation of the DC-DC topology - Voltage stress across the switch, diodes and capacitors of leg a.

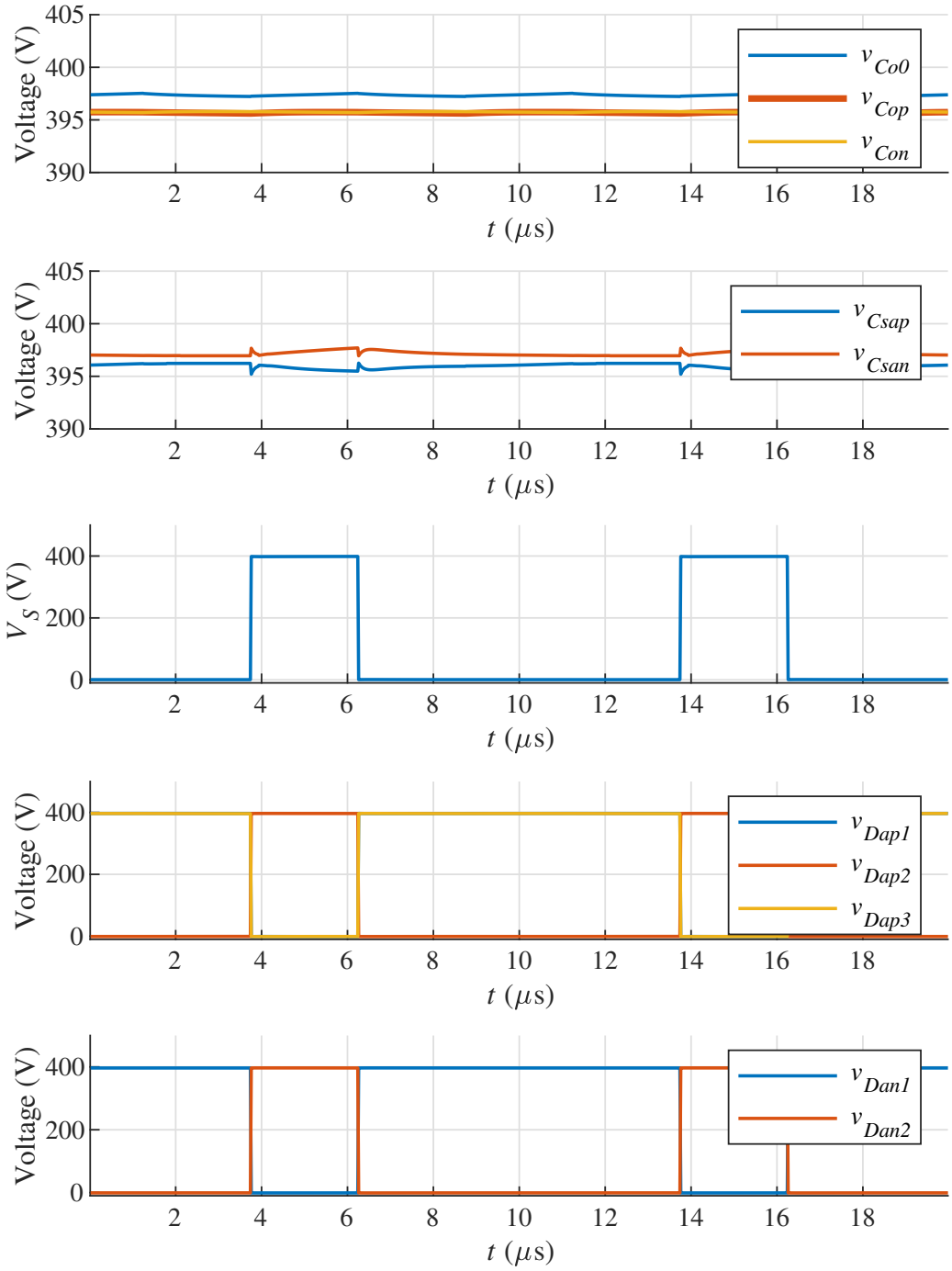


Fig. 75 – Simulation of the DC-DC topology - Current stress across the switch, diodes and capacitors of leg a.

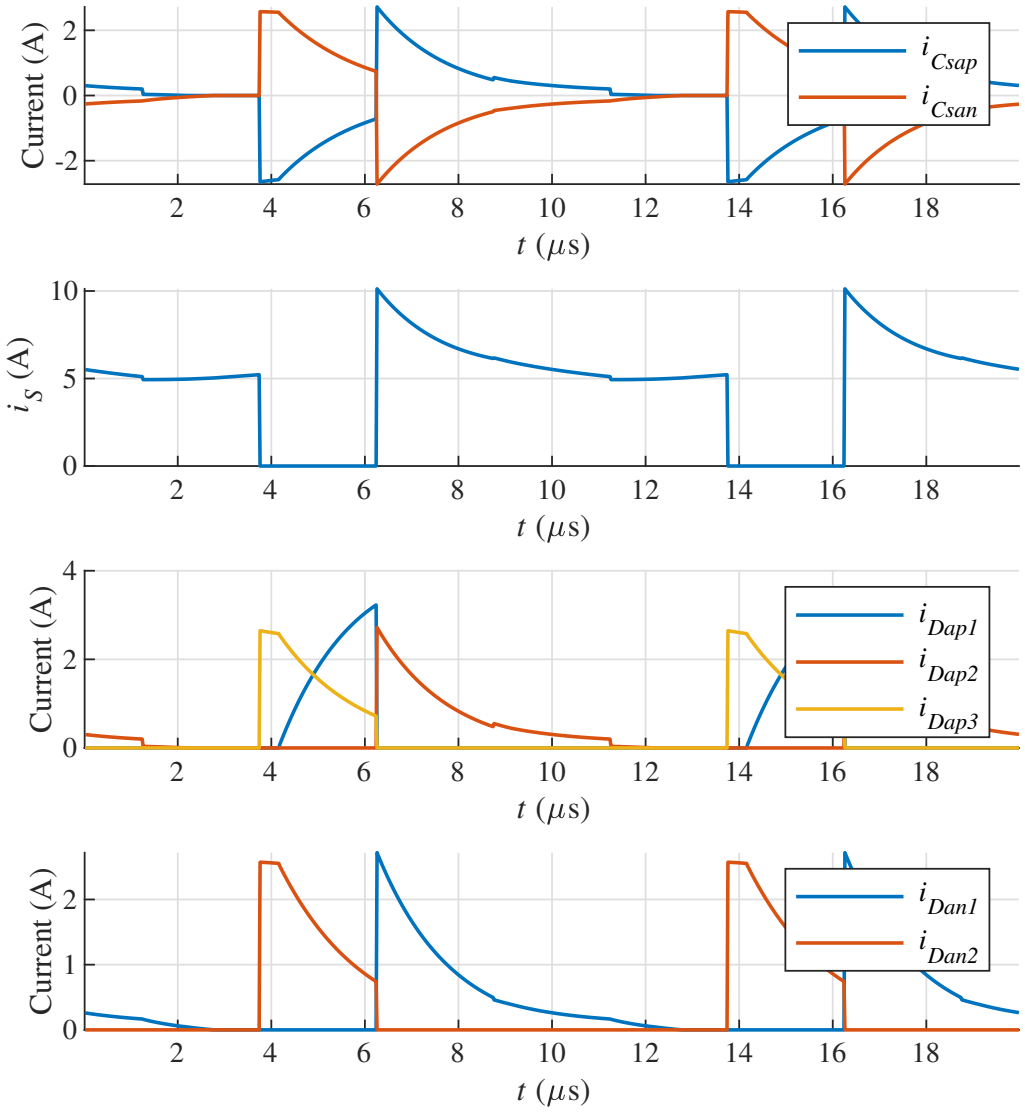


Fig. 76 – Simulation of the DC-DC topology - Duty cycle step.

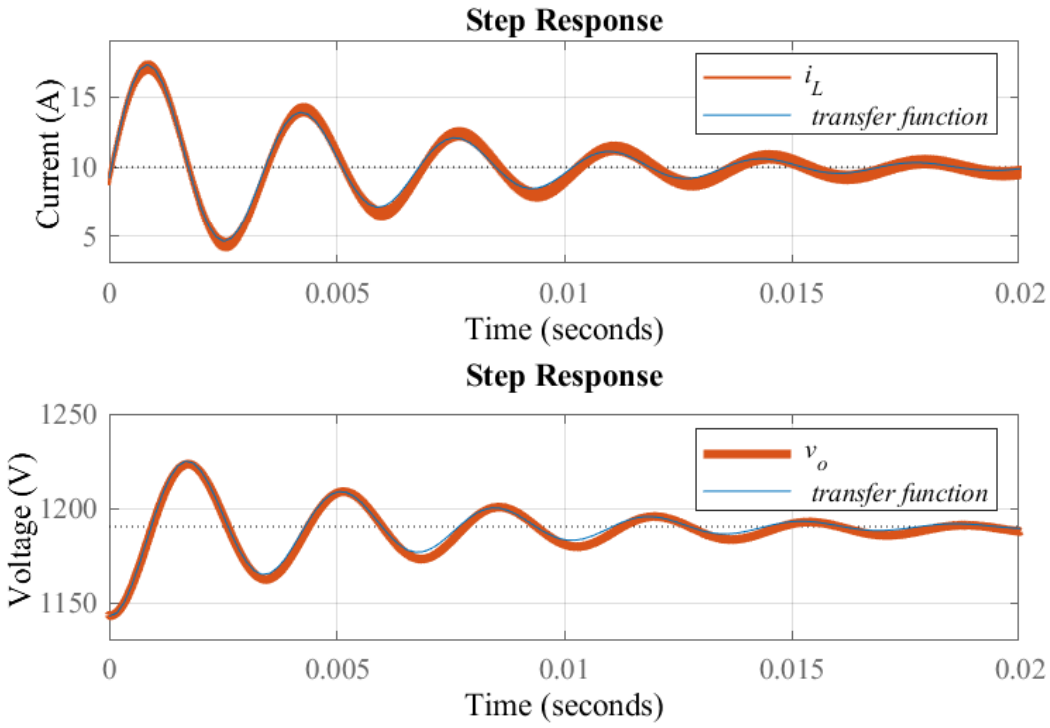


Fig. 77 – Controlled system block diagram.

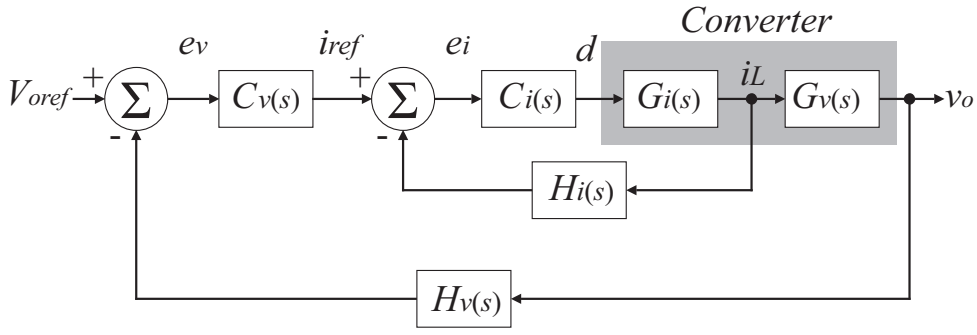
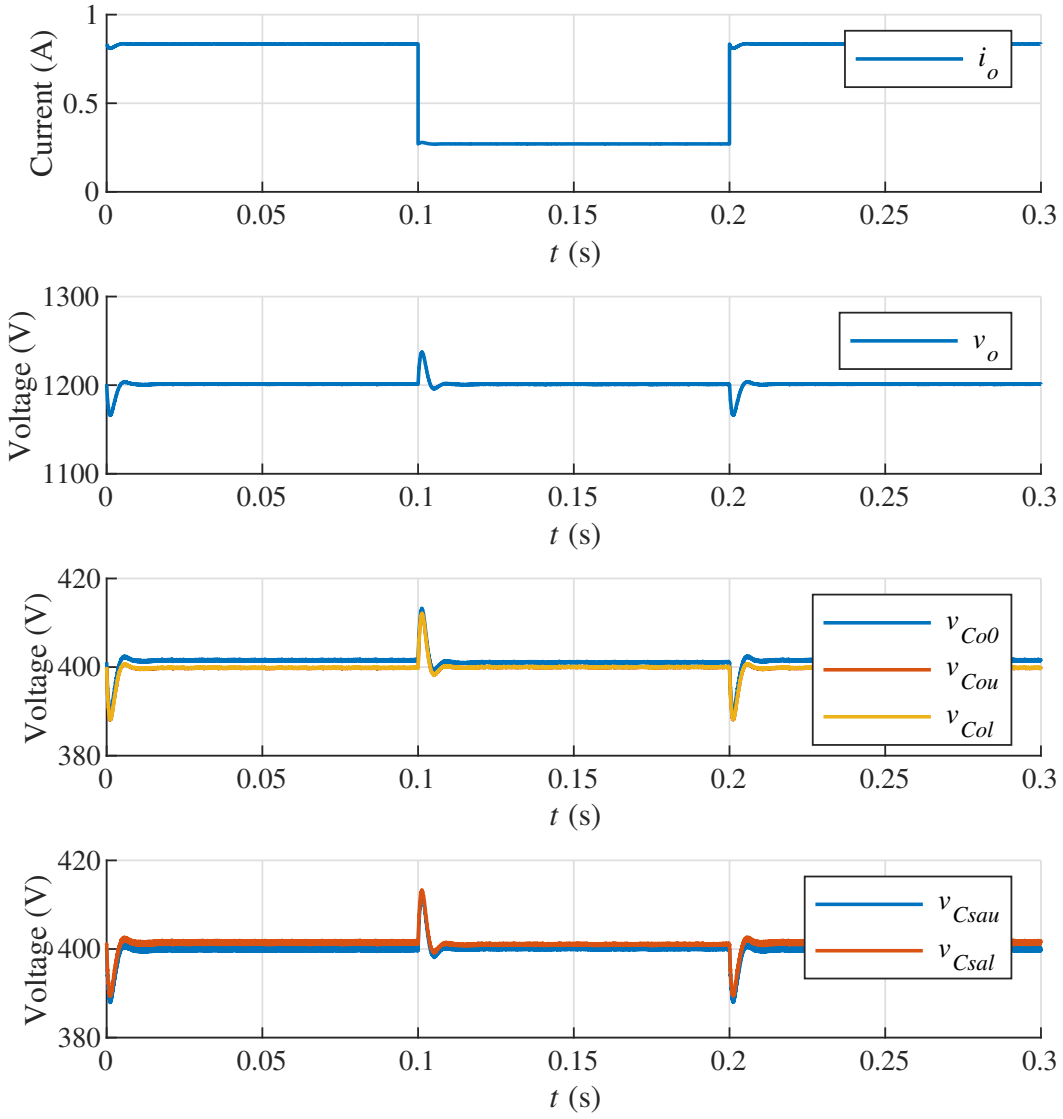


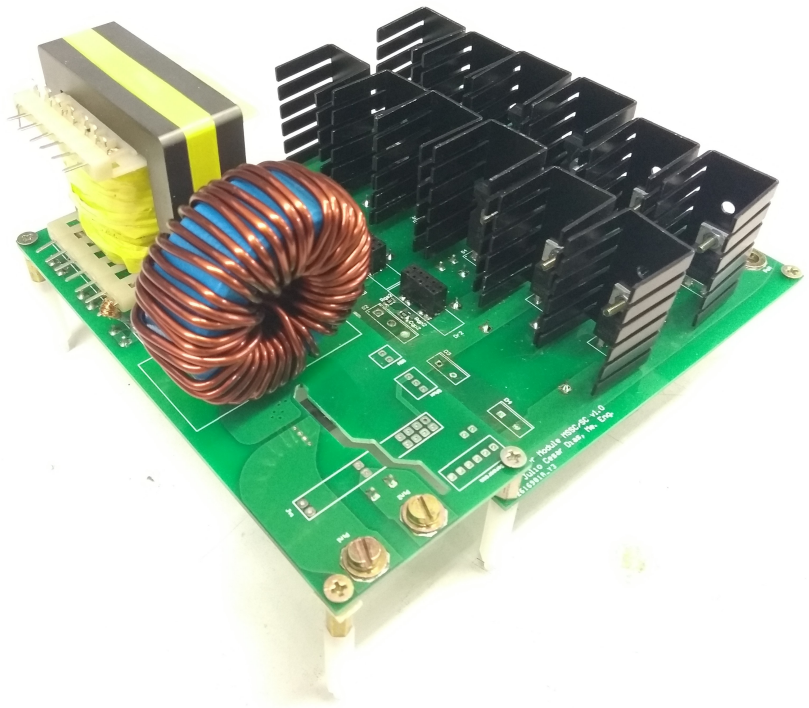
Fig. 78 – Simulation of the DC-DC topology - Output load step disturbance.



3.9 EXPERIMENTAL RESULTS

To evaluate the proposed converter a prototype was built. Since the main contribution of this thesis is to not only present the proposed concept to dc-dc converters, but to also expand the concept to unidirectional ac-dc converters, the prototype was build to suit different configurations and use the same modules for all proposed converters, the dc-dc converter, the single-phase and the three ac-dc converter. If one diode bridge is connected in the prototype input, and large capacitors at its output, it can operate as a single-phase ac-dc converter. To operate the converter as a three-phase ac-dc converter, three modules must be used and the first upper diode in each leg must be replaced by an active switch. The picture of one dc-dc module is shown in Fig. 80, this module has a power density of 420 W/L considering its rated voltage gain (100 V to 1200 V), but it was also tested with a higher power level for a higher input voltage (1800 W and 180 V), achieving a power density of 756 W/L. The specifications of the proposed converter are the same that were used for the simulations, shown in Table 3.

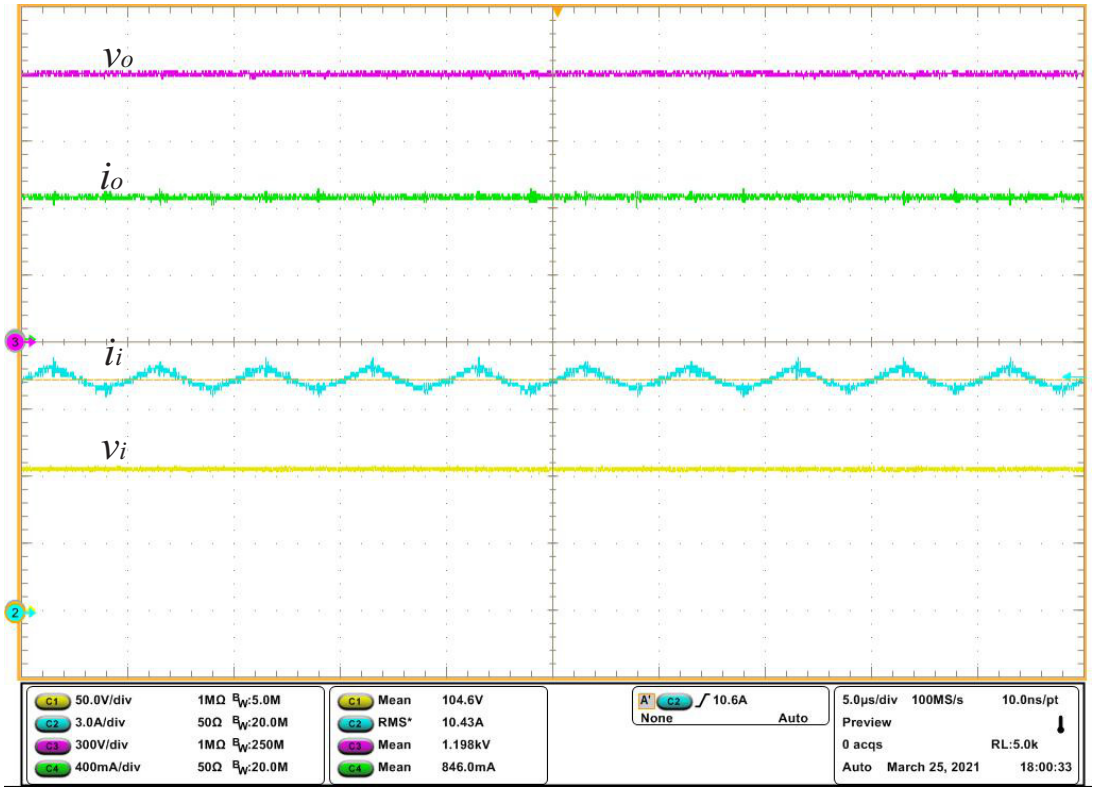
Fig. 79 – Picture of the proposed dc-dc converter.



The converter was able to increase the voltage from 100 V to 1200 V at 1 kW, as seen in Fig. 80. It can be seen that the input current presents a 200 kHz ripple, twice the switching frequency. The average input and output voltages are 104.6 V and 1198 V, respectively.

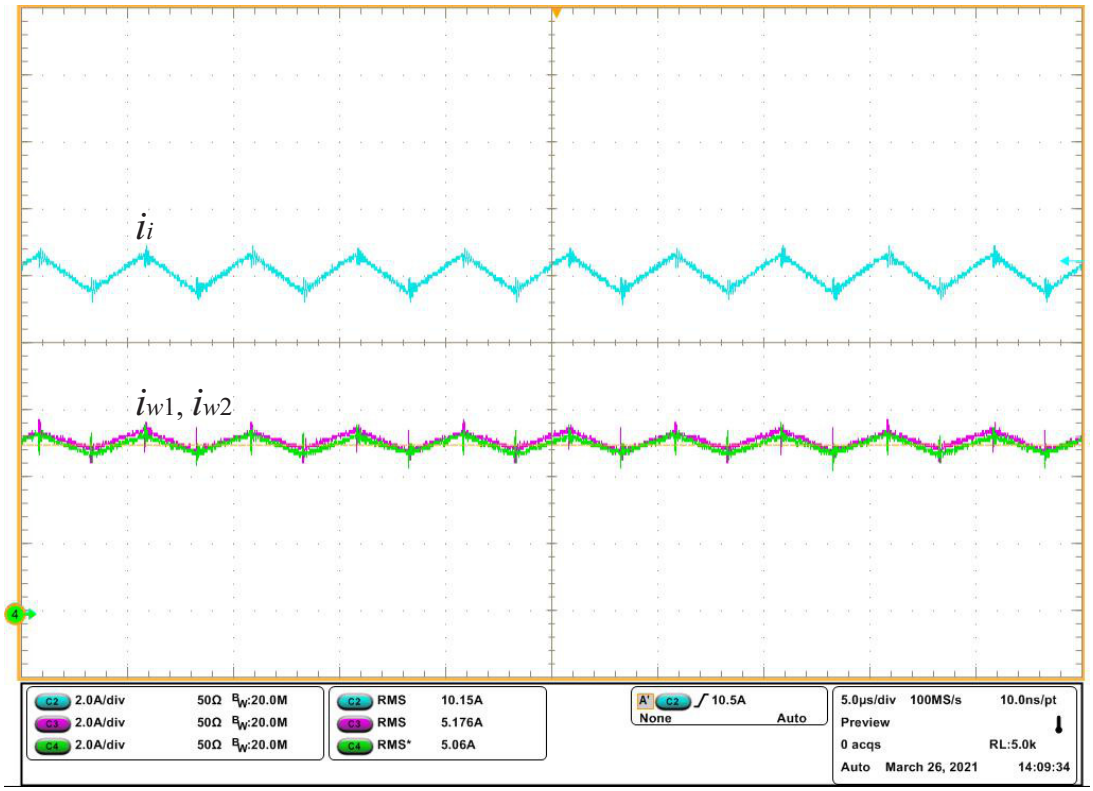
The MSSC was capable of sharing the current between the ICT windings, as can be seen in Fig. 81. There were some imbalance issues in the experimental verifications, which were solved by fixing differences in the gate drivers. The gate drivers used in this work were made with hand-made transformers for their isolated power supplies. However, with very similar gate drivers there were no balance issues. Differences between the self-inductances in simulation have not caused imbalance issues, but duty cycle differences

Fig. 80 – Experimental results for the dc-dc converter - Rated power operation.



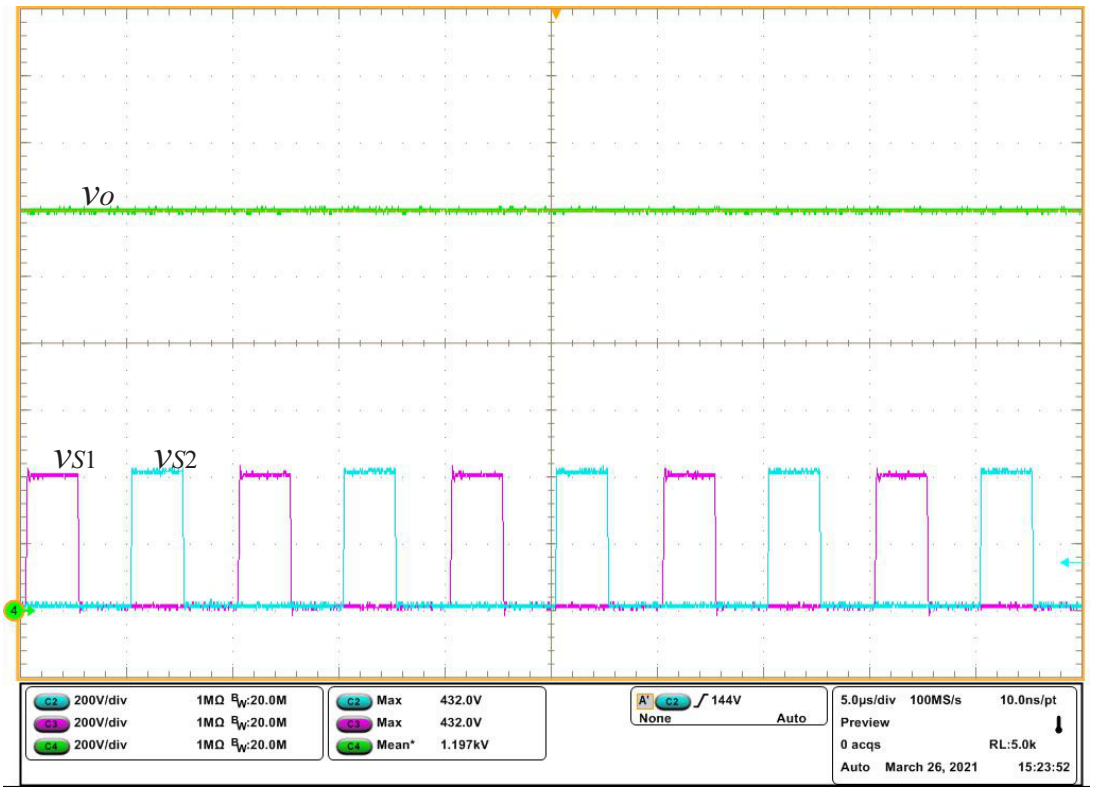
can cause imbalances. If the gate drivers are very similar the imbalance issues can be solved without using active control techniques.

Fig. 81 – Experimental results for the dc-dc converter - Inductor and ICT current.



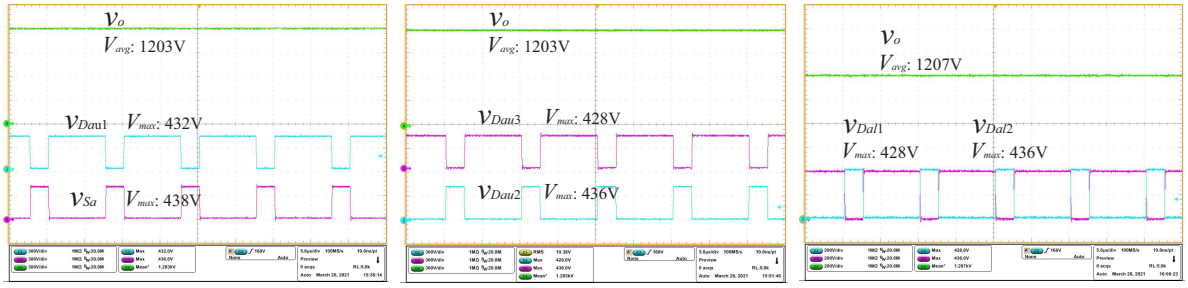
One of the main advantages of the proposed converter is the current sharing from the MSSC, the other advantage is the voltage sharing without the need of active balancing techniques due to the SC cell. This feature also makes it possible to use switches and diodes designed for lower voltages, since the voltage across them is a fraction of the output voltage. Fig. 82 shows the voltage across the switches of the proposed 3SSC. The maximum voltage on the switches is about 430 V, whereas the average output voltage is around 1.2 kV, showing the voltage sharing characteristic of the converter.

Fig. 82 – Experimental results for the dc-dc converter - Voltage on the switches.



Due to the capacitor voltage sharing, the voltage stress on the diodes is also reduced to a fraction of the output voltage. Fig. 83 shows that for an output voltage around 1200 V it is possible to use upper and lower diodes designed for a voltage about 400 V.

Fig. 83 – Voltage across the semiconductor devices: (a) Switch and upper diode D_{au1}, (b) upper diodes D_{bu2} and D_{au3} and (c) lower diodes D_{al1} and D_{al2}.

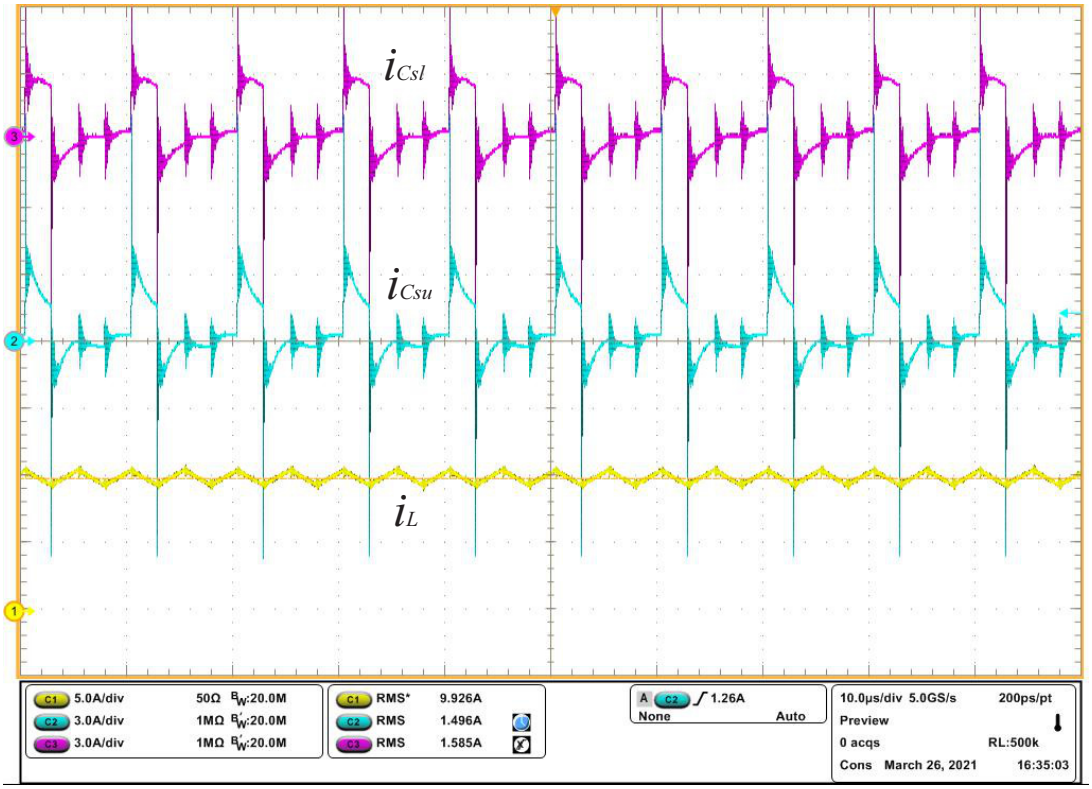


(a) (b) (c)

As mentioned in chapter 2, it is important to design the SC cell to reduce the losses due to the high currents that occur during the capacitor charge and discharge. The

current in the upper and lower cell capacitors of one leg were measured to check if the SC cell operates near the partial charge mode and to verify its shape. The experiments were performed with Rogowski probes, which can be used to evaluate the shape of the currents, but are very susceptible to noise. As can be seen in Fig. 84, the current shapes do not present high spikes besides the noise. It can also be seen that the current shape is slightly different in the upper and lower cell capacitor. This is due to the path impedances, since the switch and diodes do not have the same parasitic characteristics.

Fig. 84 – Experimental results for the dc-dc converter - Current in the cell capacitors.



To evaluate the controlability of the converter, some tests were performed by applying a load step on its output from 50% to full load and vice-versa. A simple cascaded controller with an outer voltage loop and an inner current loop was used. The controller was implemented digitally through the DSP Texas TMS320F28379D. There were no active current balancing techniques in the ICT. Since the gate drivers and switches were very similar, the current was naturally balanced, as can be seen in Fig. 85.

The efficiency of the converter was verified for three conditions with three input voltage levels. As the input voltage increases, a higher power level can be achieved, since the current is lower. In Fig. 85 it can be seen that for a higher input voltage level it is possible to achieve efficiency levels above 98%. The efficiency analysis was performed with a Yokogawa WT1800 power analyzer. It is shown also that for a lower voltage and a conversion ratio of 12 (100 V to 1200 V) it is possible to achieve a peak efficiency level above 97%. The efficiency at rated power was around 96.7%, while the theoretically calculated efficiency was around 96.6%, which shows that the idealizations performed in the theoretical analysis was adequate to design the converter.

A loss breakdown was performed to verify where most of the power is dissipated in the converter at rated power operation and a 100 V to 1200 V conversion, illustrated in Fig. 87. It can be noticed that most losses are in the switches, since they are submitted

Fig. 85 – Experimental results for the dc-dc converter - Load step.

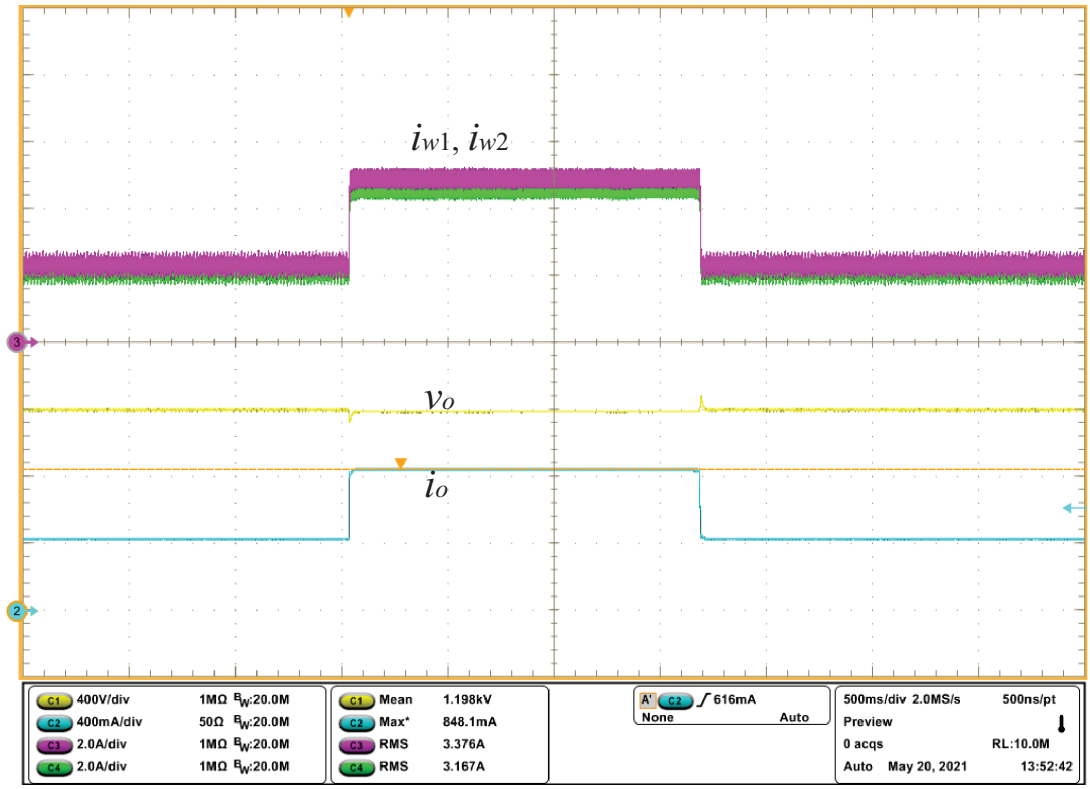
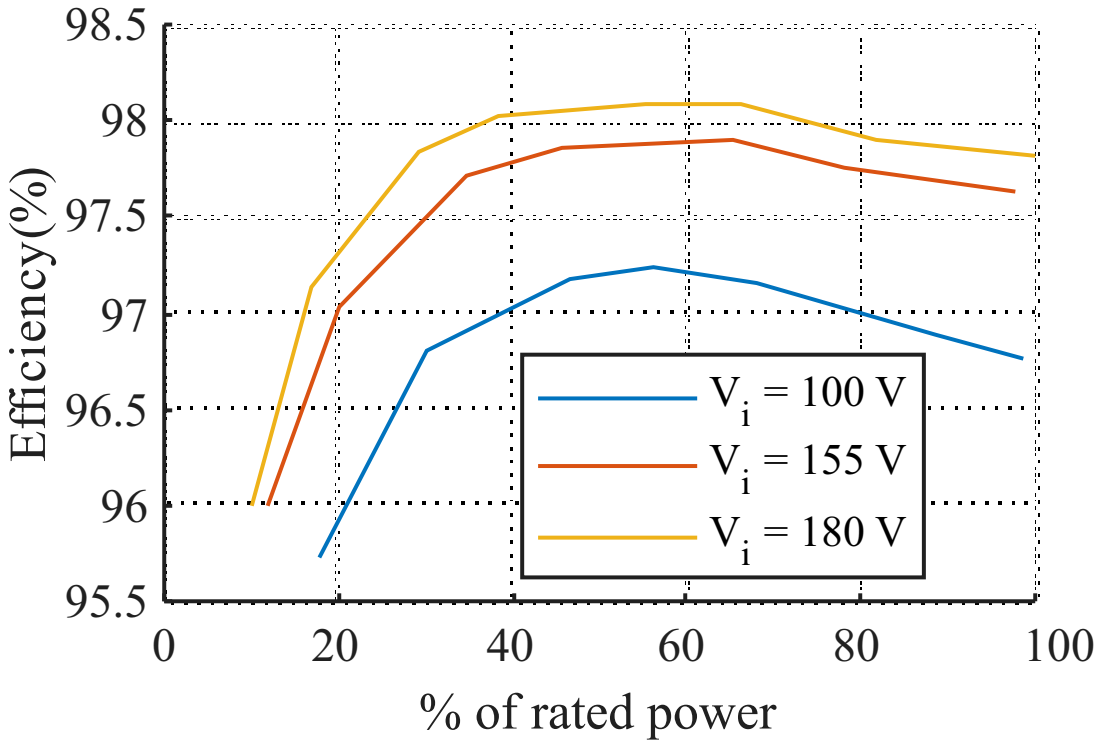


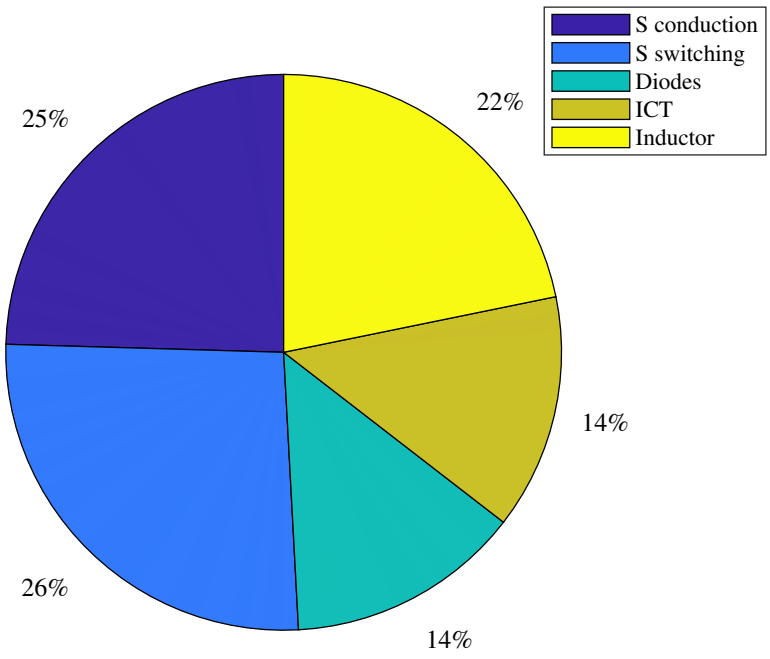
Fig. 86 – Experimental results for the dc-dc converter - Efficiency curves for a 1200 V output voltage.



to the highest current stress. The current in the diodes is the same as the output current divided by the number of legs, therefore the power loss is low, even though most of

the converter devices are diodes. Since only diodes and capacitors are used to expand the converter with more SC cells, the converter can be expanded into more levels without affecting significantly its efficiency. Is the converter is used to convert lower voltage levels, the diode losses might be more significant due to the proportion between the capacitor voltages and the diode forward voltages. In these conditions, the diodes can be replaced by MOSFETs to reduce the conduction losses and improve the converter's efficiency.

Fig. 87 – Loss breakdown for the dc-dc converter.



3.10 SUMMARY

In this chapter the boost converter with MSSC and SC was introduced. The 3SSC was used as the basic converter for the analysis and it is going to serve as a base for the ac-dc topologies introduced in this thesis.

The operation principle, static gain and inductor current ripple were analyzed for each operating region, where it was shown that the static gain of the converter is the same as the boost converter for all the duty cycle range. The current ripple was normalized based on the same gain for every region and presented similar characteristics. The maximum current ripple occurs at the middle of the duty cycle range for every region and is zero at the points region changes. Furthermore, it was shown that the inductor size is reduced because the switching frequency is multiplied by using the MSSC and due to the voltage levels across the inductor in each operational stage, that are lower than in the conventional boost converter.

The voltage and current stress in the devices were analyzed and it was observed that the insertion of an SC cell reduces the voltage stress in a relation of $m_u + m_l + 1$

and the input current is divided by n. The average current stress in every diode is the output current divided by the number of legs and the current in the switches is the sum of current of a winding and the first cell capacitor.

The dynamic analysis of the converter was performed by using the SC cell equivalent circuit, represented by an ideal transformer with a discrete turn ratio referring to the SC cell gain. It was shown that the input current dynamics are not affected by the ICT, as long as the coupling factor of the ICT is $-1/(k-1)$ and the the self inductance of every winding is the same. Due to the SC cell operation principle, the cell dynamics could be represented as an equivalent output capacitor. An equivalent circuit was obtained based on the simplifications that were made and the dynamic response of the system was modelled through space state averaging.

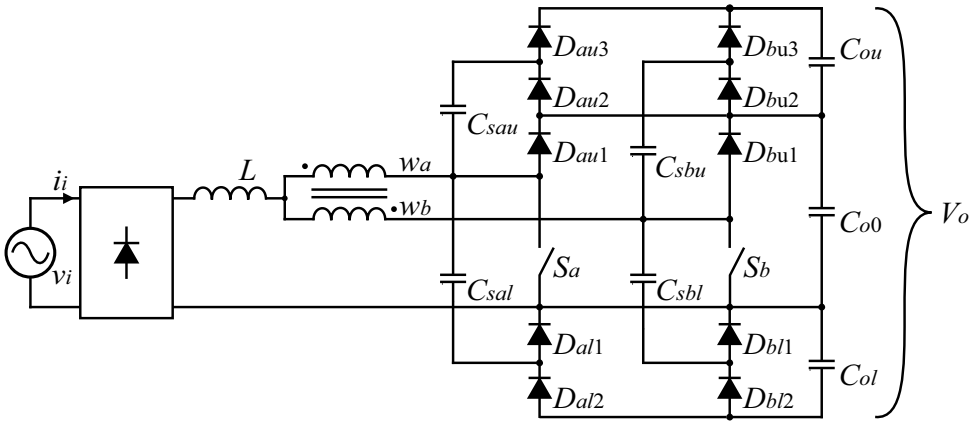
Finally, simulations and experiments were performed to evaluate the theoretical analysis and validate the concept and the waveforms matched the theoretical analysis and simulations. The transfer functions obtained with the simplified circuit matched the actual simulated circuit behavior and were used to design a voltage controller. The controller was able to regulate the voltage during load transients, and the load disturbances did not affect the SC cell voltage balance or the ICT current balance.

4 SINGLE-PHASE HYBRID BOOST RECTIFIER WITH MSSC AND SC CELLS

The boost rectifier is a widespread alternative for PFC due to its input inductor and the possibility of controlling the input current through linear strategies. Because of its similar input dynamic characteristics with the conventional boost converter, the proposed topology is also suitable for PFC applications, and its steady-state characteristics makes the converter suitable for high voltage gain with high input current without increasing its control complexity.

The HBR with MSSC and SC cell is derived from the dc-dc converter simply by inserting a diode rectifier in its input. However, this concept can be expanded into other topologies, such as the bridgeless or multilevel variations that were shown in chapter 1 or new variations exploring other SC cells. Since diode bridge modules commercially widespread, inserting a diode bridge in the input of a current-controlled boost converter can be a practical solution for PFC. The single-phase hybrid boost rectifier is shown in Fig. 88.

Fig. 88 – HBR with 3SSC and SC cells.



By controlling the inductor current in the rectifier in the same phase as the input voltage, it is possible to obtain near unit power factor. The control strategy of the proposed rectifier is the same as to a conventional boost rectifier. The controller is composed of two control loops, one outer voltage loop and an inner current loop. The output voltage controller sets a peak inductor current reference, which is multiplied by the rectified input phase reference, thus setting a current reference for the inner loop. The inner loop controls the inductor current by controlling the duty cycle value, that adjusts the current into a rectified sinusoidal shape. The dynamics of the inner loop are faster than the outer loop in a way that the inner loop is perceived as a gain by the voltage controller. This allows the controllers to be designed individually. The control strategy is described in the block diagram shown in Fig. 89.

Following the same methodology as the dc-dc converter, the output voltage is divided between capacitors and the input current is divided between windings of the ICT. The main difference regarding the selection of components are the output capacitors, which have a low frequency harmonic component that is twice the grid frequency f_g for being a full wave rectifier, similar to the conventional boost rectifier. The main waveforms of the proposed HBR are shown in Fig. 90.

Fig. 89 – Controller diagram for the single-phase rectifier.

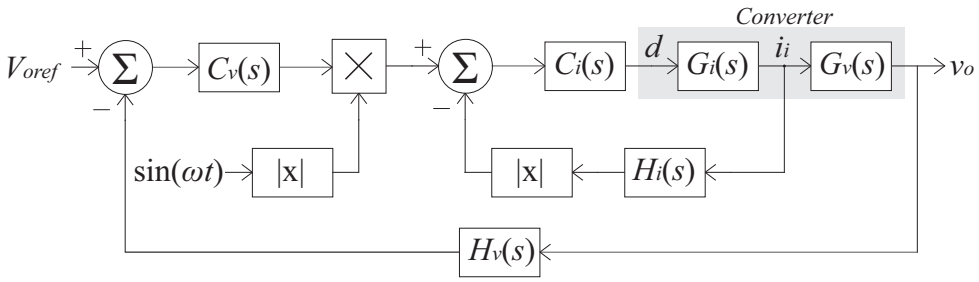
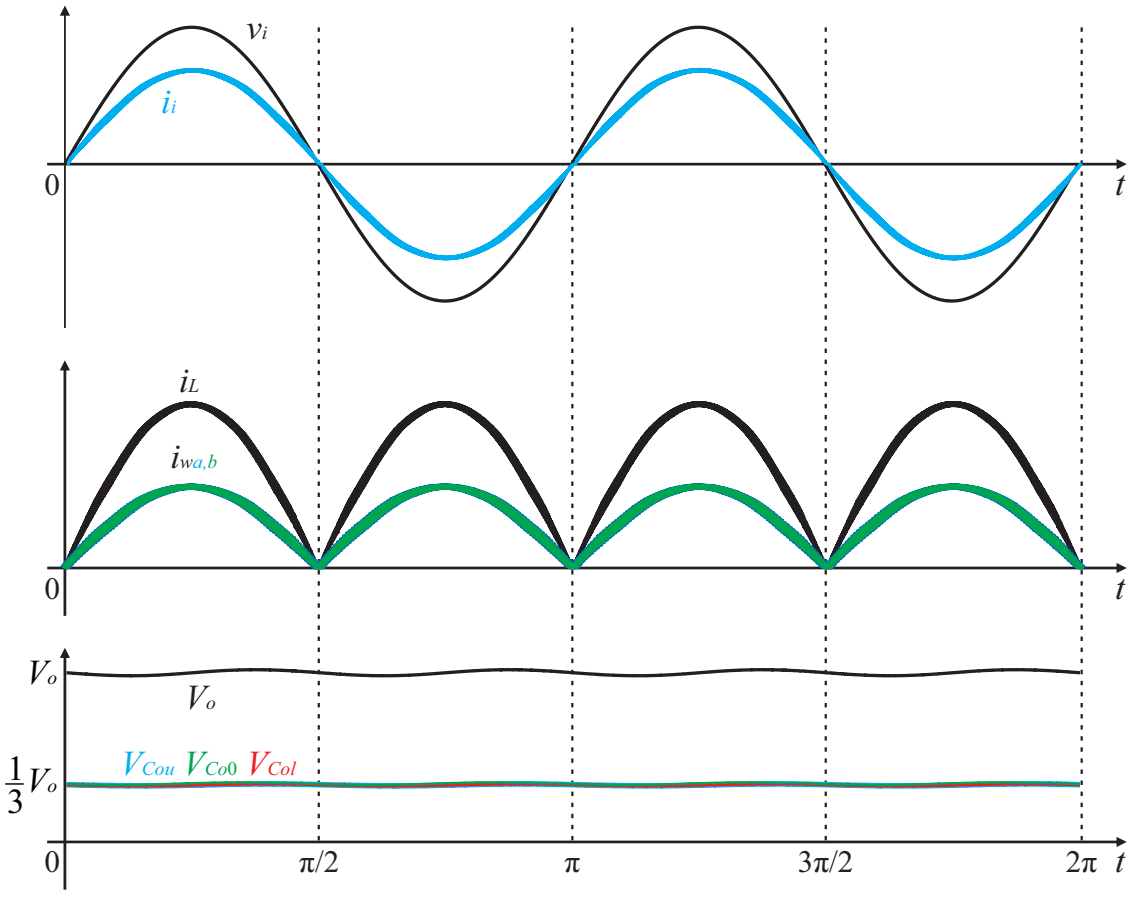


Fig. 90 – Main waveforms of the HBR with 4SSC and SC cells.



4.1 DUTY CYCLE

The static gain during the grid period is analysed in relation to the relative modulation index α, that in a conventional boost converter is described as

$$\alpha = \frac{V_p}{V_o} \tag{4.1}$$

where V_p is the input peak voltage.

The static gain is rewritten in function of α and the grid angle ωt as

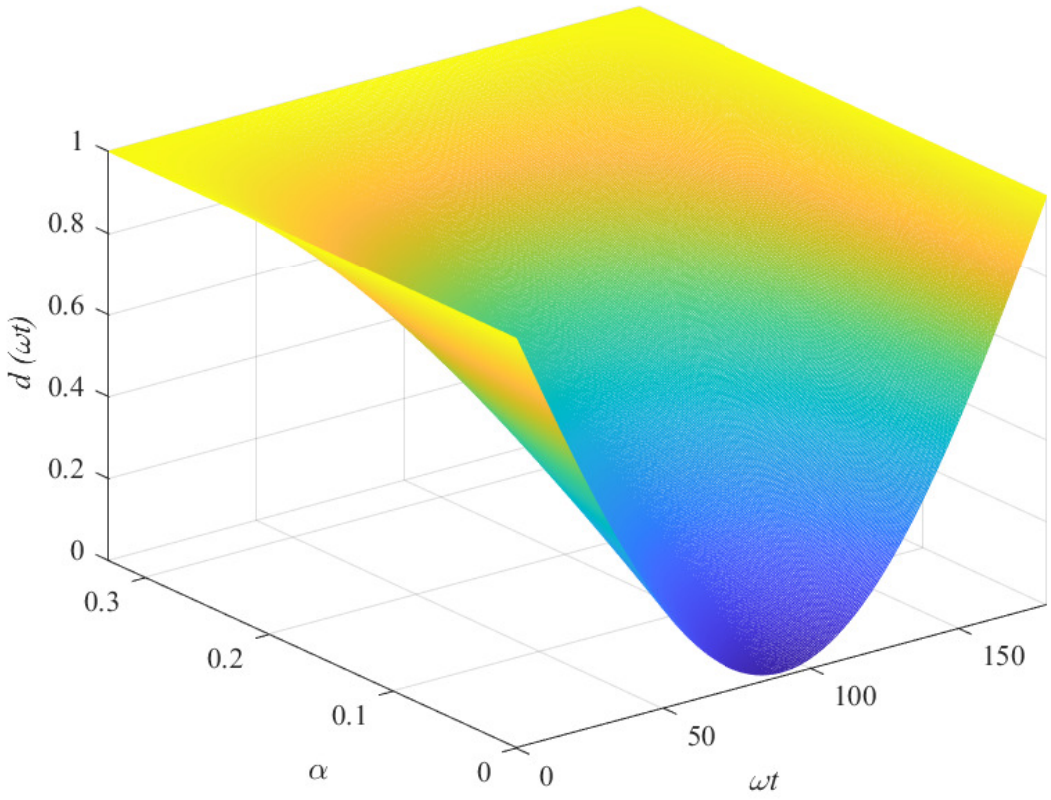
$$\frac{V_o}{|v_i(\omega t)|} = \frac{V_o}{V_p\,|\sin(\omega t)|} = \frac{1}{\alpha\,|\sin(\omega t)|} = \frac{m_u + m_l + 1}{1 - d(\omega t)}. \tag{4.2}$$

The absolute value of the input voltage is considered for this analysis, because of the diode rectifier in the input. By isolating $d(\omega t)$ in (4.1), the duty cycle is calculated in function of α and the grid angle, as described by

$$d(\omega t) = 1 - (m_u + m_l + 1)\alpha\,|\sin(\omega t)|\,. \tag{4.3}$$

The expression is plotted in function of α and ωt for $N = 1$ and is illustrated in Fig. 91, which shows that the duty cycle is 1 when $\omega t = 0$ and for a lower α value (higher voltage gain), there is a lower duty cycle variation in a grid cycle. This may affect the controllability of the converter, because it would require a better resolution of the modulator and make the system sensitive to small duty cycle changes. It is possible to solve this issue by inserting more cascaded SC cells, which shifts the graphic and allows a larger range for d.

Fig. 91 – HBR duty cycle as a function of α and ωt.



4.2 INPUT CURRENT RIPPLE

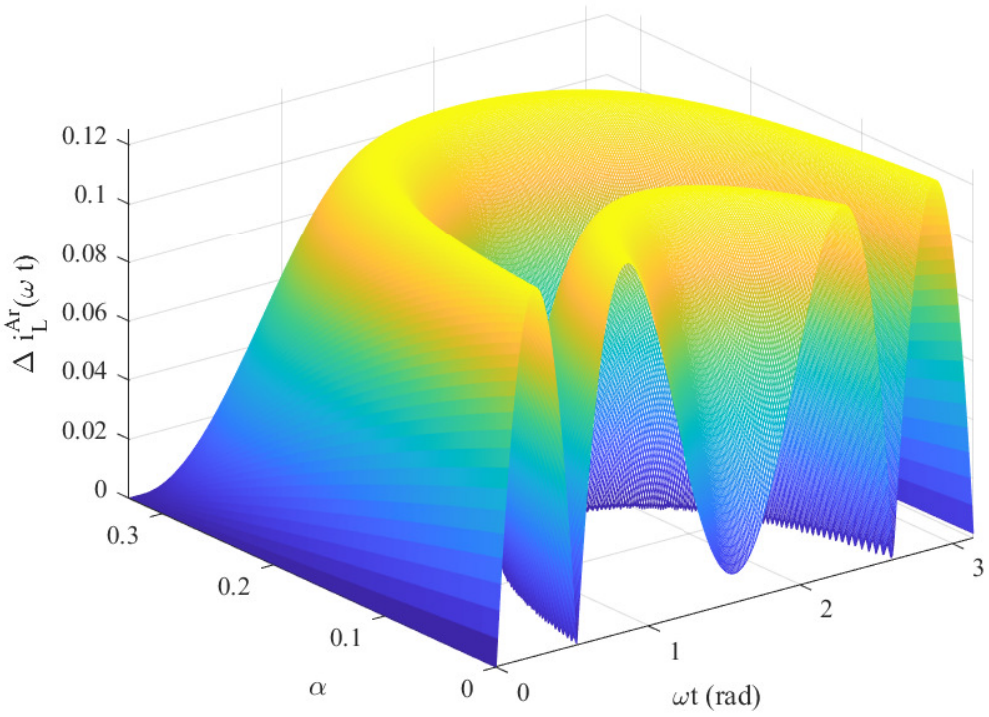
The input current in the HBR changes according to the grid phase, therefore the operation point is also variable. The input inductor is designed according to the operation point with the highest current ripple. The converter current ripple was obtained for the three operating regions in the last chapter and can be written according to the grid angle as

$$\begin{cases} \overline{\Delta i_L^{Ar}(\omega t)} = (1 - 2d(\omega t))\, d(\omega t). \\ \\ \overline{\Delta i_L^{Br}(\omega t)} = -2d(\omega t)^2 + 3d(\omega t) - 1 \end{cases} . \tag{4.4}$$

The normalized current ripple is plotted in function of α and ωt by using the relation between d and α described in (4.3). In the graphic, shown in Fig. 92, the regions that the converter operates are described according to the value of α. In a conventional HBR, the inductor is chosen according to the converter's minimum duty cycle, whether its lowest value is higher than 0.5 [103]. However, in this converter, the current ripple peaks occur in $d = 1/6$, $d = 0.5$ and $d = 5/6$. Whether the converter always operates with a higher duty cycle value, it may operate in a region that the gain is non-linear and a low duty cycle range, thus affecting the converter controllability [86, 98]. Therefore, increasing the number of SC cells could be more adequate to reduce the value of α and obtain the same gain. Thus the inductance value can be obtained by using the equations calculated in

the previous chapter for one of the three duty cycle values where the current ripple is the largest.

Fig. 92 – Normalized input current ripple.



The inductance value for the condition with the largest current ripple is described by

$$\begin{cases} L^{regA} = \frac{V_o\left(1-2\frac{1}{4}\right)\frac{1}{4}}{2\Delta i_L f_s(m_u+m_l+1)}. = \frac{V_o}{16\Delta i_L f_s(m_u+m_l+1)} \\ L^{regB} = \frac{V_o(-2\frac{3}{4}^2+3\frac{3}{4}-1)}{2\Delta i_L f_s(m_u+m_l+1)} = \frac{V_o}{16\Delta i_L f_s(m_u+m_l+1)} \end{cases} . \tag{4.5}$$

By replacing the duty cycle value with its point with largest current ripple in each region, the resulting inductance value is the same for the same current ripple, as shown in (4.5).

4.3 OUTPUT CAPACITORS

In chapter 2 a design strategy was presented for selecting the converter capacitors, considering that there is no low frequency voltage ripple. For a single-phase rectifier is also necessary to consider the low frequency ripple, that is twice the grid frequency. All output capacitors must be designed to reduce the low frequency voltage ripple, whereas the cell capacitors can be designed for a higher frequency ripple for exchanging the charge of the output capacitors through the SC cell.

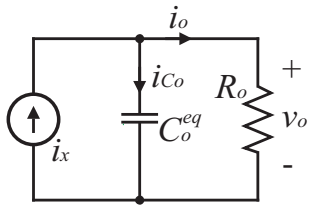
The alternative used in this thesis for selecting the output capacitors is defining a maximum output voltage ripple. For calculating the capacitance, the total output capacitance is represented by an equivalent capacitor whose value is the series association

of all output capacitors, given by

$$C_o^{eq} = \frac{C_{o0}}{m_u + m_l + 1}. \tag{4.6}$$

Different from the DC-DC converter, the cell capacitors can be neglected, since they are designed for high-frequency, thus their value do not influence much the total equivalent capacitance value. For this analysis, the equivalent circuit shown in Fig. 93 is used. In this figure, i_x represents the current delivered from the converter to the output. Only the low-frequency component is considered in this analysis.

Fig. 93 – Equivalent circuit of the converter output.



Since the topology is a full-wave rectifier, the output low-frequency component is twice the grid frequency f_g, therefore the reactive capacitance is given by

$$X_{Co^{eq}} = \frac{1}{4\pi f_g C_o^{eq}}. \tag{4.7}$$

The capacitive reactance can also be described by

$$X_{Co^{eq}} = \frac{\Delta V_o}{I_{Copp}} \tag{4.8}$$

where I_{Copp} is the equivalent output capacitor peak-to-peak current and ΔV_o is the output voltage ripple. By replacing (4.8) in (4.7), the equivalent capacitance is obtained as described by

$$C_o^{eq} = \frac{I_{Copp}}{4\pi f_g \Delta V_o}. \tag{4.9}$$

I_{Copp} is obtained by considering that the input and output power of the converter are the same, as described by

$$V_p I_p \sin(\omega t)^2 = V_o i_x(\omega t). \tag{4.10}$$

i_x is isolated in function of the output power, as described by

$$i_x(\omega t) = \frac{2P_o \sin(\omega t)^2}{V_o} = \underbrace{\frac{P_o}{V_o}}_{i_o} - \underbrace{\frac{P_o \cos(2\omega t)}{V_o}}_{i_{Co}}. \tag{4.11}$$

The peak current ripple occurs when $\omega t = \pi/2$, thus the peak-to-peak capacitor current is given by

$$I_{Copp} = 2\frac{P_o \cos(2(\pi/2))}{V_o} = \frac{2P_o}{V_o}. \tag{4.12}$$

(4.12) and (4.6) are replaced in (4.9) to obtain the minimum output capacitance

value, given by

$$C_{o0,n,p} \geq \frac{P_o}{2\pi f_g V_o \Delta V_o}. \tag{4.13}$$

4.4 OUTPUT VOLTAGE DYNAMIC ANALYSIS

The input current transfer function for the single-phase rectifier is the same as the DC-DC converter transfer function. For obtaining the output voltage transfer function some idealizations are considered: The output dynamics is much slower than the input dynamics, the input power factor is unitary, the grid frequency ripple is neglected and the converter losses are neglected as well. Furthermore, the output capacitors are considered as a single equivalent capacitor, whose value is given by the relation (4.6). By considering that, the output power is given by

$$P_o = i_o v_o = \frac{V_p I_p}{2\pi} \int_0^{2\pi} \sin^2(\omega t) d\omega t = \frac{V_p I_p}{2}. \tag{4.14}$$

where i_p is the input current peak value. Since this analysis is performed for slow dynamics, the sliding average values are considered in the grid period.

The output current i_o is isolated in the equation, resulting in

$$\langle i_o \rangle_{T_g} = \frac{V_p \langle i_p \rangle_{T_g}}{2\langle v_o \rangle_{T_g}} \tag{4.15}$$

where T_g is the grid period.

Knowing that the output current in a transient is composed by one component that flows through the capacitors and another that flows through the output resistor, the equation is rewritten as

$$C_o^{eq} \frac{d\langle v_o \rangle_{T_g}}{dt} + \frac{\langle v_o \rangle_{T_g}}{R_o} = \frac{V_p \langle i_p \rangle_{T_g}}{2\langle v_o \rangle_{T_g}}. \tag{4.16}$$

The sliding average values are decomposed into small and large signals, resulting in

$$2C_o^{eq} V_o \frac{d\widetilde{v_o}}{dt} + 2C_o^{eq} \widetilde{v_o} \frac{d\widetilde{v_o}}{dt} + 2\frac{\widetilde{v_o}^2_{T_g}}{R_o} + 4\frac{V_o \widetilde{v_o}_{T_g}}{R_o} + 2\frac{V^2_{oT_g}}{R_o} = V_p I_p + V_p \widetilde{i_p}. \tag{4.17}$$

To find the output transfer function, the Laplace transform is applied and the large signal components are removed, since they do not contribute to the transient response. The second order small signal elements are also neglected, resulting in

$$2C_o^{eq} V_o \widetilde{v_o} s + 4\frac{V_o \widetilde{v_o}}{R_o} = V_p \widetilde{i_p}. \tag{4.18}$$

By isolating the output voltage a input current peak, the transfer function is obtained, described by

$$\frac{\widetilde{v_o}}{\widetilde{i_p}} = \frac{V_p R_o}{2C_o^{eq} V_o R_o s + 4V_o}. \tag{4.19}$$

4.5 VOLTAGE STRESS AND CURRENT STRESS

The voltage stress across the switches and capacitors is the same as the dc-dc converter given by $V_o/(m_u + m_l + 1)$, since the output stage is rectified and the output capacitors are designed to attenuate the low frequency current ripple.

The current stress across the switches is affected by the input phase, since the input current is sinusoidal and the duty cycle is variable during the grid period. The diode average current is one fraction of the average output current, since the capacitors do not affect the output average current value. The RMS switch current, however, is affected by the grid angle and can be calculated by obtaining the RMS value within the switching frequency and expanding it to the grid frequency.

Knowing the moving average switch current during its ON period, calculated in chapter 3, the RMS current during the grid period is given by

$$I_{Si}^{RMS1ph} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{1}{T_s}\int_0^{d(\omega t)T_s}\left(\frac{i_L(\omega t)}{n}+2\frac{I_o}{nd(\omega t)}\right)^2 dt d\omega t}. \tag{4.20}$$

Solving the first integral results in

$$\begin{array}{l} I_{Si}^{RMS1ph} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{d(wt)}{n^2}\left(i_L^2(\omega t)+4\frac{I_o i_L(\omega t)}{d(\omega t)}+4\frac{I_o^2}{d(\omega t)^2}\right)d\omega t} \\ = \sqrt{\frac{1}{\pi n^2}\int_0^{\pi} d(wt) i_L^2(\omega t)+4I_o i_L(\omega t)+4\frac{I_o^2}{d(\omega t)}d\omega t} \end{array}. \tag{4.21}$$

To solve the second integral, the inductor current and duty cycle must be written as functions of wt, described by

$$I_{Si}^{RMS1ph} = \sqrt{\frac{1}{\pi n^2}\int_0^{\pi}\begin{array}{l} I_p^2\left[1-(m_u+m_l+1)\alpha\sin(\omega t)\right]\sin^2(\omega t) \\ +4I_o I_p\left|\sin(\omega t)\right|+4\frac{I_o^2}{1-(m_u+m_l+1)\alpha\left|\sin(\omega t)\right|} \end{array} d\omega t}. \tag{4.22}$$

The equation is simplified as

$$I_{Si}^{RMS1ph} = \sqrt{\frac{1}{\pi n^2}\left[\begin{array}{l} \frac{I_p(3\pi I_p-16(m_u+m_l+1)\alpha I_p-8\alpha I_p+48I_o)}{6} \\ +\int_0^{\pi}4\frac{I_o^2}{1-(m_u+m_l+1)\alpha\sin(\omega t)}d\omega t \end{array}\right]}. \tag{4.23}$$

The last integral results in a very complex analytical solution, therefore it should be solved using numerical methods.

By using the same method, the RMS value of the diode currents are given by

$$\left\{\begin{array}{l} i_{Diodd}^{RMS1ph} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{1}{T_s}\int_{d(\omega t)}^{T_s}\left(\frac{i_L(\omega t)}{n(m_u+m_l+1)}\right)^2 dt d\omega t} = \sqrt{\frac{1}{\pi n^2}\int_0^{\pi}\frac{i_L^2(\omega t)\sqrt{1-d(\omega t)}}{(m_u+m_l+1)^2}d\omega t} \\ = \sqrt{\frac{I_p^2}{\pi n^2(m_u+m_l+1)^2}\int_0^{\pi}\sin(\omega t)^2\sqrt{\alpha\left(m_u+m_l+1\right)\sin(\omega t)}d\omega t} \\ \\ I_{Dieven}^{RMS1ph} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{1}{T_s}\int_0^{DT_s}\left(\frac{I_o}{kd(\omega t)}\right)^2 dt d\omega t} = \sqrt{I_o^2\frac{1}{\pi n^2}\int_0^{\pi}\frac{\sqrt{d(\omega t)}}{d(\omega t)^2}d\omega t} \\ = \sqrt{\frac{I_o^2}{\pi n^2}\int_0^{\pi}\frac{\sqrt{1-(m_u+m_l+1)\alpha\sin(\omega t)}}{\left[1-(m_u+m_l+1)\alpha\sin(\omega t)\right]^2}d\omega t} \end{array}\right. \tag{4.24}$$

Table 4 – Specifications of the proposed single-phase rectifier.

Specification	**Value**
Input voltage V_i (RMS value)	127 V
Output voltage	1200 V
Output power	1300 W
Grid frequency	60 Hz
Switching frequency	100 kHz
Switched capacitors C_s	5.6 μF
Output capacitors C_o	940 μF
Input inductor L_i	250 μH
Switch resistances (Rohm SCT2080AL) R_s	80 mΩ
Diode resistances (Cree C3D04065A) R_d	100 mΩ
Diode forward voltage V_d	0.9 V

4.6 SIMULATION RESULTS

The proposed converter was simulated to assess the analysis that were made in this chapter. Some parameters used in the simulations are the same as in the single-phase circuit, since the switching cell containing the SC cells will be composed by a module that will be used for all converters for obtaining the experimental results for the final document. The simulated converter specifications are presented in Table 4.

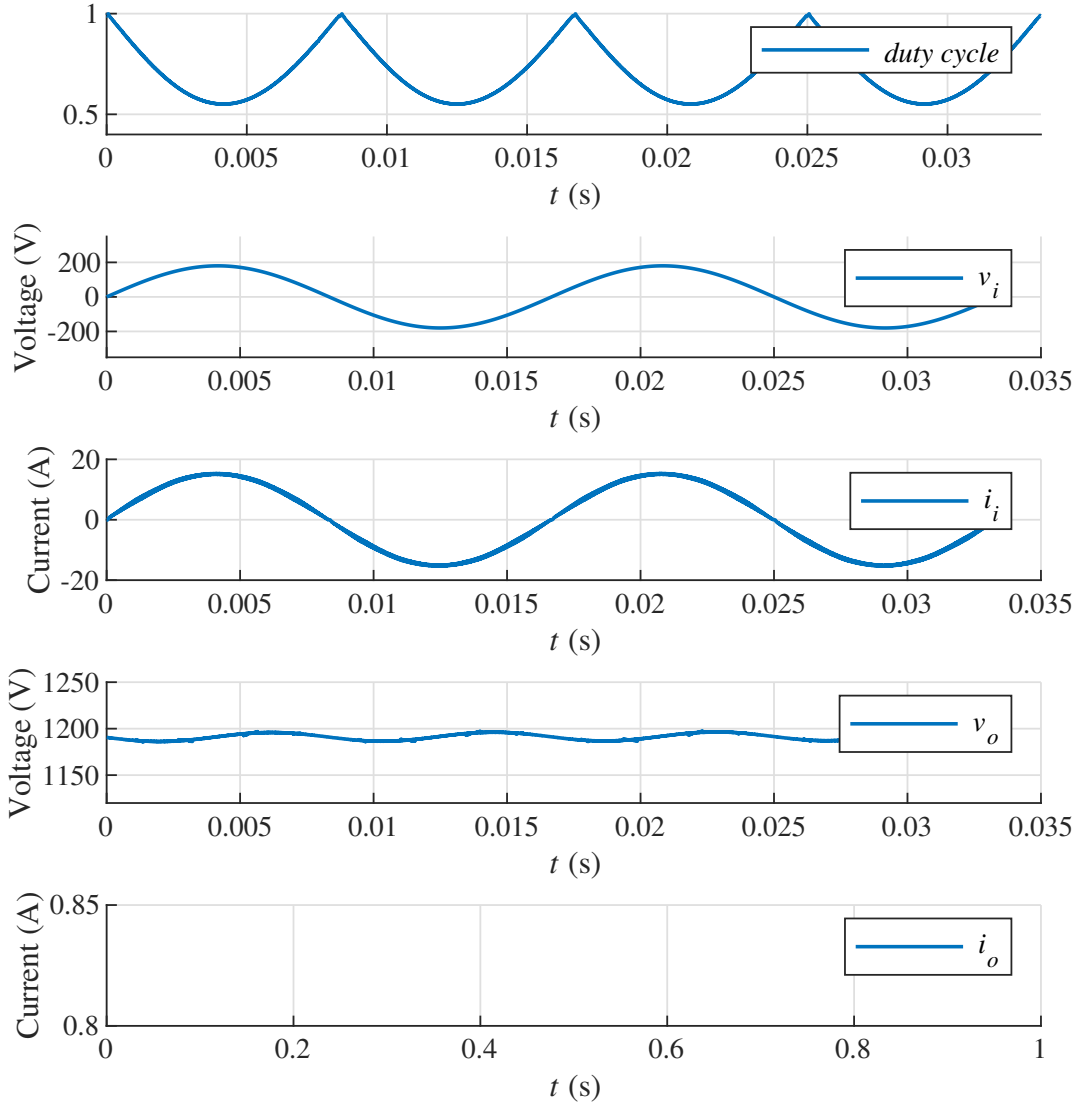
The converter was simulated in the rated power operation point, as shown in Fig. 94. In the dc-dc simulations, the converter was presented first with an open loop operation. In the ac-dc converters this is not possible, since the duty cycle must vary according to the input voltage. In the simulations it can be seen that the converter is able to obtain the desired voltage gain with a modulation index that is higher than the conventional boost converter. The input power factor of the converter is above 0.99 and the THD is 0.04, which shows that the rectifier is suitable for power factor correction.

The current shapes for the input, the inductor and ICT are shown in Fig. 95. The inductor and ICT RMS currents are, respectively, 10 A and 5 A, approximately. Since the experimental prototype uses the same circuit as in the dc-dc converter, the current ripple at its peak is 0.31 A. considering that the peak input voltage is almost half the output capacitor voltage, the duty cycle at $\pi/2$ is near 0.5, which results a low ripple according to the ripple analysis previously done in this chapter.

In the same way as in the dc-dc converter, the voltage across the capacitors is a fraction of the total output voltage and is naturally self balanced. Fig. 96 shows that the capacitors present a low frequency ripple and the total output voltage has a total voltage ripple of 8.7 V, that is approximately lower than 1% of the total voltage value. A 940 μF capacitor was used due to the available commercial capacitance values for this application and due to the current that they can handle, which is a limitation of electrolytic capacitors. The cell capacitors present a high-frequency ripple that varies in time. Since the converter duty cycle is variable and there are some moments it approaches a unit value, the energy transfer between the capacitors is affected. Therefore, it is important that all output capacitors are large enough, so that most energy is transferred when the duty cycle is near 0.5 and that the capacitors are capable to limit the low frequency ripple.

One of the main advantages of topologies with ladder SC cells is the voltage stress

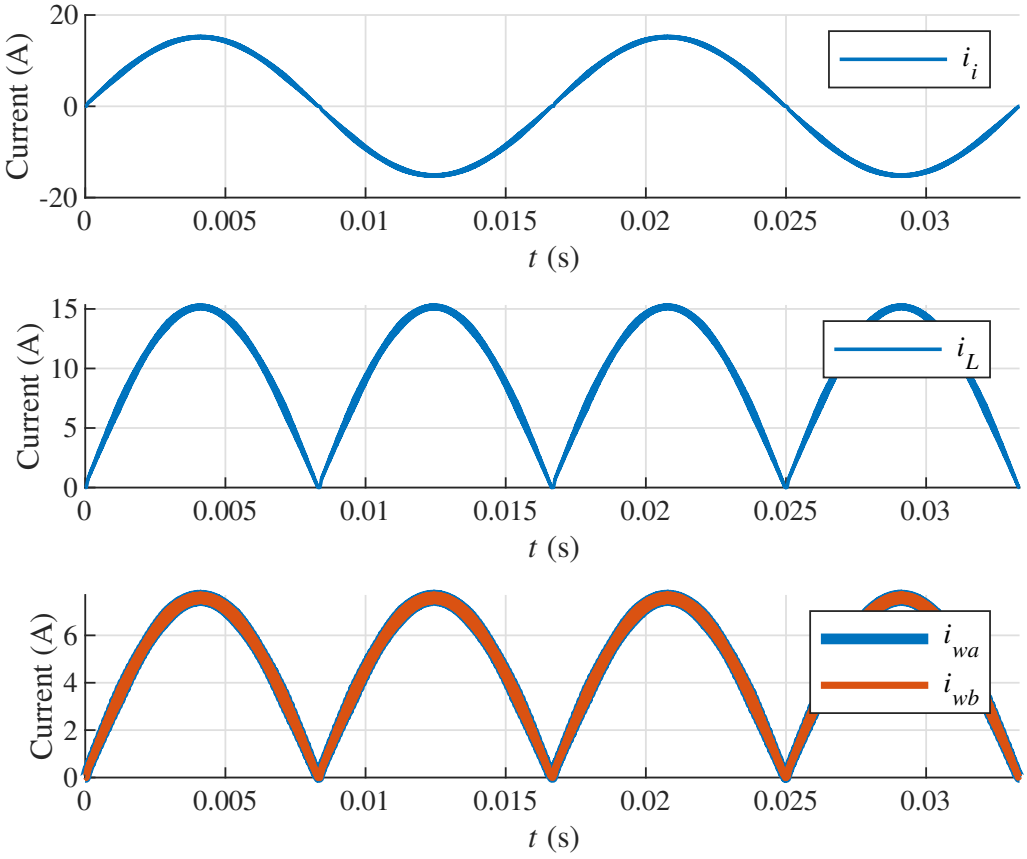
Fig. 94 – Simulation results of the single-phase ac-dc topology - Rated power.



across the switches, that is a fraction of the output voltage, since in each operational stage the device that is OFF is connected in parallel to a capacitor. The voltage stress across the semiconductor devices is shown in Fig. 97. The devices switch in all half cycles, therefore the wave shape in a larger period does not show any relevant new aspect of the voltage across the switches. Besides the low frequency voltage ripple, which can be neglected and would not be visible in the presented vertical scale.

The current stress across the switches and diodes depends on the inductor current and has a low frequency component of twice the grid frequency. The average current in the diodes is around 0.54 A, that is about half the total output current. The RMS current in the switches is around 5.87 A, whereas the calculated current is around 5.7 A. The deviation occurs due to the high equivalent resistance during the zero crossing, which causes the capacitor current ripple to increase. Therefore, the theoretical calculations must serve

Fig. 95 – Simulation results of the single-phase ac-dc topology - Current in the inductor and MIA.



as a basis for obtaining the switch current to help designing the converter, but simulations should be performed to obtain a more precise value, since the equations become too complex if the capacitor high-frequency current ripple is considered. The capacitor current ripple depends on many parasitic values, which can make the analytical models impractical in systems with many cascaded SC cells. This can be seen clearer in Fig. 98, that shows the non-linear high-frequency behavior of the current in the semiconductor devices.

The current non-linear aspect is observed in Fig. 100, that shows the cell capacitor currents during the grid period and switching period. The capacitor current presents a partial charge near to complete charge behaviour at the points with maximum current, which means there is a balance between losses and capacitor size.

A load step of 50% to 100% and vice-versa was applied to the converter to assess its dynamic response, stability and possible imbalances across the capacitor voltage. The current controller was designed for a cutoff frequency of 40k rad/s and a 60° phase margin and the voltage controller was designed for a 1 rad/s cutoff frequency and a 60° phase margin. The output voltage response must be slow, so that it does not insert harmonics to the input current reference. As can be seen in Fig 101, the transient response is slow, but it does not cause high voltage peaks and there is no voltage imbalance across the capacitors.

Fig. 96 – Simulation results of the single-phase ac-dc topology - Voltage across the capacitors of leg a and output capacitors.

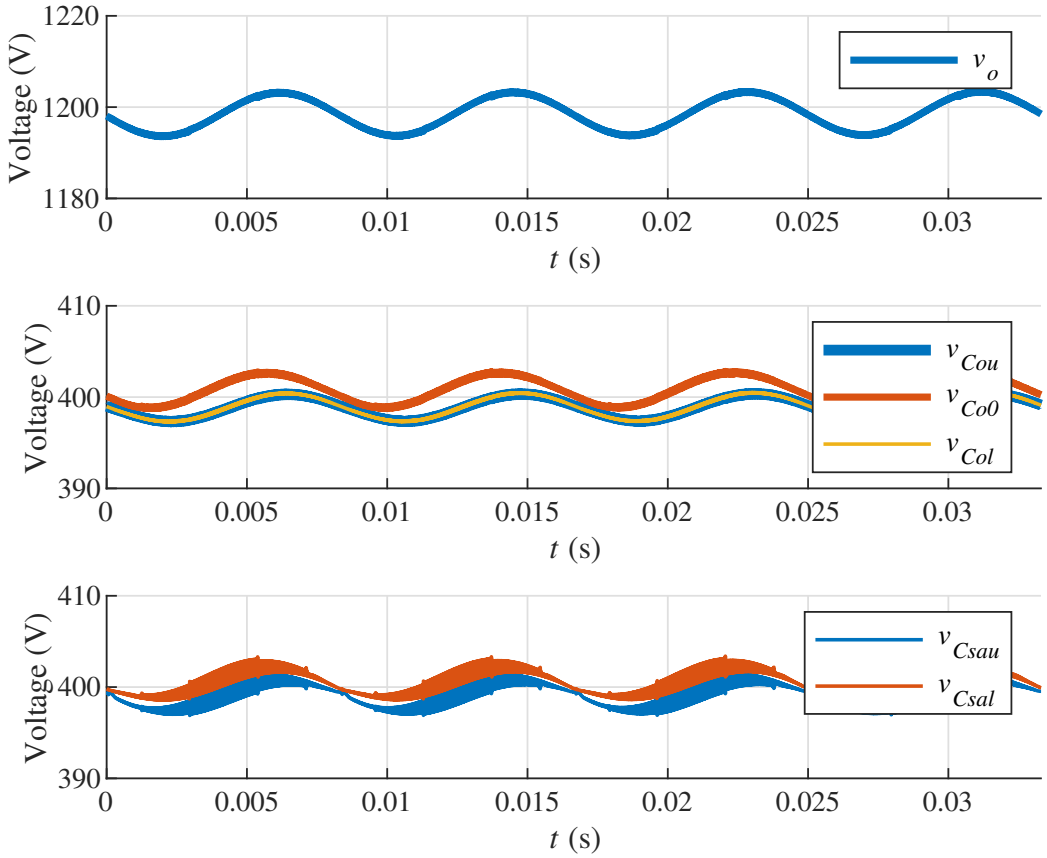


Fig. 97 – Simulation results of the single-phase ac-dc topology - Voltage stress across the switch and diodes of leg a.

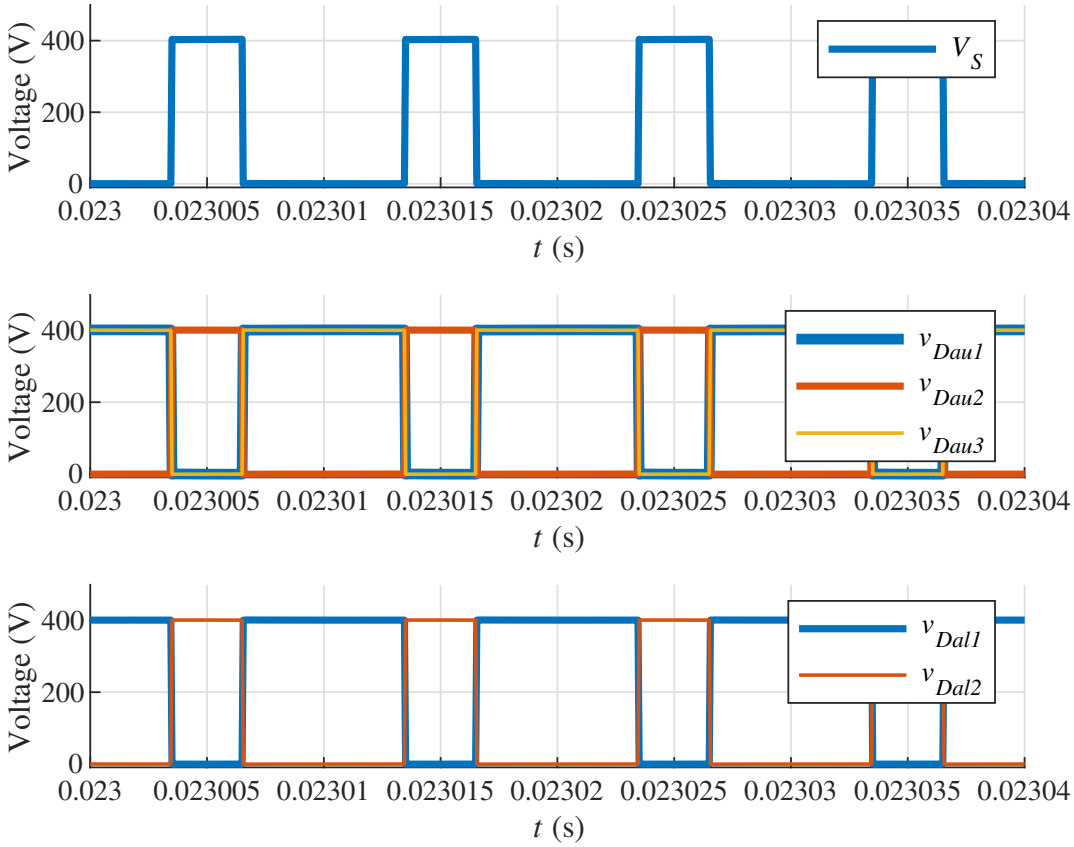


Fig. 98 – Simulation results of the single-phase AC-DC topology - Current stress in the switch and diodes of leg a during the grid period.

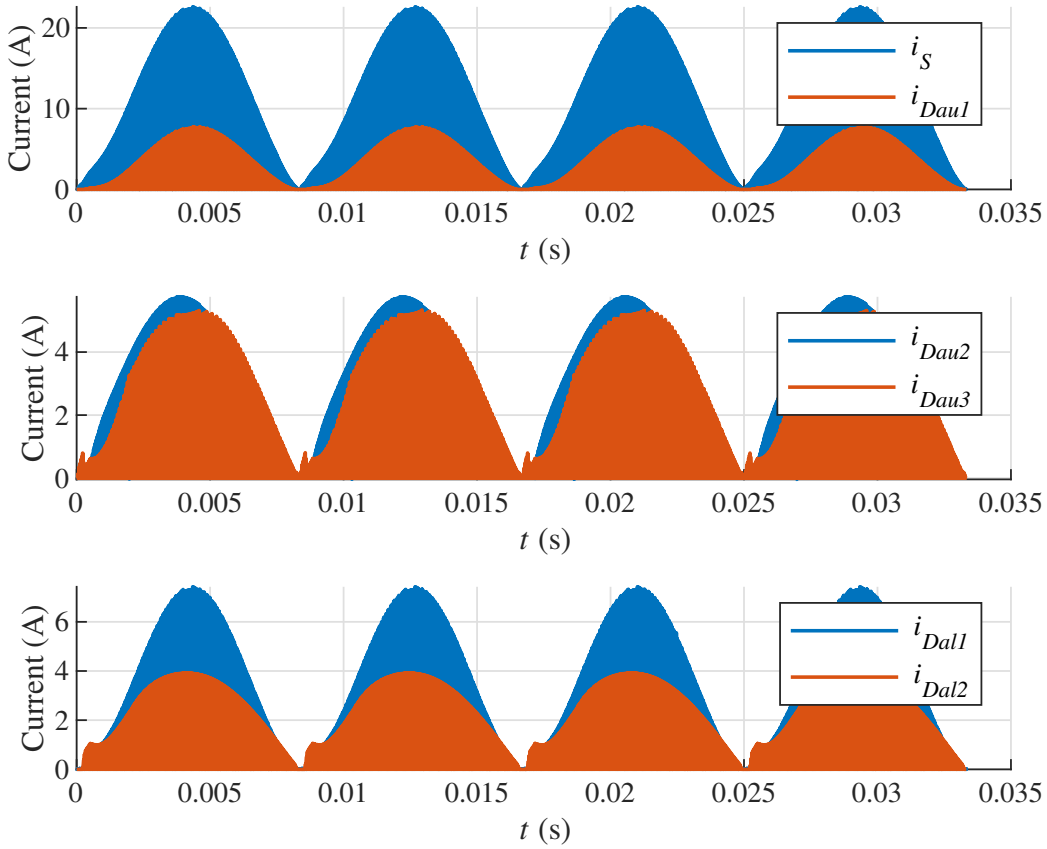


Fig. 99 – Simulation results of the single-phase AC-DC topology - Current stress in the switch and diodes of leg a during the switching period.

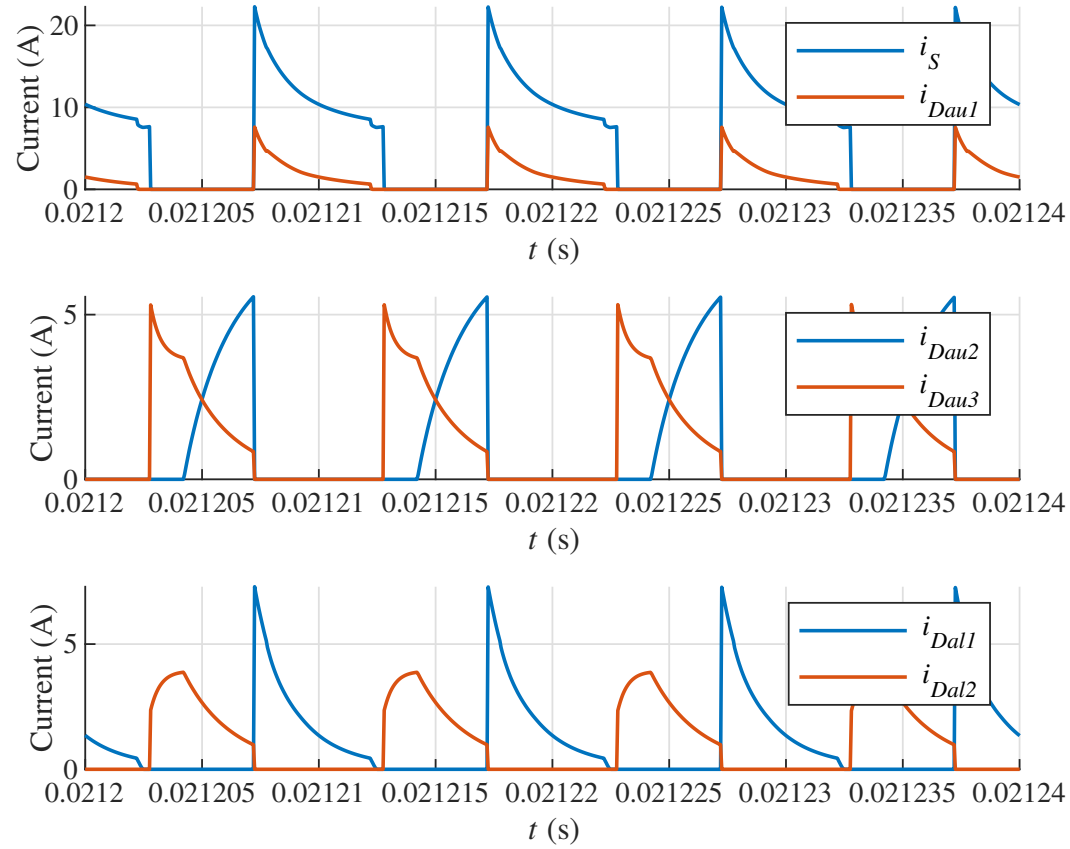


Fig. 100 – Simulation results of the single-phase AC-DC topology - Current in the cell capacitors of leg a.

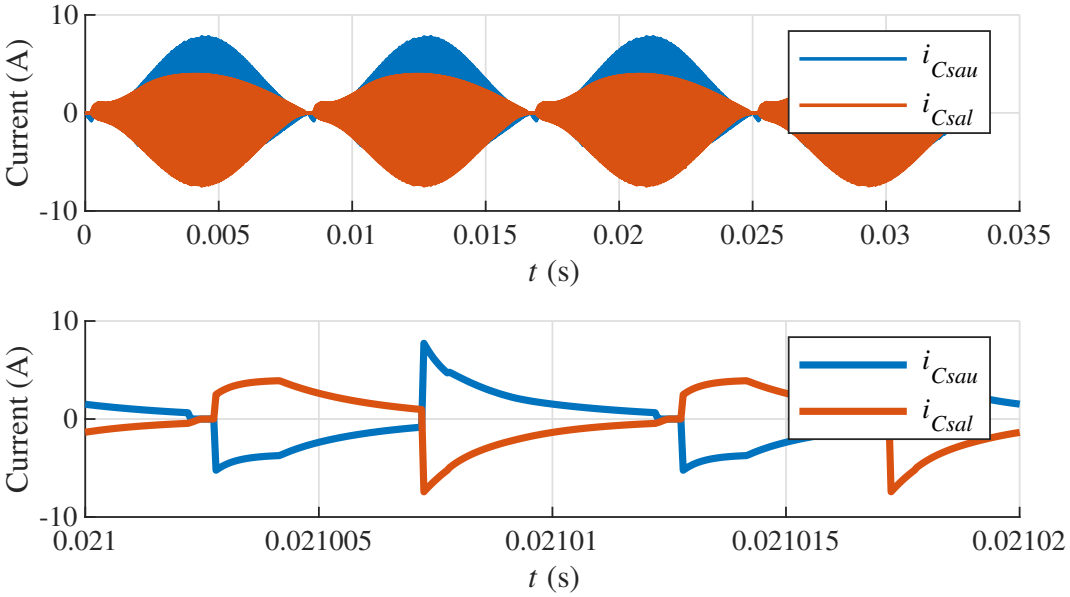
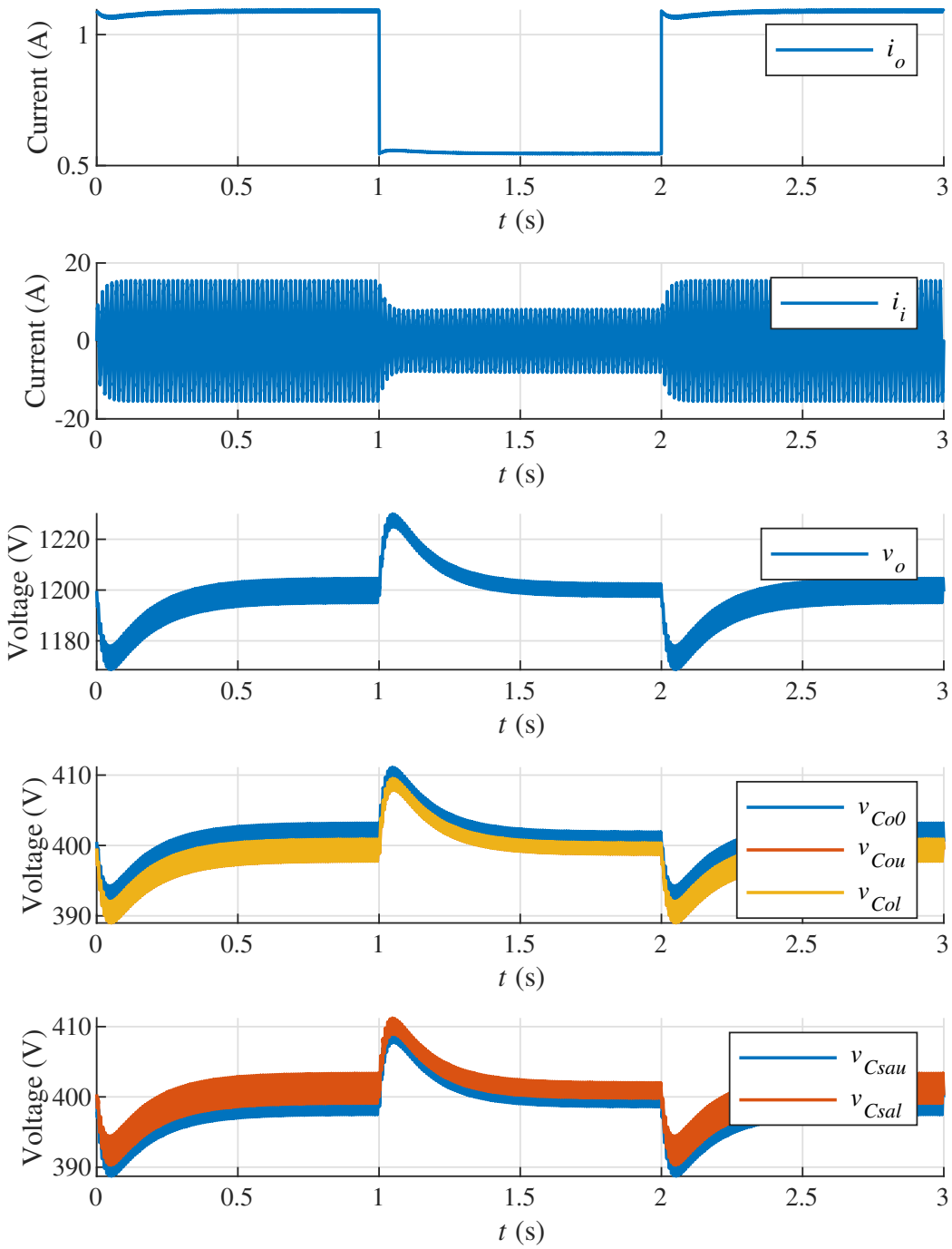


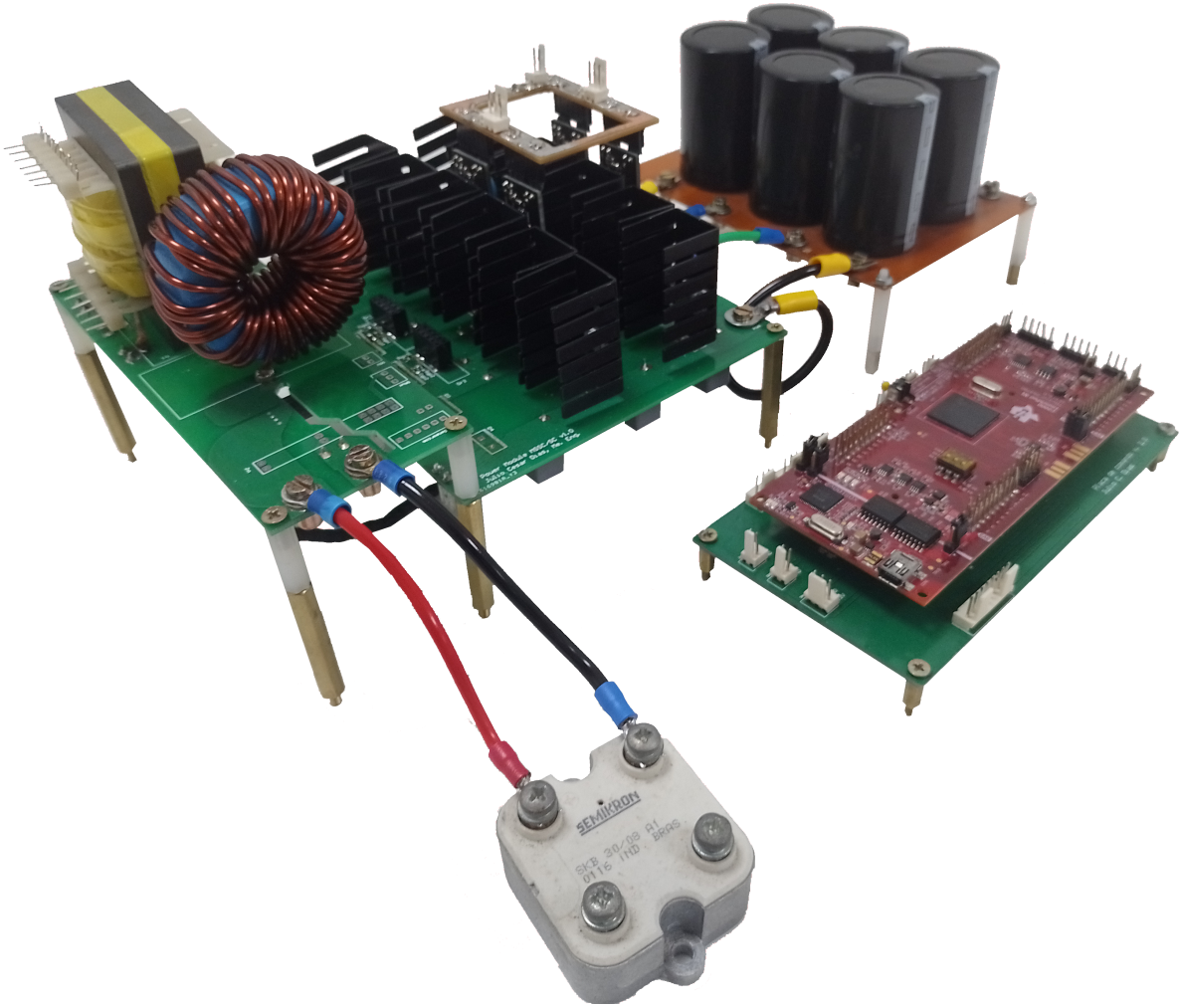
Fig. 101 – Simulation results of the single-phase AC-DC topology - Load step response.



4.7 EXPERIMENTAL RESULTS

To evaluate the ac-dc single-phase converter operation, the dc-dc module was adapted by inserting a rectifier module in its input and electrolytic capacitors in its output. The input rectifier is composed by a SKB 30/08 Semikron module with slow dynamics and each output capacitor is composed by two parallel connected $470\mu F$ capacitors from the EPCOS B43544 series. The photograph of the prototype is shown in Fig. 102, its power density is 386 W/L.

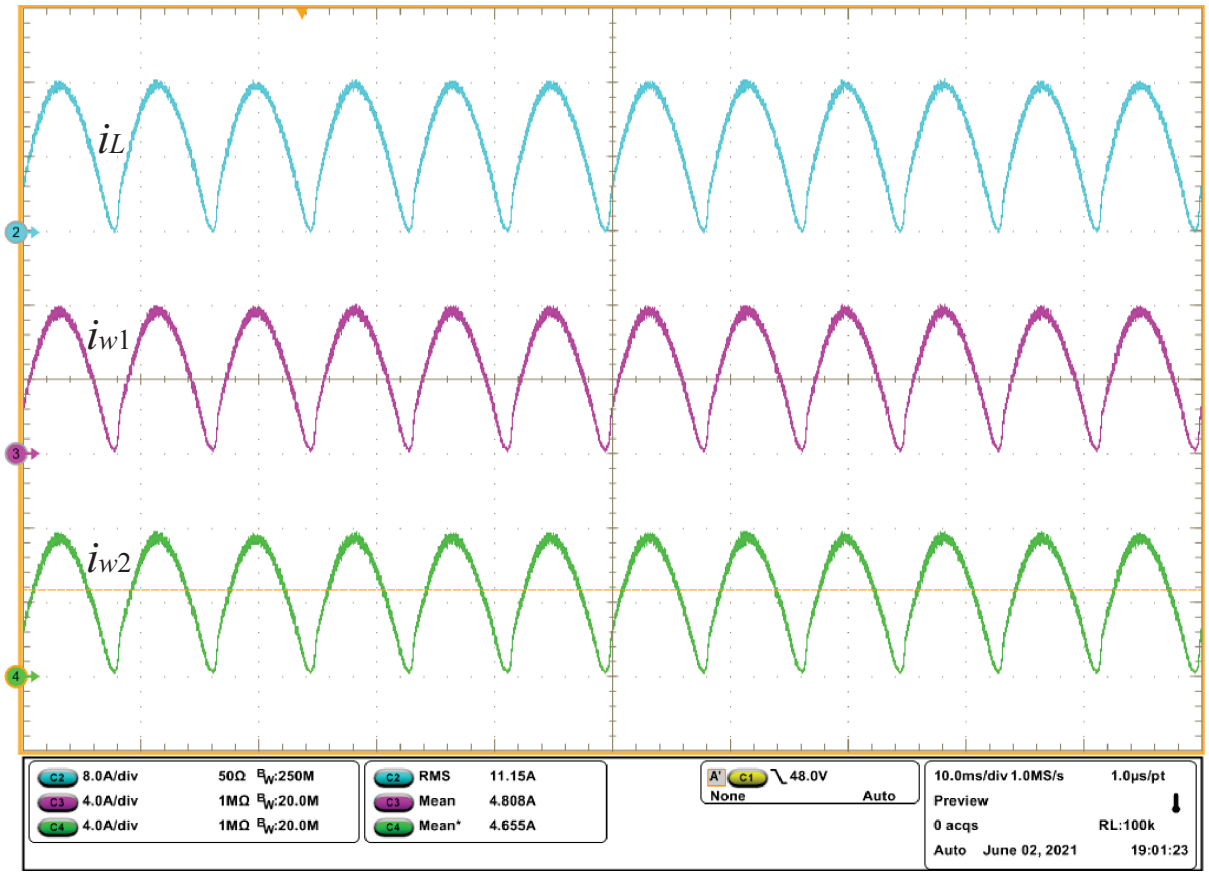
Fig. 102 – Single-phase HBR experimental prototype.



The converter was first tested at rated power and was capable of increasing the voltage from 127 V to 1200 V, as seen in Fig. 103. One advantage of using this topology is the wider duty cycle range than the conventional boost converter, which can improve the modulator resolution and make the SC cell operate with a value that improves its equivalent resistance at the point the converter processes most power. It can also be seen that the input current follows a sinusoidal shape, which provides a high input power factor (0.993) and low THD (5.1).

The input diodes used for this prototype are conventional slow diodes, which are available in a wide power range. However, the fast semiconductor devices present more drawbacks as high voltage devices are needed, since their conduction losses increase and

Fig. 103 – Single-phase ac-dc converter: Rated power operation.



their dynamics are slower. Therefore, for a proper design it is important that the current is shared between the devices, this is achieved when the inductor current is shared between the windings in the ICT. In this prototype the current balance was achieved by using similar gate drivers, without active techniques that require current sensing in all windings. The current in the input inductor and ICT windings is shown in Fig. 104.

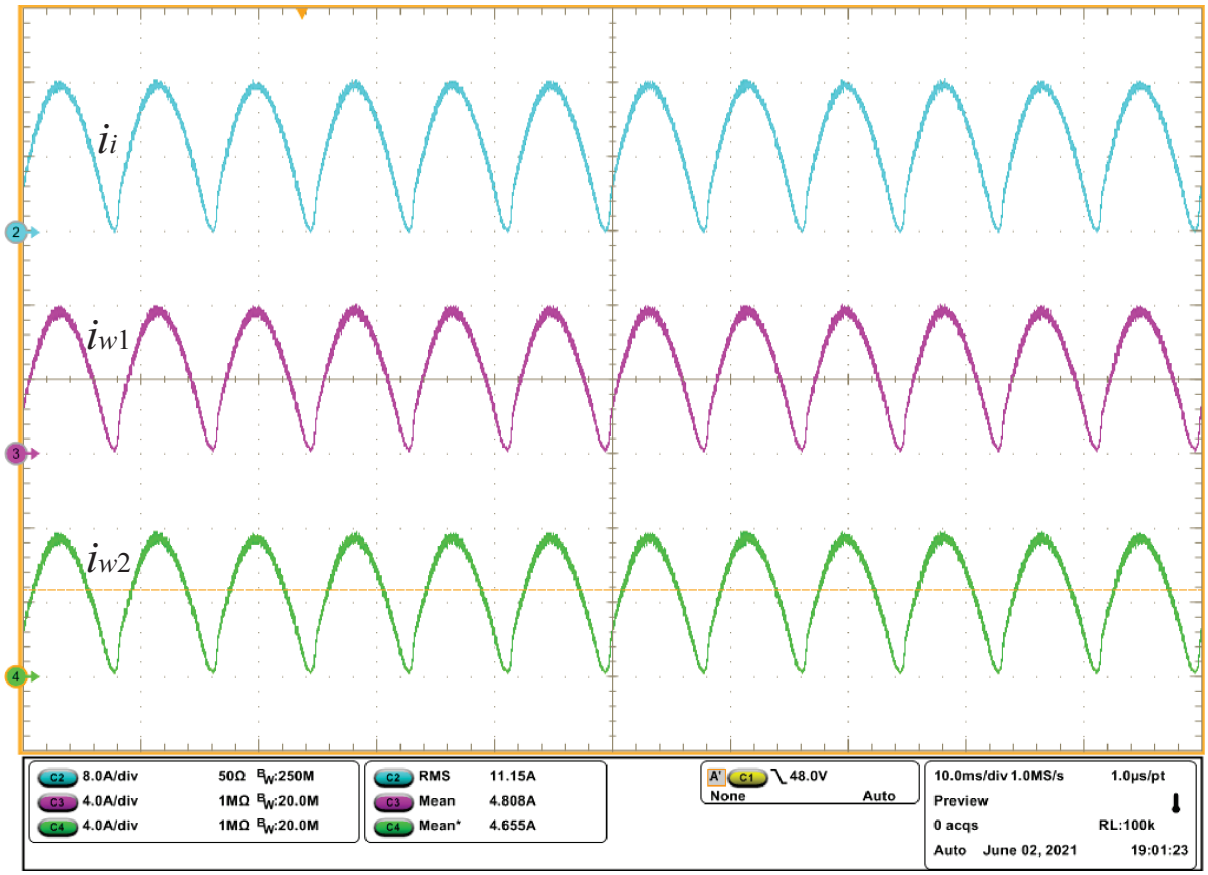
One of the main aspects of the proposed converter is the input current share in the switches, which is achieved by the MSSC. The converter can also divide the voltage between the capacitors, which results in a reduced voltage across the switches. The voltage peak on the switches and diodes is around 400 V with a 1200 V output voltage, as can be seen in Fig. 105.

The current in the capacitors in high frequency follows the same shape as in the dc-dc converter. In low frequency its amplitude is proportional to the grid current, as seen in Fig. 106.

To evaluate the controller, a load step was applied from 100% to 50% and then to back to full load, as shown in Fig. 107. There were practical issues with the mechanical switches that were used to apply the load step, since the converter has a high output voltage, therefore the step was not so abrupt due to the switch limitations. However, it can be seen that the rectifier is able to follow the output current reference and control it when there is a load change. The maximum voltage value at the overshoot was 1.25 kV, which is a very safe value for the capacitors and semiconductor devices to operate.

It is important to asses the efficiency of a power converter to verify its applicability. An efficiency curve, shown in Fig. 108, was traced and shown a maximum efficiency of 95.6%. The efficiency at rated power was about 95.4%, while the calculated value was

Fig. 104 – Single-phase ac-dc converter: Inductor current and current sharing in the ICT.

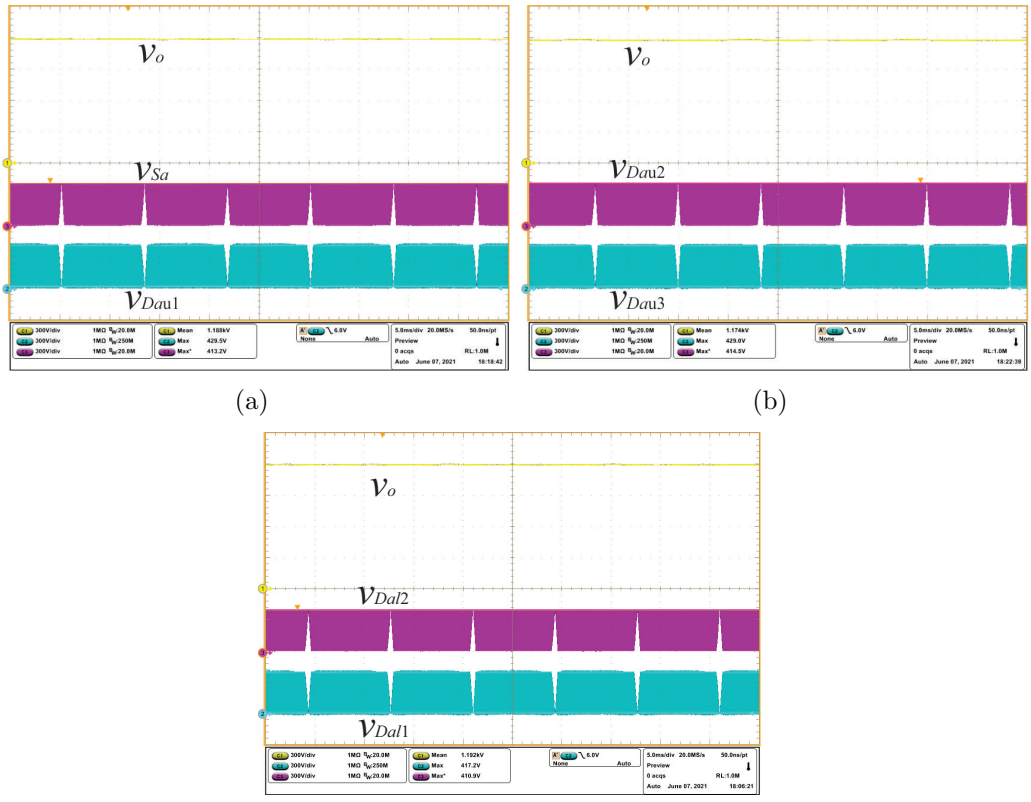


95.5%. This efficiency is lower than the dc-dc efficiency mostly due to the diode bridge and also because the ac current presents higher RMS values. This efficiency can be improved by using a synchronous rectifier or a bridgeless version of the topology, as presented in the first chapter.

The efficiency drop in the single-phase ac-dc converter compared to the dc-dc converter is mostly due to the insertion of a diode bridge in the converter's input with a low input voltage. The loss breakdown, presented in Fig. 109, shows that the the bridge diode losses are up to 36% of all losses. This could be reduced by using a bridgeless topology or by using a synchronous rectifier bridge.

Equipment that is connected to the grid with higher power levels must be designed to not affect the grid due to its harmonic content. It could be seen that the converter is capable of providing an input current with a sinusoidal shape, but it is important to evaluate the harmonic content of the current to assure that it meets standard requirements for electromagnetic emissions. The harmonic content of the input current was compared to the IEC 61000-3-2 requirements and it meets the standard requirements when operating at rated power, as illustrated in Fig. 110.

Fig. 105 – Voltage across the semiconductor devices of the single-phase ac-dc converter: (a) Switch and upper diode D_{au1}, (b) upper diodes D_{bu2} and D_{au3} and (c) lower diodes D_{al1} and D_{al2}.



(a) (b)

(c)

Fig. 106 – Single-phase ac-dc converter: Inductor current and current in the switched capacitors.

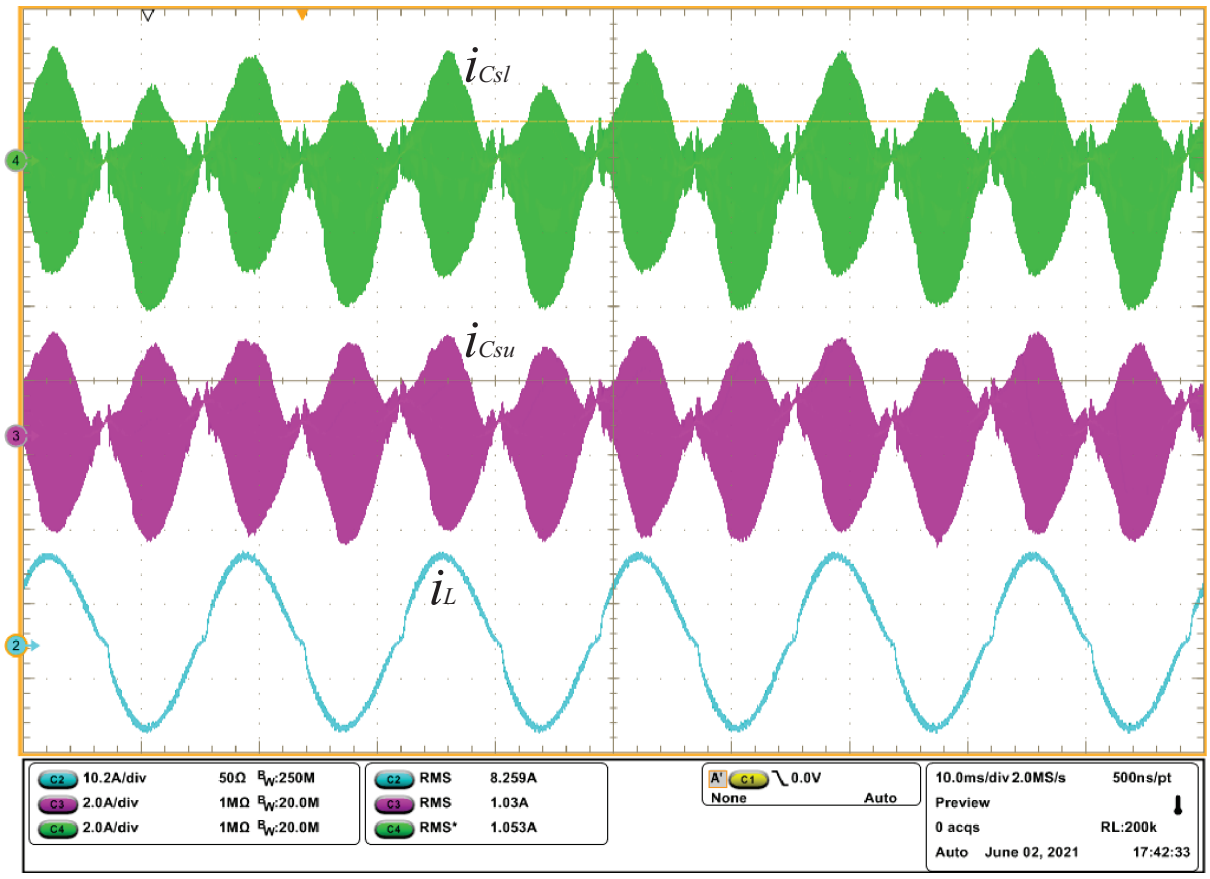


Fig. 107 – Single-phase ac-dc converter: Load step.

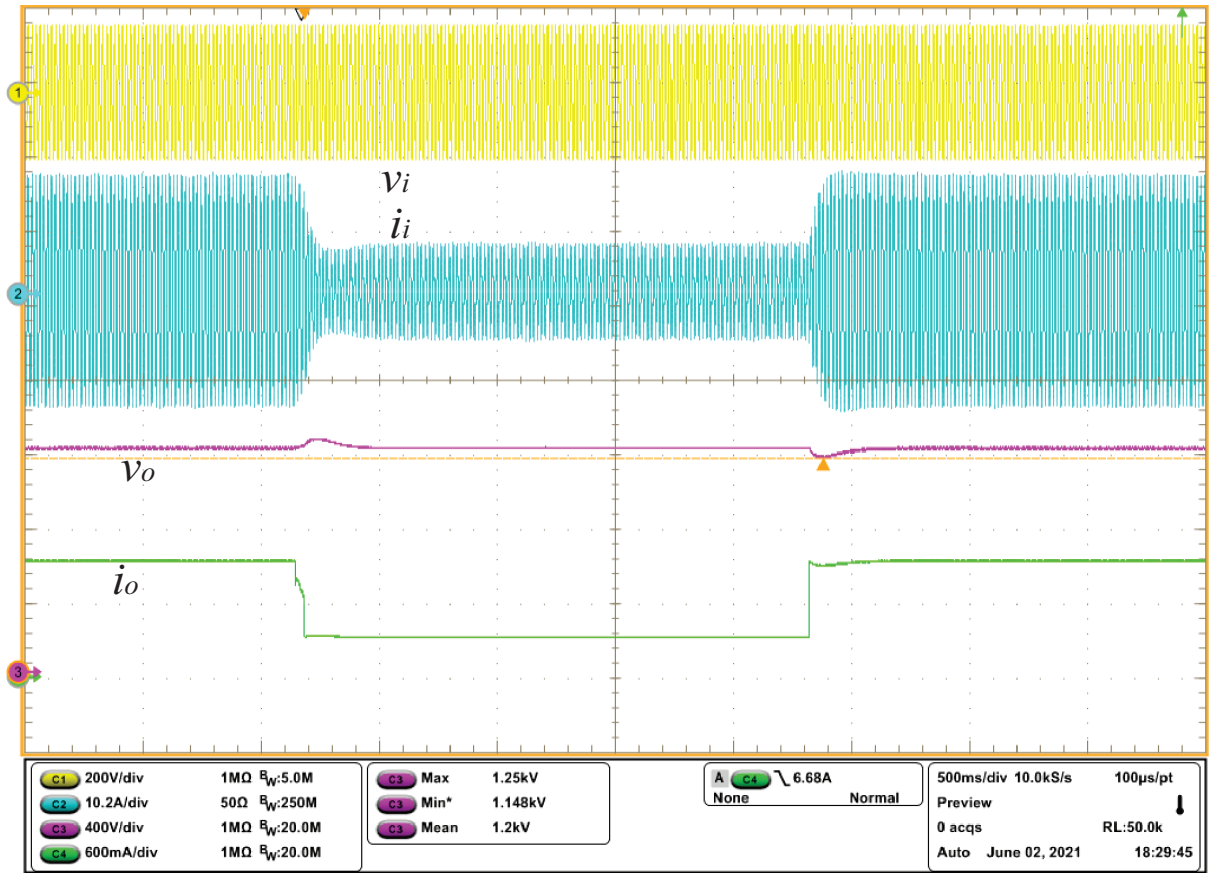


Fig. 108 – Single-phase ac-dc converter: Efficiency curve.

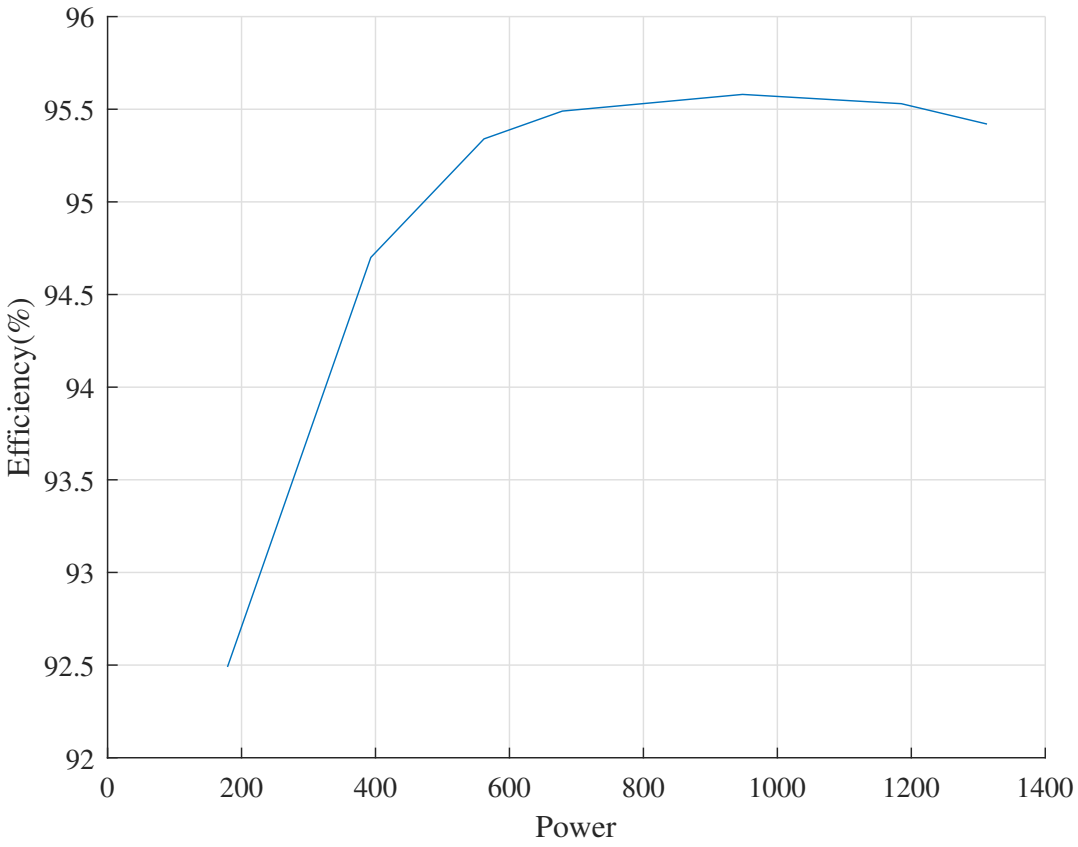


Fig. 109 – Single-phase ac-dc converter: Loss breakdown.

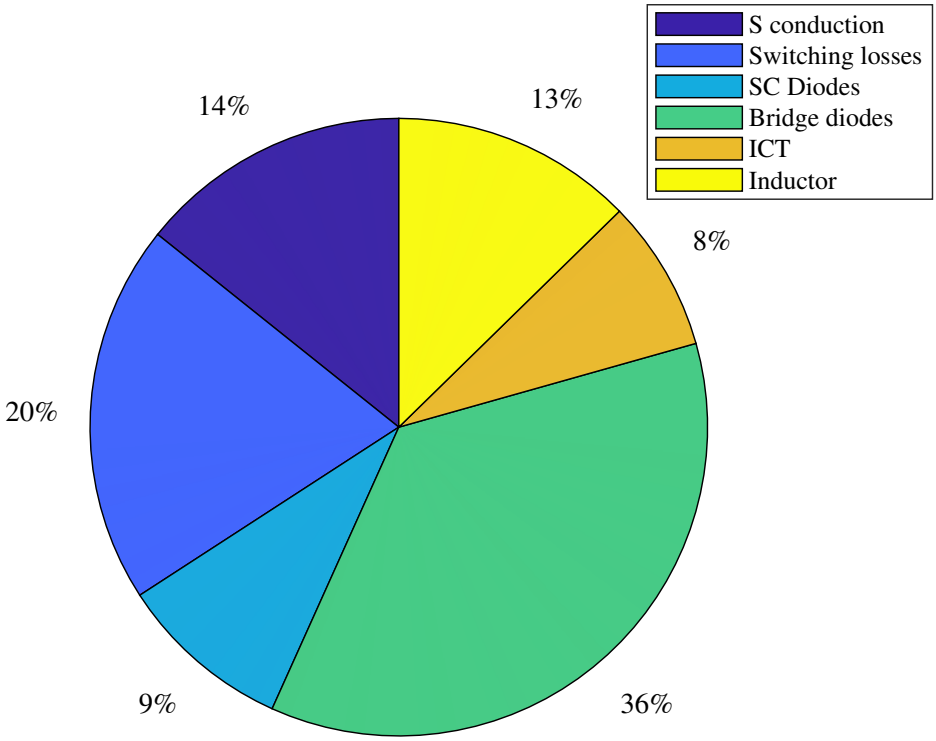
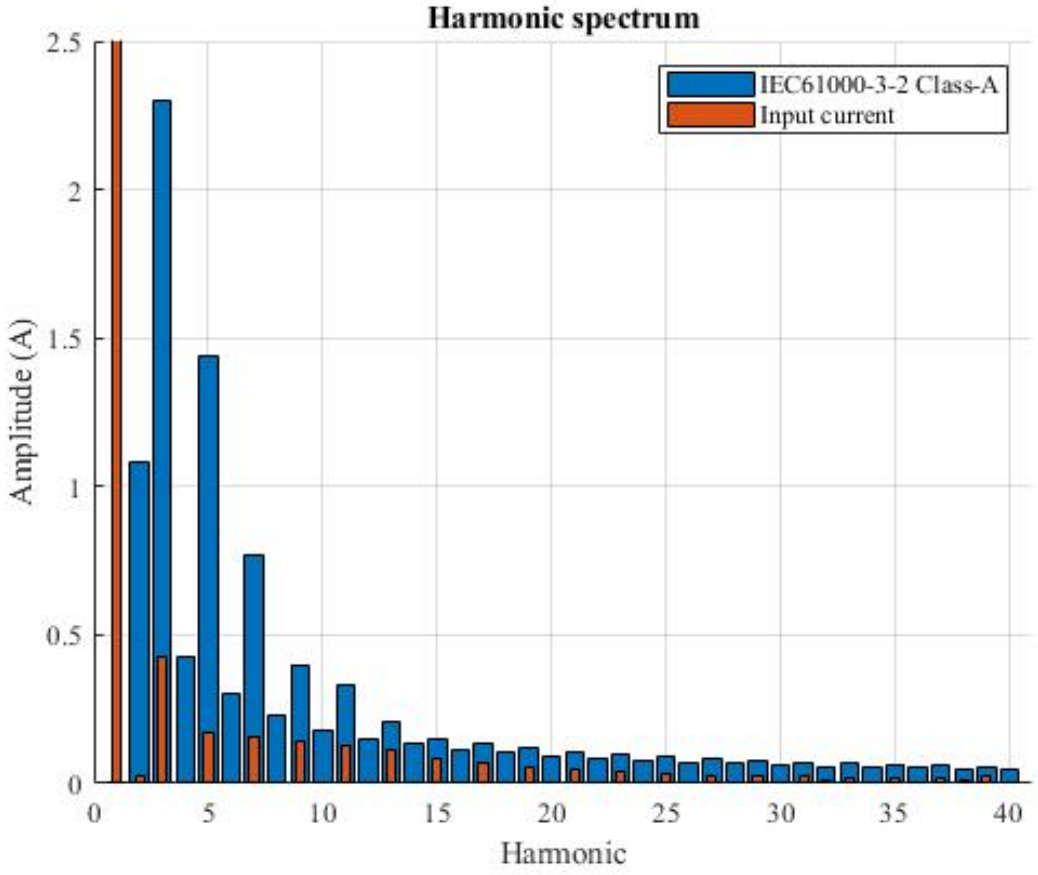


Fig. 110 – Single-phase ac-dc converter: Harmonic content.



4.8 SUMMARY

This chapter presented the analysis and simulation of the single-phase rectifier as well as the experimental results for a 127 V to 1200 V prototype. Some parts of the analysis were approached in the chapter before, since the rectifier has the same structure as the dc-dc converter. As a rectifier, it operates with a different input characteristics and has larger output capacitors to compensate the low-frequency ripple.

The duty cycle and input current ripple were analyzed in relation to the grid angle. Because of the MSSC characteristic, the inductor equation is the same for the maximum current ripple in all regions.

The output capacitor was designed for limiting the low-frequency output voltage ripple. An equivalent output capacitor was considered for its design and for obtaining the output dynamic characteristic of the converter. By designing the output capacitors considering the grid frequency and the cell capacitors using the equivalent resistance in the switching frequency, the capacitor voltages were balanced.

The voltage stress across the semiconductor devices is the same as in the dc-dc converter, but the current stress through the switches is variable, since the duty cycle and input current depend on the grid phase. Similar to the dc-dc version, the converter divides the input current between the windings of the ICT and the output voltage through the SC cells.

Simulations and experimental results were used to validate the theoretical analysis. The simulations and experiments showed that the MSSC and SC cells divided the voltage and current stress across the devices, a static gain higher than the conventional boost converter was achieved through the use of SC cells, and the MSSC cells provided a multilevel input characteristic that reduced the inductor current ripple.

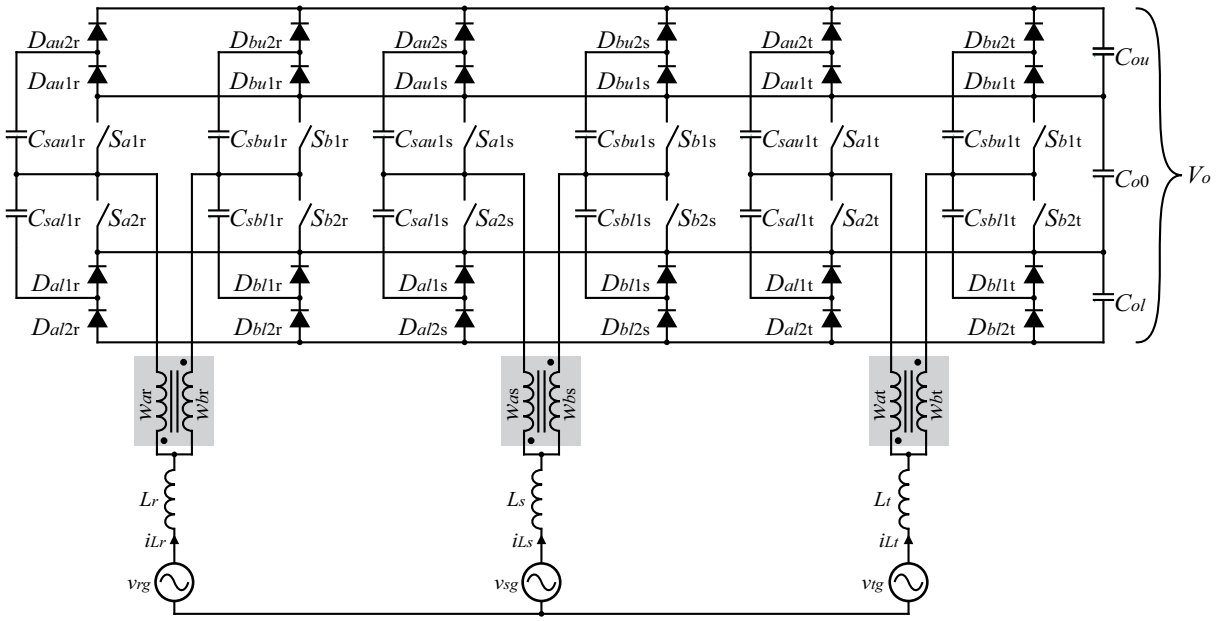
The converter controller was capable of achieving a high power factor with a low harmonic content, being able to meet international standard requirements. A load step was applied to the converter and it was verified that the current balance in the ICT and the voltage balance in the SC cells was not affected.

5 THREE-PHASE HYBRID BOOST RECTIFIER WITH MSSC AND SC CELLS

In applications with a high power demand, three-phase systems can be more practical due to the current share between phases. The concept herein proposed can be expanded into a three-phase active rectifier. Different from the previously presented single-phase converter, it is implemented without the input diode bridge. In the same way as the dc-dc proposed converter, its voltage gain is higher than the conventional boost converter, it can be expanded into more levels by adding SC cells and legs to each phase, and its input current can be controlled to achieve unit power factor.

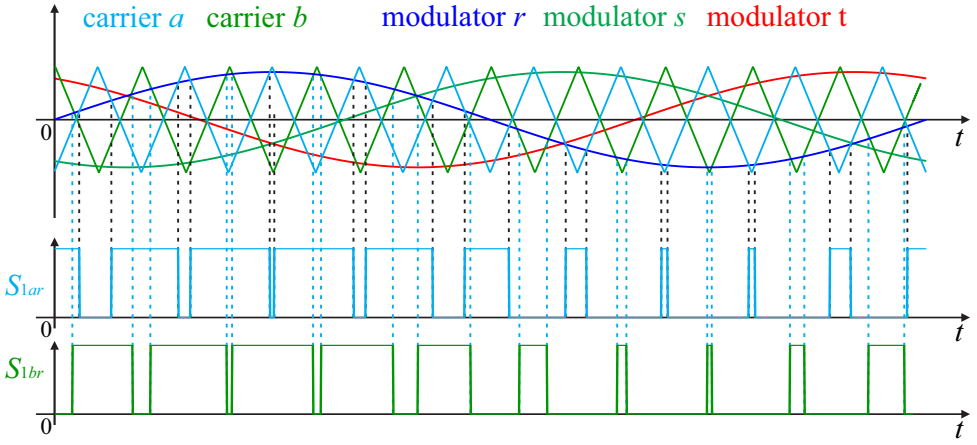
The three-phase rectifier with an upper and an lower SC cell and 3SSC will be used as the subject of study in this chapter, although the concept can be expanded into more states and SC cells or adapted to use other SC topologies. The proposed topology, shown in Fig. 111, is composed of three modules that are similar to the DC-DC converter with a synchronous switching cell. Its main advantages compared with other high-gain rectifiers in literature is the divided current across the switches, the single ground reference for the lower switches $S_{i2\varphi}$, the output voltage divided between self-balanced capacitors and the use of diodes in the stages with higher voltages, which avoids the need of drivers with high voltage isolation.

Fig. 111 – Three-phase HBR with 3SSC and SC cells.



The proposed topology has multilevel input voltage characteristic due to the the MSSC. Each state is responsible for one level in the phase voltage $v_{\varphi 0}$. Consequently, in the line-to-line voltage there are $2n + 1$ levels. Different from many multilevel topologies, the proposed converter does not require advanced modulation schemes to balance the capacitor voltages. The modulation scheme for one phase of the proposed three-phase rectifier is shown in Fig. 112. There are three phase-shifted carrier signals that are shared between all phases and they are responsible for switching each leg of all phases. The modulator signals are responsible for regulating the duty cycle of all switches of each phase.

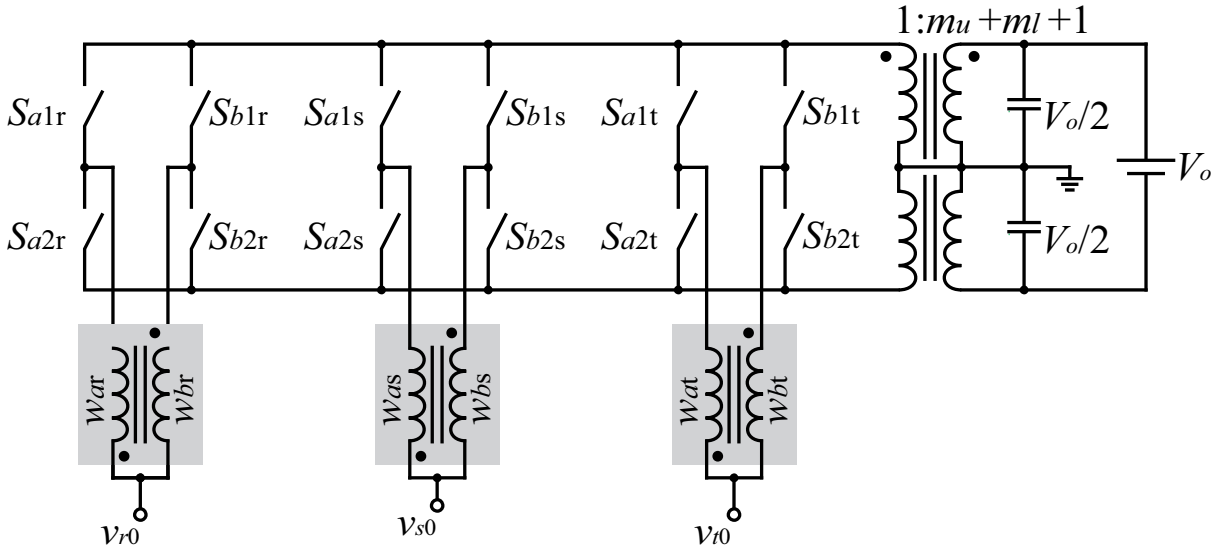
Fig. 112 – Modulation scheme of the proposed three-phase rectifier.



For the converter input analysis, an equivalent circuit shown in Fig. 113 is used. The circuit uses an ideal AC and DC transformer to represent the SC cells, as viewed by the converter input. The transformer has a center tap in its input and output that is connected to an intermediary point between two virtual capacitors. The capacitors are inserted to create a virtual ground reference, which facilitates the analysis of the three-phase converter and does not affect the converter operation. The actual circuit can be simulated with very small capacitors to emulate this model without affecting the converter dynamics. To simplify some equations, the ideal relation between the output voltage and the capacitor voltage, given by (5.1), is considered.

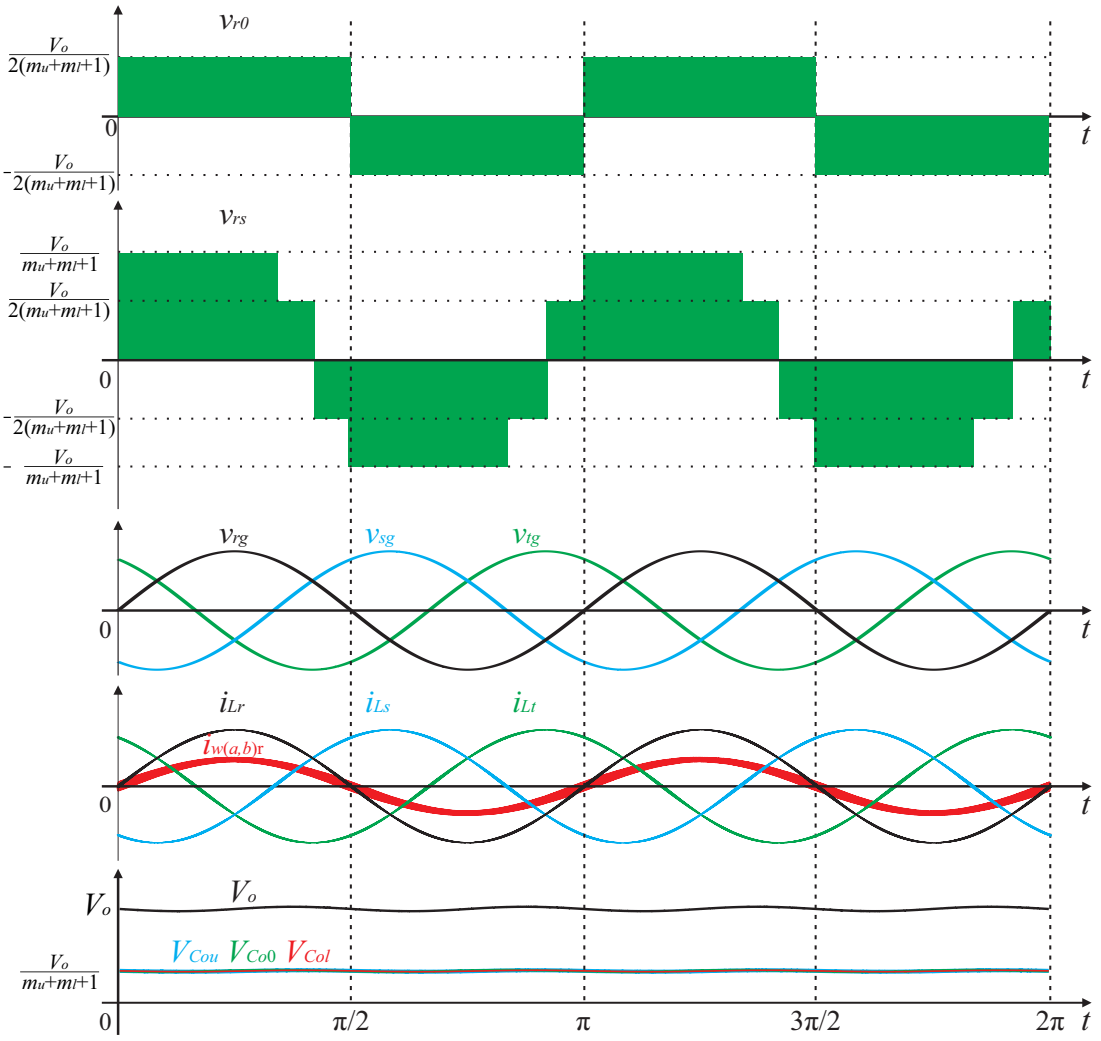
$$V_{Co0} = \frac{V_o}{m_u + m_l + 1} \tag{5.1}$$

Fig. 113 – Equivalent circuit of the proposed three-phase rectifier.



The main waveforms of the proposed topology are shown in Fig. 114.

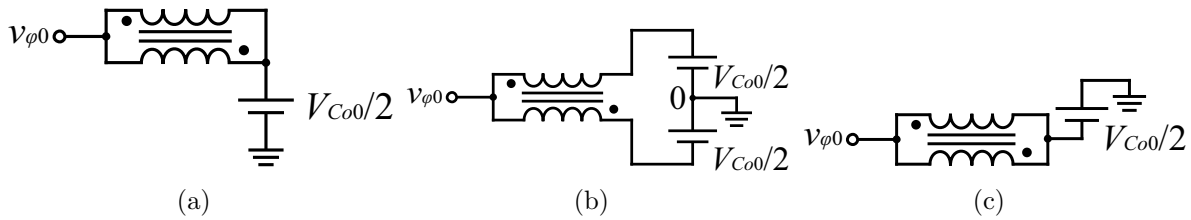
Fig. 114 – Main waveforms of the proposed three-phase rectifier.



5.1 DUTY CYCLE

The static gain and duty cycle analysis of this structure works in a similar method to the dc-dc analysis, just considering a different reference point. For this analysis, the states of a single phase are verified and, similar to the dc-dc converter, there are three operating regions for each phase and two states that switch in each of these stages. The equivalent circuits for each state are described in Fig. 115.

Fig. 115 – Equivalent circuits for the states of a single phase of the three-phase circuit: (a) State 1, (b) State 2, (c) State 3.



The values of the phase voltages $v_{\varphi 0}$ for each state are presented in Table 5.

Table 5 – Phase voltages for the states in a single phase

State	Phase voltage $V_{\varphi 0}$
State 1	$\frac{V_{Co0}}{2}$
State 2	0
State 3	$-\frac{V_{Co0}}{2}$

Knowing that for each region the converter alternate between two adjacent states (See Chapter 3), the average phase voltage values for each region are described by

$$\begin{cases} \left\langle v_{\varphi 0}^{regA}(\omega t)\right\rangle_{\frac{T_s}{2}} = \frac{2}{T_s}\left[\int_0^{d_\varphi(\omega t)T_s} 0dt + \int_{d_\varphi(\omega t)T_s}^{\frac{T_s}{2}} \frac{V_{Co0}}{2}dt\right] \\ \left\langle v_{\varphi 0}^{regA}(\omega t)\right\rangle_{\frac{T_s}{2}} = \frac{V_o}{2(m_u+m_l+1)} - \frac{V_o d_\varphi(\omega t)}{(m_u+m_l+1)} \\ \\ \left\langle v_{\varphi 0}^{regB}(\omega t)\right\rangle_{\frac{T_s}{2}} = \frac{2}{T_s}\left[-\int_{\frac{T_s}{2}}^{d_\varphi(\omega t)T_s} \frac{V_{Co0}}{2}dt + \int_{d_\varphi(\omega t)T_s}^{T_s} 0dt\right] \\ \left\langle v_{\varphi 0}^{regB}(\omega t)\right\rangle_{\frac{T_s}{2}} = \frac{V_o}{2(m_u+m_l+1)} - \frac{V_o d_\varphi(\omega t)}{(m_u+m_l+1)} \end{cases} \tag{5.2}$$

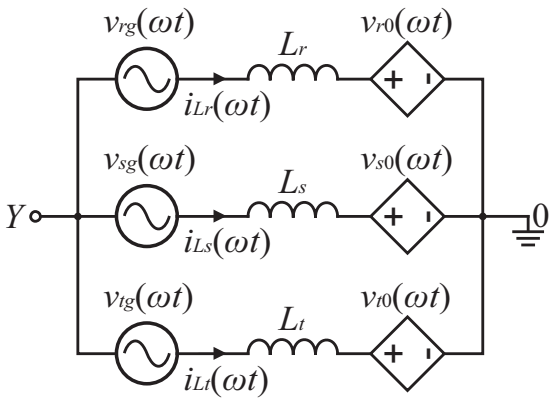
where d_φ is the duty cycle of the higher switches $S_{ij,\varphi}$ in phase φ.

The duty cycle is then isolated from the equations and rewritten as a function of V_o, resulting in

$$d_\varphi(\omega t) = \frac{(m_u + m_l + 1)\langle v_{\varphi 0}(\omega t)\rangle_{\frac{T_s}{2}}}{V_o} + \frac{1}{2}. \tag{5.3}$$

By knowing the relation between the phase voltages and the output voltage, the circuit can be represented by a simplified equivalent circuit that is used to perform the analysis of some elements of the topology. The simplified equivalent circuit is shown in Fig. 116.

Fig. 116 – Simplified equivalent circuit of the proposed three-phase rectifier.



5.2 INDUCTOR CURRENT RIPPLE

The current ripple in the inductor is a relation of the voltage across the inductor in a time period. The voltage across one inductor is given by

$$v_{L\varphi}(t) = v_{\varphi g}(t) - v_{\varphi 0}(t) + v_{Y0}(t) \tag{5.4}$$

where $v_{L\varphi g}$ is the phase voltage in phase φ and v_{Y0} is the common-mode voltage.

The common mode voltage is isolated for each phase, resulting in

$$\begin{cases} v_{Y0}(t) = v_{Lr}(t) - v_{rg}(t) + v_{r0}(t) \\ v_{Y0}(t) = v_{Ls}(t) - v_{sg}(t) + v_{s0}(t) \\ v_{Y0}(t) = v_{Lt}(t) - v_{tg}(t) + v_{t0}(t) \end{cases} \tag{5.5}$$

.

By summing the three equations and considering that sum of the grid phase voltages and currents (thus, the inductor voltages) are zero, the common-mode voltage is given by

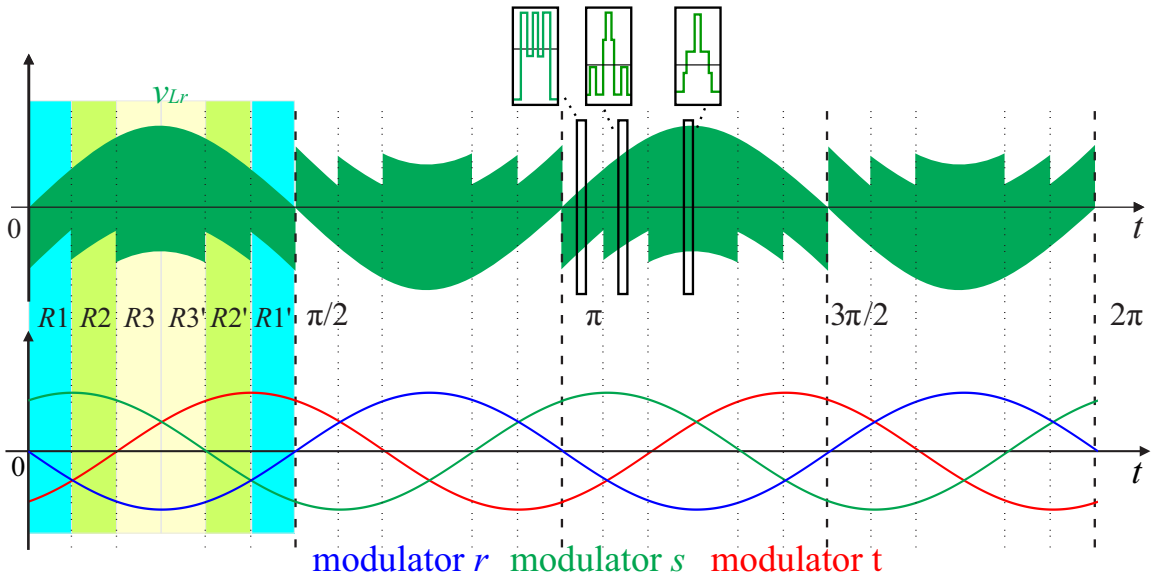
$$v_{Y0}(t) = \frac{v_{r0}(t) + v_{s0}(t) + v_{t0}(t)}{3}. \tag{5.6}$$

By replacing expression (5.6) in (5.4), the voltage across the inductor is obtained, as described by

$$\begin{cases} v_{Lr}(t) = L_\varphi \frac{di_L}{dt} = v_{rg}(t) - \frac{2v_{r0}(t) - v_{s0}(t) - v_{t0}(t)}{3} \\ v_{Ls}(t) = L_\varphi \frac{di_L}{dt} = v_{sg}(t) - \frac{2v_{s0}(t) - v_{r0}(t) - v_{t0}(t)}{3} \\ v_{Lt}(t) = L_\varphi \frac{di_L}{dt} = v_{tg}(t) - \frac{2v_{t0}(t) - v_{r0}(t) - v_{s0}(t)}{3} \end{cases} \tag{5.7}$$

In the dc-dc and the single-phase ac-dc converters the inductor voltage was represented by only two stages that occurred in one third of the switching period. In the three-phase rectifier there are more stages that depend on the grid angle and the state of each phase, which results in a more complex shape, as shown in Fig. 117.

Fig. 117 – Voltage across an inductor of the proposed three-phase rectifier.



The current ripple of an inductor can be obtained by isolating its term from (5.7)

for each operational stage. In Fig. 117 it should be noted that for each half cycle the inductor voltage presents three wave patterns, which depends on the relation between the modulator waves. The operating regions where each pattern occurs will be referred to as $R1$, $R2$ and $R3$. In the other half cycle the voltage across the inductor inverts, but the current ripple amplitude is the, thus it can be analyzed for just one half cycle. $R1$ occurs when d_r is higher than one of the other duty cycles and lower than the other. $R2$ happens when the value d_r is higher than the other duty cycle values and one of the other duty cycle values is below 0.5. The last region, $R3$ occurs when d_r is the only duty cycle whose value is over 0.5. The regions were divided between Ri and Ri' because there is a slight change in the equations, d_s is replaced by d_t, but since the modulator shapes are "mirrored", the current ripple amplitude is the same in either regions. the current ripple for each of these stages is derived and given by

$$\begin{cases} \Delta i_{Lr}^{R1} = \frac{1-2d_r(\omega t)}{2f_sL_\varphi}\left(v_{rg}(\omega t) - \frac{V_o}{3(m_u+m_l+1)}\right) \\ \Delta i_{Lr}^{R2} = \frac{1}{f_sL_\varphi}\left(v_{rg}(\omega t)(1-d_r(\omega t)) - V_o\frac{1-d_r(\omega t)-d_s(\omega t)}{6(1+m_u+m_l)}\right) \\ \Delta i_{Lr}^{R3} = \frac{1}{f_sL_\varphi}\left(v_{rg}(\omega t)\, d_s(\omega t) - V_o\frac{d_s(\omega t)-1+d_r(\omega t)}{3(m_u+m_l+1)}\right) \\ \Delta i_{Lr}^{R1'} = \frac{1-2d_r(\omega t)}{2f_sL_\varphi}\left(v_{rg}(\omega t) - \frac{V_o}{3(m_u+m_l+1)}\right) \\ \Delta i_{Lr}^{R2'} = \frac{1}{f_sL_\varphi}\left(v_{rg}(\omega t)(1-d_r(\omega t)) - V_o\frac{1-d_r(\omega t)-d_t(\omega t)}{6(1+m_u+m_l)}\right) \\ \Delta i_{Lr}^{R3'} = \frac{1}{f_sL_\varphi}\left(v_{rg}(\omega t)\, d_t(\omega t) - V_o\frac{d_t(\omega t)-1+d_r(\omega t)}{3(m_u+m_l+1)}\right) \end{cases}. \tag{5.8}$$

The input current ripple is then normalized as a function of *alpha* to obtain the points where the maximum ripple occurs. The normalized currents are given by

$$\begin{cases} \overline{\Delta i_{Lr}^{R1}} = \frac{1-2d_r(\omega t)}{2}\left(\alpha\sin(\omega t) - \frac{1}{3(m_u+m_l+1)}\right) \\ \overline{\Delta i_{Lr}^{R2}} = \left(\alpha\sin(\omega t)(1-d_r(\omega t)) - \frac{1-d_r(\omega t)-d_s(\omega t)}{6(1+m_u+m_l)}\right) \\ \overline{\Delta i_{Lr}^{R3}} = \left(\alpha\sin(\omega t)\, d_s(\omega t) - \frac{d_s(\omega t)-1+d_r(\omega t)}{3(m_u+m_l+1)}\right) \\ \overline{\Delta i_{Lr}^{R1'}} = \frac{1-2d_r(\omega t)}{2}\left(\alpha\sin(\omega t) - \frac{1}{3(m_u+m_l+1)}\right) \\ \overline{\Delta i_{Lr}^{R2'}} = \left(\alpha\sin(\omega t)(1-d_r(\omega t)) - \frac{1-d_r(\omega t)-d_t(\omega t)}{6(1+m_u+m_l)}\right) \\ \overline{\Delta i_{Lr}^{R3'}} = \left(\alpha\sin(\omega t)\, d_s(\omega t) - \frac{d_s(\omega t)-1+d_r(\omega t)}{3(m_u+m_l+1)}\right) \end{cases}. \tag{5.9}$$

A graphic of the current ripple as a function of α and ωt can then be traced, as shown in 118. It should be noticed that the maximum ripple occurs at either $\pi/2$ or $\pi/3$ and depends on α. To verify the conditions where each operation point presents the largest ripple, the normalized current ripple rewritten for these points of operation

$$\begin{cases} \overline{\Delta i_{Lr}}(\pi/3) = \alpha\frac{\sqrt{3}}{4}\left(1-(m_u+m_l+1)\alpha\sqrt{3}\right) \\ \overline{\Delta i_{Lr}}(\pi/2) = \frac{\alpha}{6}(2-(m_u+m_l+1)3\alpha) \end{cases}. \tag{5.10}$$

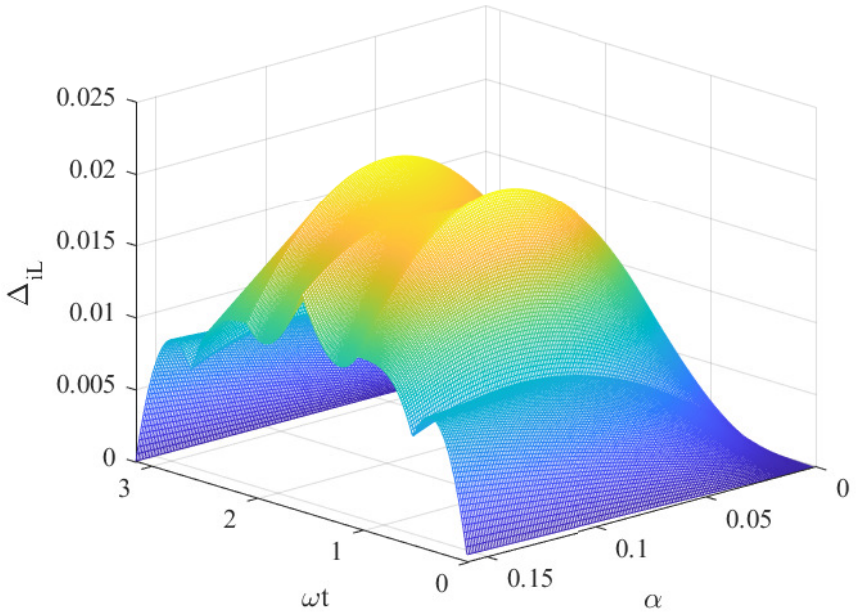
The value of α which determines whether the highest ripple is at $\pi/2$ or $\pi/3$ can be obtained by considering that both equations have the same value

$$\frac{\alpha}{6}(2-(m_u+m_l+1)3\alpha) = \alpha\frac{\sqrt{3}}{4}\left(1-(m_u+m_l+1)\alpha\sqrt{3}\right), \tag{5.11}$$

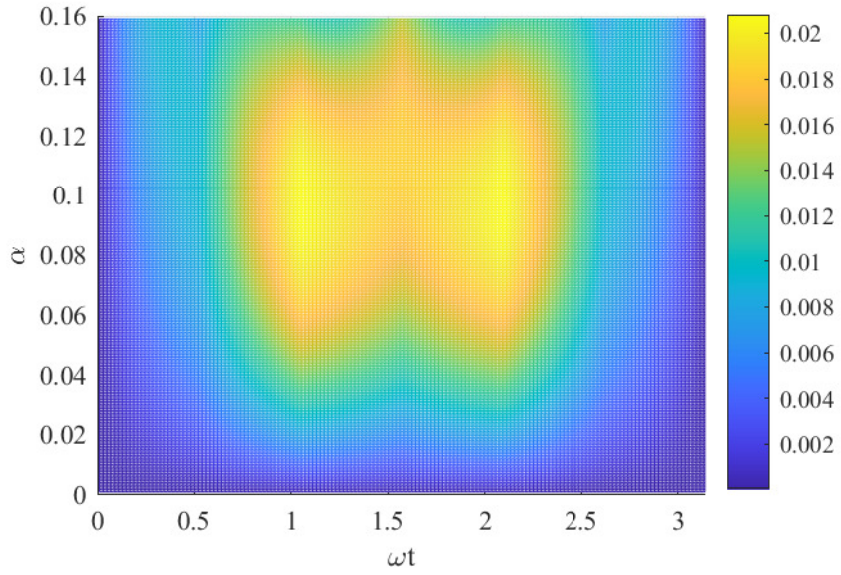
α is then isolated to verify the transition point

$$\alpha_t = \frac{3\sqrt{3}-4}{(m_u+m_l+1)3}. \tag{5.12}$$

Fig. 118 – Variation of the input current ripple in the three-phase rectifier as a function of the modulation index.



(a)



(b)

The inductance value can then be derived by replacing the operation points in (5.8). The highest ripple for an α value lower and higher than α_t are given by

$$\begin{cases} L_{\varphi}^{\alpha<\alpha_t} = \frac{\alpha V_o}{4 f_s \Delta i_L} \left[\sqrt{3} - 3a(m_u + m_l + 1)\right] \\ L_{\varphi}^{\alpha>\alpha_t} = \frac{\alpha V_o}{f_s \Delta i_L} \left[\frac{1-(m_u+m_l+1)}{2} - \frac{1}{3}\right] \end{cases} . \tag{5.13}$$

5.3 CAPACITORS

The switched capacitors are designed with the methodology shown in chapter 2, that presents the analysis of the equivalent resistance variation related to the capacitance. However, the the output power is divided between six legs. The output capacitors can also be designed by the same methodology, since in an active three-phase rectifier the output voltage low-frequency ripple can be neglected. This characteristic is important because no electrolytic capacitor is required.

In the single-phase topology, the output capacitors must have a higher capacitance value to compensate the low equivalent resistance of the cells near the grid zero passage. In the three-phase rectifier, each phase has a distinct phase-shifted duty cycle value. Therefore, there is always one phase compensating for the low equivalent resistance of the other phase.

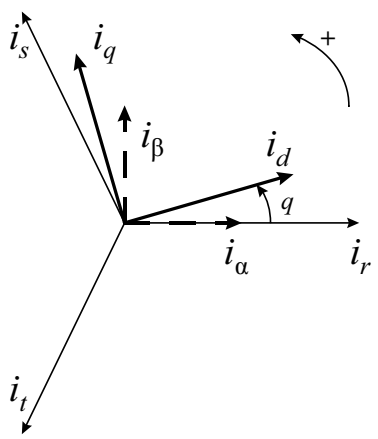
5.4 DYNAMIC ANALYSIS

The converter is controlled by two cascaded loops, an outer output voltage loop that generates a current reference to an inner current loop that has faster dynamics and regulates the duty cycle to follow the current reference. In the three-phase converter it is also not necessary to have capacitor voltage control loop as well. The currents in the ICT are also balanced as long as the gate drivers are similar.

In three-wire three-phase systems the phases cannot be controlled individually, because the phases are coupled so the current in one phase affects the current in the other two. The most common alternatives for uncoupling the currents of the three-phase rectifier are the Clarke and Park transforms.

The Clarke transform converts the three-phase currents in two ideally sinusoidal orthogonal currents i_α and i_β, that are uncoupled from each other. The Park transform is a variation of the Clarke that results in two orthogonal vectors in a synchronous reference frame, that are the direct (i_d) and quadrature (i_q) currents. The vectors obtained with the Park transform have ideally a constant amplitude and rotates according to the grid phase. A representation of the current vectors for the Clarke and Park transforms is illustrated in Fig. 119.

Fig. 119 – Current vectors in *abc* and $\alpha\beta$ rotating orthogonal reference frame and $dq0$ synchronous reference frame [123].



The main advantage of the Clarke transform is that it does not need to use PLL (Phase-locked loop) algorithms, since there is no sine calculation in the transform. The sinusoidal current reference can be the input voltage multiplied by a gain to generate the sinusoidal shape. The current follows the voltage shape, including the harmonic, which can be beneficial in rectifier circuits. In real systems the grid voltage might be flattened at its peak because of the non-linear loads connected to the grid, when the current is flattened as well, it can help reducing the power consumed at the peak. The main drawback of the Clarke transform control is that the controller follows a sinusoidal reference, instead of a constant reference, which requires faster controllers and possibly resonant controllers for the current loop.

The Park transform is more complex than the Clarke transform, since there are sine and cosine calculations, therefore a PLL (Phase-locked loop) technique is required to obtain the phase angle to perform the transform. On the other hand, the control technique is simpler because the resulting signals are continuous. Therefore, a simple PI controller is enough to provide a zero steady-state error. Furthermore, the DSP technology today allows more complex calculations. However, due to the implementation simplicity, the Clarke transform was chose to model the proposed three-phase rectifier.

In this work the phases are referred to as rst instead of abc to not be confused with the windings of the ICT. The Clarke direct and inverse transforms are given by

$$\begin{cases} \overrightarrow{V_{\alpha\beta\gamma}} = \overrightarrow{T_{\alpha\beta\gamma}} \cdot \overrightarrow{V_{rst}} \\ \overrightarrow{I_{\alpha\beta\gamma}} = \overrightarrow{T_{\alpha\beta\gamma}} \cdot \overrightarrow{I_{rst}} \\ \overrightarrow{V_{rst}} = \overrightarrow{T_{\alpha\beta\gamma}^{-1}} \cdot \overrightarrow{V_{\alpha\beta\gamma}} \\ \overrightarrow{I_{rst}} = \overrightarrow{T_{\alpha\beta\gamma}^{-1}} \cdot \overrightarrow{I_{\alpha\beta\gamma}} \end{cases} \tag{5.14}$$

where $\overrightarrow{V_{rst}}$ and $\overrightarrow{I_{rst}}$ are the voltage and current vectors in the standard reference frame and $\overrightarrow{V_{\alpha\beta\gamma}}$ and $\overrightarrow{I_{\alpha\beta\gamma}}$ are the voltage and current in the rotating orthogonal reference frame, given by

$$\begin{cases} \overrightarrow{V_{rst}} = \begin{bmatrix} v_{rg} & v_{sg} & v_{tg} \end{bmatrix}^T \\ \overrightarrow{I_{rst}} = \begin{bmatrix} i_{Lr} & i_{Ls} & i_{Lt} \end{bmatrix}^T \\ \overrightarrow{V_{\alpha\beta\gamma}} = \begin{bmatrix} v_{\alpha g} & v_{\beta g} & v_{\gamma g} \end{bmatrix}^T \\ \overrightarrow{I_{\alpha\beta\gamma}} = \begin{bmatrix} i_{L\alpha} & i_{L\beta} & i_{L\gamma} \end{bmatrix}^T \end{cases} \tag{5.15}$$

.

The Clarke direct and inverse transformation matrices are given by

$$\begin{cases} \overrightarrow{T_{\alpha\beta\gamma}} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \\ \overrightarrow{T_{\alpha\beta\gamma}^{-1}} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \end{cases} . \tag{5.16}$$

To obtain the dynamic model of the converter, the Kirchhov voltage law is applied to the circuit shown in Fig. 116.

$$\begin{cases} -v_{rg}(t) + L_\varphi \frac{di_{Lr}(t)}{dt} + v_{r0}(t) - v_{Y0}(t) = 0 \\ -v_{sg}(t) + L_\varphi \frac{di_{Ls}(t)}{dt} + v_{s0}(t) - v_{Y0}(t) = 0 \\ -v_{tg}(t) + L_\varphi \frac{di_{Lt}(t)}{dt} + v_{t0}(t) - v_{Y0}(t) = 0 \end{cases} . \tag{5.17}$$

Knowing that the moving phase voltage in half period is given by

$$\langle v_{\varphi 0}(t) \rangle_{\frac{T_s}{2}} = \frac{V_o d_\varphi(t)}{(m_u + m_l + 1)} - \frac{V_o}{2\,(m_u + m_l + 1)} \tag{5.18}$$

The expression (5.17) can be rewritten as

$$\begin{gathered} \begin{bmatrix} v_{rg}(t) \\ v_{sg}(t) \\ v_{tg}(t) \end{bmatrix} = L_\varphi \cdot I_3 \cdot \frac{d}{dt} \begin{bmatrix} i_{Lr}(t) \\ i_{Ls}(t) \\ i_{Lt}(t) \end{bmatrix} + \frac{V_o}{2(m_u+m_l+1)} . I_3 . \begin{bmatrix} d_r(t) \\ d_s(t) \\ d_t(t) \end{bmatrix} \\ - \frac{V_o}{2(m_u+m_l+1)} . I_3 - \begin{bmatrix} v_{Y0}(t) \\ v_{Y0}(t) \\ v_{Y0}(t) \end{bmatrix} \end{gathered} \tag{5.19}$$

The inverse Clarke transform is then applied to the equation

$$\begin{gathered} \overrightarrow{T^{-1}_{\alpha\beta\gamma}} \cdot \overrightarrow{V_{\alpha\beta\gamma}} = L_\varphi . I_3 \cdot \overrightarrow{T^{-1}_{\alpha\beta\gamma}} . \frac{d\overrightarrow{I_{\alpha\beta\gamma}}}{dt} + \frac{V_o}{2(m_u+m_l+1)} . I_3 . \overrightarrow{T^{-1}_{\alpha\beta\gamma}} . \overrightarrow{D_{\alpha\beta\gamma}} \\ - \overrightarrow{T^{-1}_{\alpha\beta\gamma}} \cdot \frac{V_o}{2(m_u+m_l+1)} . I_3 + \overrightarrow{T^{-1}_{\alpha\beta\gamma}} \cdot \overrightarrow{V_{Y0}} \end{gathered} \tag{5.20}$$

where

$$\begin{aligned} \overrightarrow{D_{\alpha\beta\gamma}} &= \begin{bmatrix} d_\alpha & d_\beta & d_\gamma \end{bmatrix}^T \\ \overrightarrow{V_{Y0}} &= \begin{bmatrix} V_{Y0} & V_{Y0} & V_{Y0} \end{bmatrix}^T \end{aligned} \tag{5.21}$$

The direct Clarke transform is then applied to the equation, resulting in

$$\overrightarrow{V_{\alpha\beta\gamma}} = L_\varphi . I_3 . \frac{d\overrightarrow{I_{\alpha\beta\gamma}}}{dt} + \frac{V_o}{2\,(m_u + m_l + 1)} . I_3 . \overrightarrow{D_{\alpha\beta\gamma}} + \overrightarrow{T^{-1}_{\alpha\beta\gamma}} . \left[\frac{V_o}{2\,(m_u + m_l + 1)} . I_3 + \overrightarrow{V_{Y0}} \right] \tag{5.22}$$

.

The expression can be rewritten in matrix notation, showing all elements

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_\gamma(t) \end{bmatrix} = L_\varphi . \frac{d}{dt} \begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \\ i_\gamma(t) \end{bmatrix} + \frac{V_o}{2\,(m_u + m_l + 1)} . \begin{bmatrix} d_\alpha(t) \\ d_\beta(t) \\ d_\gamma(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \sqrt{3} \left(\frac{V_o}{2(m_u+m_l+1)} + v_{Y0} \right) \end{bmatrix} \tag{5.23}$$

par Since there is intended current path for the common mode current, the third line of the system can be neglected

$$\begin{cases} v_\alpha(t) = L_\varphi . \frac{di_\alpha}{dt} + \frac{V_o}{2(m_u+m_l+1)} d_\alpha(t) \\ v_\beta(t) = L_\varphi . \frac{di_\beta}{dt} + \frac{V_o}{2(m_u+m_l+1)} d_\beta(t) \end{cases} \tag{5.24}$$

The terms of the function are then decomposed into small and large signals

$$\begin{cases} V_\alpha = L_\varphi . \left(\frac{\widetilde{di_\alpha}}{dt} + \frac{dI_\alpha}{dt} \right) + \frac{V_o}{2(m_u+m_l+1)} \left(D_\alpha + \widetilde{d}_\alpha(t) \right) \\ V_\beta = L_\varphi . \left(\frac{\widetilde{di_\beta}}{dt} + \frac{dI_\beta}{dt} \right) + \frac{V_o}{2(m_u+m_l+1)} \left(D_\beta + \widetilde{d}_\beta(t) \right) \end{cases} \tag{5.25}$$

The small signal components of the function are then isolated and the Laplace transform is applied, thus obtaining the input current transfer functions, given by

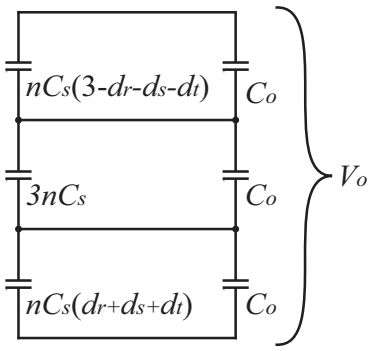
$$\begin{cases} G_{i\alpha}(s) = \frac{i_\alpha(s)}{d_\alpha(s)} = \frac{V_o}{2(m_u+m_l+1)L_\varphi s} \\ G_{i\beta}(s) = \frac{i_\beta(s)}{d_\beta(s)} = \frac{V_o}{2(m_u+m_l+1)L_\varphi s} \end{cases} \tag{5.26}$$

.

5.5 OUTPUT DYNAMIC ANALYSIS

For the output dynamic analysis, the same considerations were in the single-phase chapter are taken into account. The input power factor is considered unitary, the power losses are neglected and the output capacitors are considered as a single series equivalent capacitance. In the three-phase converter, the equivalent capacitance is calculated with the same method as the DC-DC converter. The equivalent circuit considers the duty cycles of each phase for each equivalent cell capacitor, as illustrated in Fig. 120.

Fig. 120 – Equivalent output capacitance for the three-phase rectifier.



In the three-phase rectifier the sum of all duty cycles is 1.5 if the phases are balanced, resulting in an equivalent capacitance given by

$$C_o^{eq} = \frac{2C_o^2 + 9nC_sC_o + 9n^2C_s^2}{6C_o + 15nC_s} \tag{5.27}$$

The output current is given by the sum of the capacitor and load currents, given by

$$i_o(t) = C_o^{eq}\frac{dv_o(t)}{dt} + \frac{v_o(t)}{R_o}. \tag{5.28}$$

The sliding average values are extracted from the expression and decomposed into small-signal and large-signal terms, resulting in

$$I_o(t) + \widetilde{i}_o(t) = C_o^{eq}\frac{dV_o(t)}{dt} + C_o^{eq}\frac{d\widetilde{v}_o(t)}{dt} + \frac{V_o(t)}{R_o} + \frac{\widetilde{v}_o(t)}{R_o}. \tag{5.29}$$

The large-signal components are neglected and the Laplace transform is applied and the equation is then rewritten in an output transfer function form, given by

$$\frac{\widetilde{v}_o(s)}{\widetilde{i}_o(s)} = \frac{R_o}{1 + C_o^{eq}R_os} \tag{5.30}$$

5.6 VOLTAGE AND CURRENT STRESS

As in the dc-dc and single phase ac-dc converters, the voltage across the switches is the total output voltage divided by the number of cascaded cells plus 1, since each semiconductor device is associated in parallel with a capacitor in each operational stage.

To calculate the current stress, the input current ripple and the ripple caused by the SC cell are neglected, thus the moving average current values for each operational stages are considered. This method can be used for SC cells designed with partial charge or no charge conditions. If the capacitors are designed to prioritize size over efficiency and the circuit operates in complete charge mode, the models become too complex and analytic equations might not be the ideal solution to evaluate current stress across the switches. The sum of the diode currents in each phase is equal to the total output current. Considering that the input power is the same as the output power of each phase, and knowing that the moving average current in the cell capacitors is zero, the diode currents is given by

$$\begin{array}{l} i_{Deven}(\omega t) = \frac{I_p V_p}{nV_o}\cos^2(\omega t+\phi)\left[\frac{(m_u+m_l+1)v_{\varphi g}}{V_o}+\frac{1}{2}\right] \\ i_{Dodd}(\omega t) = \frac{I_p V_p}{nV_o}\cos^2(\omega t+\phi)\left[\frac{1}{2}-\frac{(m_u+m_l+1)v_{\varphi g}}{V_o}\right] \end{array} \tag{5.31}$$

.

The average current in each diode during a grid cycle is given by

$$I_D = \frac{I_o}{3n} \tag{5.32}$$

.

Due to the bidirectional nature of the switching cell and the working principle of the converter, the current in the odd numbered diodes is the same as in the even numbered diodes phase-shifted in one half cycle. Therefore, their RMS current is the same in an entire cycle, as given by

$$\begin{array}{l} I_D^{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\int_0^{d(\omega t)}\left[\frac{I_p V_p}{nV_o}\cos^2(\omega t+\phi)\left(\frac{(m_u+m_l+1)v_{\varphi g}}{V_o}+\frac{1}{2}\right)\right]^2 dt d\omega t} \\ = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\frac{2{I_p}^2{V_p}^2\left(\sin(\omega t)^2-1\right)^2}{{V_o}^2n^2+2V_p(m_u+m_l+1)\sin(\omega t)V_o n^2}d\omega t} \end{array} \tag{5.33}$$

.

As in the previous structures, the current in the active switches is the current in one ICT winding plus the current in the diodes at the same leg that switch in the same stage, since the diodes are in the same branch as the SC capacitors. The switch current is given by

$$i_S(\omega t) = \frac{I_p\left[V_o\sin(\omega t+\phi)+V_p(m_u+m_l)\cos^2(\omega t+\phi)\right]}{nV_o}\left[\frac{(m_u+m_l+1)v_{\varphi g}}{V_o}+\frac{1}{2}\right] \tag{5.34}$$

.

The MOSFET RMS current is described by

$$I_S{}^{RMS}(\omega t) = \sqrt{\int_0^{2\pi}\left(\begin{array}{l}\left[\frac{I_p V_o\sin(\omega t)+2(m_u+m_l)V_p\cos^2(\omega t)}{V_o n+2(m_u+m_l+1)V_p\cos^2(\omega t)}\right]^2 \\ \cdot\left[\frac{V_p(m_u+m_l+1)v_{\varphi g}}{V_o}+\frac{1}{2}\right]\end{array}\right)d\omega t} \tag{5.35}$$

Table 6 – Specifications of the proposed three-phase rectifier

Specification	**Value**
Input line-to-line voltage V_i (RMS value)	220 V
Output voltage	1200 V
Output power	4 kW
Grid frequency	60 Hz
Switching frequency	100 kHz
Switched capacitors C_s	5.6 μF
Output capacitors C_o	45 μF
Input inductor L_i	38 μH
Switch resistances (Rohm SCT2080AL) R_s	80 mΩ
Diode resistances (Cree C3D04065A) R_d	100 mΩ
Diode forward voltage V_d	0.9 V

.

5.7 SIMULATION RESULTS

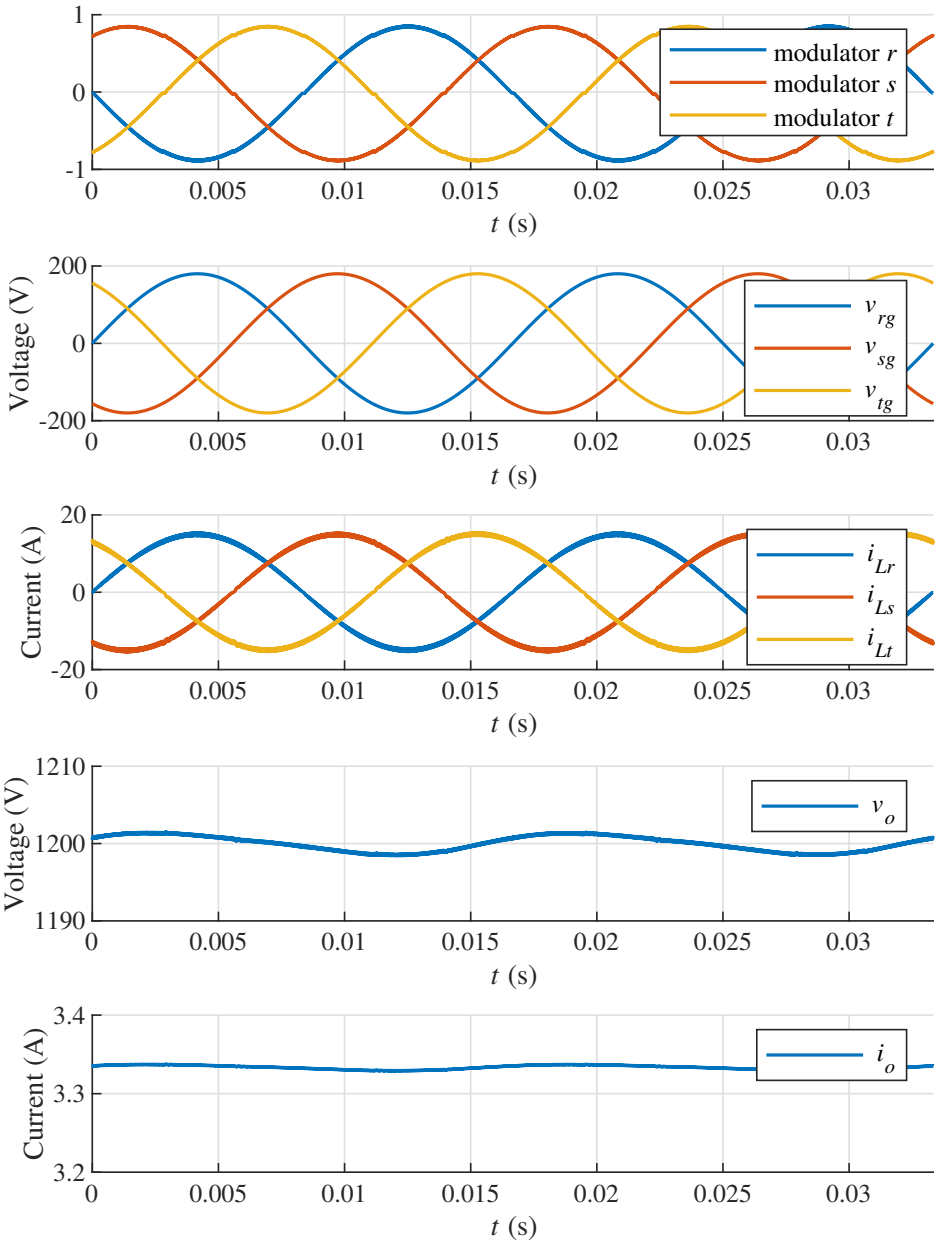
To validate the theoretical analysis, simulations were performed with the same parameters that were used in the experimental prototype, based on dc-dc modules. The specifications of the proposed topology are described in Table 6. The three-phase converter will be composed of three single-phase modules with active switches replacing the switching cell diodes. Since the power is divided by the three phases, the rated output power of this converter is three times the rated power of a single-phase module. To be able to use the same modules to validate the three-phase converter, a 220 V line-to-line voltage is used. The converter is rated for 4 kW, so that the current stress in the devices is close to the single-phase modules.

The converter was simulated at its rated operation point to evaluate its performance in steady-state. The main waveforms of the converter at full load are shown in Fig 121. The converter presents high static gain with a higher modulation index than the conventional boost rectifier and presents a high input power factor (above 0.99) with low THD (below 0.03).

One of the main differences from the single-phase topology is the characteristic of the modulator signals, that have a sinusoidal shape. Because of the SC cells, the modulation index can be higher to achieve a high voltage gain, which improves the converter controllability. On the other hand, a higher modulation index also means that there are some operating points during the grid period where the duty cycle value is near 1 or 0, which must be avoided when working with SC cells. This aspect is one of the factors that determine whether more or less cascaded SC cells should be used for a given voltage gain.

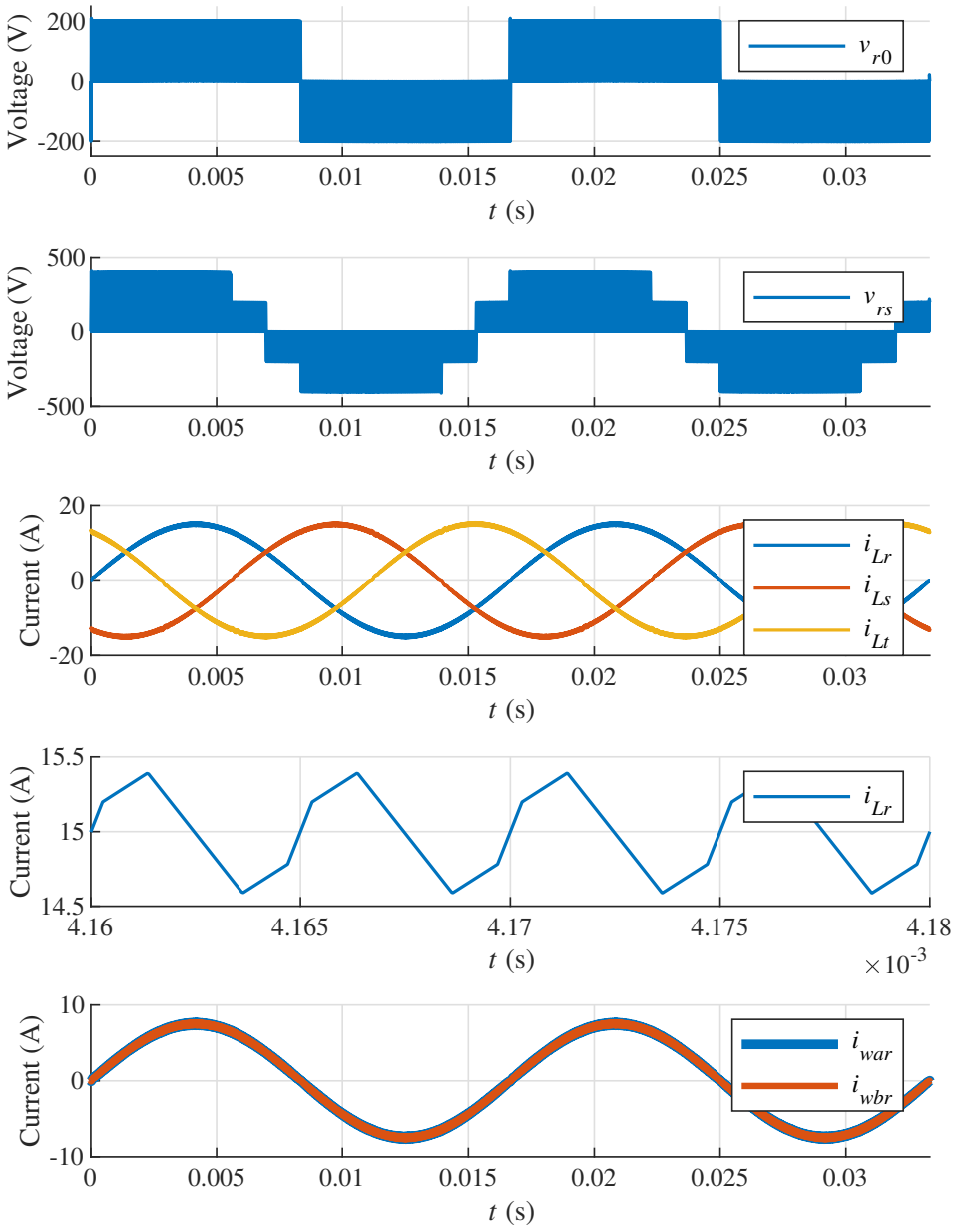
The MSSC provides an input current with low harmonic content because the switching frequency seen by the inductor is multiplied by two and also due to the multilevel characteristic of the converter input, which reduces the voltage level on the inductors. The phase and line voltages, inductor currents and ICT currents in phase a are shown in Fig. 122. The inductor current presents a high frequency ripple around 0.75 A at $\pi/2$, while the theoretical ripple value for the simulated parameters is 0.744 A. In Fig. 122 it can also be noticed that the current in the windings is half the total input current.

Fig. 121 – Simulation results of the three-phase AC-DC topology - Rated power.



The SC cell increased the converter voltage gain and divided the output voltage between the output capacitors. Since the three-phase rectifiers input power is constant, the output power does not present low-frequency ripple. Some low frequency ripple still occurs across the cell capacitors due to the duty cycle variation, that affects their charge and discharge. However, the equivalent resistance of the cells in each phase vary according to their respective duty cycle, in a way that the equivalent resistance variation in one phase does not affect the total output ripple and do not cause voltage imbalances. Furthermore,

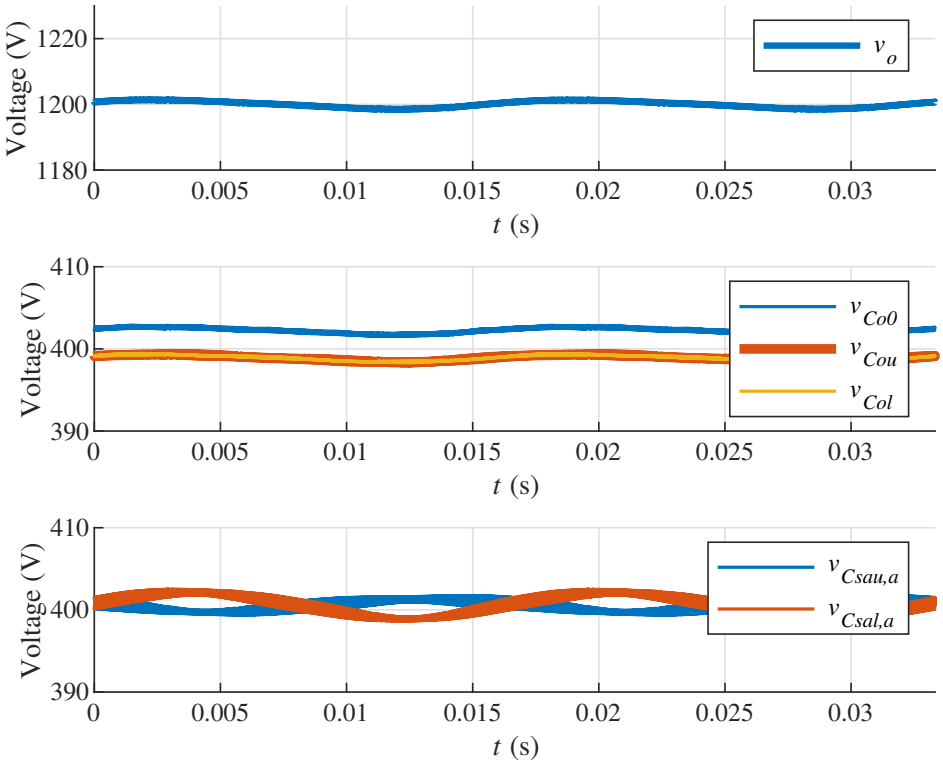
Fig. 122 – Simulation results of the three-phase ac-dc topology - Phase and line voltages and current in the inductor and ICT.



as seen in chapter 2, the equivalent resistance variation as a function of the duty cycle is low when the duty cycle value is near 0.5, which is the case of three-phase rectifiers. Due to the symmetry in the switching cell, the upper and lower capacitors have the same average voltage value, which can be seen in Fig. 123.

Because the total output voltage is divided between the capacitors, the maximum voltage across the semiconductor devices is also a fraction of the total output voltage.

Fig. 123 – Simulation results of the three-phase AC-DC topology - Voltage across the capacitors of leg a.

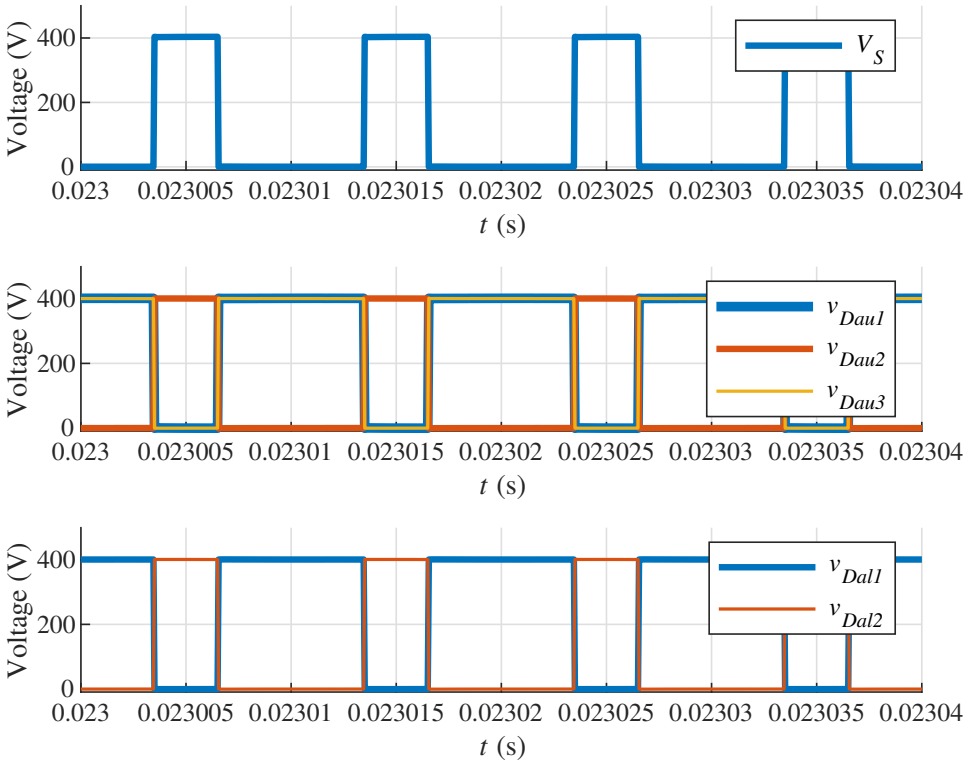


The voltages across the switches and diodes of phase r and leg a are shown in Fig. 124. This figure shows the voltage stress during the entire grid cycle does not vary, since the output voltage and the capacitor voltages are dc.

The ICT divides the total input current between the converter legs, so that faster switches with lower losses can be used. This can be seen in Fig. 125, that shows the diode and switch currents in the grid period for phase r and leg a. Fig. 126 shows the currents during the switching period, where the SC cell influence on the current and its non-linear aspect can be seen. The simulated switch RMS current is 4.12 A, whereas the theoretically calculated current is 3.9 A. The difference is due to the non-linear capacitor charging and discharging currents.

The SC cell is usually designed to operate in the partial charge mode. Fig. 127 shows that with the design methodology that was adopted in this work the cell operates near total charge mode, which is a mode that increases the converter losses. However, by operating in this region, the converter energy density can be improved by using smaller capacitors. Furthermore, in the methodology that was shown in chapter 2 the capacitor size is based on a point in the curve where the equivalent resistance starts increasing significantly for lower capacitance values, and in this method there is no need to specify the operation mode. The method is used to verify a more suitable point of operation that balances losses, cost and volume. The simulated equivalent resistance of one leg is around 7 Ω when $d = 0.5$, which is acceptable, considering that the three-phase rectifier output impedance for the rated operation point is 360 Ω and the total output current is divided

Fig. 124 – Simulation results of the three-phase AC-DC topology - Voltage stress across the switch and diodes of leg a.



between the six legs of the converter.

The converter was controlled by cascaded loops, an outer voltage loop and an inner current loop. The Clarke transform was used to uncouple the phases in the model and control the three-phase currents, as shown in the control block diagram illustrated in Fig. 128. To evaluate the converter control, load steps were applied from full load to 50% and vice-versa. The output voltage was regulated and, like the other topologies, the capacitor voltages remained balanced without additional control loops, as seen in Fig. 129.

Fig. 125 – Simulation results of the three-phase AC-DC topology - Current stress in the switch and diodes of leg a during the grid period.

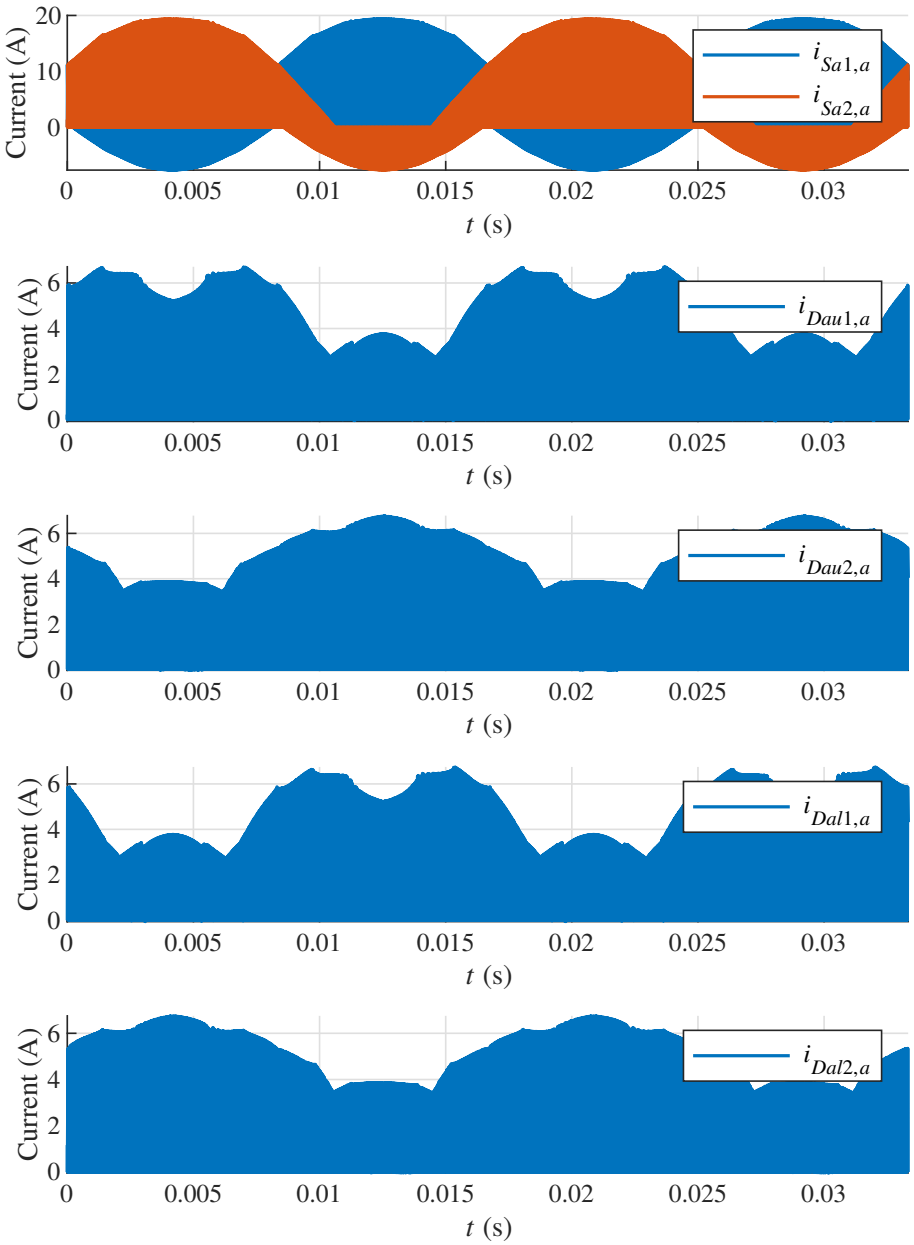


Fig. 126 – Simulation results of the three-phase AC-DC topology - Current stress in the switch and diodes of leg a during the switching period.

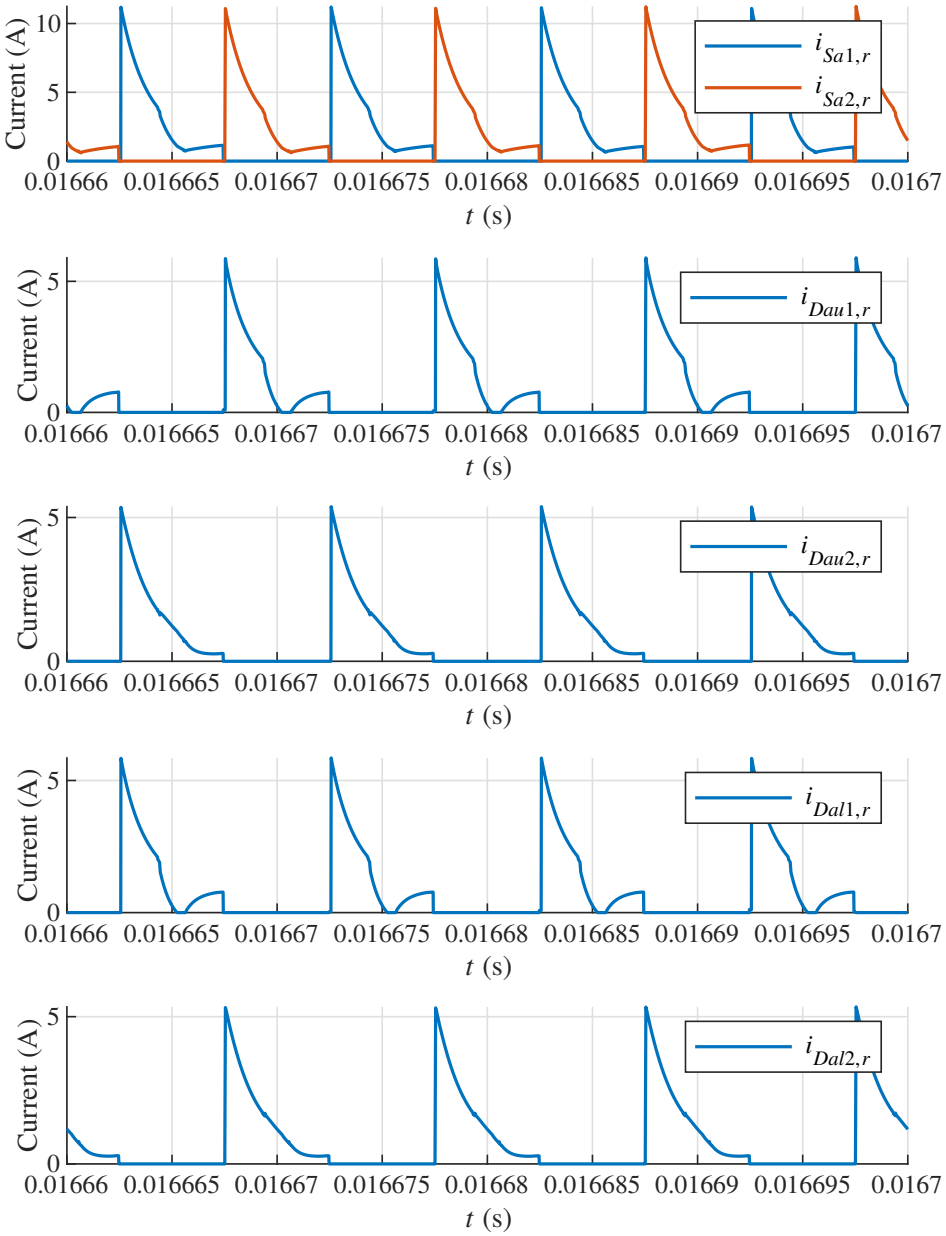


Fig. 127 – Simulation results of the three-phase AC-DC topology - Current in the cell capacitors of leg a.

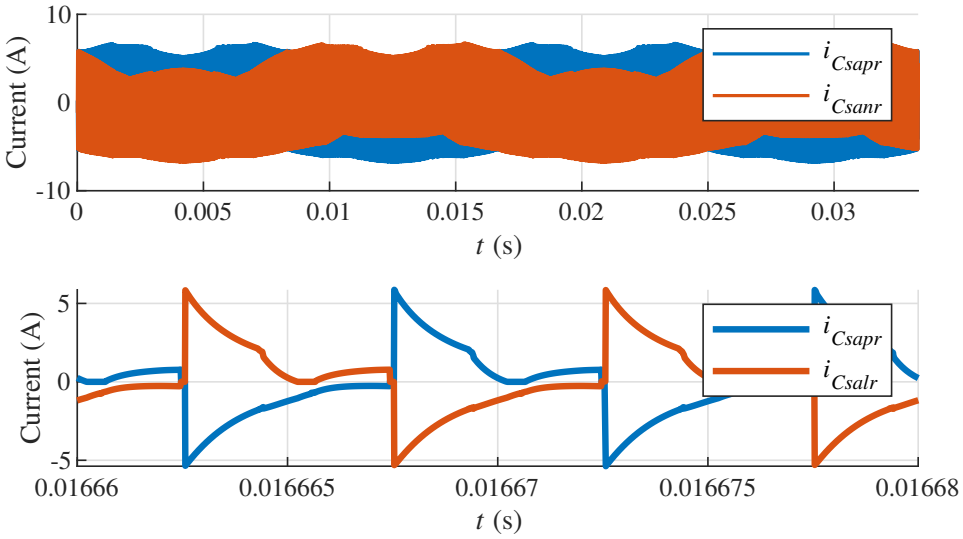


Fig. 128 – Block diagram of the three-phase controller.

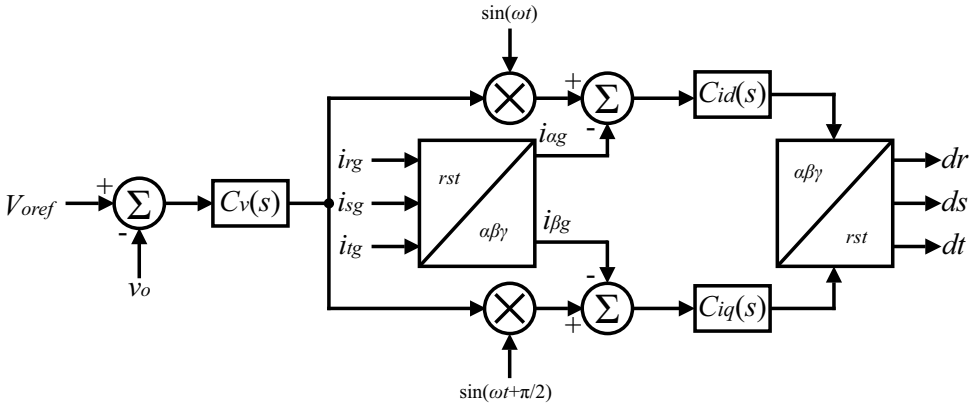
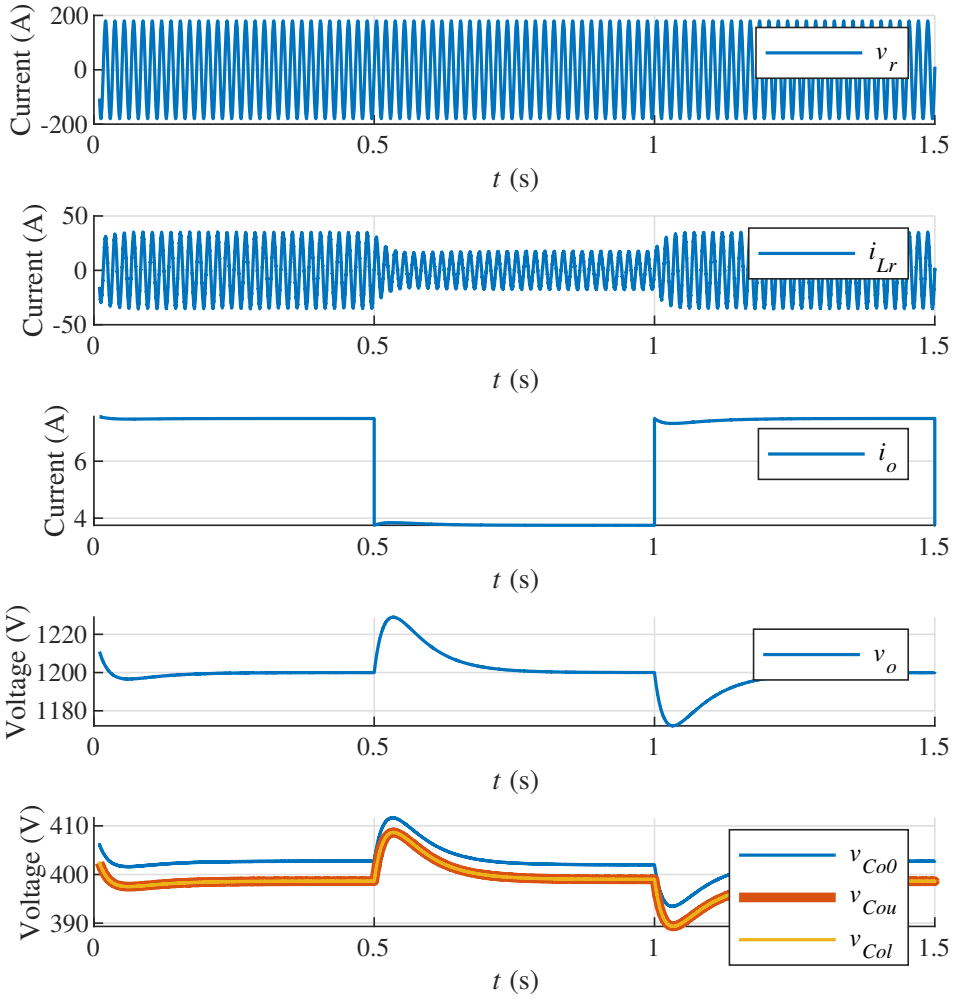


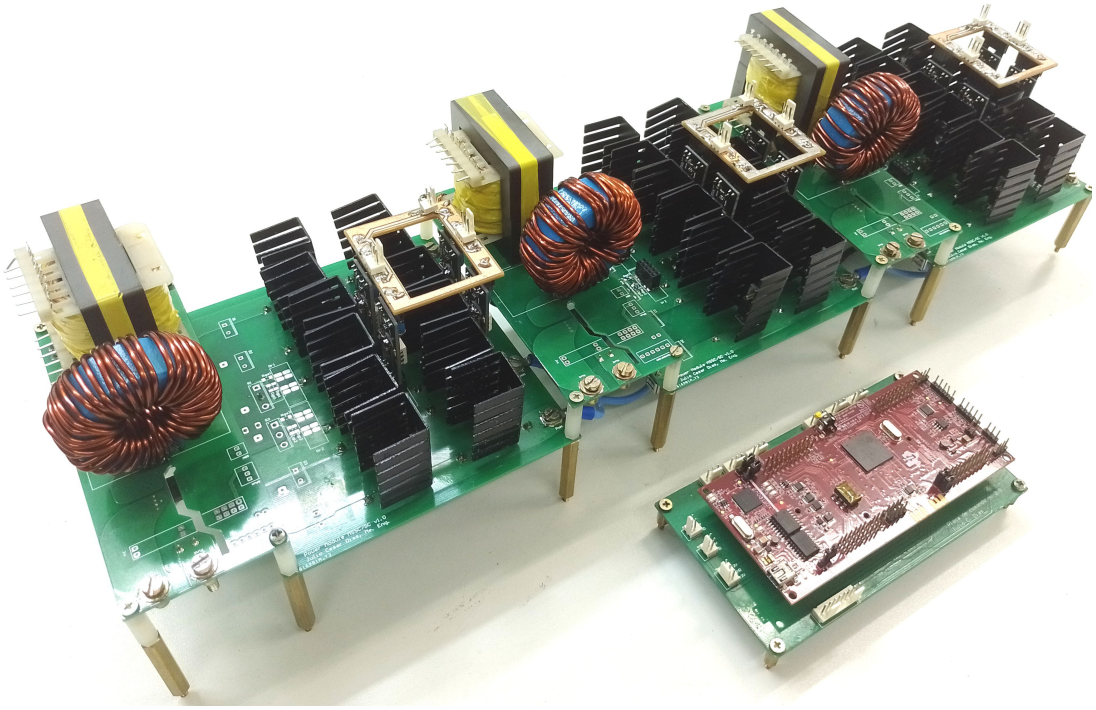
Fig. 129 – Simulation results of the three-phase AC-DC topology - Load step response.



5.8 EXPERIMENTAL RESULTS

A prototype was built to evaluate the converter herein proposed. The prototype was made with three modules of the dc-dc converter. The difference is that the first upper diode in each leg is replaced by an active switch to provide a bidirectional switching cell. By connecting the output capacitors the three-phase topology is built. The photograph of the prototype is shown in Fig. 130, its power density is 595 W/L. For presentation purposes, the cables that connect the control circuit to the power circuit were removed from the photograph.

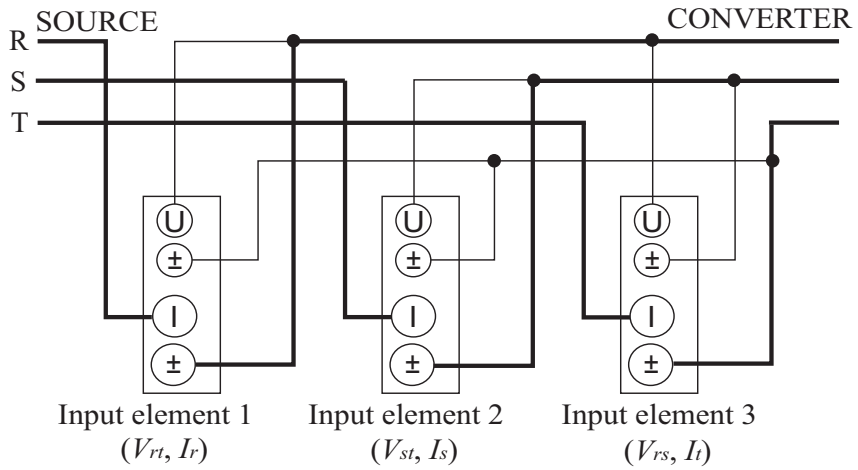
Fig. 130 – Photograph of the experimental prototype of the three-phase ac-dc converter.



Since the converter has three inputs and one output, a Yokogawa WT1800 power analyzer was used to capture the input and output voltage and currents. The power analyzer input is wired according to the scheme suggested by the manufacturer, shown in Fig. 131. The power analyzer can measure up to six voltage and current signals and its maximum input voltage is 1 kV. Three inputs were used to measure the rectifier input and the remaining three were used to read the voltage across each output capacitor. The Element 6 was used to read the output current as well, since it shares the same reference as the output load. Due to the power analyzer wiring, it is important to notice that Element 1 measures V_{rt}, not V_{tr}. The power source used to supply the converter was a California Instruments 6000LS three-phase power supply.

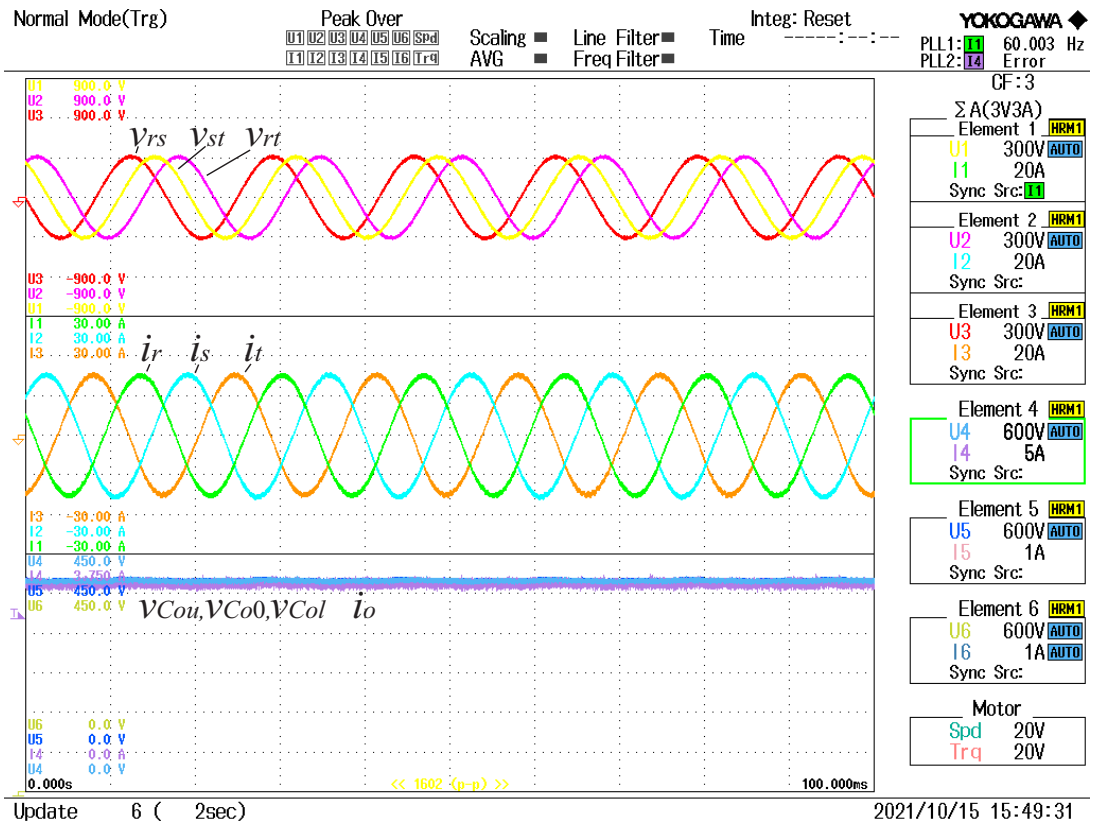
The main voltage and current waveforms were obtained to verify the converter capability to step-up the voltage and provide a high input power factor. The main waveforms are shown in Fig. 132. It can be seen that the voltages on the capacitors overlap because the output voltages are naturally balanced. The input currents follow a sinusoidal shape, showing the PFC capability of the proposed topology. The average output voltages at C_{ou}, C_{o0} and C_{ol} are 400 V, 403.8 V and 400 V, respectively, showing that the converter is capable of naturally balancing the output capacitor voltages. The difference between

Fig. 131 – Yokogawa WT1800 wiring scheme.



the output voltage and $3V_{Co0}$ is lower than 0.99, which means that the SC cell is efficient for this power level. The input power factor is 0.99 and the efficiency at rated power is 96.6%.

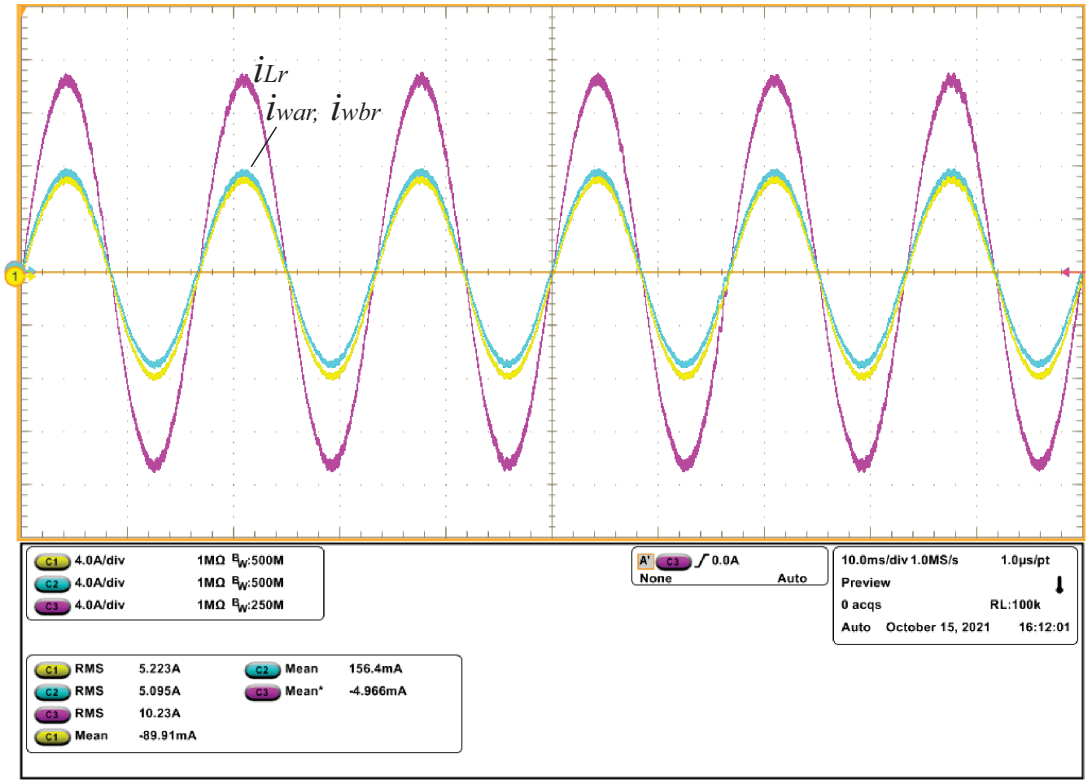
Fig. 132 – Waveforms at rated power level: window1: v_{rt}, v_{st} and v_{rt}; window2: i_r, i_s and i_t and window 3: V_{Cou}, V_{Co0}, V_{Col} and I_o.



One of the advantages of the proposed rectifier is dividing the input current between the windings of the ICT to reduce the current stress in the semiconductor devices. No active current control strategy was used to regulate the current sharing in the devices. However, since the gate drivers are similar, the current is balanced. In Fig. 133 it can be seen that the input current is shared between the windings. There is a small offset

between the currents, which can be due to some current imbalance caused by the lack of a control loop, but can be caused by the offset of the current probe used in this test. In practical experiments it was verified that the main cause of imbalance for the dc-dc modules is differences in the gate drivers. Since the dc-dc modules were designed with symmetrical gate drivers, the three-phase ICT currents were balanced as well.

Fig. 133 – Current sharing in the ICT in phase r.

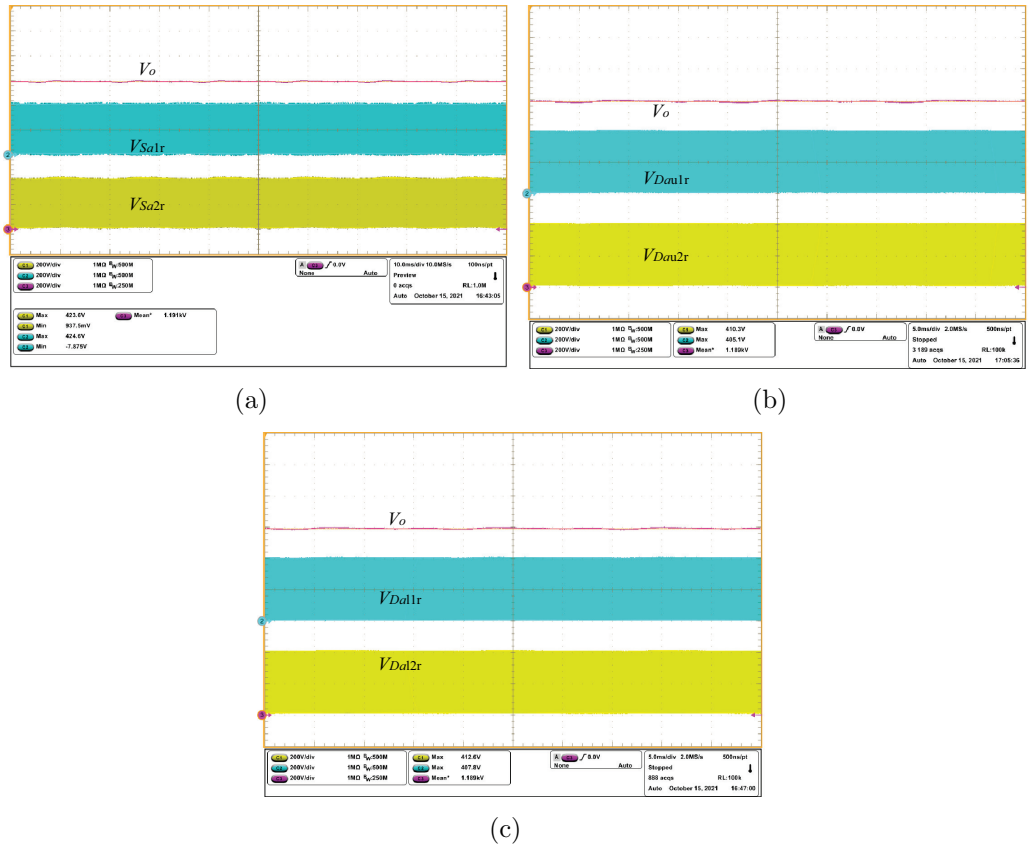


The other major advantage of the proposed topology is that the naturally balanced voltage on the capacitors provides a reduced voltage stress on the switches and diodes. When a semiconductor device is turned OFF, it is connected in parrallel with a capacitor, whose voltage is a fraction of the output voltage, which allows the use of smaller devices higher output voltages. The voltages on the switches and diodes are shown in Fig. 134. The maximum voltage across the switches and diodes are around 400 V, although they reached up to 424 V due to the parasitic inductances in the circuit, that can cause some spikes.

The current in the SC capacitors was verified with a Rogowski probe. Due to its characteristics, the Rogowski probe inserts a 60 Hz harmonic component in the signal, but it is possible to view the shape of the current. In Fig. 135 it can be seen that the amplitude of the currents in the capacitors do not vary as much as in the single-phase ac-dc converter. This happens because the duty cycle of the converter varies around 0.5, which affects the cell capacitor equivalent resistance. Since the modulation index of the rectifier is inversely proportional to the voltage gain, it can be advantageous to use the proposed concept to work in applications with higher voltage gains, such as WECS and other systems that use three-phase generators.

The ladder SC cell can be implemented in different forms. It is common to use a single capacitor on its output to reduce costs or to improve the efficiency. As the output voltage increases, it can be hard to find capacitors for high voltage ratings, therefore

Fig. 134 – Voltage across the semiconductor devices of the three-phase ac-dc converter and output voltage: (a) Switches S_{a1r} and S_{a2r} , (b) upper diodes D_{bu2r} and D_{au3r} and (c) lower diodes D_{al1r} and D_{al2}.



more capacitors may be series-associated to handle the higher voltage. The main issue of associating capacitors in series is the voltage sharing, which is solved by the SC cell configuration used in this work. Other advantage of this configuration is that series capacitors in the output can provide a divided dc-link that could be used as the input for multilevel converters. To evaluate this feature, the output load was divided between the capacitors as shown in Fig. 136.

It is possible to achieve balanced output voltages with loads connected to each output capacitor. Due to the SC natural characteristic, the balance occurs naturally, but there is a voltage drop between each stage and the voltages cannot be controlled to compensate for slight differences between them. The only to reduce the difference between the voltages is to reduce the losses in each stage, which can be achieved by increasing the capacitances and using switches with lower conduction losses. An experiment was performed where each output capacitor supplies a resistive load that consumes one third of the converter rated power. In Fig. 136 it could be seen that the voltages in the outputs was balanced.

In practical applications the output loads vary and can be unbalanced, therefore it is important that the converter is able to provide balanced output voltages. The load for the upper output was changed to consume half of the power that the other loads consume. It can be seen in Fig. 138 that the output voltages are still balanced, but there is a slightly lower difference between the voltage in the intermediary capacitor and the upper capacitor if compared to the difference between the inner output and the lower output. This occurs

Fig. 135 – Current in the input inductor L_R and cell capacitors C_{sur} and C_{slr}.

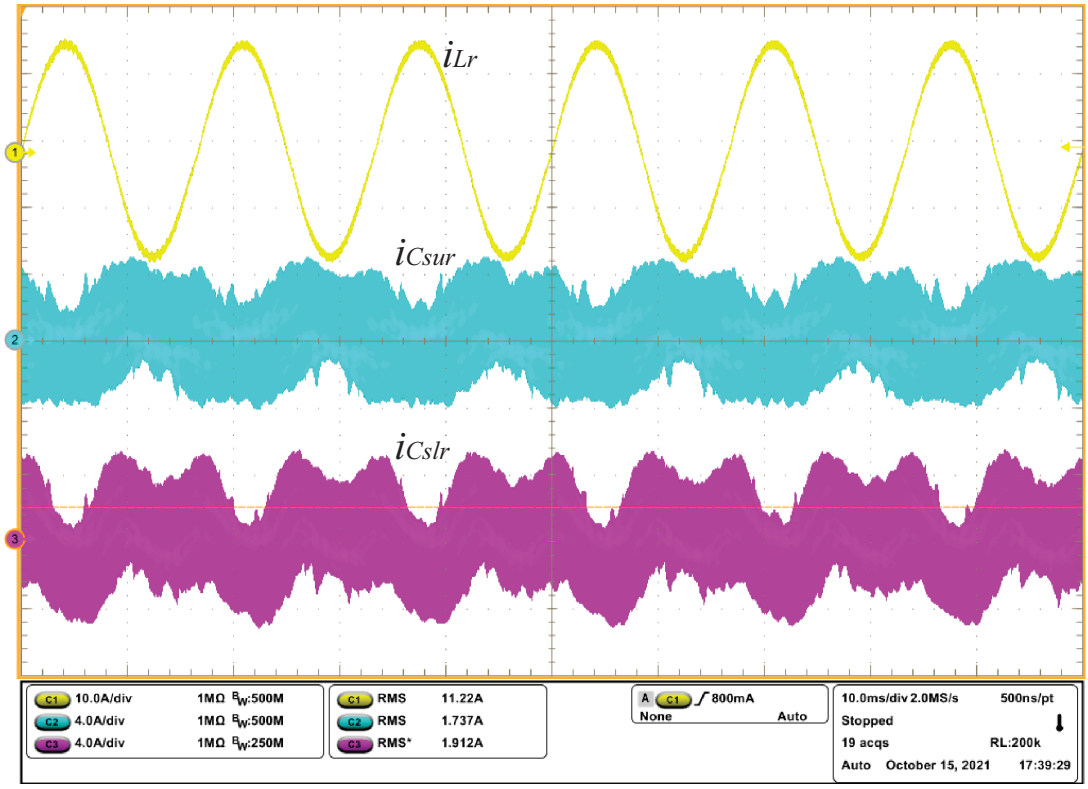
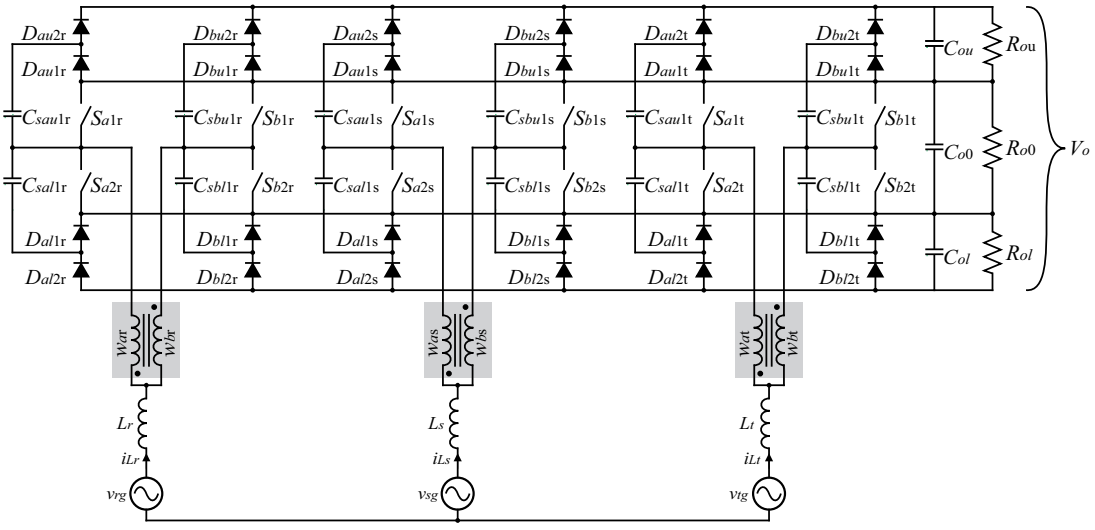


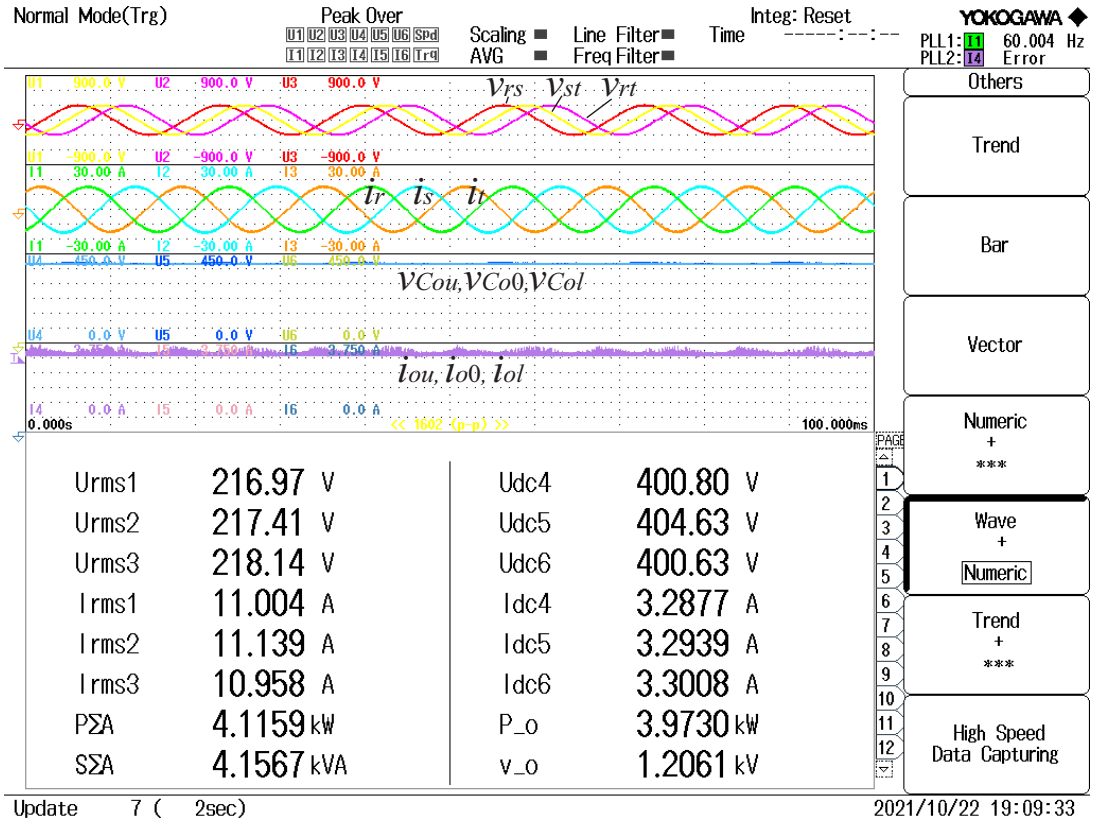
Fig. 136 – Diagram of the tested converter with the load shared between the output capacitors.



because of the SC characteristic, which reduces the equivalent resistance as the output current reduces as well, this results in a lower voltage drop.

The proposed converter is controlled to provide high input power factor and output voltage regulation. To validate the converter control, a 50% load step was applied to the output to verify if the converter is able to regulate the output voltage. In Fig. 139 it can be seen that the voltage on all output capacitors is regulated during the steps. Unfortunately, due to setup issues, it was not possible to perform an abrupt step, a small ramp can be seen in each step and that is due to the mechanical switch available to perform this test,

Fig. 137 – Three-phase ac-dc converter with balanced loads shared between the output capacitors.



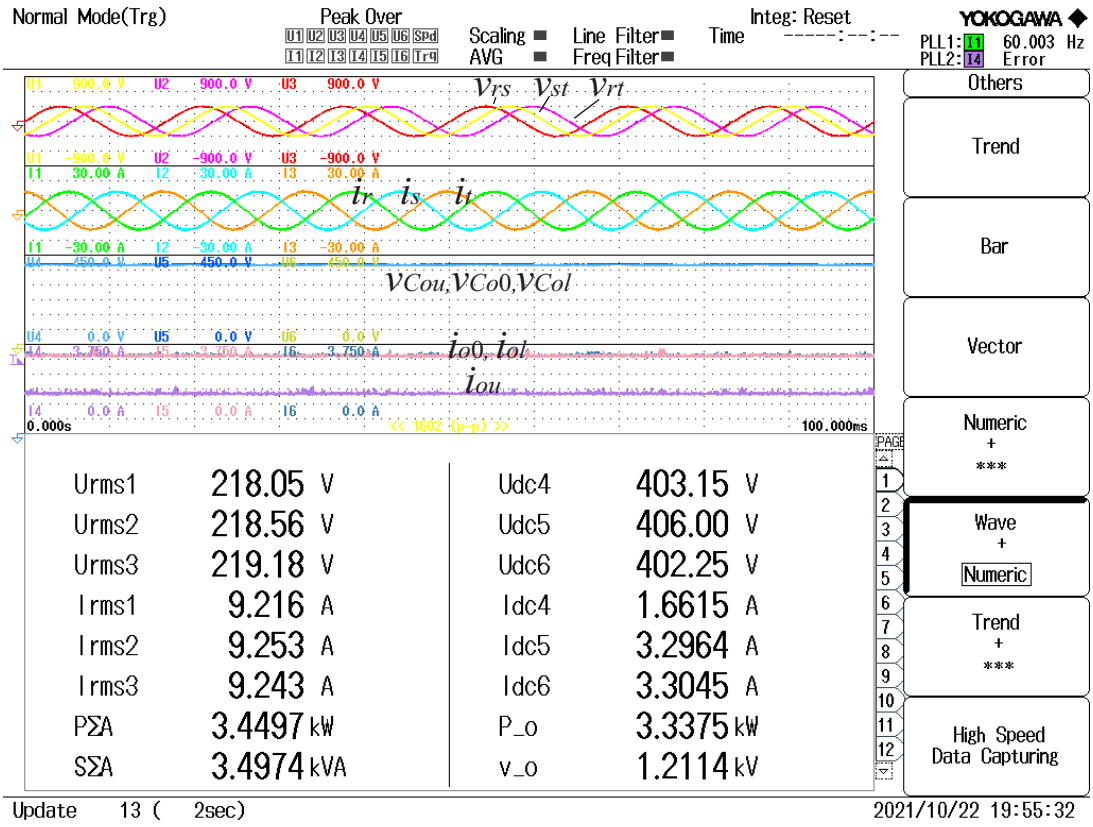
that was not adequate to the voltage and current levels of the prototype. However, it was possible to see that the controller was able to handle output load variations. This test was performed with a single load in the converter output.

The same test was also applied to the converter with shared loads at the output, where a load step was only applied to the upper output. It can be seen in Fig. 140 that the capacitor voltages are balanced and that all output capacitors are affected in the same was by the dynamics. This occurs because the input rectifying stage compensates all outputs by delivering energy to C_{o0}, while the other capacitors receive energy through the SC cell from the inner stage. If more SC cells are added, the same should happen, because the energy is delivered in stages, like a ladder, as in the name of the SC cell that is used in this work.

To evaluate the input current control, the harmonic content was compared to the international standard IEC 61000-3-4. In Fig. 141 it is noticed that the converter harmonic content is much lower than the standard requirements, being suited for PFC applications.

Finally, to evaluate the converter applicability, the efficiency curve is obtained. The peak efficiency obtained is 96.9%, which occurs at 2.7 kW, while the efficiency at rated power is around 96.4%. Some changes can be made to improve efficiency, such as optimizing the magnetic design, using larger capacitors to reduce the equivalent resistance and using active switches instead of diodes to reduce the conduction losses caused by their forward voltage. However, most losses in the three-phase converter occurred in the switches and were switching losses, as shows the loss breakdown (See Fig. 143. One way to reduce the switching losses is to reduce the current level on the switch. Reducing the switching frequency should also help reducing the switching losses in conventional converters, but

Fig. 138 – Three-phase ac-dc converter with unbalanced loads shared between the output capacitors.



in SC converters it may increase the capacitor charge and discharge current spikes and actually increase the switching losses. One alternative is to improve the SC cell by either increasing the capacitance or including an inductor in series with the capacitors to create a resonant circuit and switch at a lower current.

Fig. 139 – Load step applied to the output of the three-phase rectifier.

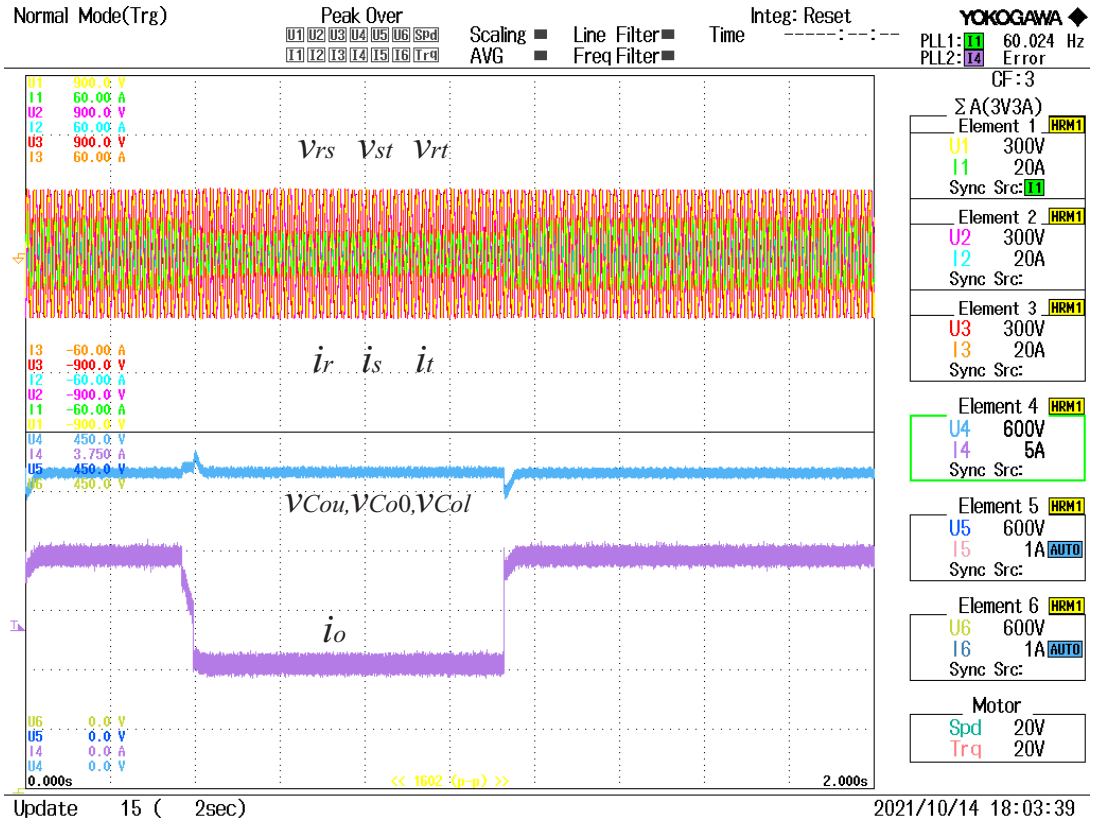


Fig. 140 – three-phase ac-dc converter with unbalanced loads shared between the output capacitors.

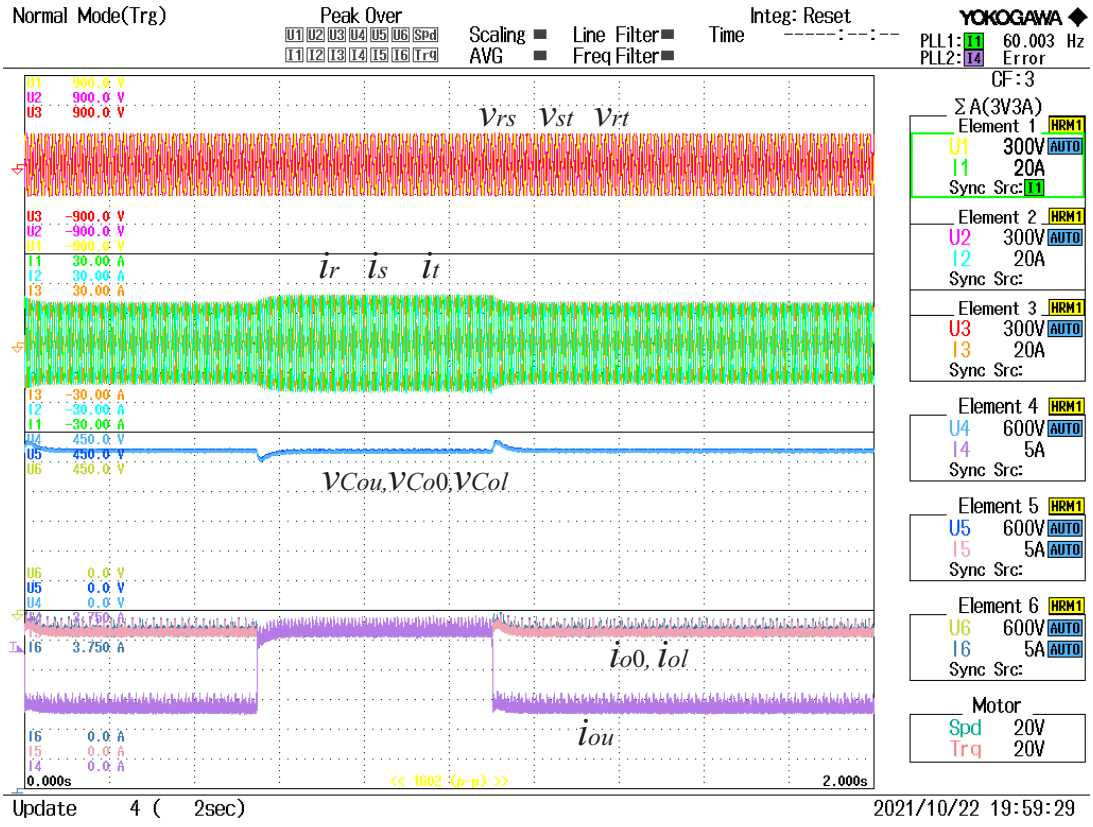


Fig. 141 – Harmonic spectrum of the three-phase ac-dc converter.

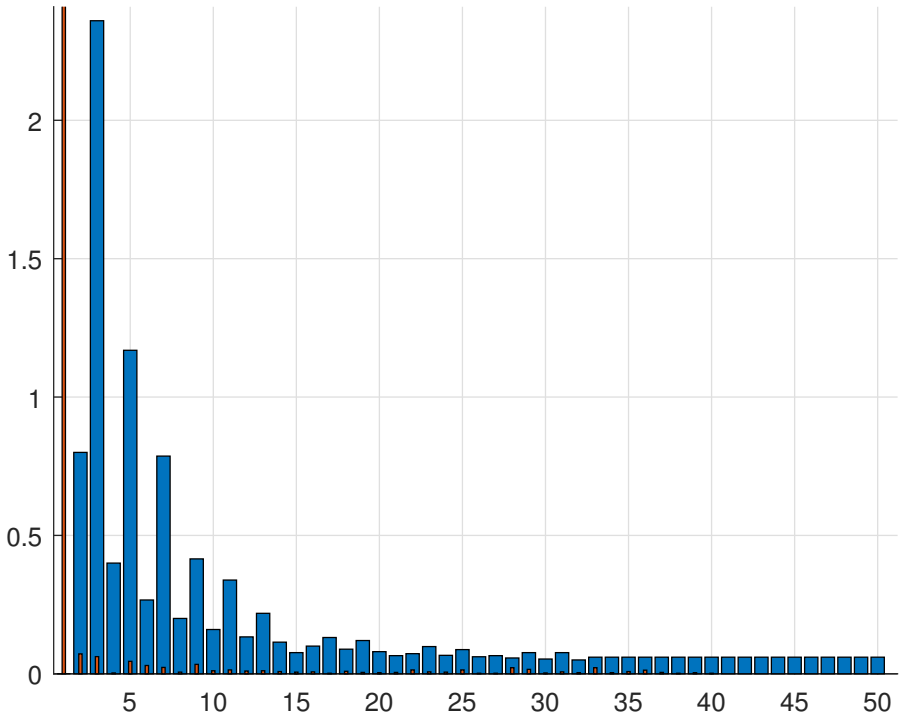


Fig. 142 – Efficiency curve of the three-phase ac-dc converter.

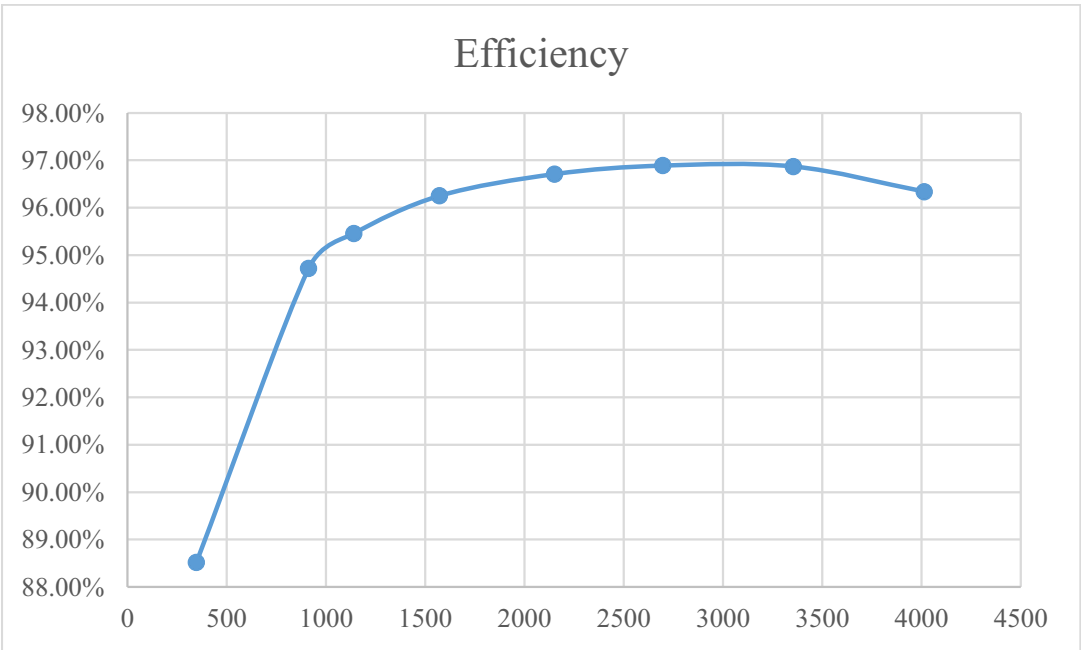
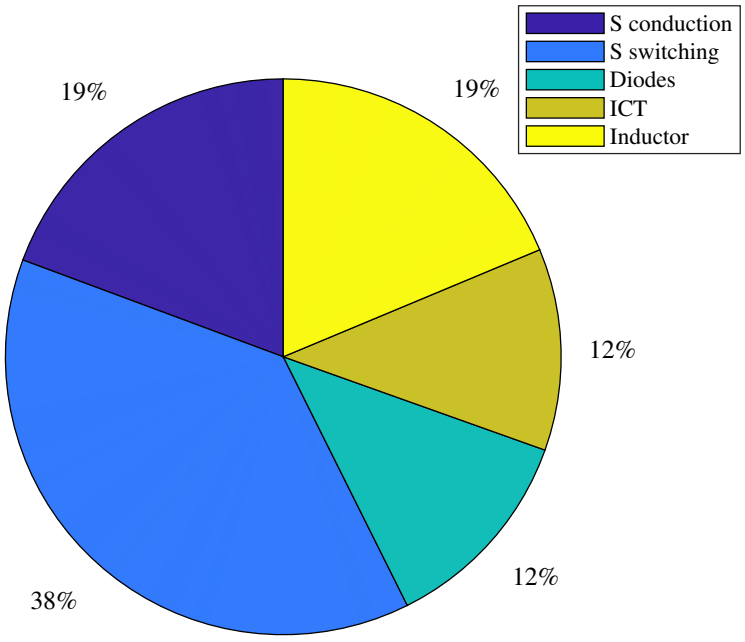


Fig. 143 – Loss breakdown of the three-phase ac-dc converter.



5.9 SUMMARY

In this chapter the theoretical analysis, simulations and experimental results of the three-phase topology were presented to evaluate the proposed concept. The topology presents the low voltage and current stress advantages and is suitable for higher power levels because of its three-phase characteristic.

The operation principle, steady-state and dynamic analysis were presented. An equivalent circuit of the SC cells with a center-tapped autotransformer was used for a simplified analysis of the SC cell, which can be complex due to its many elements. One of the advantages observed in the analysis is the multilevel characteristic of the three-phase rectifier due to the nature of the MSSC.

The input current dynamic analysis was performed by considering the equivalent circuit and the sliding average voltage value at the point the input filter is connected to the MIA. The Clarke transform was used to model the dynamics of the rectifier due to the implementation simplicity, since it does not require PLL or trigonometric calculations in the DSP.

Since the three-phase rectifier presents constant input power, the output voltage ripple can be could be neglected for sizing the capacitors. Therefore, the equivalent resistance criterion presented in Chapter 2 was used to design the output capacitors. An equivalent capacitance was used to perform the output dynamic analysis, thus simplifying the total circuit.

Simulation results showed that the converter provided a higher gain for the same modulation index as in the conventional boost three-phase rectifier. The MSSC and SC cells provided lower voltage and current stress across the switches and lower input current ripple. The same conclusion was verified in the experimental results, which were performed with semiconductor devices rated for 600 V in a converter with a 1200 V output voltage.

The simulations and experiments showed that the converter con provide a regulated output voltage with near unit power factor and low input current harmonic content, being compliant to international standard guidelines. The capacitor voltages are self-balanced during a load step and, even with a low output capacitance, the voltage transient peaks did not reach destructive levels for the switches and diodes.

One aspect of the SC cell that was chosen, the ladder cell, is that it can be implemented with multiple outputs. The output voltages are naturally balanced, but there is a slight voltage drop between the inner and the outer capacitors of the cell due to the equivalent resistance of the SC cell. This could be verified in practice as a reduction in one of the outer loads reduced the voltage drop, since there is less current and lower losses in the circuit.

Even though there are losses which cause a slight voltage drop in outer capacitors, the converter still could suit applications with series input supplies, since the difference is low and can be reduced by increasing the capacitance and reducing semiconductor losses in the circuit. It was verified that a load step at the output still maintain the capacitor voltages balanced, and this occurs as well if the output is divided with unbalanced loads. This balance occurs naturally without using extra control loops.

One of the disadvantages of the topology that was studied in this chapter is that its minimum capacitor voltage should be higher than the line-to-line voltage. However, this concept can be expanded into multilevel converters, as shown in Chapter 1, which could also improve the efficiency of the converter and require smaller input filters to reduce the

input harmonic content.

6 CONCLUSIONS

In this work the concept of integrating multistate switching cells and switched-capacitor cells in dc-dc converters was presented and then expanded to ac-dc converters as an alternative for high conversion ratio with reduced stress on the semiconductor devices. Through theoretical analysis, simulations and experimental verification it was shown that the proposed converters are capable of achieving higher voltage gain than the conventional boost converter and the conventional boost rectifier.

With the use of multistate switching cells it was possible to divide the input current component between switches while increasing the frequency as viewed by the input filter. No additional control loop was needed to balance the current in the ICT. However, it was verified in practical experiments that non-idealities in the gate driver can affect the current share in the ICT, therefore the design of this converter must take this into account, otherwise active sharing techniques should be used to mitigate the current share issue.

The SC cells provided a low voltage stress across the active switches, while increasing the voltage gain of the converter. The SC cells can be cascaded in a symmetrical way to reduce the number of cascaded stages, which can affect the converter efficiency. Although the SC cells are complex due to the effect of parasitic devices in its efficiency, it could be seen that it is possible to simplify its design with equivalent circuits without affecting the steady-state and dynamic behavior significantly. Although the proposed concept is complex and has many elements, it can be analyzed in blocks, which can be converted to simplified circuits to make its design easier to understand and implement. Even with the simplifications, the theoretical efficiency values are close to the practical efficiency at rated power. This shows that it is possible to use simpler circuits to represent the converters for design purposes.

The ac-dc converters provided input currents with low harmonic content and a controlled output without additional control loops. Although the single-phase rectifier reduced the voltage and current stress in the dc-dc stage, the losses in the diode bridge are a limitation. A slow rectifier module was used at the input of the ac-dc converter and it increased the converter losses significantly. Using the bridgeless topology proposed in the introduction or using a synchronous bridge would reduce the losses.

In the dc-dc converter and the three-phase ac-dc converter most losses were switching losses in the active switches. To reduce them it is possible to increase the number of legs to reduce the instant current, use larger capacitors to reduce the charge and discharge spikes in the SC cell, or explore new topologies with soft switching.

The output characteristic of the Ladder cell integrated to the rectifier was explored in the three-phase converter, where it could be seen that the output can be divided in multiple balanced series outputs. The voltage across the outputs is naturally balanced due to the inherent characteristic of the SC-cell, which associates capacitors in parallel at each switching stage and guarantees that the voltage on the capacitors is the same. It was seen that a reduced output current in one of the outputs reduced the voltage drop as well, showing how the voltage drop in the virtual equivalent resistance affects the voltage share.

All experiments were performed with dc-dc modules associated in different ways to generate the ac-dc converters. It was possible to achieve an output voltage value of 1200 V with 650 V semiconductor devices, since the voltage stress on the switches is one third of the total output voltage. The dc-dc converter provided a voltage gain of 100 to

1200 V, and it was verified that with a higher input voltage it is possible to improve the efficiency and operate at higher power levels with the same prototype. The single-phase ac-dc converter provided a voltage gain of 127 to 1200 V by adding a diode bridge to its input and capacitors to its output. Finally, the three-phase ac-dc converter provided a 220 to 1200 V gain by using three dc-dc modules paralleled on its output.

The three-phase ac-dc converter was tested with a single load at its output and a load for each output resistor. In both cases the converter could regulate the output voltage with balanced capacitor voltages, even though the output loads were not balanced. The voltages also remained balanced when submitted to load disturbances.

One limitation of the topologies that were studied in this work is the incapability to work with a voltage lower than the line-to-line voltage, a common limitation of boost topologies, which can be addressed by integrating the concept to multilevel topologies. The presented concept could be expanded to other types of interleaving topologies and switched capacitor converters, but only its integration in the conventional boost rectifier was presented for conciseness.

The major potentials of the proposed concept are renewable applications and motor drives. The dc-dc converter can be used in photovoltaic or fuel-cell systems to increase the voltage levels and provide energy to the utility grid or loads that require higher voltage levels. The rectifier topologies can be used to extract power from wind energy harvesting systems or to operate as preregulators for multilevel inverters, often used for motor drives. Its output characteristic provides multiple regulated and balanced outputs that can supply either multilevel inverters or dc-dc converters associated in a series-input configuration.

6.1 FUTURE WORKS

The purpose of a doctoral dissertation is not only to draw new conclusions on a new field, but to also introduce a new research field that can be expanded into new works. This work introduced the concept of integrating multistate switching cells with switched-capacitor converters, which is a field that can be expanded in several ways:

- Exploring different ICT associations to increase the number of levels in the MSSC;
- Exploring the use of different SC cells;
- Exploring techniques to reduce the losses in the single-phase ac-dc converter;
- Applying the concept in multilevel topologies to reduce the voltage stress on the devices;
- Using space vector modulation techniques to improve the input harmonic content;
- Evaluating the use of the proposed techniques in converters with slower dynamics;
- Inserting inductors in the SC cell to explore the soft-switching capability of the SC cells;
- Conceiving new topologies to achieve soft-switching in the active switches.

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APPENDIX A – 4SSC implementation issues with commercial cores

The three-main ways of implementing the three-phase ICT with commercial cores are:

1. varying the number of turns in each winding to equalize the self inductances
2. using the same number of turns for all windings and assuming different self inductance values
3. equalizing the self inductances with a gapped core

The first alternative sub-utilizes the core, because the only condition needed to the average magnetic flux be zero is that all windings have the same number of turns, otherwise there is an average flux which requires a larger core.

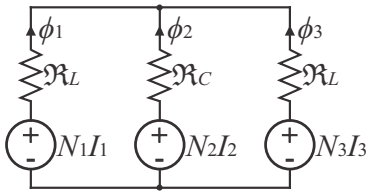
The second alternative is impractical because, as seen in Chapter 3, the ICT dynamics cannot be neglected in the converter transfer function if the self inductances are not equalized.

The third alternative solves the dynamics and average flux issues of the first and the second alternatives. However, it significantly reduces the self and mutual inductances in the ICT, which increases the current ripple in each leg. This might require larger filters and increases the switch current RMS and peak values, resulting in higher switching and conduction losses.

A.1 RELUCTANCE ANALYSIS

To analyze the average magnetic flux in each leg of the ICT, the equivalent magnetic circuit of the three-phase transformer can be analyzed through KVL and KCL. The magnetic circuit is shown in Fig. 144.

Fig. 144 – Magnetic circuit of the three-phase ICT.



Considering a commercial E core, whose lateral legs have half the cross section of the center leg, the reluctance of the legs is given by

$$\begin{cases} \mathfrak{R}_{\boldsymbol{L}} = \frac{2l_{gL}}{\mu_0 A_e} \\ \mathfrak{R}_{\boldsymbol{C}} = \frac{l_{gC}}{\mu_0 A_e} \end{cases} \tag{A.1}$$

where $\mathfrak{R}_{\boldsymbol{L}}$ and $\mathfrak{R}_{\boldsymbol{C}}$ are, respectively, the reluctance of the lateral and central legs of the ICT, $\boldsymbol{l_{gC}}$ and $\boldsymbol{l_{gC}}$ are the air-gap lengths, $\boldsymbol{\mu_0}$ is the vacuum permeability and $\boldsymbol{A_e}$ is the effective area of the core. To equalize the self inductances of a transformer the number of turns or the reluctance must be changed. To equalize the reluctance, either the cross section of the core or the air gap can be modified. Most commercial core are asymmetrical, thus it is not possible to change its area. Commercial gapped cores have an air-gap in the center leg, which can make it possible to equalize the inductance. However,

an air-gap reduces the inductance significantly, affecting the current ripple and the switch losses.

By changing the number of turns, the inductances can be balanced, however, the average magnetic flux in the transformer legs is affected. The average magnetic flux of each leg can be obtained by applying the Kirchooff laws in the magnetic circuit. Considering that the current is balanced between the legs of the transformer, the flux is given by

$$\begin{cases} \langle \boldsymbol{\phi_L} \rangle = \boldsymbol{I_w} \frac{(\boldsymbol{N_L} - \boldsymbol{N_C})}{\boldsymbol{2\Re_C + \Re_L}} \\ \langle \boldsymbol{\phi_C} \rangle = \boldsymbol{I_w} \frac{\boldsymbol{2(N_C - N_L)}}{\boldsymbol{2\Re_C + \Re_L}} \end{cases} . \tag{A.2}$$

where it is noticed that the condition for the average flux to be zero is to have the same number of turns in each leg.

A.2 CURRENT RIPPLE IN THE ICT

The current ripple in the ICT legs can be calculated by analyzing the voltages on its windings, given by

$$\boldsymbol{V_{wi}} = \boldsymbol{L_{ii}} \frac{\boldsymbol{di_{wi}(t)}}{\boldsymbol{dt}} + \sum_{\boldsymbol{j=1 \wedge j \neq i}}^{\boldsymbol{n}} \boldsymbol{M_{ij}} \frac{\boldsymbol{di_{wj}(t)}}{\boldsymbol{dt}}. \tag{A.3}$$

In the 3SSC it is possible to model the transformer with a magnetizing and a leakage inductance, but in three-phase transformers, whose ideal coupling factor is not 1, it is more practical to model it with a magnetizing inductance matrix. The current ripple can be analyzed for one operational stage through the expression

$$\begin{bmatrix} \boldsymbol{L_{aa}} & \boldsymbol{M_{ab}} & \boldsymbol{M_{ac}} \\ \boldsymbol{M_{ba}} & \boldsymbol{L_{bb}} & \boldsymbol{M_{bc}} \\ \boldsymbol{M_{ca}} & \boldsymbol{M_{cb}} & \boldsymbol{L_{cc}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{\Delta i_{wa}} \\ \boldsymbol{\Delta i_{wb}} \\ \boldsymbol{\Delta i_{wc}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V_{wa} \Delta t} \\ \boldsymbol{V_{wb} \Delta t} \\ \boldsymbol{V_{wc} \Delta t} \end{bmatrix}. \tag{A.4}$$

By considering an ideal transformer, the matrix can be rewritten as

$$\begin{bmatrix} \boldsymbol{L_{ii}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} \\ -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & \boldsymbol{L_{ii}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} \\ -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & \boldsymbol{L_{ii}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{\Delta i_{wa}} \\ \boldsymbol{\Delta i_{wb}} \\ \boldsymbol{\Delta i_{wc}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V_{wa} \Delta t} \\ \boldsymbol{V_{wb} \Delta t} \\ \boldsymbol{V_{wc} \Delta t} \end{bmatrix}. \tag{A.5}$$

The resulting system cannot be solved in the way it is currently written because the equations are linearly dependent. It is known that the sum of the instant currents in the ICT is equal to the input inductor current, thus a complementary equation can be substituted in the system to make it solvable, resulting in

$$\begin{bmatrix} \boldsymbol{L_{ii}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} \\ -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} & \boldsymbol{L_{ii}} & -\frac{\boldsymbol{L_{ii}}}{\boldsymbol{2}} \\ \boldsymbol{1} & \boldsymbol{1} & \boldsymbol{1} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{\Delta i_{wa}} \\ \boldsymbol{\Delta i_{wb}} \\ \boldsymbol{\Delta i_{wc}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V_{wa} \Delta t} \\ \boldsymbol{V_{wb} \Delta t} \\ \boldsymbol{\Delta i_L} \end{bmatrix}. \tag{A.6}$$

By using the Gauss-Jordan method the current ripple in the ICT is given by

$$\begin{cases} \boldsymbol{\Delta i_{w1}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} - \frac{\mathbf{2}\boldsymbol{V_{w2}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}}} - \frac{\mathbf{2}\boldsymbol{V_{w3}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}} \\ \boldsymbol{\Delta i_{w2}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} - \frac{\mathbf{2}\boldsymbol{V_{w1}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}}} - \frac{\mathbf{2}\boldsymbol{V_{w3}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}} \\ \boldsymbol{\Delta i_{w3}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} - \frac{\mathbf{2}\boldsymbol{V_{w1}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}}} - \frac{\mathbf{2}\boldsymbol{V_{w2}}\boldsymbol{\Delta t}}{\mathbf{3}\boldsymbol{L_{ii}} \end{cases} . \tag{A.7}$$

Since the ripple in all windings is the same, the total ripple in the switching period can be calculated for each region by summing the ripple values for either all the stages that the switch of a phase is ON or all the stages that the respective switch is OFF. Therefore, the current ripple in each region for a winding of the ICT is given by

$$\begin{cases} \boldsymbol{\Delta i_{wi}^{RegionA}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} + \frac{\mathbf{4}\boldsymbol{d}\boldsymbol{V_o}}{\mathbf{9}(\boldsymbol{m_u}+\boldsymbol{m_l}+\mathbf{1})\boldsymbol{L_{ii}}\boldsymbol{f_s}} \\ \boldsymbol{\Delta i_{wi}^{RegionB}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} + \frac{\mathbf{4}\boldsymbol{V_o}}{\mathbf{27}(\boldsymbol{m_u}+\boldsymbol{m_l}+\mathbf{1})\boldsymbol{L_{ii}}\boldsymbol{f_s}} \\ \boldsymbol{\Delta i_{wi}^{RegionC}} = \frac{\boldsymbol{\Delta i_L}}{\mathbf{3}} + \frac{\mathbf{4}(\mathbf{1}-\boldsymbol{d})\boldsymbol{V_o}}{\mathbf{9}(\boldsymbol{m_u}+\boldsymbol{m_l}+\mathbf{1})\boldsymbol{L_{ii}}\boldsymbol{f_s}} \end{cases} . \tag{A.8}$$

It can be seen that a low transformer self inductance affects a lot the current ripple, which can affect the converter losses. Therefore it is important to have a well designed ICT to implement the 4SSC.

APPENDIX B – Schematic Diagrams

CASO SEJA NECESSÁRIO TRABALHAR COM TENSÕES DE ACIONAMENTO DIFERENTES DESTE PROJETO:

N1 = 6 (Primário)

AJUSTE DA TENSÃO POSITIVA

Secundário: N2 = Vpos*(6/7.5)

AJUSTE DA TENSÃO NEGATIVA

Terciário: N3 = |Vneg|*(6/7.5)

VERIFICAR TENSÃO MAXIMA NO OPTO HCPL3180

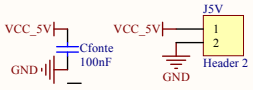
ENROLAMENTOS DO TRAFO:

N1 = 5 (Primário)

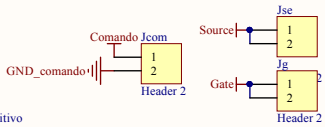
N2 = 18 (Secundário)

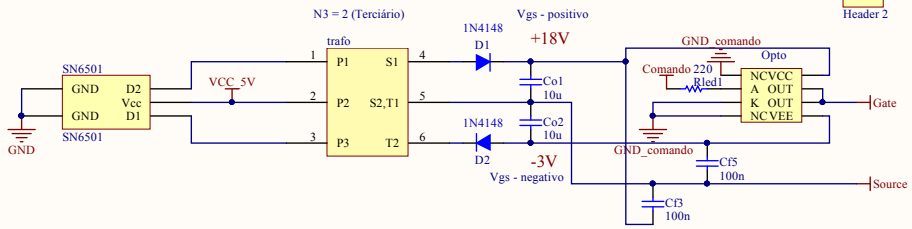
N3 = 2 (Terciário)

ALIMENTAÇÃO DO DRIVER DE 15V



PINOS DOS SINAIS DE ENTRADA/SAÍDA DO DRIVER





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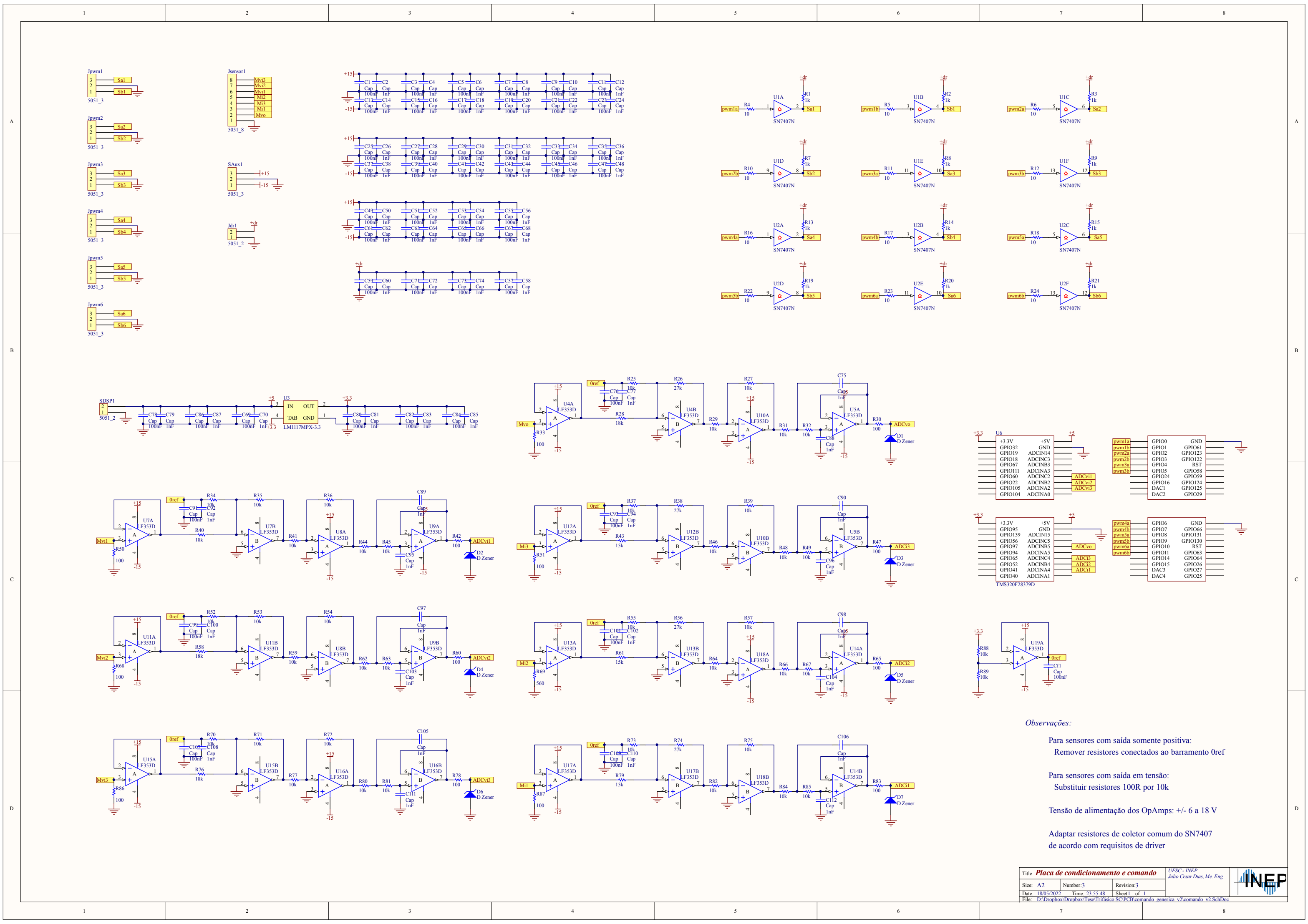
Size: A4	Number: Última modificação - 24/04/2018		Revision: 4
Date: 19/05/2022		Sheet:	of
File: D:\Dropbox\...\Sheet_driver.SchDoc		Drawn By:	Julio Cesar Dias


Observações:
Para sensores com saída somente positiva:
Remover resistores conectados ao barramento 0ref
Para sensores com saída em tensão:
Substituir resistores 100R por 10k
Tensão de alimentação dos OpAmps: +/- 6 a 18 V
Adaptar resistores de coletor comum do SN7407
de acordo com requisitos de driver
Title Placa de condicionamento e comando
UFSC - INEP
Julio Cesar Dias, Me. Eng
Size: A2
Number:3
Revision:3
Date: 18/05/2022
Time: 23:55:48
Sheet1 of 1
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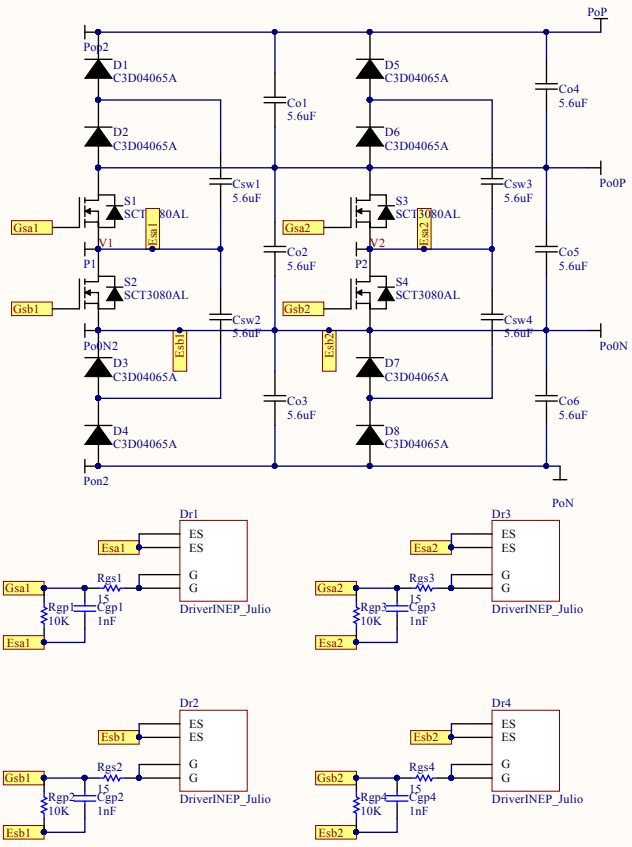

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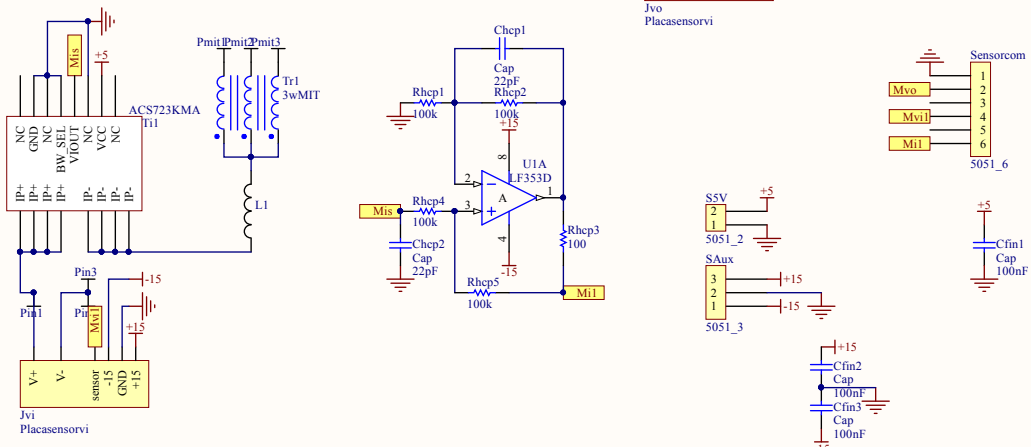
Altium


Mis
+5
NC
GND
NC
NC
BW_SEL
VOUT
VCC
VCC
NC
IP+
IP+
IP+
IP+
IP-
IP-
IP-
IP-
ACS723KMA
Ti1
PmitI
Pmit2
Pmit3
Tr1
3wMIT
L1
Pin3
-15
Pin1
Pin2
Mvi1
+15
V+
V-
sensor
-15
GND
+15
Jvi
Placasensorvi
Chcp1
Cap
22pF
Rhcp1
100k
Rhcp2
100k
+15
8
U1A
LF353D
A
2
3
1
4
-15
Mis
Rhcp4
100k
Chcp2
Cap
22pF
Rhcp3
100
Rhcp5
100k
Mi1
PVo+
PVo-
Mvo
-15
+15
V+
V-
sensor
-15
GND
+15
Jvo
Placasensorvi
Sensorcom
Mvo
Mvi1
Mi1
1
2
3
4
5
6
5051_6
S5V
+5
2
1
5051_2
SAux
3
2
1
+15
-15
5051_3
+5
Cfin1
Cap
100nF
+15
Cfin2
Cap
100nF
Cfin3
Cap
100nF
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19/05/2022
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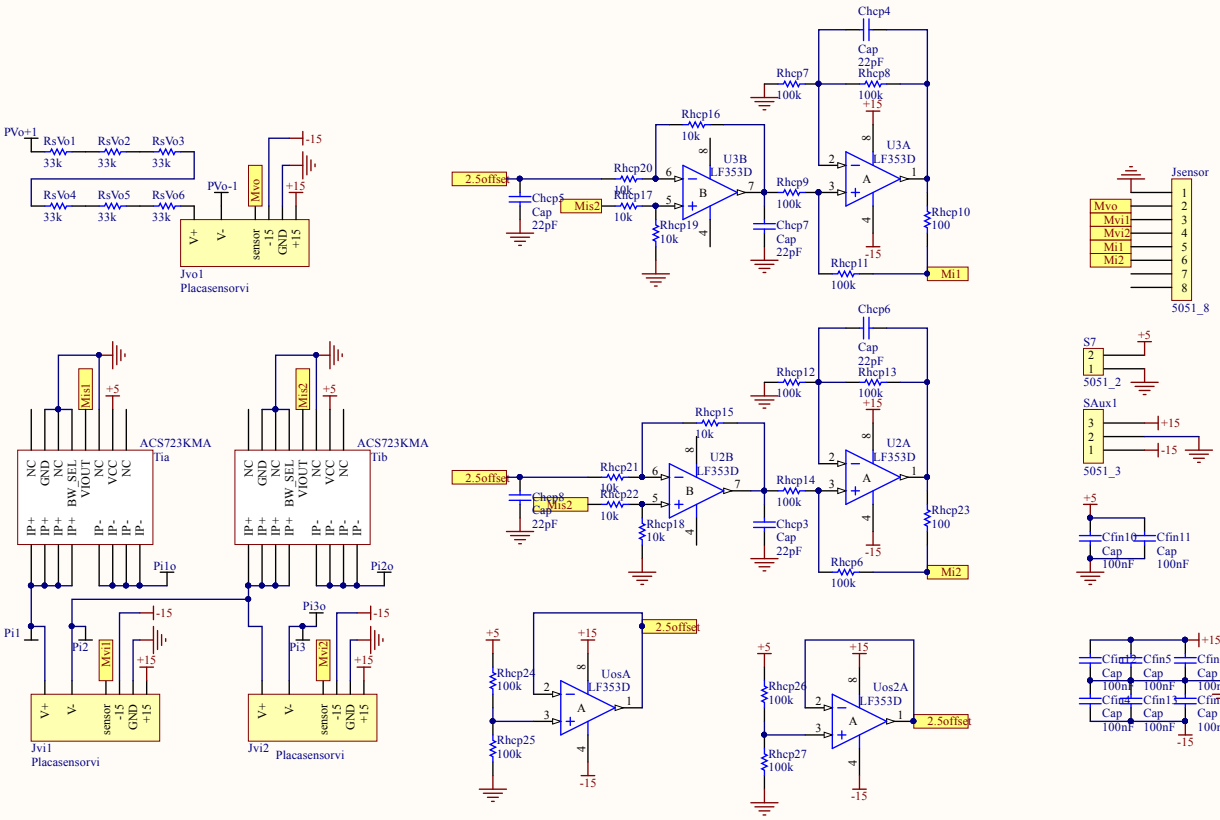

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