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Luís Henrique Rodovalho Moreira de Lima

Analog Artificial Mechanoreceptor

Florianópolis
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Luís Henrique Rodovalho Moreira de Lima

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Prof. Jorge Manuel dos Santos Ribeiro Fernandes, Ph.D.
Universidade de Lisboa

Cosimo Gentile, Dr.
Centro Protesi INAIL

Prof. Jefferson Luiz Brum Marques, Ph.D.
Universidade Federal de Santa Catarina

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Prof. Cesar Ramos Rodrigues, Dr.
Supervisor:

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Dedico esse trabalho a meus pais, Osvaldo e Marta.

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RESUMO

A amputação traumática de membros superiores, especialmente a perda de mãos e dedos, resulta em deficiências severas para suas vítimas, incluso a manipulação de objetos em tarefas do dia-a-dia. Essa partes do corpo podem ser substituídas por próteses, e avanços tecnológicos recentes, dentro de suas limitações, podem até mesmo recuperar o sentido de tato, posição e movimento das mãos. A interface eletrônica entre a prótese e seu usuário pode ser melhorada através da emulação de sensores mecânicos biológicos localizados na pele da ponta dos dedos: os mecanoreceptores. Esta tese propõe e discute o desenvolvimento de mecanoreceptores analógicos artificiais para circuitos integrados, com o objetivo de miniaturizar e aprimorar as interfaces eletrônicas de próteses. Além disso, várias técnicas de circuitos analógicos utilizadas no projeto são propostas, como topologias de amplificadores de ultra baixa transcondutância e tensão de alimentação baseados em inversores.

Palavras-chave: Mecanorreceptor. Processamento analógico de sinais. Amplificadores de ultra baixa transcondutância. Amplificadores de ultra baixa tensão de alimentação. Amplificadores baseados em inversores.

RESUMO EXPANDIDO

Introdução e Revisão Bibliográfica

A amputação traumática de membros superiores, especialmente a perda de mãos e dedos, resulta em deficiências severas para suas vítimas, incluso a manipulação de objetos em tarefas do dia-a-dia. Essa partes do corpo podem ser substituídas por próteses, e avanços tecnológicos recentes, dentro de suas limitações, podem até mesmo recuperar o sentido de tato, posição e movimento das mãos. A interface eletrônica entre a prótese e seu usuário pode ser melhorada através da emulação de sensores mecânicos biológicos localizados na pele da ponta dos dedos: os mecanoreceptores.

Os mecanoreceptores são células sensoriais que respondem e pressão e vibração localizadas nas terminações nervosas da pele de mamíferos. Eles são classificados de acordo com a resposta em função da força aplicada na pele. Caso haja resposta apenas a variação da força aplicada, são classificados com de rápida adaptação (*Fast Adapting*). Caso, além da resposta à variação, também haja resposta para pressão constante na pele, são considerados de lenta adaptação (*Slow Adapting*).

Mecanoreceptores artificiais são alternativas eletrônicas de suas versões biológicas. Eles são geralmente compostos de um transdutor, que converte a força aplicada a sua superfície numa grandeza elétrica, e uma interface com processamento de sinais que traduz os sinais para pulsos de forma análoga à natural, para assim serem melhor interpretados pelo cérebro humano. Pesquisas anteriores desenvolveram interfaces com processamento de sinais digitais, que necessitam um conversor analógico-digital para que o sinal de saída do transdutor seja processado. A proposta dessa tese é um mecanorreceptor artificial com processamento puramente analógico, de forma que não seja necessária conversão intermediária dos sinais para o domínio digital.

Apesar da vantagem de não requerer uma conversão analógica-digital, o mecanoreceptor artificial analógico ainda tem seus problemas resultantes de uma indispensável miniaturização. A mão humana contém milhares de mecanoreceptores biológicos, sendo assim, uma interface eletrônica entre os sensores de uma prótese de mão biônica necessitaria emular o maior número de mecanoreceptores possível e, simultaneamente, ocupar pouco espaço e consumir pouca energia. A implementação desse sistema em um circuito integrado usando apenas circuitos analógicos é inviável considerando técnicas convencionais processamento de sinais analógicos. Essas técnicas convencionais utilizam componentes passivos e, sendo as os sinais biológicos de baixíssima frequência, os componentes passivos utilizariam muito espaço na pastilha de silício e não seria possível a integração eficiente de múltiplos mecanoreceptores em um circuito integrado. Para contornar esse problema, são utilizadas filtros analógicos com componentes ativos de ultra baixa transcondutância, que por sua vez, são explorados e aperfeiçoados nessa tese.

Modelo do Mechanorreceptor

Antes de proceder com o projeto do mecanorreceptor artificial analógico, os modelos empíricos previamente usados de suas versões digitais foram estudados e adaptados para considerar limitações de procesamento de sinais analógicos ausentes no processamento digital. O modelo do funcionamento do mecanoreceptor foi dividido em duas partes: o sub-modelo de transcondução, relativo a transformação da força aplicada numa corrente elétrica, e o modelo dinâmico neuronal, relativo ao comportamento do mecanoreceptor como neurônio.

O sub-modelo de transdução é por sua vez dividido em dois componentes: estático e dinâmico. O componente estático é relativo à aplicação constante de uma força na pele, enquanto o modelo dinâmico é relativo à variação dessa força. Enquanto o componente estático é proporcional à magnitude da força aplicada, o modelo dinâmico é proporcional a sua derivada. A diferenciação pura é uma operação impossível de ser realizada por filtros analógicos, portanto, foi necessário adaptar o modelo para utilizar a diferenciação com ganho finito para frequências infinitas na forma de um filtro passa-alta.

O sub-modelo neuronal foi adaptado do modelo básico de integração-e-disparo com perdas. O modelo original representa a membrana do neurônio como um capacitor em paralelo com um resistor, sendo a tensão da membrana função da corrente de entrada. Um neurônio artificial feito com circuitos analógico utilizando os parâmetros desse modelo necessitaria capacitores e resistores demasiadamente grandes para a implementação em circuitos integrados. Por essa razão, o resistor foi substituído por uma fonte de corrente não-linear controlada pela tensão da membrana, que é mais fácil e eficiente de ser implementada em circuitos analógicos.

Projeto do mecanoreceptor artificial analógico

Levando em consideração o modelo de mecanoreceptor adaptado proposto nessa tese, um protótipo de mecanoreceptor analógico foi projetado e simulado utilizando parâmetros de processo de fabricação reais. Técnicas de polarização direta de substrato foram utilizadas no projeto do transdutor para reduzir a mínima tensão de alimentação do sistema, reduzindo assim a potência consumida.

O processamento analógico de sinais, em especial os filtros passa-alta que implementam os componentes dinâmicos do sub-modelo de transcondução, utilizaram diversas técnicas inéditas desenvolvidas durante a pesquisa: a linearização de trandutores ativos feitos a partir de inversores CMOS e a redução de transcondutância através de espelhos de corrente paralelo-trapezoidal. O modelo neuronal foi feito a partir de um oscilador controlado por corrente composto por um *Schmitt trigger* e uma fonte de corrente substituindo o resistor do modelo de integração-e-disparo com perdas original.

Por último, o sistema completo foi simulado e seus resultados foram comparados com medições de mecanoreceptores biológicos, demonstrando assim a viabilidade do circuito para a fabricação de um protótipo.

Conclusões

Um mecanorreceptor artificial analógico proposto foi descrito, projetado e simulado. As topologias de circuitos analógicos desenvolvidas durante a pesquisa possibilitam a fabricação de múltiplos mecanorreceptores em um único circuito integrado, uma vez que seu uso diminue a área utilizada pelos componentes básicos do sistema com baixo prejuízo de performance. Alternativamente, os mesmos circuitos podem ser adaptados para diversas aplicações que envolvam processamento de sinais biomédicos.

Os mecanoreceptores artificiais são apenas parte de um sistema maior de próteses biônicas e suas interfaces neurais. Trabalhos futuros incluiriam a fabricação do protótipo e sua utilização em estudos e aplicações médicas. Adicionalmente, o mecanoreceptor artificial analógico poderia ser utilizado como interface entre sensores e redes neurais pulsadas.

Palavras-chave: Mecanorreceptor. Processamento analógico de sinais. Amplificadores de ultra baixa transcondutância. Amplificadores de ultra baixa tensão de alimentação. Amplificadores baseados em inversores.

ABSTRACT

Upper limb amputation, in special hand and finger amputations, results in severe disabilities to its victims, including the manipulation of delicate objects in everyday tasks. Those missing body parts can be replaced by prosthesis, and recent advances in technology, within its limitations, can even restore the sense of touch and tactile feedback. The electronic interface between prosthesis and user can be improved by mimicking actual biological mechanical sensors located in the fingertip skin: the mechanoreceptors. This thesis proposes and explains the design of analog artificial mechanoreceptors for integrated circuits aimed at the miniaturization and improvement of prosthesis electronic interfaces. Additionally, several analog circuit techniques needed for its design are proposed, such as ultra-low-transconductance, ultra-low-voltage and inverter-based amplifiers.

Keywords: Mechanoreceptor. Analog signal processing. Ultra-low-transconductance amplifiers. Ultra-low-voltage amplifiers. Inverter-based amplifiers.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND ACRONYMS

ASP	Analog Signal Processing
BMI	Brain-Machine Interface
CCO	Current Controlled Oscillator
CMOS	Complementary Metal-Oxide-Silicon
DIBL	Drain Induced Barrier Lowering
DTMOS	Dynamic Threshold voltage MOSFET
FA-I	Fast Adapting type I
FA-IA	Fast Adapting type I tranconduction submodel A
FA-IB	Fast Adapting type I tranconduction submodel B
FPGA	Field Programmable Gate Array
FSR	Force Sensitive Resistor
Gm-C	Transconductor-capacitance
LIF-A	Leaky Integrate-and-Fire model A
LIF-B	Leaky Integrate-and-Fire model B
MIM	Metal–Insulator–Metal
NMOS	N-type Metal-Oxide-Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-type Metal-Oxide-Semiconductor
SA-I	Slow Adapting type I
SA-IA	Slow Adapting type I tranconduction submodel A
SA-IB	Slow Adapting type I tranconduction submodel B
SNN	Spiking Neural Networks

LIST OF SYMBOLS

τ	Time constant
$u(t)$	Membrane potential
u_{rest}	Membrane resting potential
ϑ	Threshold criterion
u_{rst}	Membrane reset potential
I_{rh}	Rheobase current threshold
I_{leak}	Non-linear leakage current
I_{leak0}	Constant leakage current
R_{FSR}	Force sensitive resistor resistance
G_{FSR}	Force sensitive resistor conductance
I_D	Drain current
I_F	Forward current
I_R	Reverse current
i_f	Forward inversion coefficient
i_r	Reverse inversion coefficient
I_S	Normalization current
μ	Charge mobility
C'_{ox}	Oxide capacitance per unit of area
ϕ_t	Thermal voltage
V_P	Pinch-off voltage
V_T	Threshold voltage
g_{mg}	Gate small-signal transconductance
g_{mg}	Source small-signal transconductance
g_{mg}	Drain small-signal transconductance
g_{mg}	Bulk small-signal transconductance
S_{eq}	Transistor array equivalent aspect ratio
S_u	Single unit transistor aspect ratio
A	Transistor array active area
A_T	Transistor array total area
V_A	Early voltage
I_{Sdio}	Diode scale current
n_{dio}	Diode ideality factor
V_Q	CMOS inverter quiescent voltage
I_Q	CMOS inverter quiescent current
V_{REF}	Reference voltage
I_{BIAS}	Biasing current

CONTENTS

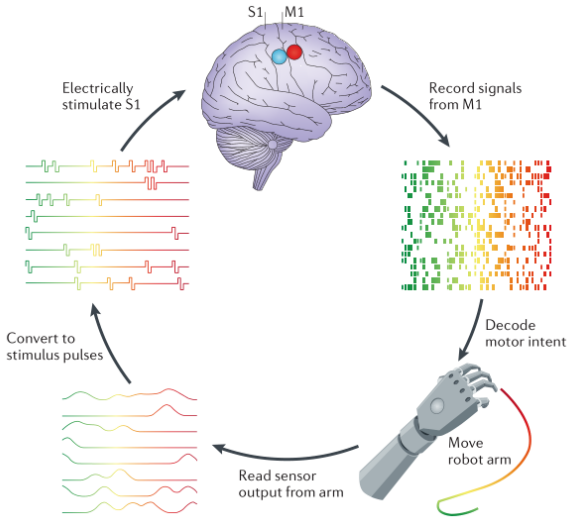
1 INTRODUCTION

1.1 BRAIN-MACHINE INTERFACES

Proprioception (TUTHILL; AZIM, 2018) is the sensation of body position and movement. It is responsible for tactile feedback needed for everyday tasks, as typing, tying shoestrings, holding forks, etc. Accordingly estimates using the 2017 global burden of disease results, in 2017 alone, 57.7 million people were living with limb amputation due to traumatic causes worldwide (MCDONALD et al., 2020). The loss of upper limbs, mostly importantly, the loss of hands, burden its victims' daily lives not only with incredible loss of touch sense, but also the ability to properly manipulate delicate objects.

The use of prosthesis as a replacement for lost limbs is an ancient treatment (FINCH, 2011). With advances in technology, better prosthesis are developed by using robotics (BENSMAIA; MILLER, 2014) to restore not only motor function of lost limbs by user control, but also to restore sensory function responsible for tactile feedback (GEORGE et al., 2019).

Figure 1 – Closed-Loop Brain Machine Interface



Source: (BENSMAIA; MILLER, 2014)

The aforementioned closed-loop sensorimotor control involving tactile feedback, as shown in Figure 1, is a result of Brain-Machine Interface (BMI) (CALDWELL et al., 2019), where a computer (interface) translate the prosthesis (machine) sensors input signals, then stimulates the user brain in a manner it can process this information. Then, the user intentions, coded as brain signals, are decoded by the computer and controls the prosthesis movements, closing the loop with this tactile feedback.

The tactile feedback main advance is the development of intra-cortical microstimulation (FLESHER et al., 2016), which enabled the direct brain stimulation by using

microelectronics, such as the Utah Electrode Array (MAYNARD et al., 1997; NORMANN; FERNANDEZ, 2016) and the TIME electrodes (BORETIUS et al., 2010). This technology enabled real-time sensory feedback using bidirectional hand prostheses (RASPOPOVIC et al., 2014).

Further research (ODDO et al., 2016) improved the artificial touch sense by providing texture feedback. This achievement was result of implementing a better brain-machine interface by properly translating the prosthesis sensor signal. Those signals were improved by emulating actual biological sensors: the mechanoreceptors (JOHANSSON; VALLBO, 1983).

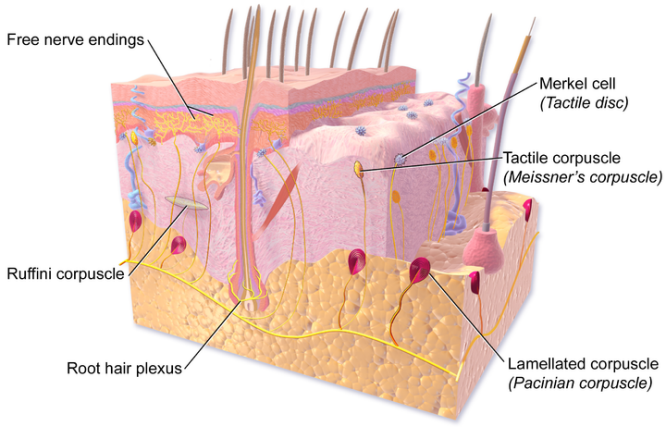
1.2 MECHANORECEPTORS

Mechanoreceptors, or mechanoreceptive units (JOHANSSON; VALLBO, 1983), are tactile sensory cells that respond to mechanical pressure and vibration and are located at nerve endings at the glabrous (hairless) mammalian skin. There are four principal types of mechanoreceptors, as shown in Figure 2: Meissner corpuscles, Ruffini endings, Merkel discs and Pacinian corpuscles. They are classified by the kind of response to a sustained step indentation to skin, as shown in Figure 3. The Slowly Adapting type respond with a sustained discharge as the skin is still pressed, while the Fast Adapting type respond with a burst of impulses only at the onset and removal of the stimulus. They are also classified accordingly to the contrast of the sustained and onset/removal responses: as type I, for large contrast, and type II, for small contrast.

The response of mechanoreceptors located at the fingertips were extensively studied in (BIRZNIEKS et al., 2001). This experiment provided the quantitative results which is the basis of this work. It consisted of repetitive measurements of 196 afferent nerve impulses of various subjects receiving a controlled stimulus. The stimulus consisted of repeated pressure step signals at the fingertips at several angles, as shown in Figure 4. The pressure signal was divided in four phases and varied from 0.2 to 4 N. The first phase was a 250 ms inter-stimulus interval with minimum pressure, followed by a protraction phase characterized by an 125 ms sinusoidal ramp, a plateau phase with a 250 ms sustained signal at maximum pressure, and, finally, a 250 ms retraction phase symmetrical to the protraction phase.

The experiment resulted in the classification of three kinds of mechanoreceptors, two responses reproduced here: Slow Adapting type I (SA-I), shown in Figure 5a, and Fast Adapting type I (FA-I), shown in Figure 5b. The SA-I stimulus response was characterized by a high discharge frequency at the protraction phase, a sustained but slowly decaying frequency at the plateau phase, and almost no response at the retraction phase. Contrastingly, the FA-I stimulus response was characterized by asymmetrical discharges only at the protraction and retraction phases.

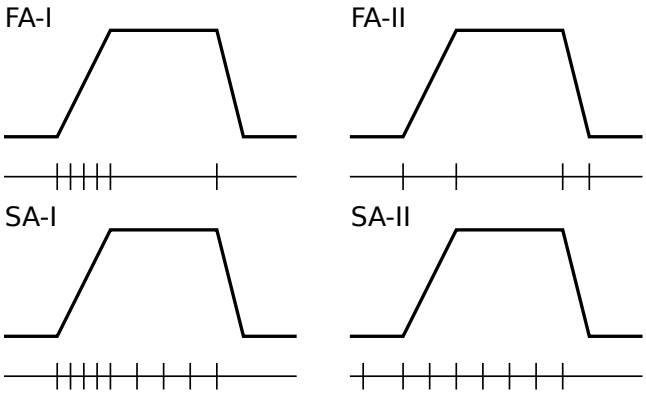
Figure 2 – Tactile Receptors in the Skin: Meissner corpuscles, Ruffini endings, Merkel discs and Pacinian corpuscles



Tactile Receptors in the Skin

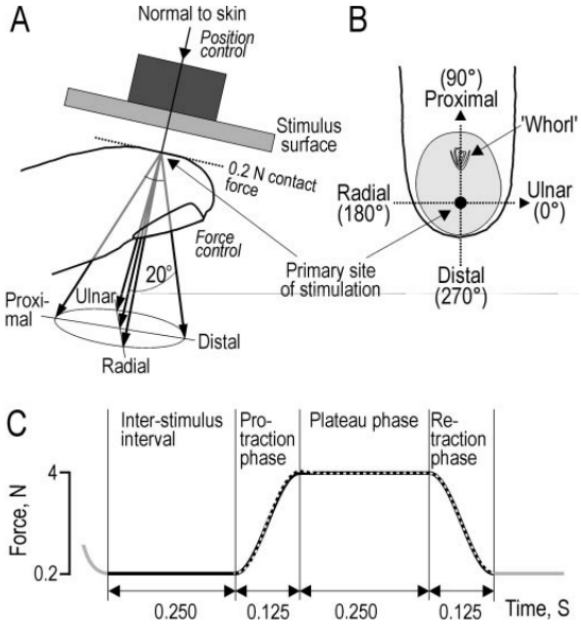
Source: (MEDICAL, 2014)

Figure 3 – Mechanoreceptors classification for accordingly to impulse discharge (lower trace) as result of applied force (upper trace) as function of time



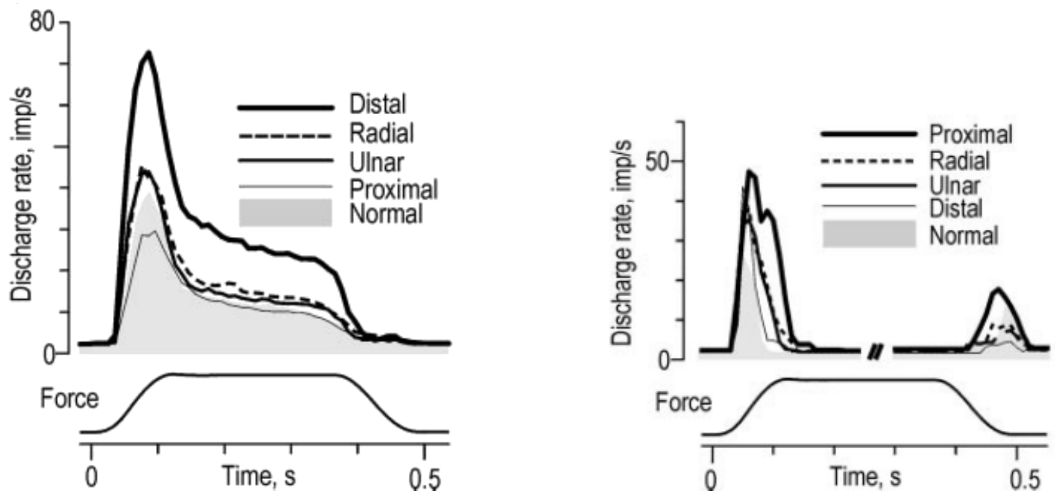
Source: Author, adapted from (JOHANSSON; VALLBO, 1983)

Figure 4 – Mechanoreceptor experiment: forces are applied to the fingertips in five different directions (A) in the selected area (B) with a controlled force $\times$ time profile (C)



Source: (BIRZNIEKS et al., 2001)

Figure 5 – Mechanoreceptors instantaneous discharge frequency as function of applied force

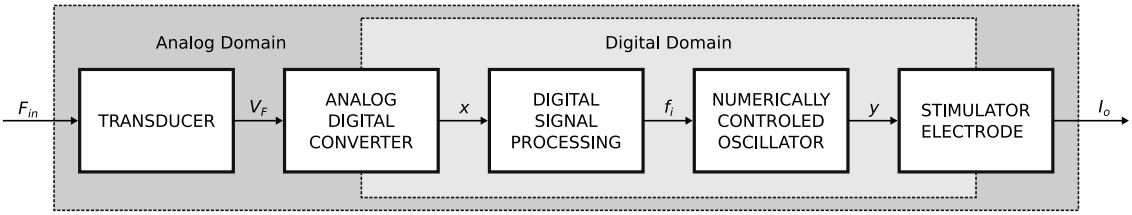


(a) SA-I (b) FA-I

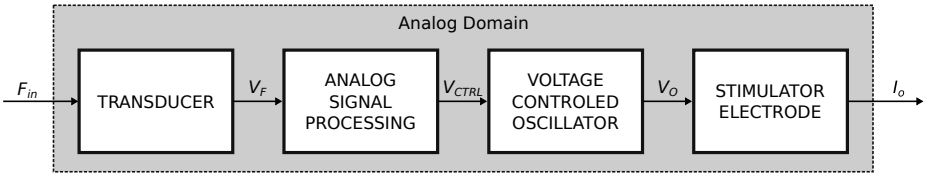
Source: (BIRZNIEKS et al., 2001)

1.3 ARTIFICIAL MECHANORECEPTOR SYSTEM

Figure 6 – Artificial mechanoreceptor system level approaches - (a) mixed-signal approach converts analog signals proportional to the applied force to digital domain before processing, and (b) analog only approach processes signal in the analog domain without any further conversion



(a) Mixed-Signal



(b) Analog only

Source: Author

The biological mechanoreceptor previously discussed could be replaced by an artificial counterpart as long as its output signal could be interpreted by the brain. An artificial mechanoreceptor should be designed using a pressure sensor and transducer to translate the applied force into an electrical quantity (LEE et al., 2019), signal processing units to translate the input signal into a format understandable by the brain (KIM et al., 2012), which is coded as a discharging frequency, and, finally, electrodes to perform brain stimulation (BORETIUS et al., 2010).

Figs. 6a and 6b show the artificial mechanoreceptor mixed-signal and analog only block diagrams. Both approaches have in common the transducer and the electrodes, but differ from each other in how they process the signals. The mechanoreceptor response is modeled by differential equations and non-linear functions (KIM et al., 2012; LEE et al., 2016). The mixed-signal approach first converts the input signal into digital signals with an analog-to-digital converter, process them in the digital-domain accordingly to the mechanoreceptor model, then converts the processed signal back into the analog domain in the shape of electrical pulses, which will then stimulate the brain using electrodes. This thesis proposition is the analog only approach. Its main advantage is that it bypasses the analog-digital conversion by processing the input signal directly in the analog domain.

Both approaches to the artificial mechanoreceptor design has its advantages and disadvantages. The main disadvantage of the mixed-signal approach is the increased

complexity and signal resolution loss due to signal conversion and quantization. However, the analog only approach depends on its design blocks accuracy to process the input signals properly, so it would require a calibration circuit to reduce the inaccuracies introduced by the variability of its analog components. Additionally, the analog blocks non-ideal aspects, such as non-linearity and noise, decreases signal fidelity.

At least, most importantly, the main challenge of both approaches is miniaturization, as the prosthesis sensor element count and density improves (LEE et al., 2015) to reach the human level tactile resolution, which relies on thousands single mechanoreceptors in each hand (JOHANSSON; VALLBO, 1983). One possible solution is to read all sensor elements with a very fast shared analog-to-digital converter and process the results with an almost real-time digital signal processing unit. Another solution is to provide each sensor element its own signal processing unit, analog or digital, to process each one of them in parallel. Considering the analog approach, each unit must be as small and power-efficient as possible to enable lots of artificial mechanoreceptors inside a single integrated circuit. However, this itself is challenging, as it is non-trivial to make the analog filters used in the signal processing units for biomedical signals (ARNAUD et al., 2006).

Additionally, the digital domain signal processing, as done by conventional computers with standard binary logic, does not use the full potential of the mechanoreceptor spike-based signal nature. An analog artificial mechanoreceptor, in theory, could better interact with neuromorphic Spiking Neural Networks (SNN) and analog computing (HAENSCH et al., 2018). Such neural networks based on advanced neuron models (IZHIKEVICH, 2003) were used to categorize naturalistic textures (RONGALA et al., 2015), although by using standard computer architectures to emulate the SNN.

This thesis main objective is the implementation of mechanoreceptor analog only approach as an alternative to existing designs (KIM et al., 2012; LEE et al., 2016). The focus will be in the development of new circuit topologies for transducers, analog processing units and oscillators to reduce supply voltage, power consumption and integrated circuit silicon area. This thesis will not present any stimulator circuits, nor brain signal acquisition and prothesis designs, as it is outside its proposed scope.

1.4 THESIS CONTRIBUTIONS

In order to implement the analog artificial mechanoreceptor, the following topics were proposed and researched:

- Modeling and numerical computation of mechanoreceptors and neurons.
- Analog implementation of previously numerical only artificial mechanoreceptors.

- Voltage amplifier design techniques to increase input and output range, voltage gain and power supply reduction, by using transistor arrays and forward-body-biasing, for the design of force-to-current transducers.
- Inverter-based operational transconductance amplifiers with improved linearity and ultra-low-transconductance, for the design of very low frequency analog filters.
- Schmitt trigger based current controlled oscillators for artificial neuron design.

1.5 THESIS ORGANIZATION

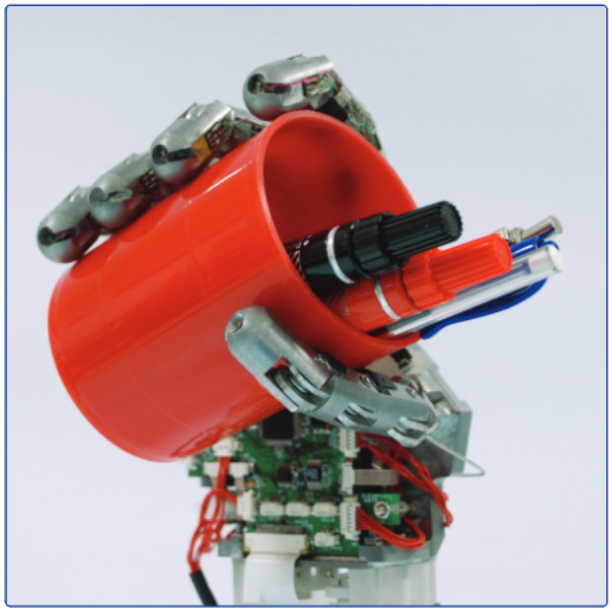
This thesis content is organized as follows. Chapter 2, Literature Review, will briefly discuss present-day prosthesis, sensors and artificial mechanoreceptor development. Also, it will make an overview of ultra-low transconductance amplifiers, a crucial element for analog signal processing design. The following Chapter 3, will explain current mechanoreceptor models and propose small adaptations to include the non-ideal behavior of analog circuits. Chapter 4 will present this thesis proposed artificial mechanoreceptor design, explain each of its circuits and challenges, show simulation results and compare them with experimental measurements available in medical literature. Finally, Chapter 5 will show some conclusions and expectations for future works. Furthermore, several appendices were added to explain in detail the analog circuit techniques necessary for the artificial mechanoreceptor design, such as the inverter-based ultra-low-transconductance and ultra-low-voltage amplifier circuits techniques.

2 LITERATURE REVIEW

2.1 FORCE SENSITIVE SENSOR

An advanced prosthesis, such as SmartHand transradial prosthesis (CIPRIANI et al., 2011) shown in Figure 7, not only replaces the lost limb, but also has sensors to read force, position and temperature signals. Force or pressure sensors are widely available, as they are routinely used in several non-medical applications. The most accurate force sensors are load cells (MULLER et al., 2010). However, conventional load cells are rigid, which is a serious disadvantage for natural skin emulation.

Figure 7 – The SmartHand transradial prosthesis



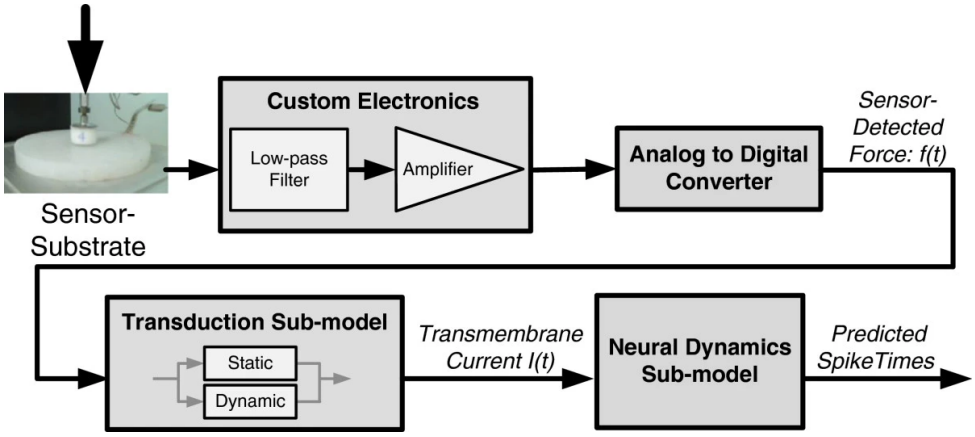
Source: (CIPRIANI et al., 2011)

Another solution is Force Sensitive Resistor (FSR) based sensors. They are already used for grip pressure measurement (JENSEN et al., 1991), and full systems using this approach are commercially available (DEBELISO et al., 2009; TEKSCAN, 2020b) with hundreds of individual sensor elements. Many commercial flexible force sensitive sensors (INTERLINK ELECTRONICS, 2019; TEKSCAN, 2020a) were evaluated (DABLING et al., 2012; PARMAR et al., 2017; SWANSON et al., 2019) and modeled (SCHOFIELD et al., 2016; PAREDES-MADRID et al., 2018). The FSR main disadvantage is its non-linear force-to-conductance gain and hysteresis, which greatly decreases its precision. However, this should not be a serious problem, as the human skin mechanical properties are not linear (WU, J. Z. et al., 2003).

2.2 ARTIFICIAL MECHANORECEPTORS

The SA-I artificial mechanoreceptor system proposed in (KIM et al., 2012) is shown in Figure 8. This work proposed a force sensor in simulated skin and neural model mimic tactile SA-I afferent spiking response to ramp and hold stimuli. This system is composed of a custom electronics block and analog-to-digital converter, which converts the sensor applied force signal into an electrical signal and then converts it to the digital domain.

Figure 8 – SA-I artificial mechanoreceptor system



Source: (KIM et al., 2012)

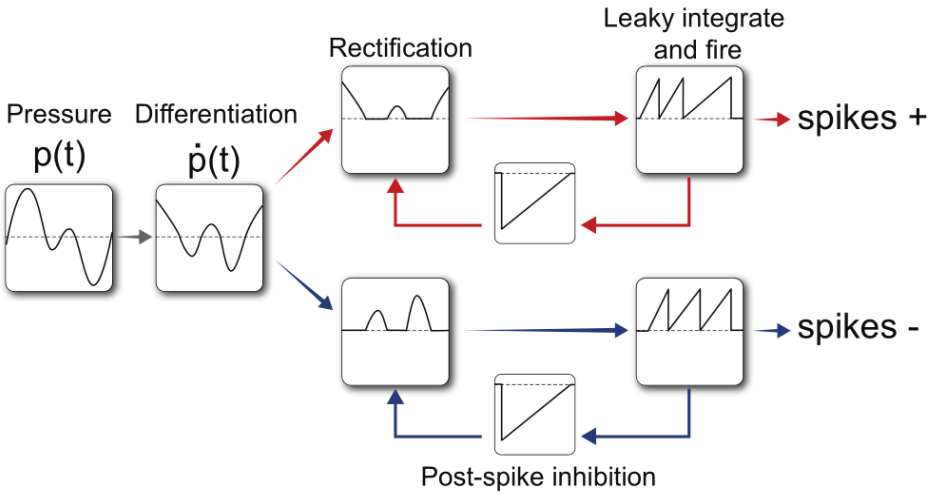
The mechanoreceptor model itself was implemented in the digital domain by digital signal processing. The model was separeted into two sub-models: the transconduction sub-model and the neuronal dynamics sub-model. The transduction sub-model processes the input force signal using two components: the static and the dynamic. The static component is proportional to the applied force while the dynamic component is proportional to the applied force rate of change. The dynamic component models the mechanoreceptor behavior due to the ramp part of the stimuli, which corresponds to the protraction phase of the mechanoreceptor experiment (BIRZNIEKS et al., 2001), as shown in Figure 4 in the previous chapter.

The transduction sub-model feeds the subsequent neuronal dynamics sub-model, based on the simple integrated-and-fire neuron model, which predicts the neuron discharge times based on its electrical current input. This mechanoreceptor parameters were extracted and the system was validated from experimental data acquired from experiments using *ex vivo* mouse skin.

The artificial mechanoreceptor system from (LEE et al., 2016), shown Figure 9, focuses on the FA-I model and its Field Programmable Gate Array (FPGA) implementation. The FA-I mechanoreceptor behavior differs from the SA-I behavior as it does not have a static component. The dynamic component itself is separated in two parts. One as result from the applied force positive rate of change and other based on the

negative rate. This work implements those different component responses by using two distinct neuron model instances, each one with its own parameters. Another key difference from this work to the previous one is that the neuronal sub-model is improved to account for the neuron post spike inhibition, which works as a feedback loop to control the neuron firing threshold. The FPGA design focus intent is to be able to process several sensor units (LEE et al., 2015) in real-time, so the entire system can be useful for brain-machine interfaces (LEE et al., 2019).

Figure 9 – FA-I artificial mechanoreceptor system



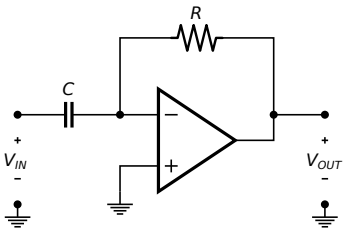
Source: (LEE et al., 2016)

Both artificial mechanoreceptor approaches use numerical computation to model the mechanoreceptor behavior. This thesis, instead, proposes to implement the mechanoreceptor model with analog circuits. The mechanoreceptor dynamic components are modeled as very low frequency differentiators. Those very low frequency differentiators are relatively easy to implement with discrete components, using the ideal operational amplifier based differentiator (SEDRA, A. S. et al., 1998) shown in Figure 10. However, an entire system prototype built this way would have a large size, specially if there would be exclusive analog units for each sensor element. The solution is miniaturization, as all analog units are fabricated in a single integrated circuit. This solution, however, brings another challenge: very low frequency filters on integrated circuits.

2.3 ULTRA-LOW-TRANSCONDUCTANCE AMPLIFIERS

The analog artificial mechanoreceptor should be able to emulate the Slow Adapting (SA) and Fast Adapting (FA) behaviors (Figure 3) by creating a pulse signal with proper instantaneous discharge frequency (Figures 5a and 5b). An analog artificial mechanoreceptor should implement the model differential equations (KIM et al., 2012) with only analog components. The ideal analog differentiator, shown in Figure 10 is

Figure 10 – Operational Amplifier based ideal differentiator



Source: Author

defined by the time constant $\tau = RC$, which should be in the order of miliseconds, accordingly to the model.

To build large time constant filters on-chip is a challenging task because of prohibitive on-chip capacitances required for a few Hz range of operation. Several approaches were proposed in order to reduce the size of capacitors while implementing filters on-chip with large time-constants, hence, such topologies can be classified into two categories: pseudo-resistors (HARRISON; CHARLES, 2003) and Transconductor-capacitance (Gm-C) topologies (YUAN, 2008).

Although very low frequencies can be achieved by using pseudo-resistors, they have an inherent and uncontrolled sensitivity to the Complementary Metal-Oxide-Silicon (CMOS) process variation and bias conditions, implying filter instability due to its poor linearity and high harmonic distortion. On the other hand, Gm-C topologies offer a combination of features like the control of transconductance reduction, power savings, and reduced silicon area through small capacitors size.

Figures 11a and 11b show a passive and an active high-pass filter implementations, respectively. The latter circuit replaces the former one passive resistor with an active load made with an transconductor, so $\tau = C/G_m$. The ideal resistor is a linear device, as it obeys the Ohm's law, and its real world counterpart behaves close enough. The ideal transconductor is also linear, but its real counterpart is made of active devices, such as transistors, which are very non-linear by nature.

Figure 11 – Passive and active implementations of an analog high-pass filter

(a) Passive (b) Active

Source: Author

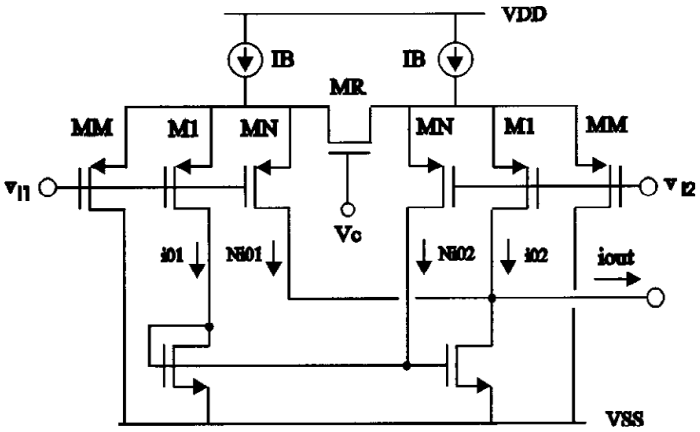
The Operational Transconductance Amplifier (OTA) transconductance is proportional to the input transistor channel inversion and aspect ratio (SCHNEIDER; GALUP-MONTORO, 2010). A very low transconductance can be achieved through biasing input transistors with a very small current and/or very small transistor aspect ratios, which is ultimately limited by leakage currents (LINARES-BARRANCO; SERRANO-GOTARREDONA, 2003) and active area. Unfortunately, the transconductance linearity is also proportional to the transistor inversion, and a low linearity results in high signal distortion. In order to design high-linearity and low-transconductance OTAs, many techniques were developed. Some approaches are based on bulk-driven (KULEJ, 2015; ABBASALIZADEH et al., 2015) or drain-driven topologies (RODRIGUES; SILVA, R., 2015), as drain and bulk transconductances are a fraction of the gate transconductance for the same channel inversion levels and aspect ratios. other commonly used techniques include splitting the output current of the differential input pair, applying a partial positive feedback (GARDE, 1977; SILVA-MARTINEZ; SALCEDO-SUÑER, 1997), or adopting parallel-series current mirrors with very large ratios to attenuate the output signal (KINGET et al., 1992; ARNAUD et al., 2006).

Figure 12 shows an ultra-low transconductance OTA (SILVA-MARTINEZ; SALCEDO-SUÑER, 1997), which implements in field two techniques first proposed for bipolar transistors: current splitting and transconductance cancellation. This a single-stage single-ended output OTA composed of the conventional differential pair, which is made of symmetrical transistors M_1. The differential pair is biased by the tail current sources. The M_M transistors are in parallel with M_1, and shared the same gate and source terminal connections, but its drain terminals are connected to the negative power supply VSS, so only part of the tail current IB flows to the active load made of NMOS transistors. This technique splits the current between M_1 and M_M proportionally to their dimensions, and ultimately results in a lower transconductance. The second technique, transconductance cancellation, consists of cross coupling the drain terminals of transistors M_1 and M_N, but M_N aspect ratio is slightly smaller than M_1, so their corresponding transconductances are subtracted and the original transconductance is partially canceled.

Figure 13 shows conventional single-ended symmetrical OTA (ARNAUD et al., 2006) with parallel-series current mirrors. The key aspect of this technique is the non-unity gain current mirror made of a total 2N identical transistors connected as N-parallel and N-series arrays (GALUP-MONTORO et al., 1994). This results in an extremely small output current attenuated by a N^2 factor, so the differential pair transconductance is also attenuated by the same factor.

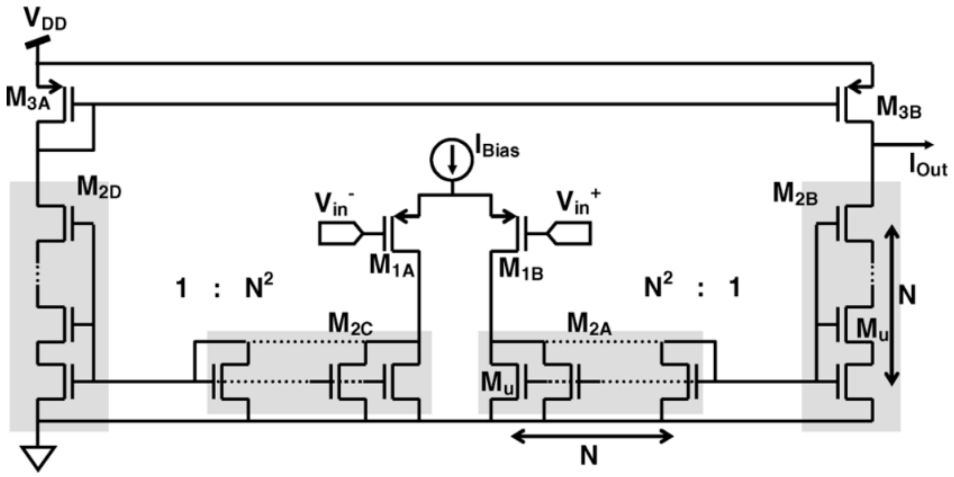
Current-splitting and parallel-series current-mirrors are OTA design techniques which ultimately balances the OTA linearity and ultra-low transconductances. In this thesis, the analog artificial mechanoreceptor will be designed using a novel technique

Figure 12 – OTA with current splitting and transconductance cancellation technique



Source: (SILVA-MARTINEZ; SALCEDO-SUÑER, 1997)

Figure 13 – OTA with parallel-series current mirrors



Source: (ARNAUD et al., 2006)

which combines the two techniques into the current-splitting parallel-trapezoidal current mirrors (RODOVALHO et al., 2021). This technique consists in replacing the current mirror series array by a trapezoidal array (GALUP-MONTORO et al., 1994) and using the current splitting technique. Furthermore, the differential pair OTAs are replaced by inverter-based amplifiers (RODOVALHO, 2020a) with ultra-low-voltage supply voltages to decrease the analog artificial mechanoreceptor total power consumption.

The proposed artificial mechanoreceptor uses various analog circuit design techniques to achieve area and power efficiency, so it can successfully integrate and emulate as many mechanoreceptor units as possible. A whole chapter will be dedicated to the design of the analog artificial mechanoreceptor, while appendices will describe the analog circuit techniques in detail. However, before presenting the actual design, the mechanoreceptor model which this work is based on will be presented in the next chapter.

3 MECHANORECEPTOR MODELS

3.1 MECHANORECEPTOR MODELS REVIEW

The SA-I mechanoreceptor model proposed in (KIM et al., 2012), shown in the previous chapter in Figure 8, is separated into two sub-models: the transconduction sub-model and the neuronal dynamics sub-model. The transduction sub-model transforms the applied force into a current which stimulates the neuron. Then, the neuron firing rate is modeled by the neural dynamics model. The transconduction sub-model is formulated by (1), where $F(t)$ is the applied force as function of time, $F'(t)$ is the rate of change of applied force, β is the intercept constant current, k_s is the static gain, k_d is the dynamic gain, and h is the time step between samples.

$$I(t) = \beta + k_s F(t) + k_d |F'(t)| \tag{1}$$

This transconduction sub-model can be described in the discrete time domain as in the following SA-I mechanoreceptor transconduction sub-model A (SA-IA) algorithm:

Algorithm 1 SA-I mechanoreceptor transconduction sub-model A

for each new sample $F[n]$ **do**
  $F'[n] \leftarrow F[n] - F[n-1]$
  if $F[n]' > 0$ **then**
    $f'_{abs}[n] \leftarrow F[n] - F[n-1]$
  else
    $f'_{abs}(n) \leftarrow F[n-1] - F[n]$
  end if
  $I[n] \leftarrow \beta + k_s F[n] + k_d f'_{abs}[n]$
  $F[n-1] \leftarrow F[n]$
end for

The neuronal dynamics sub-model used in (KIM et al., 2012) is the leaky integrate-and-fire model. This SA-I model in special shows an increase in the neuron firing rate at the protraction phase, so the output current $I(t)$ increases for both $F(t)$ positive and negative changes. This behavior is more suitable to the SA-II mechanoreceptor (BIRZNIEKS et al., 2001), as its firing pattern is a mix of the SA-I and FA-I firing patterns.

The FA-I mechanoreceptor model proposed in (LEE et al., 2016), shown in the previous chapter in Figure 9, uses a similar approach to the previous SA-IA model. However, the transconduction sub-model is greatly simplified, as the FA-I firing pattern has no static component. In this model, the protraction and retraction firing patterns are independently processed by two independent neuron sub-models, each with its own input signals derived from the applied force. The transconduction sub-model, similarly to the previous model, can be adapted to the previous model format by defining two input currents, I_+ and I_-, where

$$I_{+}(t) \leftarrow \max\{F'(t), 0\}, \tag{2}$$

$$I_{-}(t) \leftarrow \max\{-F'(t), 0\} \tag{3}$$

and

$$\max\{x, y\} = \begin{cases} x, & \text{if } x > y \\ y, & \text{otherwise} \end{cases} \tag{4}$$

This behavior, similarly with the previous SA-IA, can be described by the Fast Adapting type I tranconduction submodel A (FA-IA) algorithm:

Algorithm 2 FA-I mechanoreceptor transconduction sub-model A

for each new sample $F[n]$ **do**
  if $(F[n] + F[n-1]) > 0$ **then**
    $I_{+}[n] \leftarrow F[n] - F[n-1]$
    $I_{-}[n] \leftarrow 0$
  else
    $I_{+}[n] \leftarrow 0$
    $I_{-}[n] \leftarrow F[n-1] - F[n]$
  end if
  $F[n-1] \leftarrow F[n]$
end for

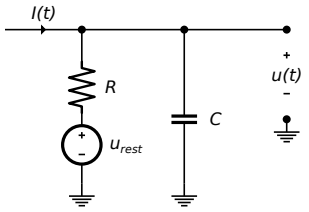
Constrastingly to the mechanoreceptor model from (KIM et al., 2012), this model has an equally simple but yet extremely non-linear neuronal dynamics sub-model, where the simple leak integrate-and-fire neuron model is replaced by simple but yet extremely non-linear model, were the resistor leakage current I_R is replaced by an adaptive threshold potential ϑ and the membrane potential $u(t)$ increases by a non-proportional rate accordingly to the applied force changes $F'(t)$.

3.2 NEURON MODEL

The mechanoreceptor operation, as any other neuron cell, can be roughly described by the leaky integrate-and-fire model (LAPICQUE, 1907; BRUNEL; VAN ROSSUM, 2007; GERSTNER, W. et al., 2014), show in Figure 14 where the cell membrane is acts as a capacitor C in parallel with a leakage resistor R. As the neuron is excited by a variable current $I(t)$, the membrane potential $u(t)$ increases in relation to the cell resting potential u_{rest}, as described by (5).

$$\begin{aligned} I(t) &= I_R(t) + I_C(t) \\ &= \frac{u(t) - u_{rest}}{R} + Cu'(t) \end{aligned} \tag{5}$$

Figure 14 – Leaky integrate-and-fire A (LIF-A) circuit diagram modeling the neuron membrane potential



Source: Author

If the membrane potential $u(t)$ reaches the threshold criterion ϑ, the neuron fires and $u(t)$ is set to the reset potential u_{rst}. If the applied input current $I(t)$ is lower than the rheobase current threshold $I_{rh} = \vartheta/R$, the neuron never fires. If $I(t) \gg I_R(t)$, the instantaneous neuron discharge frequency $f(t)$ for a constant current input is approximately $I(t)/[C(\vartheta - u_{rst}]$.

This neuron model can be adapted to a discrete time system as the following discrete time Leaky Integrate-and-Fire model A (LIF-A) algorithm, where n is the sample number and T is the sample period.

Algorithm 3 Leaky Integrate-and-Fire Model A

for each new sample $I[n]$ **do**
  $u[n] \leftarrow k_a \times I[n] + k_b \times u[n-1] + k_c$
  if $u[n] > \vartheta$ **then**
    $u[n] \leftarrow u[n] - \vartheta + u_{rst}$
    $s[n] \leftarrow 1$
  else
    $s[n] \leftarrow 0$
  end if
end for

The algorithm is based on (5), as this differential equation is solved numerically by using the Euler backward method (BUTCHER, 2004). The parameters k_x are calculated by extracting the continuous model R and C parameters and the sample period T, so $k_a = R/(1 + RC/T)$, $k_b = RC/T(1 + RC/T)$ and $k_c \approx u_{rest}$.

The LIF-A model can be further simplified into the the leaky integrate-and-fire model B (LIF-B), show in Figure 15, where the resistive based leakage current I_R is replaced by a non-linear leakage current $I_{leak}(t, u)$, formulated as

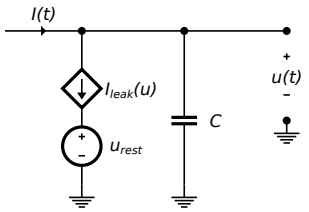
$$I(t) = I_{leak}(u) + I_C(t) \tag{6}$$

and

$$I_{leak}(u)) = \begin{cases} I_{leak0}, & \text{if } u > u_{rest} \\ 0, & \text{otherwise} \end{cases} \tag{7}$$

where I_{leak0} is a constant current leakage for $u(t) > u_{rest}$. Consequently, for this model, the rheobase current $I_{rh} = I_{leak0}$, and the instant frequency $f(t)$ is equal to $[I(t) - I_{leak0}]/[C(\vartheta - u_{rst})]$.

Figure 15 – Leaky integrate-and-fire B (LIF-B) circuit diagram modeling the neuron membrane potential



Source: Author

The Leaky Integrate-and-Fire model B (LIF-B) model can be described in the discrete time domain as in the following algorithm, where the parameter $k = T/C$.

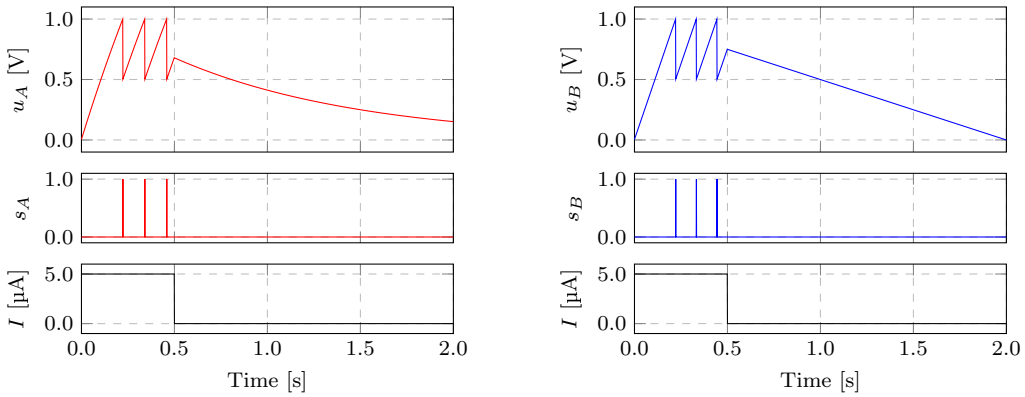
Algorithm 4 Leaky Integrate-and-Fire Model B

for each new sample $I[n]$ **do**
  $u[n] \leftarrow u_{rest} + k \times (I[n] - I_{leak0})$
  if $u[n] > \vartheta$ **then**
    $u[n] \leftarrow u[n] - \vartheta + u_{rst}$
    $s[n] \leftarrow 1$
  else
    if $u[n] < u_{rest}$ **then**
      $u[n] \leftarrow u_{rest}$
    end if
    $s[n] \leftarrow 0$
  end if
end for

The differences between these models are easily visualized in the following simulation results, as shown in Figure 16. Both models have the same u_{rest}, u_{rst} and ϑ, as 0, 0.5 and 1 V, respectively, and the same capacitance C as 1 µF. The models diverge as the LIF-A model has an 1 MΩ resistance R and LIF-B model has a 500 nA leakage current I_{leak0}. Both models have the same step input current signal, and similar pulse signal patterns. However, as the input switches to zero, the model A membrane potential u_A decreases exponentially, and model B u_B decreases linearly until it reaches u_{rest}.

However, the simple leaky integrate-and-fire neuron model is very limited, as it cannot reproduce discharge patterns which exhibit adaptation, such as the mechanoreceptors. More advanced models, such as the Hodgkin-Huxley model (HODGKIN; HUXLEY, 1952), quadratic integrate-and-fire model (IZHIKEVICH, 2003), and adaptive exponential integrate-and-fire model (BRETTE; GERSTNER, Wulfram, 2005), can be

Figure 16 – Leaky integrate-and-fire model simulation



(a) LIF-A (b) LIF-B

Source: Author

used to describe the mechanoreceptor adaptive behavior at the cost of increased complexity. Moreover, the tactile signals from the fingertips are a composition of several mechanoreceptor outputs (BIRZNIEKS et al., 2001), and also is a function of the complex mechanical properties (WU, J. Z. et al., 2003) of the skin, such as direction and area of contact (JENMALM et al., 2003; JOHANSSON; FLANAGAN, 2009). Therefore, if a simple model, such as the integrate-and-fire neuron model were used to describe the mechanoreceptor response, it must also model the neuron input accordingly.

3.3 PROPOSED SA-I MECHANORECEPTOR MODEL

The previous models can be improved by making some small changes. The previously discussed Slow Adapting type I tranconduction submodel A (SA-IA) has only two components: the static and dynamic. The dynamic component results in the higher neuron firing rate at the protraction phase, but also increases the firing rate at the retraction phase. This sub-model also does not take into account the slow decay of the firing rate at the plateau phase, accordingly to the mechanoreceptor experiment from (BIRZNIEKS et al., 2001).

For this reason, it is proposed in this thesis to separate the transconduction sub-model in three output current components I_A, I_B and I_C, so

$$I(t) = I_A(t) + \max\{I_B(t), 0\} + \max\{I_C(t), 0\} \tag{8}$$

where I_A is the proportional to the applied force current component, defined as

$$I_A(t) = k_A F(t), \tag{9}$$

I_B is the protraction phase current component, defined by the differential equation

$$I_B(t) = \alpha_B F'(t) - \beta_B I'_B(t) \tag{10}$$

and I_C is slow decaying current component, defined by the differential equation

$$I_C(t) = \alpha_{C1} F'(t) - \beta_C I'_C(t) \tag{11}$$

The current components I_B and I_C can be described in the s-domain as a linear time-invariant system as

$$\frac{I_x(s)}{F(s)} = \frac{\alpha_x}{\beta_x} \cdot \frac{s}{s + 1/\beta_x} = K_x \cdot \frac{s}{s + 2\pi f_x} \tag{12}$$

where K_x is the filter gain and f_x is the filter corner frequency.

One of they key differences between the proposed sub-model and the previous one is that the dynamic component, besides being split in two, is a time-invariant high-pass filter. The pure and ideal signal derivative is very susceptible to high frequency signals, as the signal amplitude increases proportionaly with the signal frequency. Therefore, the resulting current component transduction gain should be limited for frequencies above a certain limit, which is the high-pass filter corner frequency. For frequencies significantly lower than this corner frequency, the high-pass filter behaves as an differentiator.

The other key difference is the signal rectification, so negative current components do not stimulate the neuron. This sub-model is described in the discrete time domain in Algorithm 5, the Slow Adapting type I tranconduction submodel B (SA-IB), where $k_{x1} = K_x k_{x2}$ and $k_{x2} = 1/(1 + 2\pi f_x T)$.

Figures 17a, 17b and 17c, shows the full SA-I mechanoreceptor model simulation results with a 1 ms sampling time T, by using the SA1-B transduction and LIF-B neuron sub-models. The transduction model algorithm parameters are calculated using the following continuous time parameters: k_A = 1 µA/N,K_B = 8 A/A,f_B = 20 Hz,K_C = 2 A/A, and f_C = 2 Hz. The neuron sub-model parameters values for C and I_{leak0} are 500 nF and 500 nA, respectively. The force input is equivalent to the input signal used in the mechanoreceptor experiment from (BIRZNIEKS et al., 2001).

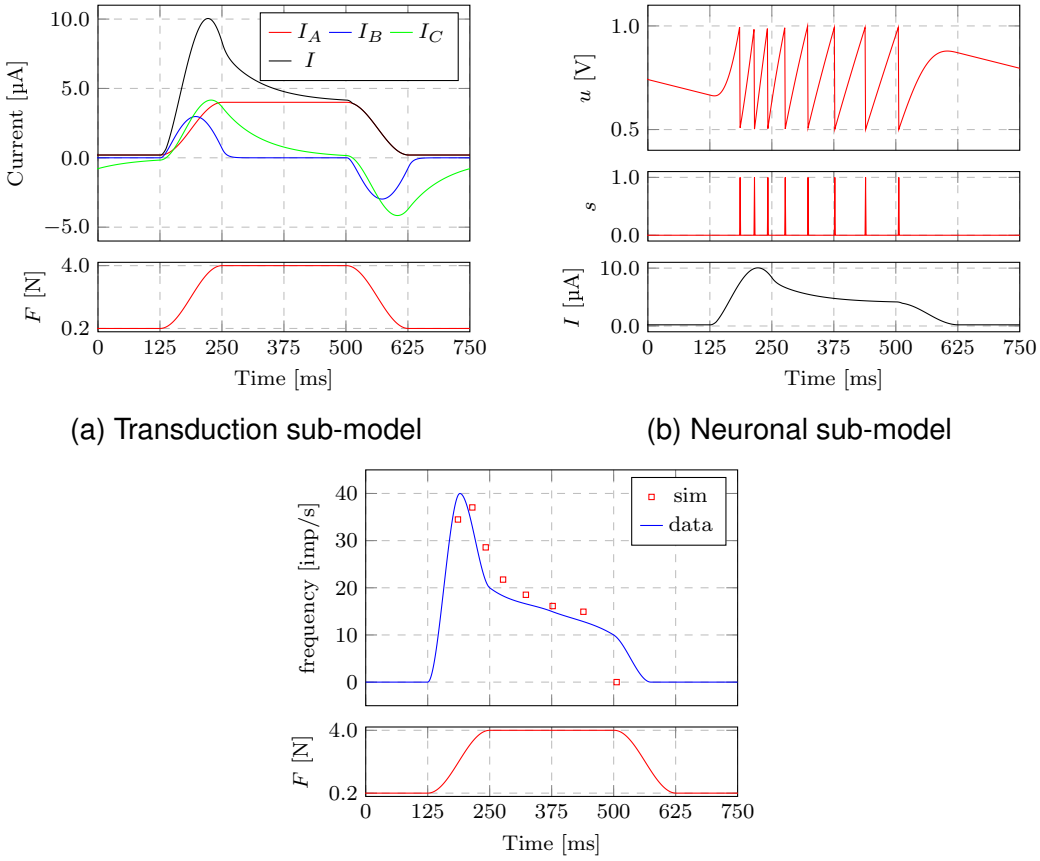
As can be seen in Figure 17a, I_A shape is an exact copy of the force input F. The dynamic current component I_B is proportional to the input signal derivative, as the filter corner frequency is significantly higher than the signal frequency harmonics. Those two current components are similar to the static current component and dynamic from the SA-IA sub-model. The main difference comes from the I_C current component, which is result from the high-pass filter with a very low corner frequency. The I_C component is responsible for the sub-model total current I slow decay. Additionally, I_B and I_C negative values does not contribute to the output current.

Algorithm 5 SA-I mechanoreceptor transconduction sub-model B

for each new sample $F[n]$ **do**
  $F'[n] \leftarrow F[n] - F[n-1]$
  $I_A \leftarrow k_a \times F[n]$
  $I_B[n] \leftarrow k_{b1} \times F'[n] - k_{b1} \times I'_2[n]$
  $I_C[n] \leftarrow k_{c1} \times F'[n] - k_{c2} \times I'_3[n]$
  if $I_B[n] > 0$ **then**
    $I_{B+}[n] \leftarrow I_B[n]$
  else
    $I_{B+}[n] \leftarrow 0$
  end if
  if $I_C[n] > 0$ **then**
    $I_{C+}[n] \leftarrow I_C[n]$
  else
    $I_{C+}[n] \leftarrow 0$
  end if
  $I[n] \leftarrow I_A + I_{B+} + I_{C+}$
  $f[n-1] \leftarrow F[n]$
  $I_2[n-1] \leftarrow I_2[n]$
  $I_3[n-1] \leftarrow I_3[n]$
end for

Subsequently, the transduction sub-model current output, which is the input of the neuron sub-model, triggers the response shown in Figure 17b. The neuron instantaneous discharging frequency f is shown in Figure 17c, and is calculated as the inverse of interval between one neuron discharge impulse and the next one. As observed, the simulation results, show that instantaneous frequency from the proposed model, depicted as points at the time of each neuron discharge, has a similar response to the data acquired in the mechanoreceptor experiment, which is depicted as a curve.

Figure 17 – SA-I model simulation results



(a) Transduction sub-model

(b) Neuronal sub-model

(c) Output frequency

Source: Author

3.4 PROPOSED FA-I MECHANORECEPTOR MODEL

The Fast Adapting type I tranconduction submodel B (FA-IB), described by the Algorithm 6, is an extended version of FA-IA sub-model, but the derivative is replaced by a high-pass filter and there is different weights for the protraction and retraction phases, which corresponds to the I_A and I_B current components. Additionally, both current components are summed and stimulate a single neuron sub-model, instead of two distinct neurons, as in (LEE et al., 2016).

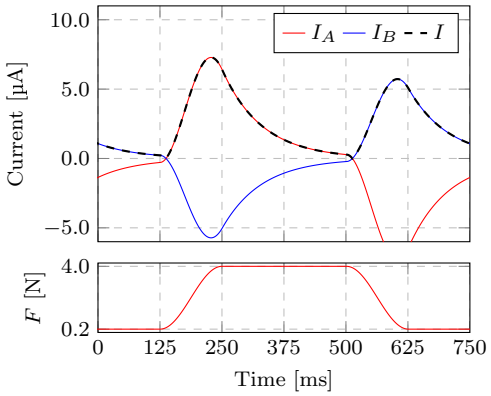
Figures 18a, 18b and 18c, shows the full FA-I mechanoreceptor model simulation results with a 1 ms sampling time T, by using the FA1-B transduction and LIF-B neuron sub-models. The transduction model algorithm parameters are calculated the same way as the SA-IB parameters, using the following continuous time parameters: k_A = 3.5 µA/N,k_B = 2.75 µA/N, and f = 2 Hz, so $k = 1/(1 + 2\pi fT)$. The neuron sub-model parameters values are C = 500 nF and I_{leak0} = 1 µA. The force input is also equivalent to the input signal used in the mechanoreceptor experiment from (BIRZNIEKS et al., 2001).

As can be seen in Figure 18a, the transduction model output current I is com-

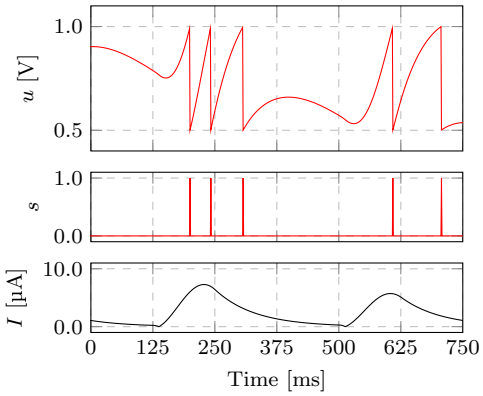
Algorithm 6 FA-I mechanoreceptor transconduction sub-model B

for each new sample F[n] **do**
  $F'[n] \leftarrow F[n] - F[n-1]$
  $I_0[n] \leftarrow k \times (F'[n] + I_0[n-1])$
  if $I_0[n] > 0$ **then**
    $I[n] \leftarrow k_A \times I_0[n]$
  else
    $I[n] \leftarrow k_B \times I_0[n]$
  end if
end for
$F[n-1] \leftarrow F[n]$
$I_0[n-1] \leftarrow I_0[n]$

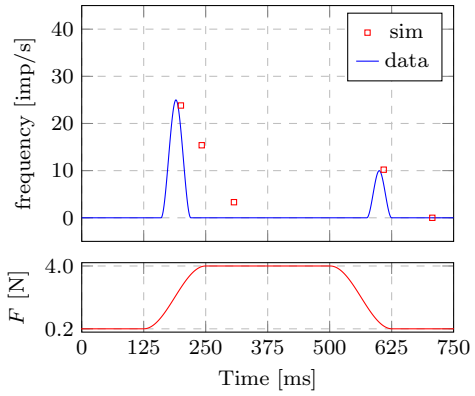
Figure 18 – FA-I model simulation results



(a) Transduction sub-model



(b) Neuronal sub-model



(c) Output frequency

Source: Author

posed by two dynamic current components I_A and I_B. The current components are calculated as $I_A = k_A * I_0$ and $I_B = k_B * I_0$, and are not explicitly processed in the algorithm. The neuron sub-model simulation results are shown in Figures 18b and 18c. The simulated neuron instantaneous discharging frequency is also compared to the data from the mechanoreceptor experiment. the maximum amplitude for the protraction

and retraction phase matches the experimental data. However, the protraction phase response is slightly delayed.

3.5 CHAPTER SUMMARY AND CONCLUSIONS

In this chapter, the model simulations are results from numerical computations. The previous works used simple algorithms to model the SA-I (KIM et al., 2012) and FA-I mechanoreceptor (LEE et al., 2016) behavior. Both works gathered data inputs from electronic transducers and subsequently fed them to their models to validate their findings. In this work, the proposed models are variations of the previous works models which, mainly, uses high-pass filters instead of plain differentiators. The high-pass filter implementation is slightly more complex and performance intensive. However, this thesis main goal is to develop analog artificial mechano-receptors, and ideal differentiators are impossible to fabricate, so the proposed model is more suitable to describe their behavior. Also, it is important to state that no simplified model can accurately describe the mechanoreceptor behavior, since it is only an approximation. An artificial mechanoreceptor based on this model would rely on the brain plasticity (MILLER; WEBER, 2011) to adapt to those signals imperfections.

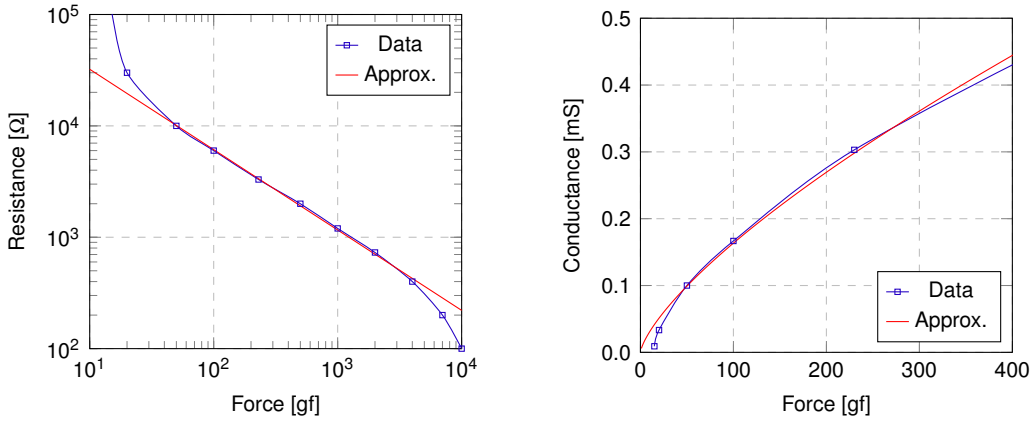
4 ANALOG ARTIFICIAL MECHANORECEPTOR

The previous chapter described the SA-I (KIM et al., 2012) and FA-I (LEE et al., 2016) mechanoreceptor models and their numerical implementation. Their physical implementation can be done by using the mixed-signal approach, as shown in Figures 6a and 8, where the transducer analog signal is converted to the digital domain and all signal processing is done digitally. This thesis focuses on the analog approach, shown in Figure 6b, which all signals are processed in the analog domain.

The following sections will describe every block used in the analog artificial mechanoreceptor system in the transistor level, as designed for the TSMC 180 nm node technology, and then simulated to validate its results.

4.1 FORCE SENSITIVE RESISTOR MODEL

Figure 19 – FSR400 model data measurement and simulation results



(a) Resistance × Force (b) Conductance × Force

Source: Author

The Interlink Electronics FSR 400 (INTERLINK ELECTRONICS, 2019) force sensitive resistor typical force curve is shown in Figure 19a. The sensor resistance can be modeled by (13), similarly as stated in (SCHOFIELD et al., 2016), as the equivalent resistance R_{FSR} of two parallel resistors R_0 and R_F, where R_0 is the non-actuated resistance and R_F is a force dependent variable resistance.

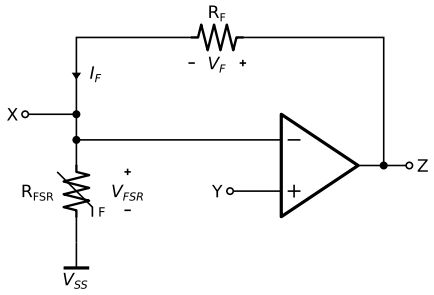
$$R_{FSR} = \frac{1}{G_{FSR}} \approx R_0 \parallel R_F \approx \frac{1}{G_0 + G_F} = \frac{1}{G_0 + aF^m} \tag{13}$$

The parameters a and m can be estimated by using the log-log data points provided by the supplier in the component datasheet. Considering that the resistor curve does not show hysteresis and the parameters R_0 = 10 MΩ, a = 170 Ω·gf and m = 0.72, this model is fairly accurate in the 50 g to 4000 g force input range.

Figure 19b shows the approximated sensor conductance actuated force dependence derived from (13). As can be shown, the equivalent conductance G_{FSR} varies almost linearly with the actuated force, as the slope factor m is close to unity. Consequently, the equivalent resistance is inversely proportional to the actuated force and should not be used as the sensor output as its force dependence is highly non-linear.

4.2 TRANSDUCER CIRCUIT

Figure 20 – Force-to-voltage transducer circuit diagram



Source: Author

Figure 20 shows the force-to-voltage transducer circuit diagram. The transimpedance amplifier (PAREDES-MADRID et al., 2017) forces a constant voltage drop $V_{FSR} = V_X - V_{SS}$ at the force sensitive resistor R_{FSR}, which outputs a voltage V_Z proportional to the force sensitive resistor conductance G_{FSR}. The operational amplifier forces V_X to follow V_Y, so V_Y can be used as a voltage reference to control the transducer force-to-voltage gain. Another way to control the voltage gain is by varying the feedback resistance R_F magnitude, which can be done by using replacing it by a variable resistor with digital control.

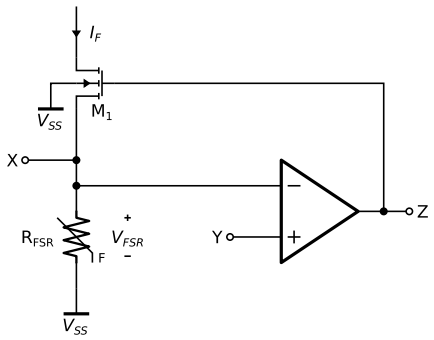
$$\begin{aligned} V_Z &\approx V_X + V_{FSR} G_{FSR} R_F \\ &\approx V_X + V_{FSR} a F^m R_F \end{aligned} \tag{14}$$

It must be noticed that the operational amplifier must be able to output proportional to applied force current

$$I_F = V_{FSR} G_{FSR} = (V_X - V_{SS}) G_{FSR} = \frac{V_Z - V_X}{R_F} \tag{15}$$

otherwise the circuit will not function properly. The maximum output voltage V_{Zmax} and maximum feedback current I_{Fmax} conditions happens for the maximum applied force F_{max}, which results in the minimum force sensitive conductance G_{FSRmin}. This ultimately limits the required minimum supply voltage and operational amplifier voltage excursion for proper operation.

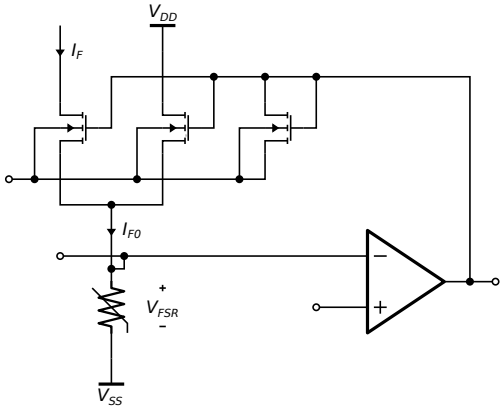
Figure 21 – Force-to-current transducer circuit diagram



Source: Author

Figure 21 shows the force-to-current transducer. This approach works almost exactly as the previous one, but there is no direct conversion between the output current I_F to an output voltage. The operational amplifier does not need to provide the output current, as its only function is to provide a feedback loop control to force V_X to follow V_Y. It is still limited by the maximum output current I_{Fmax}, as it I_F is equal to the N-type Metal-Oxide-Semiconductor (NMOS) transistor drain current I_{D1}, which is itself a function of the gate-to-source voltage $V_{GS1} = V_Z - V_X$ and the transistor aspect ratio S_1. However, S_1 can be made large enough to allow a significantly low V_Z, and consequently, a lower supply voltage.

Figure 22 – Improved force-to-current transducer circuit diagram



Source: Author

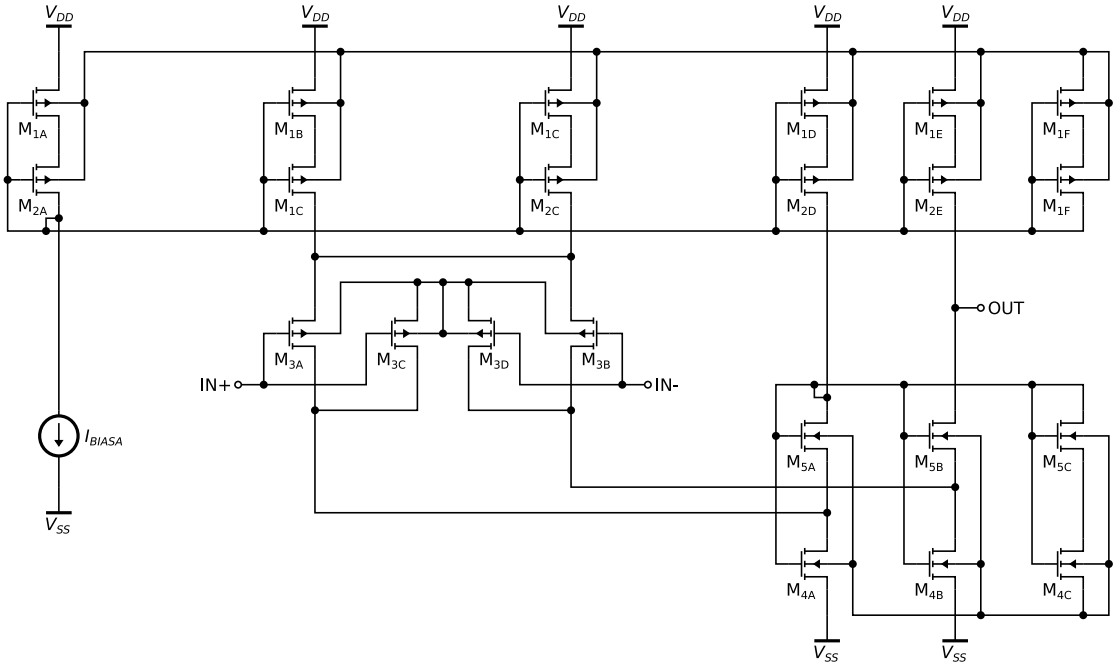
Figure 21 shows the improved force-to-current transducer. It works as the previous circuit, but it uses two other techniques to decrease the output current I_F and V_{GS1} without increasing the transistor size. First of all, the entire system power usage is proportional to the system total current consumption and its supply voltage, as $P_{total} = V_{DD} \times I_{total}$. It important that the subsequent circuits use as little current as possible. The improved circuit splits the initial proportional-to-force current I_{FO} into I_{D1} and I_{D2}, using the same technique proposed in (SILVA-MARTINEZ; SALCEDO-SUÑER,

1997). Since both transistors M_1 and M_2 have the same gate-to-source V_{GS} and bulk-to-source V_{BS} voltages, and are operating in the saturation region, I_F is proportional to the aspect ratios, so $I_F = I_{D1} = (S_1/S_2)I_{D2}$. This technique can be even further improved by using series-parallel transistor arrays (GALUP-MONTORO et al., 1994), to achieve the maximum S_1/S_2 possible (FIORELLI et al., 2004).

The second technique is the transistor forward-body-biasing. In the previous force-to-current transducer, the transistor M_1 terminal is connected to V_{SS}, so $V_{BS} = -V_X$ and its reverse-body-biased. The improved transconductor uses a third transistor M_3, which forward-body-bias the transistor M_1 and M_2 using the technique proposed in (LINDERT et al., 1999), which will be further explored in Appendix D. Transistor arrays, forward-body-biasing and current splitting techniques are further explored in Appendices B, D and C, respectively.

Figure 23 shows the operational amplifier used in the transducer circuit.It is a variation of the folded cascode operational transconductance amplifier (OTA) proposed in (FERREIRA; SONKUSALE, 2014) with a gate-driven differential pair input. This OTA topology differs from the conventional folded cascode OTA as the output stage uses transistors in the self-cascode configuration. Transistors $M_{1A\text{-}E}$ are $M_{2A\text{-}E}$ P-type Metal-Oxide-Semiconductor (PMOS) current mirrors, as they replicate the biasing current I_{BIASA}. Those current mirrors use trapezoidal arrays (GALUP-MONTORO et al., 1994; DE CEUSTER et al., 1996) to increase the output impedance.

Figure 23 – Operational Amplifier transistor level circuit diagram



Source: Author

The differential pair is made of transistors $M_{3A,B}$ and use forward-body-biasing to increase the OTA common-mode input voltage excursion (LEHMANN; CASSIA, 2001).

Transistors $M_{3C,D}$ limits the differential pair parasitic substrate due to forward-body-biasing (LINDERT et al., 1999).

Transistors $M_{4A,B}$ and $M_{5A,B}$ compose a NMOS self-cascode current mirror, as all transistors gate terminals are connected to transistor M_{5A} drain terminal. For a conventional folded cascode OTA, transistors $M_{4A,B}$ and $M_{5A,B}$ would be biased independently by an additional biasing circuit. The self-cascode current mirrors advantage is that it allows a larger output voltage excursion than the conventional cascode current mirrors considering similar biasing currents and power supplies. Additionally, the current-mirrors use forward-body-biasing to decrease the minimum voltage supply requirement. Transistors M_{1F}, M_{2F}, M_{4C} and M_{5C} also function as substrate parasitic current limiters. More details about those techniques are available in Appendices D and C.

All transistors in the force-to-current transducer and operational amplifier circuit diagrams are rectangular transistor arrays. Their dimensions are shown in Table 1 and 2. It worth noticing that every single PMOS transistor has the same width, 6 µm, and every NMOS device has also the same width, 1.5 µm. Additionally, all transistors have a 0.5 µm channel length. The differences are only how the arrays are arranged.

Table 1 – Transducer rectangular arrays dimensions

	m	*n*	*W* [µm]	*L* [µm]		*m*	*n*	*W* [µm]	*L* [µm]
M_1	4	4	1.5	0.5	M_2	16	1	1.5	0.5
M_1	8	1	1.5	0.5					

Source: Author

Table 2 – Operational amplifier rectangular arrays dimensions

	m	*n*	*W* [µm]	*L* [µm]		*m*	*n*	*W* [µm]	*L* [µm]
$M_{1A\text{-}E}$	4	4	6.0	0.5	$M_{2A\text{-}E}$	16	1	6.0	0.5
M_{1F}	8	1	6.0	0.5	M_{2F}	8	1	6.0	0.5
$M_{3A\text{-}B}$	16	1	1.5	0.5	$M_{3C\text{-}D}$	16	1	1.5	0.5
$M_{4A\text{-}E}$	4	4	1.5	0.5	$M_{5A\text{-}E}$	16	1	1.5	0.5
M_{4C}	8	1	1.5	0.5	M_{5C}	8	1	1.5	0.5

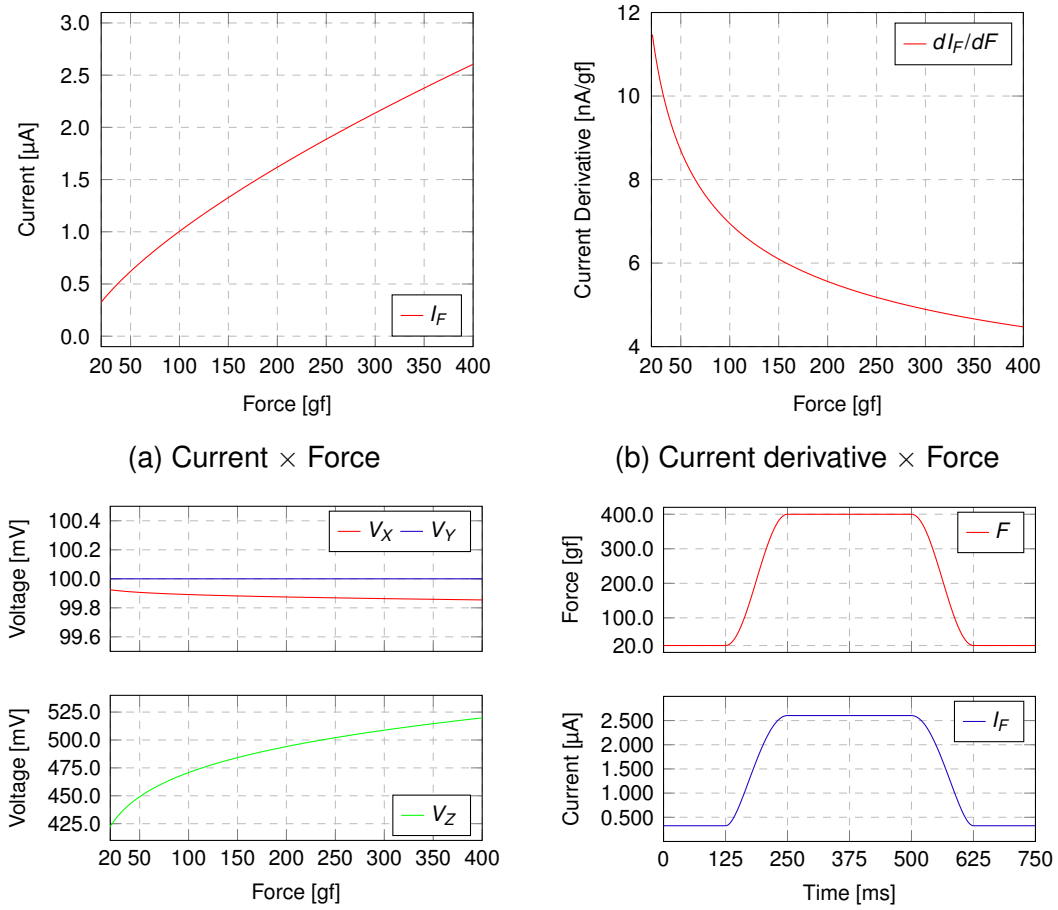
Source: Author

Figure 24a shows the improved force-to-current transducer characteristic curve for typical process parameters, room temperature and a 0.7 V supply voltage. The operational amplifier biasing current I_{BIASA} was set at 100 nA. All transistor level simulations used standard MOSFET transistor models from the TSMC 180 nm process design kit. As can be noticed, the output current is proportional to G_{FSR}, as previously shown in Figure 19b. For this reason, the transducer characteristic curve is not linear, since G_{FSR} is not, due to the the force sensitive resistor non-linearity. This non-linearity is better visualized in 24b, which shows the force-to-current transducer gain, which varies from

approximately 12 nA/gf to approximately 4 nA/gf for an 20 to 400 gf applied force input range. This ultimately decreases the transducer linear resolution, but it is still adequate for the artificial mechanoreceptor requirements, since the biological mechanoreceptors are also very non-linear (WU, J. Z. et al., 2003).

Figure 24c shows that V_X follows V_Y, as result from the negative feedback loop, as seen in Figure 22. Also, V_Z maximum value is within the supply voltage boundaries, 175 mV less than V_{DD}, with a small-margin to guarantee that the transducer will still work properly at worst case process corners. Finally, Figure 24d shows the transient simulation considering the force input signal F similar in magnitude to the one used in the mechanoreceptor experiment, as detailed in Figure 4.

Figure 24 – Transducer DC characteristic curves and transient simulation results



(a) Current × Force

(b) Current derivative × Force

(c) Voltage × Force

(d) Transient simulation results

Source: Author

4.3 ANALOG SIGNAL PROCESSING BLOCK

4.3.1 SA-I Analog Signal Processing Block

The mechanoreceptor transduction sub-model, as proposed in (KIM et al., 2012) and shown in Figure 8, outputs a current as function of the input force. This output current is itself split into two components: static and dynamic. The static component could be implemented by a simple transducer, as explained in the previous section. However, the dynamic component, which is proportional to the input force derivative, must be further processed. In Chapter 3, the SA-I transduction sub-model A (Algorithm 1) was described as a numeric computation algorithm implementation of the SA-I mechanoreceptor model from (KIM et al., 2012). The force input signal derivative is easily implemented numerically with a discrete time differentiator, but an ideal differentiator is impossible to implement with analog circuits. For this reason, the SA-I transduction sub-model B was proposed. This model replaces the differentiator by a high-pass filter. Furthermore, the first-order high-pass filter response itself can be approximated to an ideal differentiator for input signal frequencies significantly lower than its cut-off frequency.

Figure 25 shows the SA-I Analog Signal Processing (ASP) circuit diagram, which is the analog implementation of the SA-I transduction model.

The SA-I ASP circuit receives as input the output from the force-to-current transducer. The current controlled voltage source converts the input current I_F into a voltage $V_F = V_1$, but first it attenuates I_F by a $1/k_1$ factor and creates an voltage offset proportional to the biasing current I_{BIASF}. The transconductor G_{m1} is connected in the load configuration with its output terminal connected to the inverting input terminal and behaves as a resistor.

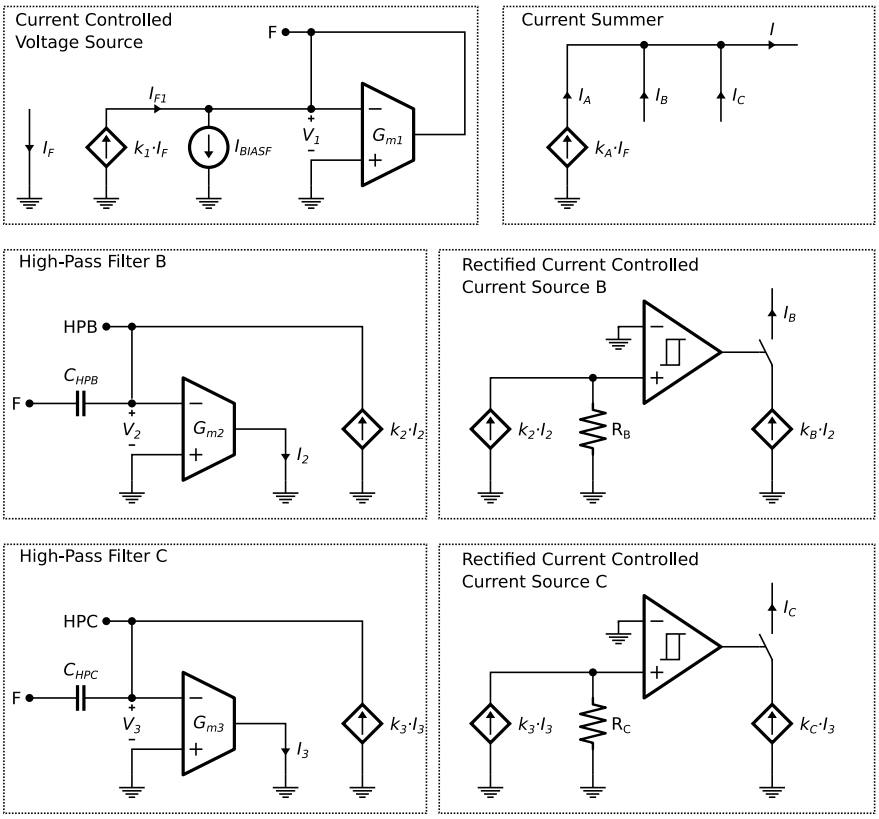
$$V_F = V_1 = \frac{k_1 I_F - I_{BIASF}}{G_{m1}} \tag{16}$$

The voltage signal V_F is the input of the two high-pass filters which outputs the SA-I mechanoreceptor dynamic current components I_B and I_C, as described by the transduction sub-model B equations (10),(11). The high-pass filters output voltages V_{HPA} and V_{HPB} are a function of the transconductances G_1 and G_2, and attenuation factors and k_1 and k_2, respectively, accordingly to (17) which is the implementation of the model equation (12).

$$\frac{V_{HPX}(s)}{V_F(s)} = \frac{s}{s + \dfrac{k_N G_{mN}}{C_x}} = \frac{s}{s + 2\pi f_{cX}} \tag{17}$$

Each transconductor G_{mN} output is replicated three times. The first time, in the feedback loop, which implements the high-pass filter. The second and third times are

Figure 25 – SA-I ASP complete circuit diagram



Source: Author

replicated in the rectified voltage controlled current sources. For positive transconductor output currents I_N, the voltage controlled source switches are closed, so the current component $I_X = k_X I_N$, otherwise the switch is open and $I_X = 0$. This circuit implements the function $\max\{I_X, 0\}$, described in (4) and used in (8).

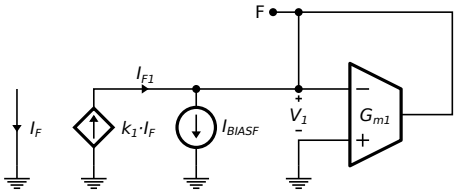
Finally, all current components I_A, I_B and I_C are summed to output the tranduction current I, implementing the full transduction sub-model.

Each of those separate parts can be implemented with different analog circuits, employing different techniques to achieve the same results. The design challenge is to implement those circuits with the least area and power usage; tolerance to process, supply voltage and temperature (PVS) variability; and the circuits must function as closely as possible to its intended ideal behavior.

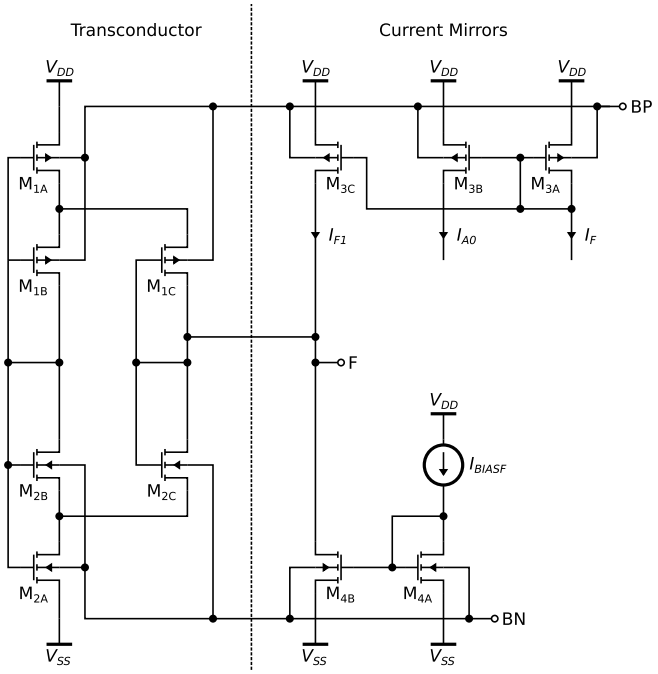
Figure 26 shows the circuit diagram of the previously discussed current controlled voltage source. Table 3 shows each transistor array dimensions in this circuit. The current mirror made of transistors $M_{3A,B}$, replicates the input current I_F, which is the force-to-current transducer output current, then subtracts it by the biasing current I_{BIASF}. The transconductor is implemented as a CMOS inverter (RODOVALHO, 2020a; RODOVALHO et al., 2020) made of the transistors M_{1C} and M_{2C} with its input and output terminals connected. Transistors $M_{1A,B}$ and $M_{2A,B}$ composes a source

degeneration circuit which improves the inverter linearity to make the output voltage V_F as possible. Terminals BP and BN provides the inverter with the biasing voltages V_{BP} and V_{BN} to control its transconductance. Appendix E explains the inverter as a transconductor, as also its linearization and biasing circuits.

Figure 26 – Current controlled voltage source circuit diagram



(a) Simplified circuit diagram



(b) Transistor level circuit diagram

Source: Author

Table 3 – Current controlled voltage source circuit array dimensions

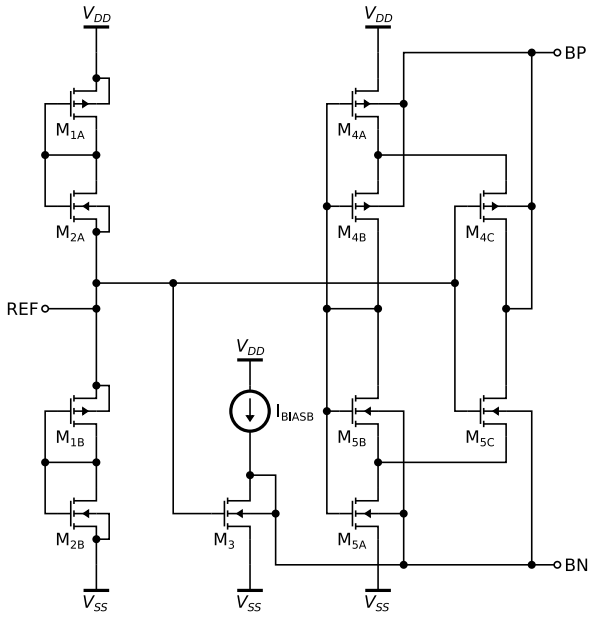
	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A\text{-}C}$	2	8	6.0	0.5	$M_{2A\text{-}C}$	2	8	1.5	0.5
M_{3A}	8	2	6.0	0.5	M_{3B}	4	2	6.0	0.5
M_{3C}	4	2	6.0	0.5	$M_{4A,B}$	2	4	6.0	0.5

Source: Author

Figure 27 shows the circuit that provides the biasing V_{BP} and V_{BN} to all the ASP transconductors. Table 4 shows all its transistor array dimensions. First, transistors $M_{1A,B}$ and $M_{2A,B}$ compose identical inverters with their inputs and output terminals connected. They function as very large resistances, since terminal REF

voltage V_{REF} is half the positive voltage supply V_{DD}, considering that $V_{DD} = 0$, so $V_{DD} - V_{REF} = V_{REF} - V_{SS}$. The biasing current I_{BIASB} defines the biasing voltage V_{BN}, and the remaining circuit defines the biasing voltage V_{BP}, so the previously discussed current-controlled voltage source outputs $V_F = V_{DD}/2$ for $I_{F1} = I_{BIASF}$

Figure 27 – Transconductor biasing circuit diagram



Source: Author

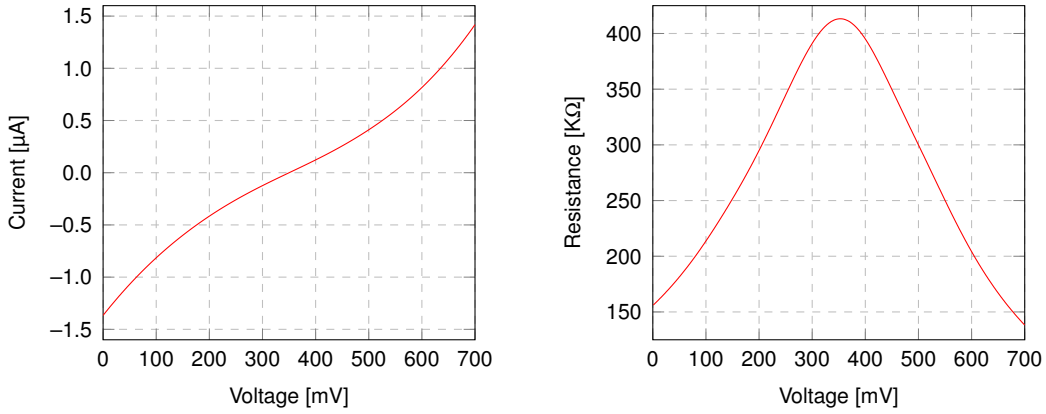
Table 4 – Transconductor biasing circuit array dimensions

	m	*n*	*W* [µm]	*L* [µm]		*m*	*n*	*W* [µm]	*L* [µm]
$M_{1A\text{-}B}$	2	8	6.0	0.5	$M_{2A\text{-}B}$	2	8	1.5	0.5
M_3	16	2	6.0	0.5	$M_{4A\text{-}C}$	8	4	6.0	0.5
$M_{5A\text{-}C}$	16	2	6.0	0.5					

Source: Author

Figures 28a and 28a show current controlled voltage source transconductor DC characteristic curve and its resistance, respectively. As can be seen in Figure 28a, the transconductor input current, considering that its input terminal and output terminals are connected to each other, is zero when the input voltage is approximately half the supply voltage, which is 350 mV. This is a direct result of the biasing circuit proper operation even considering process parameters variability. The transconductor uses a linearization technique, but its clear that the transconductor characteristic curve is significantly non-linear for input voltages outside its linear range between 300 and 500 mV. The inverse of this curve first derivative dV/dI is the transconductor input resistance in the load configuration, as shown in Figure 28b. It shows that this transconductor behaves as a non-linear resistor of about 413 KΩ at its maximum value, at 350 mV.

Figure 28 – Current controlled voltage source transconductor DC characteristic curve



(a) Input current × input voltage (b) Resistance × input voltage

Source: Author

Considering that the inverter transconductance is approximatelly G_{m1}, the current controlled voltage source can be expressed as

$$V_F = \left(\frac{S_{3B}}{S_{3A}} \cdot I_F - \frac{S_{4B}}{S_{4A}} \cdot I_{BIASF} \right) G_{m1} + \frac{V_{DD}}{2} \tag{18}$$

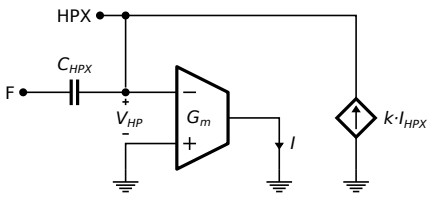
The next circuit is the high-pass circuit, as shown in Figure 29. This circuit is made of two parts: the linearized inverter, which functions as the transconductor, and the current mirror, which works as a current controlled current source. The transconductor is the same linearized inverter from the previously discussed current controlled voltage source. However, this circuit employs current mirrors with very large current attenuation factors, such as the parallel-series current mirrors (FIORELLI et al., 2004). The first current mirrors are parallel-trapezoidal current mirrors with split output current, which combines the techniques from (SILVA-MARTINEZ; SALCEDO-SUÑER, 1997) and (KINGET et al., 1992). The current mirror attenuation factor is a function of the transistors aspect ratios, so the attenuation factor k_N from (17) is defined as

$$\frac{1}{k_N} \approx \frac{S_{3B}}{S_{3A}} \cdot \frac{S_{3D}}{S_{3C}} \cdot \frac{S_{6B}}{S_{6A}} \tag{19}$$

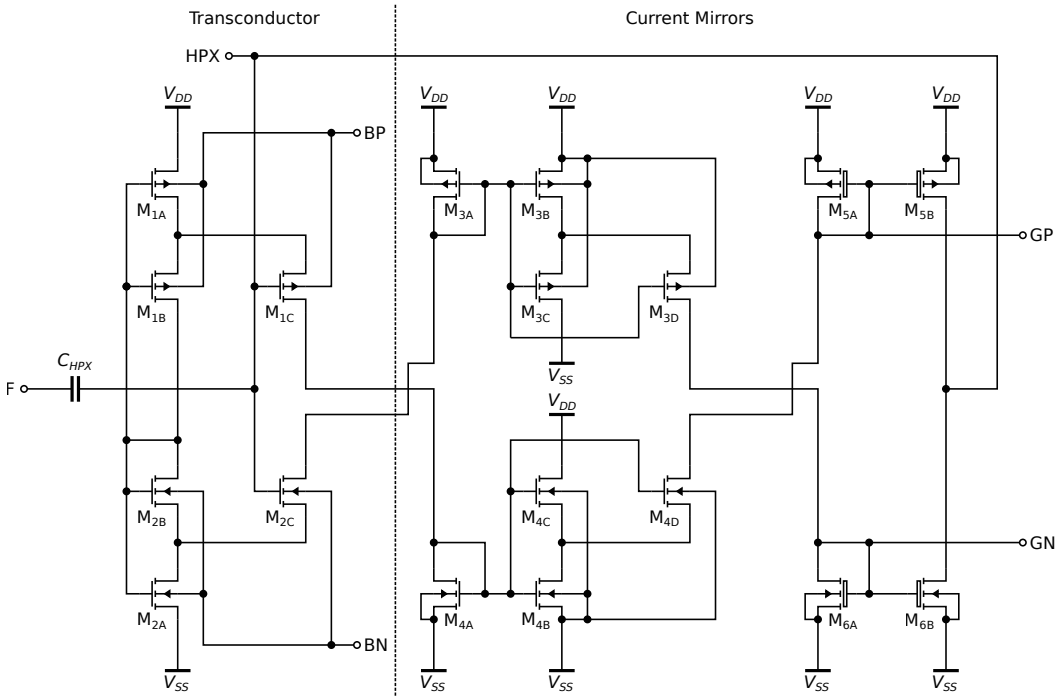
The second current mirror is parallel-series outputs the voltages V_{GP} and V_{GN}, which are used to replicate the output currents I_N, as transconductor G_{mN} behaves as OTA with multiple outputs (WU, J.; EL-MASRY, 1998). The parallel-trapezoidal current mirror and the inverter transconductance lowering techniques are further discussed in Appendices C and E.

The high-pass filters B and C have the exact same transistor dimensions, as shown in Table 5. They only differ in the capacitor size, as C_{HPB} is a single 20 × 20

Figure 29 – High-pass filter circuit diagram



(a) Simplified circuit diagram



(b) Transistor level circuit diagram

800 pF Metal–Insulator–Metal (MIM) capacitor, and C_{HPC} is 11 parallel 20 $\times$ 20 800 pF MIM capacitor, totaling 8.8 pF.

Table 5 – High-pass filter circuit array dimensions

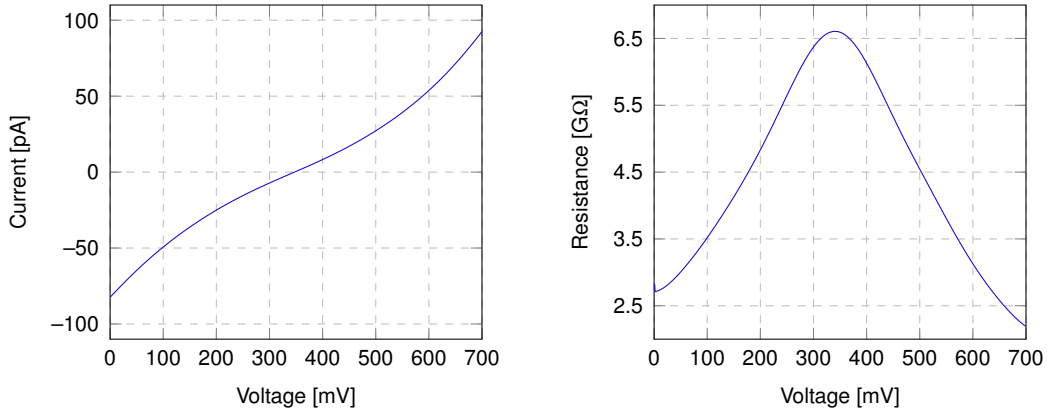
	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A\text{-}C}$	2	8	6.0	0.5	$M_{2A\text{-}C}$	2	8	1.5	0.5
$M_{3A,C}$	8	1	6.0	0.5	$M_{3B,D}$	2	4	6.0	0.5
$M_{4A,C}$	8	1	1.5	0.5	$M_{4B,D}$	2	4	1.5	0.5
M_{5A}	16	1	6.0	0.5	M_{5B}	2	8	6.0	0.5
M_{6A}	8	2	1.5	0.5	M_{6B}	2	4	1.5	0.5

Source: Author

Figure 30a shows the high-pass filter transconductor DC characteristic curve, which has a similar shape to the previously discussed current controlled voltage source transconductor. This behavior was expected, since both transconductors have the same biasing voltages and transistor array dimensions. The only difference is the current mir-

rors, which decreases the input current magnitude for the same input voltage, resulting in a maximum resistance of 6.6 GΩ, which is about 16000× greater than the other transconductor. Considering the high-pass filters A and B respective capacitances C_{HPB} and C_{HPC}, the resulting corner frequencies f_{cB} and f_{cC} are 30 and 2.7 Hz, respectively.

Figure 30 – High-pass filter transconductor DC characteristic curve

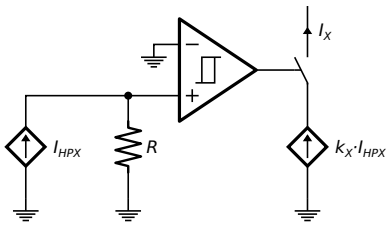


(a) Input current × input voltage (b) Resistance × input voltage

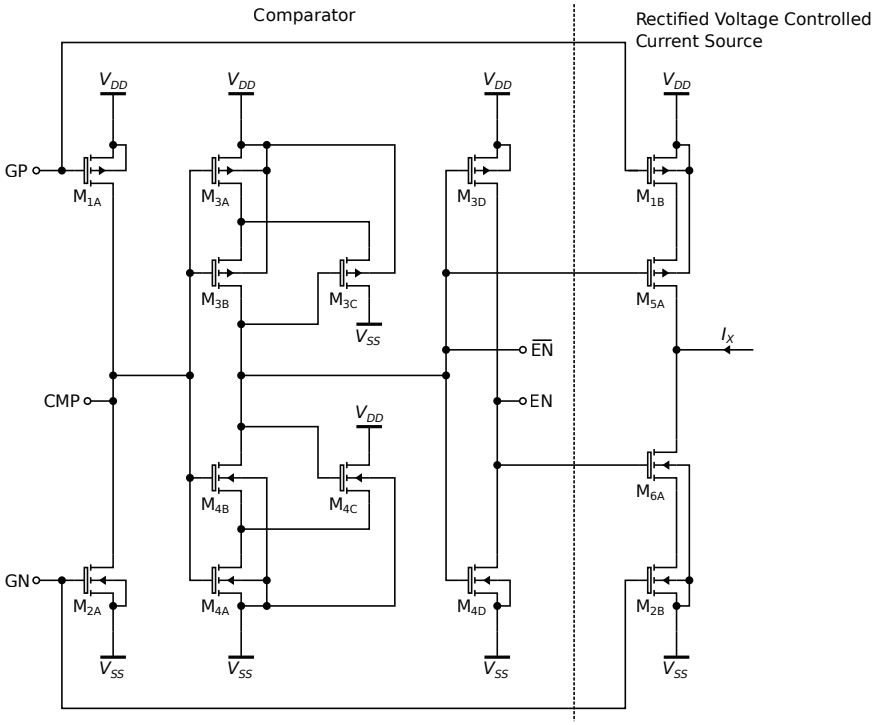
Source: Author

Figure 31 shows the SA-I rectified current controlled current source circuit diagram and Table 6 shows each transistor arrays dimensions. Both current controlled current sources B and C have the same circuit topology, only differing by the dimensions of transistors M_{2A} and M_{2B}.

Figure 31 – SA-I rectified current controlled current source circuit diagram



(a) Simplified circuit diagram



(b) Transistor level circuit diagram

Source: Author

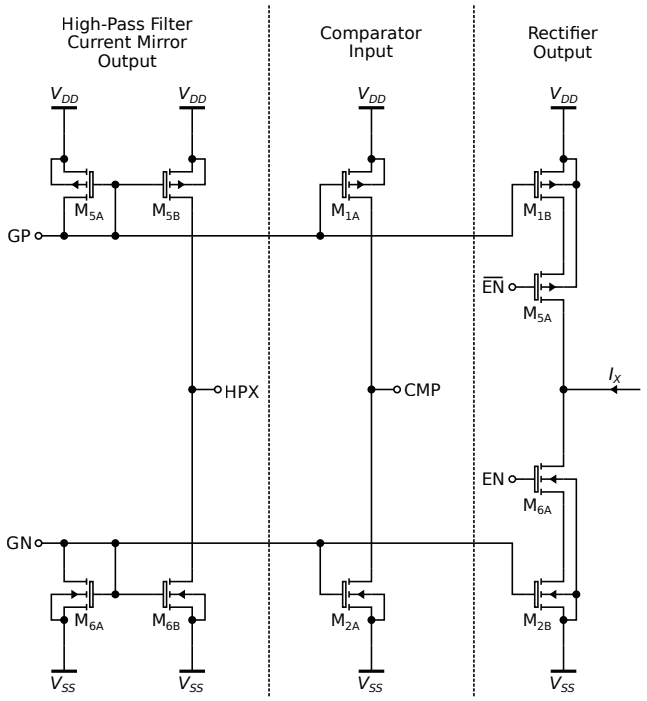
Table 6 – SA-I rectified current controlled current source circuit array dimensions

	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
M_{1A}	4	2	6.0	0.5	M_{1B}	4	2	6.0	0.5
$M_{2A}(I_B)$	16	8	1.5	0.5	$M_{2B}(I_B)$	16	8	1.5	0.5
$M_{2A}(I_C)$	2	8	1.5	0.5	$M_{2B}(I_C)$	2	8	1.5	0.5
M_{3A}	16	1	6.0	0.5	M_{3B}	8	1	6.0	0.5
M_{3C}	2	4	6.0	0.5	M_{3D}	2	1	6.0	0.5
M_{4A}	16	1	1.5	0.5	M_{4B}	8	1	1.5	0.5
M_{4C}	2	4	1.5	0.5	M_{4D}	2	1	1.5	0.5
M_{5A}	2	1	6.0	0.5	M_{6A}	2	1	1.5	0.5

Source: Author

This current sources receives as input voltages V_{GP} and V_{GN} from the high-pass filter current mirrors, so it can replicate, amplify and rectify the attenuated transconductor output current I_N. The high-pass filter second current mirror, as shown in Figure 29, is connected to the rectifier, shown in Figure 31, with the terminals GP and GN, as depicted in the simplified diagram shown in Figure 32. This is the direct application of the multiple output transconductor technique (WU, J.; EL-MASRY, 1998).

Figure 32 – High-pass current mirror with multiple outputs



Source: Author

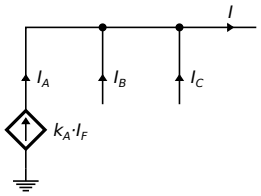
The rectified output current is proportional to I_N, so $I_X = k_X I_N$, where k_X is the ratios between S_{6B}, from the high-pass filter transistor output, and S_{2B}, from the rectifier circuit. The same current is replicated at the comparator input, and generates

the voltage V_{CMP}, and the digital control signals EN and $\overline{\text{EN}}$. The comparator circuit itself is made of a Schmitt trigger and an inverter, and shows a small hysteresis.

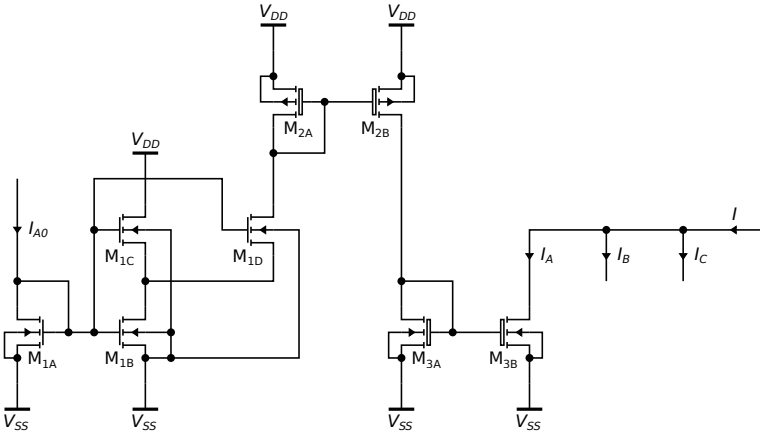
The current component I_A is proportional to the the input current I_F. Figure 33 shows the summer and Table 7 shows its transistor arrays dimensions. This circuit attenuates the input current I_F by a $1/k_A$ factor and sums the resulting current I_A with the other currents I_B and I_C. Its current mirrors are similar to the ones present in the high-pass filter circuit, and so outputs a current attenuated by

$$k_A \approx \frac{I_{A0}}{I_F} \cdot \frac{S_{1B}}{S_{1A}} \cdot \frac{S_{1D}}{S_{1C}} \cdot \frac{S_{2B}}{S_{2A}} \cdot \frac{S_{3B}}{S_{3A}} \tag{20}$$

Figure 33 – SA-I current summer circuit diagram



(a) Simplified circuit diagram



(b) Transistor level circuit diagram

Source: Author

Table 7 – SA-I current summer circuit array dimensions

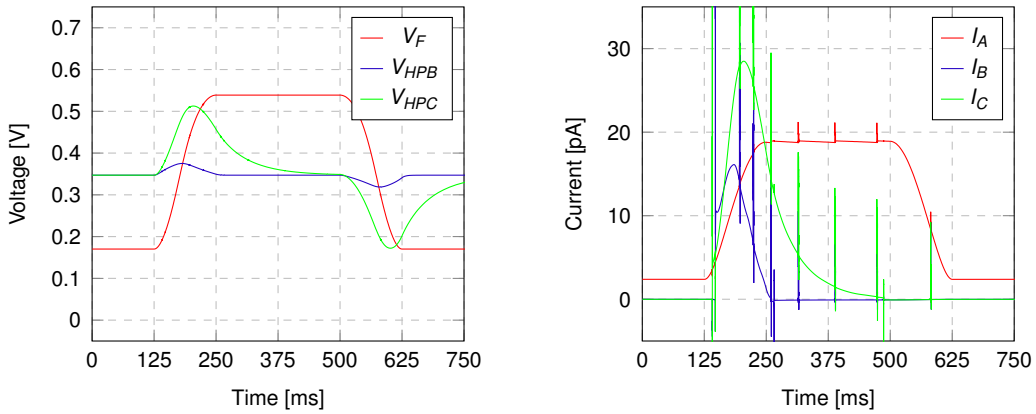
	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A,C}$	8	1	1.0	0.5	$M_{1B,D}$	2	4	1.0	0.5
M_{2A}	16	1	6.0	0.5	M_{2B}	2	8	6.0	0.5
M_{3A}	8	2	1.0	0.5	M_{3B}	2	4	1.0	0.5

Source: Author

Figures 34a and 34b shows the SA-I ASP transient simulation results for a 0.7 V supply voltage, 200 nA I_{BIASB}, and 700 nA I_{BIASF}, at room temperature and typical process parameters. The current input I_F generate the signal voltages V_F at the current

controlled voltage source, and signal voltages V_{HPA} and V_{HPB} for their respective high-pass filters. Then it outputs the current components I_A, I_B and I_C, which will compose the SA-I ASP output current I. This current is going to feed the current controlled oscillator, which implements the leaky integrate-and-fire neuron model.

Figure 34 – SA-I ASP transient simulation results



(a) Voltage signals

(b) Current signals

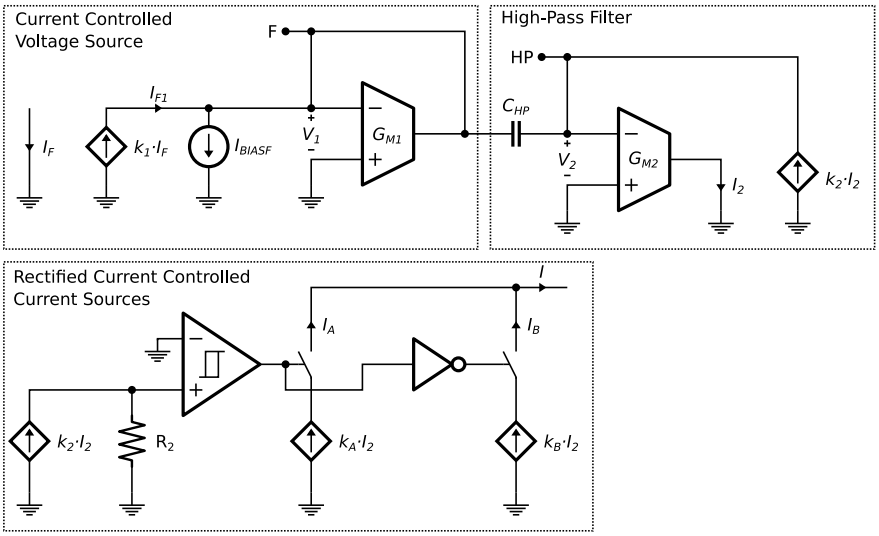
Source: Author

4.3.2 FA-I Analog Signal Processing

The FA-I ASP circuit diagram, shown in Figure 35 is similar to the SA-I ASP. The key differences are that it does not have a static current, and that the current components I_A and I_B are generated by the same high-pass filter block to save area and power. The FA-I high-pass filter is exactly the same as the SA-I high-pass filter C. The rectified current controlled current sources are similar to a full-wave signal rectifier with different gains for the positive and negative signal input excursion.

Figure 36 shows the FA-I rectified current controlled current source circuit diagram. As the SA-I counterpart, it also has a Schmitt trigger and inverter to generate the control signals EN and $\overline{\text{EN}}$. However, there is an additional circuit that inverts the current signal mirrored from the high-pass filter, and it is enabled only when the other signal is disabled.

Figure 35 – FA-I ASP complete circuit diagram



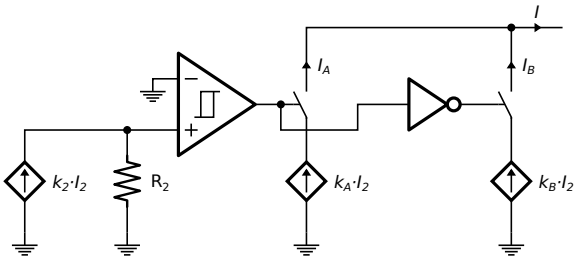
Source: Author

Table 8 – FA-I rectified current controlled current source circuit array dimensions

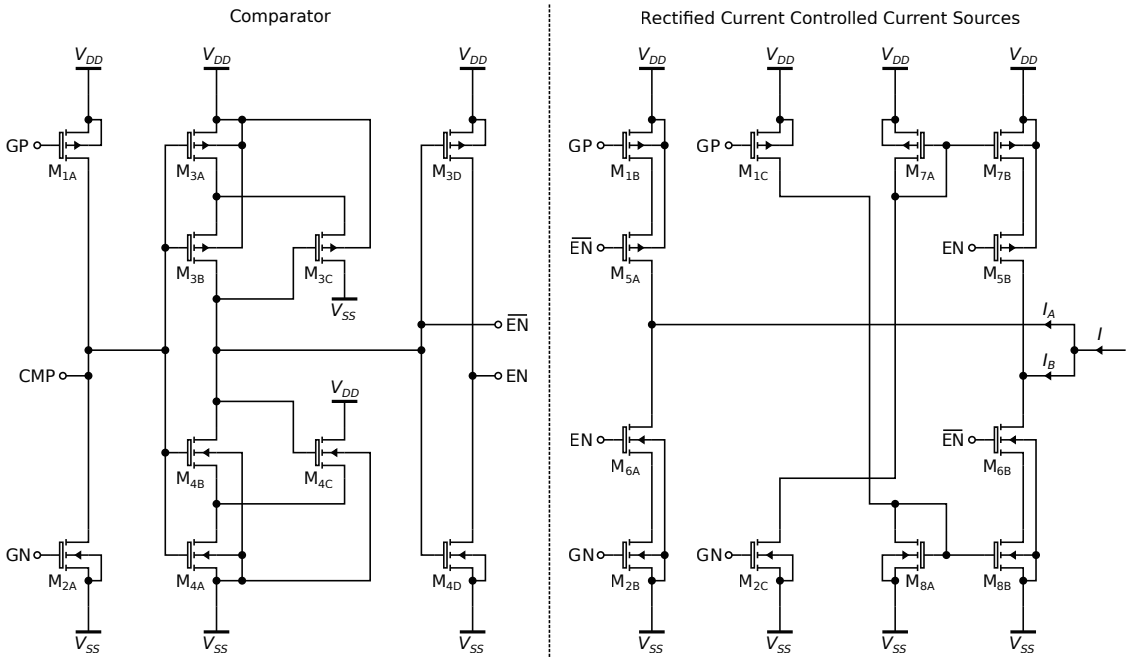
	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
M_{1A}	4	2	6.0	0.5	M_{1B}	3	4	6.0	0.5
M_{2A}	4	2	1.5	0.5	M_{2B}	3	4	1.5	0.5
M_{3A}	16	1	6.0	0.5	M_{3B}	8	1	6.0	0.5
M_{3C}	2	4	6.0	0.5	M_{3D}	2	1	6.0	0.5
M_{4A}	16	1	1.5	0.5	M_{4B}	8	1	1.5	0.5
M_{4C}	2	4	1.5	0.5	M_{4D}	2	1	1.5	0.5
$M_{5A,B}$	2	1	6.0	0.5	$M_{6A,B}$	2	1	1.5	0.5
M_{1C}	2	4	6.0	0.5	M_{2C}	2	4	1.5	0.5
$M_{7A,B}$	2	4	6.0	0.5	$M_{8A,B}$	2	4	1.5	0.5

Source: Author

Figure 36 – FA-I rectified current controlled current source circuit diagram



(a) Simplified circuit diagram

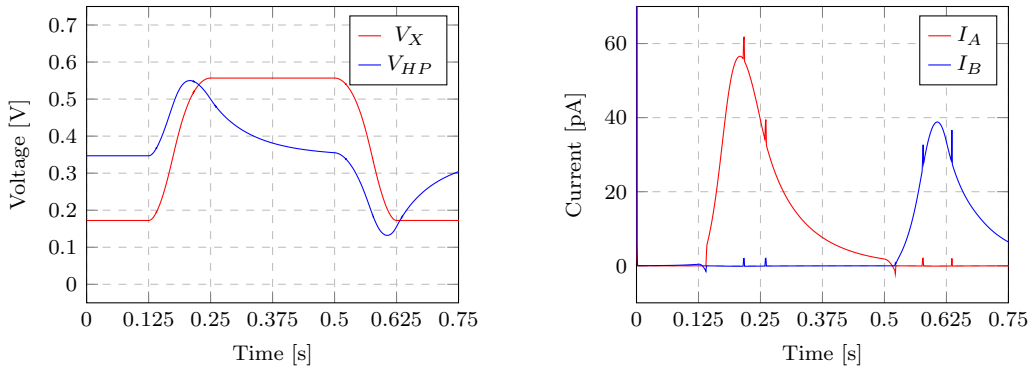


(b) Transistor level circuit diagram

Source: Author

Figures 37a and 37b shows the FA-I ASP transient simulation results for the same conditions used in the SA-I simulations. The current input I_F generate the high-pass signal voltage V_{HP}. Then it outputs the rectified current components I_A, and I_B, which will compose the FA-I ASP current output I.

Figure 37 – FA-I ASP transient simulation results



(a) Voltage signals

(b) Current signals

Source: Author

4.4 CURRENT CONTROLLED OSCILLATOR (CCO)

The previously proposed transducer and ASP circuits together are the transduction sub-model implementations of the mechanoreceptor model discussed in Chapter 3. The neuronal dynamics sub-model can have many different circuit implementations (INDIVERI et al., 2011). In this work, the simplest model was chosen: the leaky integrate-and-fire. This model can be implemented by the Current Controlled Oscillator (CCO) circuit shown in Figure 38, which is a variation of the conventional Schmitt trigger based relaxation oscillator (SINISCALCHI et al., 2020). Its transistor array dimensions are shown in Table 9.

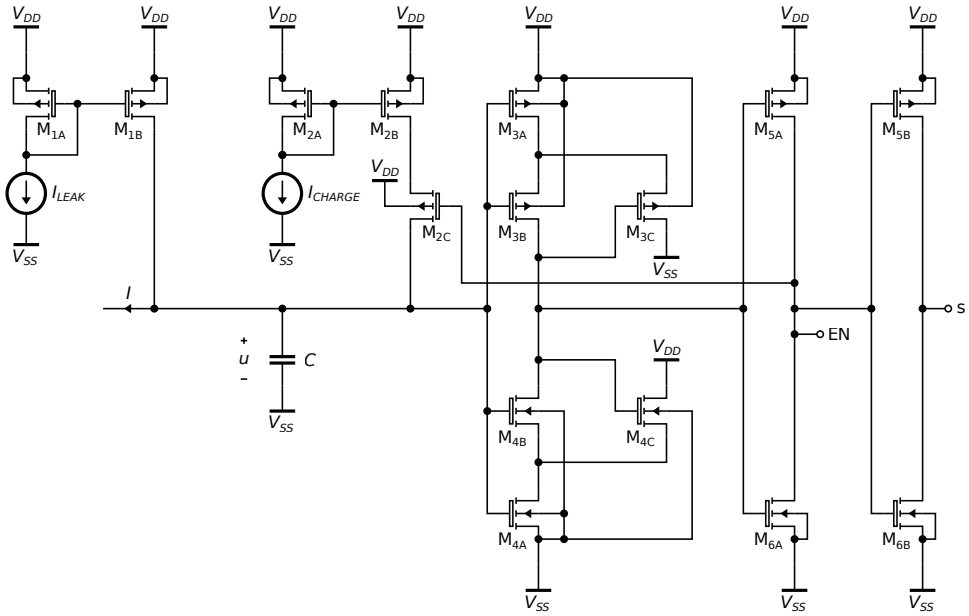
Table 9 – CCO circuit array dimensions

	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A,B}$	2	4	6.0	0.5	$M_{2A,B}$	2	4	6.0	0.5
M_{3A}	16	1	6.0	0.5	M_{4A}	16	1	1.5	0.5
M_{3B}	2	4	6.0	0.5	M_{4B}	2	4	1.5	0.5
M_{3C}	8	1	6.0	0.5	M_{4C}	8	1	1.5	0.5
$M_{5A,B}$	2	1	6.0	0.5	$M_{6A,B}$	2	1	1.5	0.5

Source: Author

This circuit implements the leaky integrate-and-fire sub-model B, described by (6). Transient simulation results with 2 pA leakage current I_{LEAK}, 1 nA charging current

Figure 38 – Current controlled oscillator (CCO) circuit diagram



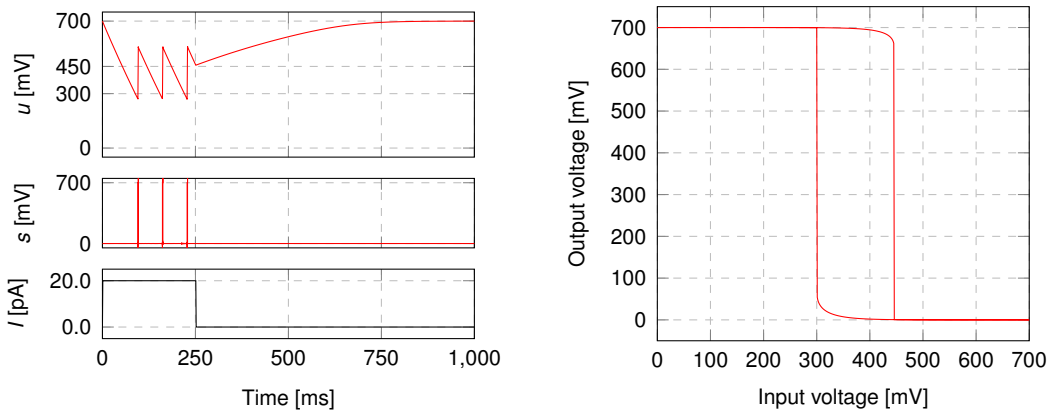
Source: Author

I_{CHARGE}, and 1.8 pF input capacitance C is shown in Figure 39. The circuit implementation differs from the previously discussed sub-model, as its operation is reversed. The membrane resting potential u_{rest} is at the supply voltage at steady state, if the input current I is less than the I_{LEAK}. If $I > I_{LEAK}$, then the capacitor is discharged, instead of charged, until it reaches the voltage threshold ϑ, then the capacitor is charged by a current $I_{CHARGE} - I$ until the membrane potential u reaches the reset potential u_{rst}. Both ϑ and u_{rst} are limited by the Schmitt trigger hysteresis window, as shown in Figure 39b. Schmitt trigger design for ultra-low-voltage supplies and hysteresis window characterization is further detailed in (MELEK, L. A. P. et al., 2016; SILVA JÚNIOR et al., 2021). Additionally, its hysteresis window size can be controlled by forward-body-bias, as proposed in (RODOVALHO, 2020b).

It is worthy noticing that those thresholds are not exactly defined by the hysteresis window, since there is a switching delay between the charging current on and off states. The other non-ideal aspect of this circuit implementation is that the leakage current is not constant for any u. As it approaches the supply voltage, the current mirror output transistor M_{1B} starts operating in the linear region and it behaves as a resistor, instead of a current source.

The full mechanoreceptor system is composed of the transduction sub-model, implemented by the transducer and ASP modules, and the neuronal dynamics sub-model, implemented by the CCO. By connecting the the SA-I ASP output current I at the CCO input, biased with a single 5 pA I_{LEAK}, a 1 nA I_{CHARGE}, and a single 30×30 1.8 pF C, for typical process parameters, 0.7 V supply voltage and room temperature,

Figure 39 – CCO standalone transient and DC simulation results

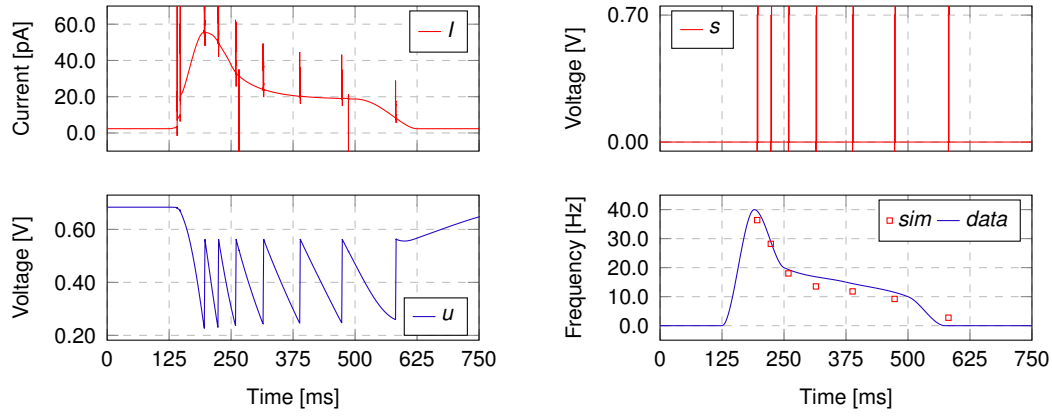


(a) Transient simulation (b) Schmitt trigger DC characteristic curve

Source: Author

the whole mechanoreceptor system simulation outputs the signals shown in Figures 40a and 40b. As can be seen, at each firing event, marked the CCO output signal *s*, the membrane potential *u* charges very fast, causing glitches in the input signal *I*. There is also a *I* initial glitch due to rectification of the dynamic current components I_A and I_B. Otherwise, the CCO instantaneous firing frequency is similar to the model numerical computation simulations shown in Figure 18c, which is itself similar to the intended SA-I mechanoreceptor firing patterns extracted from experimental data (BIRZNIEKS et al., 2001), as shown in Figure 5a.

Figure 40 – SA-I CCO transient simulation input and output signals



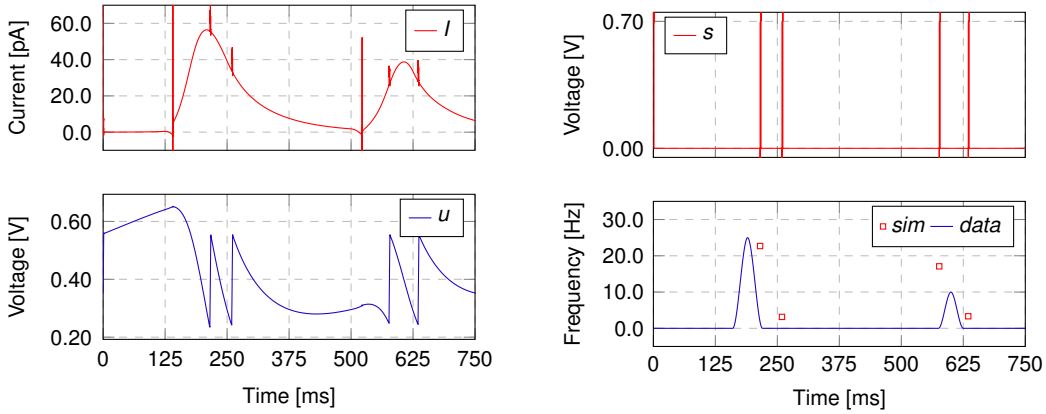
(a) Input signals (b) Output signals

Source: Author

The FA-I artificial analog mechanoreceptor implementation is similar to the SA-I one. However, besides using the FA-I ASP output *I*, the CCO input capacitance is increased to 5.4 pF, using three parallel 30 $\times$ 30 µm MIM capacitor. Also as expected, the FA-I artificial analog mechanoreceptor, has a similar signals and firing pattern to the

numerical computation model, so they match closely the mechanoreceptor experiment results, as shown in Figures 41a and 41b.

Figure 41 – FA-I CCO signals



(a) Input signals (b) Output signals

Source: Author

4.5 CHAPTER SUMMARY

The analog artificial mechanoreceptor system was divided into three parts: transducer, analog signal processing (ASP) module and current controlled oscillator (CCO). The chosen transducer topology was the force-to-current kind instead of the force-to-voltage one, as it allows lower supply voltage operation, and consequently, lower power consumption.

The SA-I and FA-I ASP modules, which are the analog implementation of the transduction sub-models proposed in the last chapter, use analog blocks to implement their digital counterparts, performing operations such as differentiation, rectification, multiplication and addition. In special, an ultra low transconductance was needed to implement the very low high-pass filters corner frequencies which was needed by the differentiation operation.

The Schmitt trigger based CCO is a rather simple circuit whose behavior is similar to the leaky integrate-and-fire neuron used by the mechanoreceptor model. Finally, the transducer, ASP and CCO were simulated together and its results were compared to the available experimental data, and thus, validated its functionality.

5 CONCLUSION

The electronic interface between a prosthesis and its user must translate its sensor electrical signals into a format that the user brain can understand, to restore the sense of touch and tactile feedback. The focus of this thesis was to model and design artificial mechanoreceptors to mimic its biological counterparts, so this interface translation could be more accurate.

The proposed mechanoreceptor model was an adaptation of previous ones already found in the medical sensors literature, with a small changes to reflect the non-ideal behavior of analog electronic circuits. This adapted model was used in the design of two kinds of analog artificial mechanoreceptors: the Slow Adapting type I and the Fast Adapting type II. Both were designed using a real integrated circuit process design kit. The transistor level simulations showed that the proposed artificial mechanoreceptor output has a similar response to a biological one, as compared to measurement results taken from literature.

Many novel analog circuit design techniques were used to implement the artificial mechanoreceptor, in special inverter-based ultra-low transconductance and ultra-low-voltage amplifiers. These circuit techniques are not exclusive to analog artificial mechanoreceptors, as their target use is very wide. So, they could be further explored and used in another biomedical applications. Furthermore, the same mechanoreceptor could be used as an interface between real world stimulus advanced spike-based neural networks.

This thesis findings were limited to simulation results only. Future works should use the actual implementation of an artificial mechanoreceptor prototype and comparison with a larger dataset of biological mechanoreceptor signals. Later, the integrated circuit prototype could be paired with a real prosthesis and make an interface with its user, so its main objective could be accomplished.

Appendix

APPENDIX A – UNIFIED CURRENT CONTROL MODEL

In this work, the circuit analysis is derived from the all-region MOSFET model Unified Current Control Model (SCHNEIDER; GALUP-MONTORO, 2010) described by the Equations (21), (22) and (23). Considering that the MOSFET is a symmetrical device, the transistor drain current I_D is the subtraction of the forward and reverse currents I_F and I_R, as shown in (21). The forward and reverse currents are proportional to the forward and reverse inversion coefficients i_f and i_r and the normalization current I_S, as shown in (22), which is function of the charge mobility μ, the oxide capacitance per area C'_{ox}, the slope factor n, the thermal voltage ϕ_t and the channel width and length W and L. The forward and reverse inversion coefficients, also considering the MOSFET symmetrical behaviour, can be described by the function $f(i)$, shown in (23), which is equal to the function $f(V)$ of the pinch-off voltage V_P, the source or drain voltages V_S and V_D and the thermal voltage ϕ_t.

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{21}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SQ} \frac{W}{L} \tag{22}$$

$$\begin{gathered} f(V) = f(i) \\ \frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \end{gathered} \tag{23}$$

Considering the approximation for the pinch-off voltage

$$V_P \approx \frac{V_{GB} - V_T}{n} \tag{24}$$

where, V_T is the transistor threshold voltage, the inversion coefficient function $f(V)$, described in (25), can be formulated considering the transistor terminal voltages referred to the bulk terminal voltage V_B (V_{GB} and $V_{S(D)B}$) or to the source and drain terminal voltage V_S and V_D ($V_{GS(D)}$ and $V_{BS(D)}$).

$$f(i) = \frac{V_P - V_{S(D)B}}{\phi_t} \approx \frac{V_{GB} - V_T - nV_{S(D)B}}{n\phi_t} = \frac{V_{GS(D)} + (n-1)V_{BS(D)} - V_T}{n\phi_t} \tag{25}$$

If the MOSFET is biased in the saturation operation region ($i_f \gg i_r$), so $I_D \approx I_S i_f$, then drain current is function of the voltage differential between the gate-source and bulk-source differential voltages V_{GS} and V_{BS}. This way, the bulk terminal can be modeled as a second gate terminal with its effectiveness attenuated by a factor $(n-1)$.

The transistor small-signal transconductances g_{mg}, g_{mg}, g_{mg} and g_{mg}, are defined as the partial derivatives

$$g_{mg} = \frac{\vartheta I_D}{\vartheta V_G}; g_{ms} = \frac{\vartheta I_D}{\vartheta V_S}; g_{md} = \frac{\vartheta I_D}{\vartheta V_D}; g_{mb} = \frac{\vartheta I_D}{\vartheta V_B}; \tag{26}$$

and are related to each other by the equation

$$g_{mg} + g_{md} + g_{mb} = g_{ms}; \tag{27}$$

The source and gain transconductances can be expressed as function of the inversion level, so

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{28}$$

Furthermore, it can be shown that, by definition,

$$\frac{g_{mg}}{g_{mb}} = (n-1) \tag{29}$$

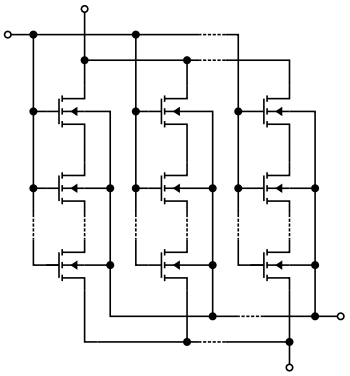
and by combining (27) and (29)

$$g_{mg} = \frac{g_{ms} - g_{md}}{n} \tag{30}$$

APPENDIX B – TRANSISTOR ARRAYS

B.1 RECTANGULAR TRANSISTOR ARRAYS

Figure 42 – Rectangular array circuit diagram



Source: Author

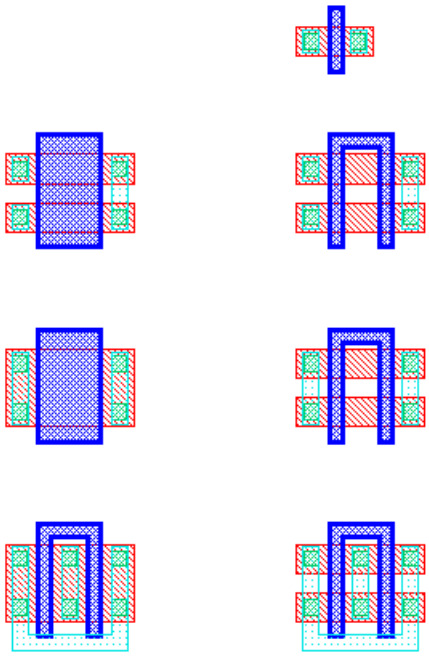
Composite series transistor or transistor arrays, such as those shown in Figures 42 and 44 can be modeled as a single transistor (GALUP-MONTORO et al., 1994) with a higher output impedance (ARNAUD et al., 2006; SILVA, Rafael Sanchotene et al., 2019; BRAGA et al., 2019). The rectangular array, shown in Figure 42, is a m by n matrix of single transistors composed by m parallel columns of n series single transistors. The rectangular equivalent transistor aspect ratio S_{eq} is a function of the single transistor aspect ratio S_u, as shown in (31). The rectangular array total gate area $A = (mn)A_u$, where A_u is the gate area of the single transistor.

$$S_{eq} = \frac{W_{eq}}{L_{eq}} = \frac{m \cdot W_u}{n \cdot L_u} = \frac{m}{n} \cdot S_u \tag{31}$$

Figure 43 shows the layout of several rectangular transistor arrays using the TSMC 180 nm process design kit. Transistor A is a minimum length single transistor. Transistor arrays B1, C1 and D1 are series, single and parallel transistor arrays, respectively, using the exact same area. Transistors arrays B2, C2 and D2 are rectangular arrays made of four single minimum length transistors each, but arranged in distinct ways.

Table 10 shows the transistor array dimensions. As can be seen, all transistor arrays, with the exception of transistor A, have the same total area calculated by the perimeter of the square including the dark blue polysilicon layer and the red diffusion layer. It also can be shown that transistor arrays B1 and D1 has the lowest and highest equivalent aspect ratio S_{eq}, respectively, and single transistor C1 has the most active area A per total area A_T. Transistor arrays B2, C2 and D2 has the same active area, but all of them have less than its simpler counterparts, since there are design rules

Figure 43 – Rectangular array layout



dictating the minimum pitch between transistor channels drawn by the polysilicon layer and a minimum pitch between different diffusion layers.

Table 10 – Rectangular arrays dimensions

	m	n	W [µm]	L [µm]	S_{eq}	A [µm^2]	A_T [µm^2]	A/A_T
A	1	1	0.42	0.18	2.3333	0.0756	1.0120	0.075
B1	1	2	0.42	0.90	0.2333	0.7560	3.0132	0.251
B2	1	4	0.42	0.18	0.5833	0.3024	3.0132	0.100
C1	1	1	1.12	0.90	1.2444	1.0800	3.0132	0.335
C2	2	2	0.42	0.18	2.3333	0.3024	3.0132	0.100
D1	2	1	1.12	0.18	12.444	0.4032	3.0132	0.134
D2	4	1	0.42	0.18	9.3333	0.3024	3.0132	0.100

Source: Author

In order to compare the electrical characteristic of each transistor array, DC and AC simulations were run to extract the transistor array drain current I_D, threshold voltage V_T and its gate, source, drain and bulk small-signal transconductances g_{md}, g_{mg}, g_{ms} and g_{mb}. All simulations set $V_G = V_D = 0.5$ V and $V_B = V_S = 0.0$ V, except for the V_T extraction, where $V_D = 0$ V. Tables 11 and 12 show the simulation results summary.

First of all, transistors arrays A, B1, C1 and D1 have different single transistor lengths and widths. This reflects on the extracted V_T, as transistors with different channel dimensions also have different threshold voltages (RATNAKUMAR, 1982) due to drain-induced barrier lowering (Drain Induced Barrier Lowering (DIBL)). Consequently, despite all transistors having the same terminal voltages, they output different

Table 11 – Rectangular arrays small-signal parameters I

	g_{md} [nS]	g_{mg} [µS]	g_{ms} [µS]	g_{mb} [µS]	I_D [µA]	V_T [mV]
A	1.021	31.83	41.28	8.430	2.141	531.7
B1	0.013	3.272	4.154	0.869	0.240	479.6
B2	0.067	7.691	9.809	2.051	0.510	531.7
C1	0.079	13.97	17.91	3.857	0.853	501.4
C2	0.498	30.67	39.34	8.165	2.048	531.7
D1	3.808	125.2	163.3	34.31	6.928	553.7
D2	4.085	127.3	165.5	33.72	8.565	531.7

Source: Author

Table 12 – Rectangular arrays small-signal parameters II and I_D mismatch

	g_{mg}/I_D [V^{-1}]	I_D/g_{md} [V]	g_{mg}/g_{md} [dB]	g_{mg}/g_{mb} -	g_{mg}/A [µS/µm^2]	σ_{I_D}/μ_{I_D} [%]
A	14.87	2.10	29.9	0.265	421.0	15.6
B1	13.63	18.4	48.0	0.265	4.328	4.41
B2	15.07	7.65	41.2	0.266	25.43	8.00
C1	16.38	10.8	45.0	0.276	13.86	4.39
C2	14.98	4.11	35.8	0.266	101.4	7.73
D1	18.02	1.82	30.3	0.274	310.5	7.97
D2	14.86	2.10	29.9	0.265	421.0	7.41

Source: Author

transconductance-to-current ratios g_{mg}/I_D, as they operate in different inversion levels.

As transistor arrays A, B2, C2 and D2 have the same single transistor dimensions, they all have the same threshold voltage V_T. Transistor arrays A and C2 have the same aspect ratio S_eq, so they output approximately the same drain current I_D. Transistor arrays B2 and D2 output approximately 0.25 and 4 times the C2 current. Moreover, all transistor arrays have the same g_{mg}/I_D ratio (SILVEIRA et al., 1996), an important parameter in analog circuit design. This behavior is also the key aspect of highly area-efficient non-unity gain current mirrors based on transistor arrays (FIORELLI et al., 2004), which were used extensively in this thesis.

The single transistor A and the transistor array C2 have the same equivalent aspect ratio S_eq, however, transistor A outputs a higher drain current I_D. This is the result of short-channel effects and channel length modulation (ARORA, 2012), as both transistor arrays have different Early voltages $V_A = g_{md}/I_D$. The Early voltage itself can be simplified as $V_A = V_E L$, where V_E is a technology dependent parameter and L is the channel length. It can be shown that B2 and C2 have equivalent channel length L_{eq} 4× and 2× larger than A1, respectively, and it reflects proportionally on the their respective V_A values. Transistor array B1, however, still has the highest V_A and, consequently, the larger intrinsic voltage gain $A_V = g_{mg}/g_{md}$ than B2, despite using the same total area

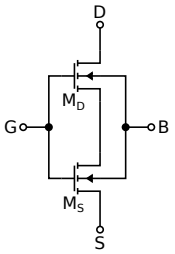
A_T.

Furthermore, their gate transconductances g_{mg} are also proportional to their aspect ratios. Since they have the same active area, they have widely different g_{mg}/A ratios. This way, high performance and low area analog circuits should avoid using series arrays. The opposite is true for ultra-low-transconductance amplifiers, as the main goal is to attain lower transconductances per area. Another key aspect of rectangular arrays are that they have similar g_{mg}/g_{mb} ratios, resulting in approximately the same transistor slope factors n, so different arrays can be forward-body-biased by the same biasing circuit.

Additionally, 1000 mismatch only (no global process variability enabled) monte carlo simulation runs were performed. The transistor mismatch is proportional to the active area square root (PELGROM et al., 1989) and the transistor inversion (SCHNEIDER; GALUP-MONTORO, 2010). Consequently, transistor arrays B2, C2 and D2 have approximately half the transistor A drain current mismatch, show as the ratio between the drain current standard deviation σ_{I_D} and average μ_{I_D}. Even so, transistor array C1 has the least mismatch, as it has a larger active area, despite using the same total area than the other arrays.

B.2 TRAPEZOIDAL TRANSISTOR ARRAYS

Figure 44 – Composite transistor circuit diagram



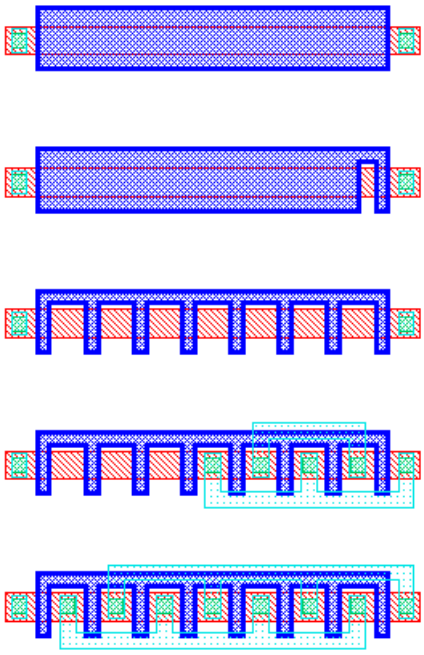
Source: Author

The composite transistor, shown in Figure 44, is composed by two separate transistors M_D and M_S. The composite transistor equivalent aspect ratio S_{eq} is a function of each composing transistors aspect ratio S_D and S_S, as shown in (32).

$$S_{eq} = \frac{S_D \cdot S_S}{S_D + S_S} \tag{32}$$

Trapezoidal arrays are composite transistors made of rectangular arrays using the same single transistor dimensions. Since every single transistor has the same dimension, all transistors have the same characteristics. In order to compare the trapezoidal array effectiveness, five transistor arrays were designed using the same total area A_T, as shown in Figure 45. Table 13 shows their respective dimensions.

Figure 45 – Composite transistor layout



Source: Author

Table 13 – Trapezoidal arrays dimensions

		m	n	W [µm]	L [µm]	S_{eq}	A [µm^2]	A_T [µm^2]	A/A_T
E		1	1	0.42	5.22	0.0805	2.1924	5.6856	0.386
F	M_D	1	1	0.42	4.79	0.0845	2.0874	5.6856	0.367
	M_S	1	1	0.42	0.18				
G1	M_S	1	1	0.42	0.18	0.2917	0.6048	5.6856	0.106
	M_D	1	7	0.42	0.18				
G2	M_D	4	1	0.42	0.18	0.5490	0.6048	5.6856	0.106
	M_S	1	4	0.42	0.18				
G3	M_D	7	1	0.42	0.18	2.0416	0.6048	5.6856	0.106
	M_S	1	1	0.42	0.18				

Source: Author

Transistor E is a single transistor with the maximum length allowed by the area restrictions. Composite transistor F is made of (GIRARDI et al., 2005) two transistors with different channel lengths and the same width. Trapezoidal transistor arrays G1, G2 and G3 are made of eight transistors arranged in different ways. Transistor array G1, specially, could be described as a single rectangular series array.

AC, DC and monte carlo simulations were run with similar operation conditions than the previous rectangular array ones and their results are summarized in Tables 14 and 15. First of all, transistor E has an active area about 4$\times$ than G1, despite using the same total area. Consequently, it has half of the resulting drain current mismatch. Although G1, G2 and G3 have the same active area, G3 mismatch is much greater. In

fact, its drain current, aspect ratio and mismatch is similar to the previously simulated single transistor A, except it has a Early voltage V_A 10$\times$ larger.

Table 14 – Trapezoidal arrays small-signal parameters I

	g_{md} [nS]	g_{mg} [µS]	g_{ms} [µS]	g_{mb} [µS]	I_D [µA]	V_T [mV]
E	31.73	1.550	1.963	0.410	0.120	441.4
F	36.85	1.587	2.010	0.419	0.123	442.6
G1	180.7	3.886	4.941	1.038	0.256	531.7
G2	103.5	6.988	8.869	1.870	0.461	531.7
G3	691.1	23.52	29.91	6.316	1.531	531.7

Source: Author

Table 15 – Trapezoidal arrays small-signal parameters II and I_D mismatch

	g_{mg}/I_D [V^{-1}]	I_D/g_{md} [V]	g_{mg}/g_{md} [dB]	g_{mg}/g_{mb} -	g_{mg}/A [nS/µm^2]	σ_{I_D}/μ_{I_D} [%]
E	12.96	37.82	53.8	0.264	0.709	2.36
F	12.90	33.38	52.7	0.264	0.760	2.51
G1	15.18	14.17	46.7	0.267	6.425	5.77
G2	15.17	44.54	56.6	0.268	11.55	7.46
G3	15.36	22.15	50.6	0.269	38.89	14.9

Source: Author

The single transistor E and composite transistor F Early voltage and intrinsic voltage gains are similar. In fact, composite transistor F voltage gain is slightly lower. It is a consequence of its transistor M_D, which is a single transistor with minimum length, having a much larger threshold voltage V_T than its transistor M_S, which negates this technique effectiveness for these simulation operation conditions and design process kit. The solution is to increase M_D width, but that would also increase the total area and decrease the active area per total area ratio A/A_T.

The rectangular array G1 has a considerably smaller intrinsic voltage gain than single transistor E. However, the trapezoidal array G2 has the largest voltage gain. G2 also shows slightly more mismatch than G1, but significantly less mismatch than G3. G2 main design characteristic is that it combines parallel and series arrays, similarly as previously done with non-unity gain current mirrors (FIORELLI et al., 2004).

Although the simulations presented here show that rectangular arrays are less effective than single transistors with larger channel lengths and same area, for different fabrication process technologies, the opposite can be true (FERREIRA; SONKUSALE, 2014), due to halo implants needed in more advanced transistor technologies.

Nevertheless, the main advantage of transistor arrays is not voltage gain or mismatch reduction. Their advantage for circuit design is the extreme regular layouts

and parameter predictability, as only a single transistor needs to be characterized. Moreover, conventional parallel-series current mirrors can replace its series arrays with trapezoidal ones and implement the current-splitting technique (RODOVALHO et al., 2021) in ultra-low-transconductance OTAs.

APPENDIX C – CURRENT MIRRORS

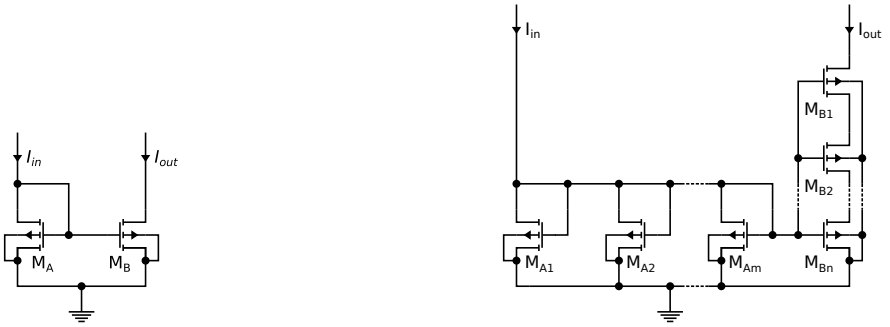
C.1 BASIC CURRENT MIRRORS

Figure 46a shows a conventional current mirror. If the transistors M_A and M_B are identical and both transistors are biased in the saturation region ($I_D \approx I_F$), it can be concluded that the output current I_{out} is approximately the input current I_{in}. If the transistors have different aspect ratios, then

$$I_{out} = A_I I_{in} = \frac{S_B}{S_A} I_{in} \tag{33}$$

where A_I is the current gain, which is is the ratio of the transistors M_A and M_B aspect ratios S_A and S_B, which is valid considering that both transistors have the same threshold voltage V_T.

Figure 46 – Current mirror



(a) Current mirror (b) Series-parallel current mirror

Source: Author

Process variability aside, transistors with different channel lengths have different threshold voltages (RATNAKUMAR, 1982) due to drain-induced barrier lowering (DIBL). A better current mirror can be designed by replacing transistors M_A and M_B with transistor arrays, as result the output current I_{out} is the ratio of their respective equivalent aspect ratios. Figure 46b is an example of parallel-series current mirror composed by a transistor array M_A consisting of m parallel transistors and by a transistor array M_B consisting of n series transistors, so

$$I_{out} = \frac{S_{eq-B}}{S_{eq-A}} I_{in} = \frac{I_{in}}{mn} = \frac{I_{in}}{N^2} \tag{34}$$

In addition to DIBL, the current mirror output current is also function of the transistor channel length L and the drain-source voltage V_{DS} due to the channel-length modulation effect (CLM) (ARORA, 2012). The output current I_{out} itself can be approximated as a first order function

$$I_{out} = A_I I_{in} + V_{out} G_o \tag{35}$$

where the output conductance G_o, the inverse of the output impedance R_{out}, is a function of the Early voltage V_A, which is itself function of a technological parameter V_E and the channel length L, as shown in (36).

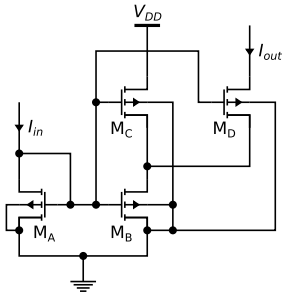
$$G_o = \frac{1}{R_o} = \frac{dI_{out}}{dV_{DS}} \approx \frac{I_{out}}{V_A} = \frac{I_{out}}{V_E L} \tag{36}$$

C.2 CURRENT SPLITTING CURRENT MIRROR

Series-parallel current mirrors can achieve greater current gain, reduced area usage and less process variability compared to to parallel-only current mirrors (FIORELLI et al., 2004). This technique was used in (ARNAUD et al., 2006) to achieve very low transconductance OTAs without sacrificing linearity and process variability tolerance.

The parallel-series current mirror attenuation can be further improved by replacing the series transistor array by a trapezoidal transistors array, as shown in Figure 47.

Figure 47 – Current splitting current mirror



Source: Author

The trapezoidal array is made of transistors $M_{B\text{-}D}$, however, the current mirror output is connected to M_D drain terminal only, so M_B drain current I_{D-B} splits between M_C and M_D drain currents I_{D-C} and I_{D-D} proportionally, so

$$I_{D-B} = I_{D-C} + I_{D-D} \tag{37}$$

and

$$\frac{I_{D-B}}{I_{in}} = \frac{I_{D-C} + I_{D-D}}{I_{in}} = \frac{S_B \cdot (S_C + S_D)}{S_A \cdot (S_B + S_C + S_D)} \tag{38}$$

Considering that

$$I_{out} = I_{D-D} \approx \frac{S_D}{S_C} \cdot I_{D-C} \tag{39}$$

the current mirror gain A_I is the combination of (38) and (39), and can be approximated for $S_C \gg S_B + S_D$ as

$$A_I = \frac{I_{out}}{I_{in}} \approx \frac{S_B}{S_A} \cdot \frac{S_D}{S_C} \tag{40}$$

If transistors $M_{A,C}$ are parallel arrays of m elements and $M_{B,D}$ are series arrays of n elements, then

$$I_{out} = \frac{S_{eq-B}}{S_{eq-A}} \cdot \frac{S_{eq-D}}{S_{eq-C}} \cdot I_{in} = \frac{I_{in}}{(mn)^2} = \frac{I_{in}}{N^4} \tag{41}$$

In another words, the current splitting current mirror attenuation is proportional to N^4, while the parallel-series current mirror is proportional to N^2 while using half as many transistor elements.

Nevertheless, this current mirror topology also has its own disadvantages. In addition to the conventional mirror output resistance R_o, this proposed split current mirror is also dependent of the positive supply voltage V_{DD}, as M_C drain terminal is connected to it. Consequently, any variation in the supply voltage also results in variations at the output current. Depending on the S_D/S_C ratio, the drain current I_{D-C} variation can be in the same order of I_{out} magnitude.

APPENDIX D – FORWARD-BODY-BIASING

Figures 48a and 48b show three distinct diode MOSFET configurations. Figure 48a shows a MOSFET in the conventional diode configuration with short circuited gate and drain terminals ($V_G = V_D = V_X$) and short circuited bulk and source terminals ($V_B = V_D = 0$). Figure 48b shows a forward-body-biased MOSFET diode configuration, based on the Dynamic Threshold voltage MOSFET (DTMOS) transistor (ASSADERAGHI et al., 1994), which the bulk terminal is also shorted to the drain terminal ($V_G = V_B = V_D = V_X$), so $V_{BS} > 0$.

Figure 48c shows a variation of the previous DTMOS diode configuration, the augmented DTMOS (LINDERT et al., 1999). In this configuration, the transistor M_Z bulk terminal is connected indirectly to its gate terminal by using the transistor M_{Z0} to limit the parasitic bulk current I_{BZ}.

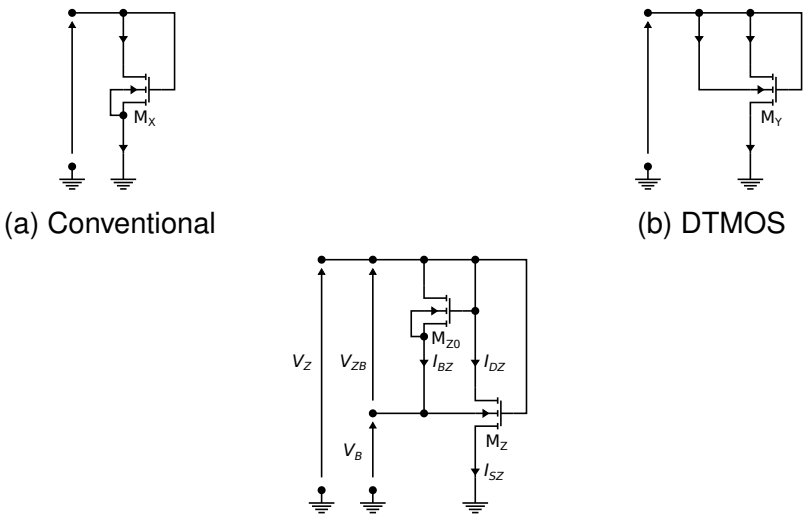
However, if the bulk-source voltage V_{BS} is positive, the diode formed by the pn junction between the p-substrate and n-doped source will be forward biased and there will be a non-negligible current I_B flowing from the bulk to the source terminal. Considering that the MOSFET is also biased in weak inversion ($i_f \ll 1$), the drain current I_D can be approximated to

$$I_D \approx 2e^1 I_S \exp\left(\frac{V_{GS} + (n-1)V_{BS} - V_T}{n\phi_t}\right) \tag{42}$$

and I_B can be approximated to

$$I_B \approx I_{Sdio} \exp\left(\frac{V_{BS}}{n_{dio}\Phi_t}\right) \tag{43}$$

Figure 48 – Transistor diode configurations

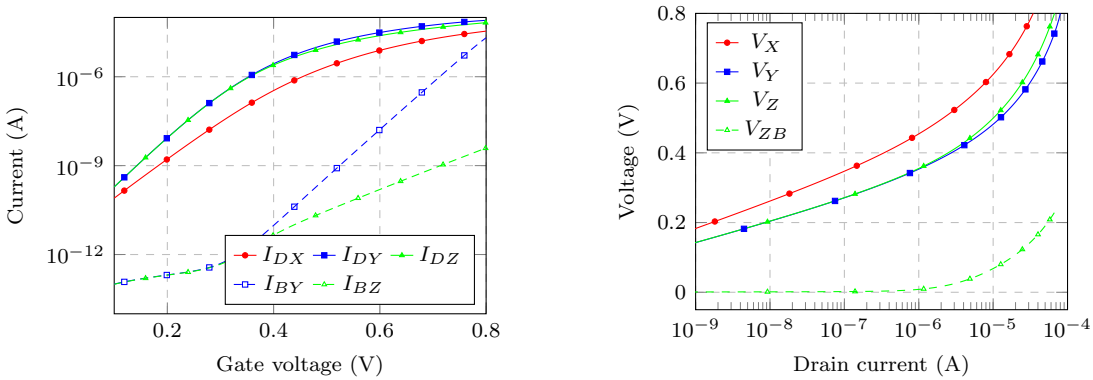


(a) Conventional (b) DTMOS

(c) Buffered DTMOS

Source: Author

Figure 49 – Transistor in diode configuration DC transfer functions



(a) Current × Voltage (b) Voltage × Current

Source: Author

where I_{Sdio} is the diode scale current and n_{dio} is the diode ideality factor, accordingly to the Shockley diode equation (SHOCKLEY, 1949).

Figures 49b and 49a shows the voltage-current curves for the diode configurations shown in Figures 48a and 48b. Transistors M_X and M_Y are identical low-V_T transistors, but M_Y is forward body-biased. First of all, it can be noticed that, while operating in weak inversion, M_Y drain current I_{DY} is much larger than the bulk current I_{BY}, which increased exponentially with V_Y, as expected. The source current I_{SY}, which is the sum of I_{DY} and I_{BY}, is approximately I_{DY} while $I_{DY} \gg I_{BY}$. When the transistor M_Y starts operating in moderate inversion, I_{DY} stops increasing exponentially while I_{BY} does not, until I_{BY} is greater than I_{DY}.

Also, it can be noticed that, for the same drain current ($I_{DX} = I_{DY}$), the transistor M_X gate voltage V_X is greater than transistor M_Y gate voltage V_Y. Also, since $i_{fX} \approx i_{fY}$ if $I_{DX} = I_{DY}$, considering (25), it can be inferred that

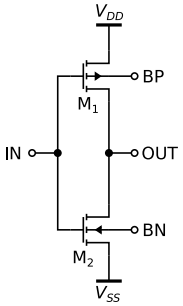
$$V_X \approx nV_Y = V_Y + (n-1)V_Y = V_Y + \Delta V_T \tag{44}$$

where ΔV_T is also an approximation for the threshold voltage body-effect (KAENEL et al., 1994). This threshold voltage reduction resulted from forward body-biasing is a known analog circuit supply voltage reduction technique (CHATTERJEE et al., 2005).

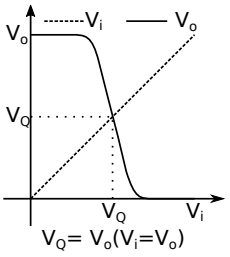
APPENDIX E – CMOS INVERTERS

E.1 CMOS INVERTER ANALYSIS

Figure 50 – CMOS Inverter



(a) Schematic



(b) Transfer Function

Source: Author

The CMOS inverter, depicted in Figure 50, consists in a PMOS transistor staked on a NMOS transistor, with the input signal connected to both gate terminals. The inverter quiescent output voltage V_Q is the input voltage that results in an equal output voltage. The quiescent current I_Q is the inverter DC current while $V_{IN} = V_Q$. The quiescent current I_Q can be calculated accordingly to the UICM model (SCHNEIDER; GALUP-MONTORO, 2010) simplified for weak inversion operation, as shown in 45,

$$I_D = I_S e^1 \exp\left(\frac{V_{GS} + (n-1)V_{BS} - V_T}{n\phi_t}\right) \tag{45a}$$

$$I_Q = I_{S_N} e^1 \exp\left(\frac{V_Q + (n-1)V_{BN} - V_T}{n\phi_t}\right) \tag{45b}$$

$$I_{S_{N(P)}} = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L} \tag{45c}$$

where I_S is the normalization current, which is function of the charge mobility μ, the oxide capacitance per area C'_{ox}, the slope factor n, the thermal voltage ϕ_t and the channel width and length W and L. Considering that V_Q is kept constant, by biasing independently the PMOS and NMOS bulk terminal voltages V_{BP} and V_{BN}, the quiescent current increases exponentially with $(n-1)V_{bn}$.

The inverter DC characteristic curve can be simplified into a linear voltage amplifier by extrapolating small signal parameters to large signal operation. The transfer function (46) is defined by the small signal voltage gain A_V and this approximation is

Figure 51 – Quiescent Voltage Extraction Circuits

(a) Quiescent Voltage (b) Initial Quiescent Voltage

Source: Author

only valid while both PMOS and NMOS transistors operate in saturation and in weak inversion. The voltage gain A_V is function of the inverter transconductance G_m and output conductance G_o, which are respectively function of the PMOS and NMOS transistors gate-drain small signal transconductance g_{mg} and drain conductance g_{md}, accordingly to the UICM model. Finally, these small signal parameters are function of the slope factor n, the thermal voltage ϕ_t and the Early voltage V_A.

$$V_o = A_V \left(V_Q - V_{in} \right) + V_Q \tag{46a}$$

$$G_m = g_{mg_P} + g_{mg_N} = \frac{I_Q}{\phi_t} \left(\frac{1}{n_P} + \frac{1}{n_N} \right) \approx \frac{2I_Q}{n\phi_t} \tag{46b}$$

$$G_o = g_{md_P} + g_{md_N} = I_Q \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right) \tag{46c}$$

$$A_V = G_m R_o = \frac{G_m}{G_o} \approx \frac{1}{n\phi_t \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right)} \tag{46d}$$

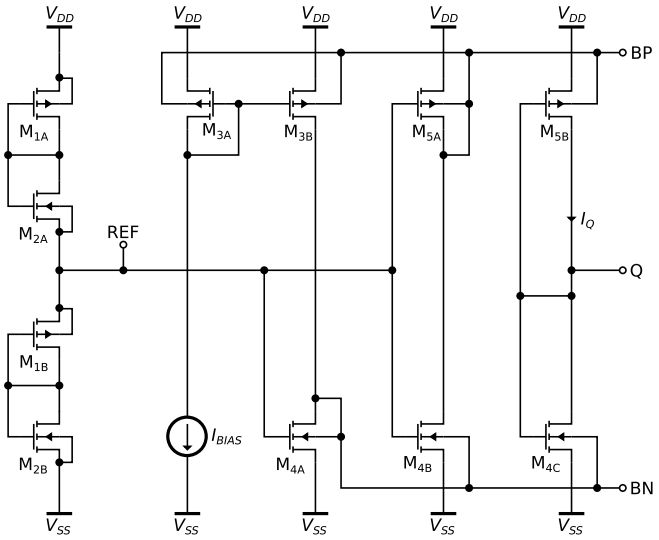
The quiescent output voltage V_Q can be controlled by body biasing, since V_Q varies almost proportionally with the bulk terminal voltages V_{bp} and V_{bn}, as shown by (47). Figures 51a and 51b shows the circuits used to extract V_Q and the initial quiescent voltage V_{Q0}. Considering operation in weak inversion, the initial quiescent voltage V_{Q0} is defined by (47b), obtained for $V_{IN} = V_{OUT} = V_{BP} = V_{BN}$, as derived in (MELEK, L. A. et al., 2014). Also, as inferred from (47b), V_{Q0} is sensitive to process and temperature variations.

$$V_Q \approx V_{Q0} + \frac{G_{mb}}{G_m + G_o}\left(V_{Q0} - \frac{V_{BP} + V_{BN}}{2}\right) \approx V_{Q0} + (n-1)\left(V_{Q0} - \frac{V_{BP} + V_{BN}}{2}\right) \tag{47a}$$

$$V_{Q0} \approx \frac{V_{DD}}{2} + \frac{V_{T_P} + V_{T_N}}{2n} - \frac{\phi_t}{2}\ln\left(\frac{I_{S_P}}{I_{S_N}}\right) \tag{47b}$$

E.2 INVERTER BIASING

Figure 52 – Inverter biasing circuit



Source: Author

As discussed previously, the inverter quiescent voltage and current V_Q and I_Q are a function of temperature, transistor dimensions, and process, supply voltage and temperature (PVT) variability. Various biasing circuits were proposed to bias V_Q (CHATTERJEE et al., 2005; VIERU; GHINEA, 2011) and I_Q (VLASSIS, 2012). The biasing circuit shown in 52 is a variation of the circuit proposed in (RODOVALHO, 2020a). It was designed for the TSMC 180 nm process using standard transistors and its array dimensions are shown in Table 16.

Table 16 – Inverter biasing circuit array dimensions

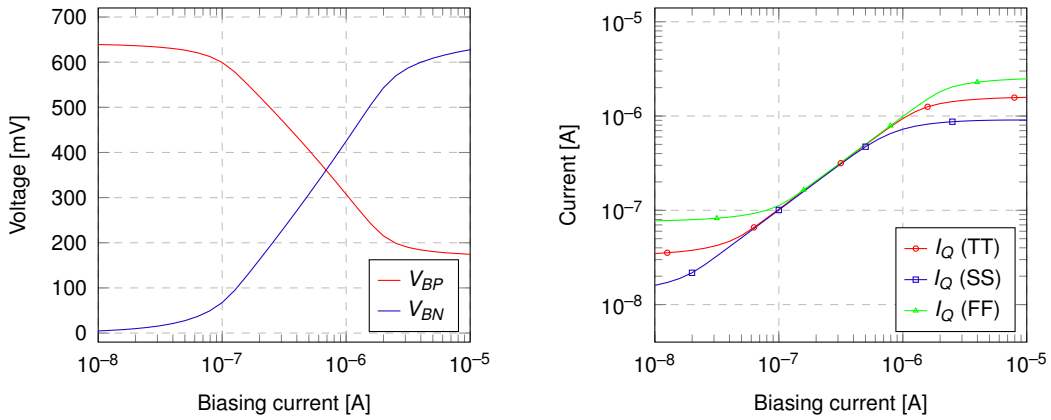
	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A\text{-}B}$	2	8	6.0	0.5	$M_{2A\text{-}B}$	2	8	1.5	0.5
$M_{3A,B}$	2	8	6.0	0.5	$M_{4A\text{-}C}$	2	8	1.5	0.5
$M_{5A,B}$	2	8	6.0	0.5					

Source: Author

Transistors $M_{1A,B}$ and $M_{2A,B}$ compose identical inverters with their inputs and output terminals connected. They function as very large resistances, since terminal REF voltage V_{REF} is half the positive voltage supply V_{DD}, considering that $V_{DD} = 0$, so $V_{DD} - V_{REF} = V_{REF} - V_{SS}$. The biasing current I_{BIAS} is mirrored by the current mirror made of transistors $M_{3A,B}$, and transistor M_{4A} defines the biasing voltage V_{BN}, as its drain and bulk terminals are connected to each other and its gate terminal is connected to REF node. Afterwards, the same principle is applied to the biasing voltage V_{BP}, which is defined by transistor M_{5A}. The replica inverter with input and output terminals connected to each other, made of transistors M_{4A} and M_{5C}, is the V_Q and I_Q extraction circuit.

Figure 53a shows the biasing voltages V_{BP} and V_{BN} as function of the biasing current I_{BIAS} for a 0.7 V supply voltage, typical process parameters and 27 ℃ temperature. As can be seen, the circuits functions properly with an I_{BIAS} ranging from about 100 nA to 2 µA for typical process parameters, as V_{BN} varies from 100 to 600 mV and both transistors M_{3B} and M_{4A} are operating in the saturation region. For lower or higher voltages, these transistors operate in the linear region and the circuit does not function properly. Figure 53b shows the resulting I_Q for corners TT (typical), SS (slow-slow) and FF (fast-fast). For these corners, the transistors threshold voltage V_T and transistor mobility µ reaches their extremes, so it reflects in changes in I_Q biasing range. The intersection of all corners I_{BIAS} range is then limited to 100 to 700 nA

Figure 53 – Biasing circuit I_{BIAS} sweep



(a) Biasing voltages

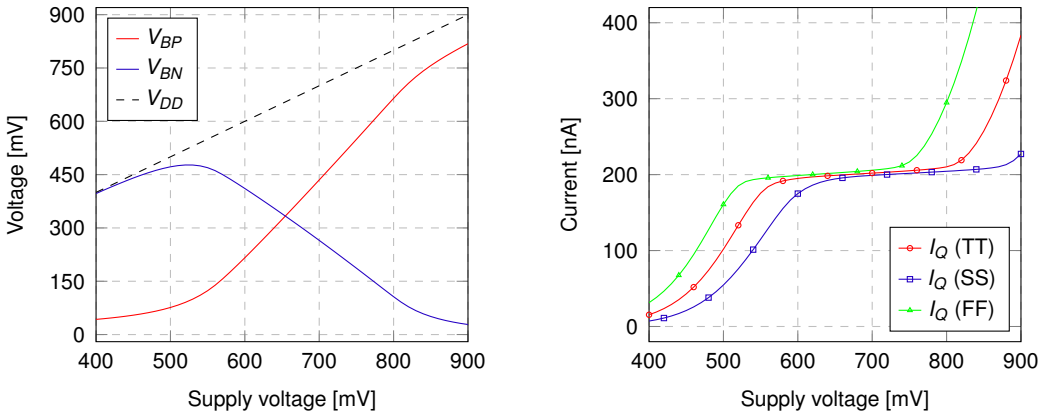
(b) Quiescent current

Source: Author

Figure 53a shows the biasing voltages V_{BP} and V_{BN} as function of the biasing current I_{BIAS} for a supply voltage DC sweep from 400 to 900 mV for typical parameters and room temperature. As V_{DD} increases, so does V_{REF}, and V_{BP} and V_{BN} to keep $V_Q = V_{REF}$ and $I_Q = I_{BIAS}$. The circuit works properly for supply voltages between 550 and 800 mV, as V_{BP} and V_{BN} allow all transistors to in the biasing circuit to operate in

the saturation region. Again, process corners severely limit the supply voltage range to between 650 to 750 mV.

Figure 54 – Biasing circuit supply voltage sweep

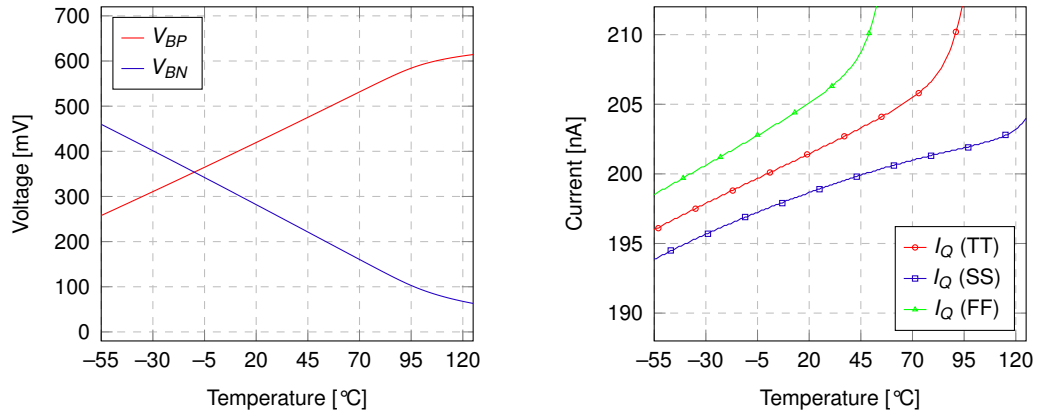


(a) Biasing voltages (b) Quiescent current

Source: Author

Finally, Figure 53a shows the biasing voltages V_{BP} and V_{BN} as function of the biasing current I_{BIAS} for a temperature sweep from -55 to 125 ℃ for a 0.7 V supply voltage and typical parameters. As the temperature increases, the transistors V_T decreases, so V_{BP} and V_{BN} change to compensate this effect. The circuits works properly for voltages between -55 and 95 ℃. However, the circuit temperature I_Q correction is also dependent of process, in special for the FF corner in these operation conditions.

Figure 55 – Biasing circuit temperature sweep



(a) Biasing voltages (b) Quiescent current

Source: Author

For comparison sake, monte carlo simulations were run for the biasing circuit and the V_Q extractor circuit from Figure 51a with BP connected to V_{DD} and BN connected

to V_{SS}. Tables 17 and 18 shows the V_Q and I_Q monte carlo simulation results summary for 1000 runs at room temperature. Each parameter was simulated considering process only, mismatch only and all. As can be noticed, for process variability only, the biasing circuit works almost flawlessly. For the non-biased V_Q extractor, I_Q varies greatly considering process variability, with a normalized standard deviation almost 27.2 % from the average value. The biasing circuit inaccuracy is almost exclusively a result of mismatch, and its normalized standard deviation is ten times lower then the non-biased circuit. Mismatch can be further reduced by increasing the inverter transistor arrays dimensions (BRAGA et al., 2019).

Table 17 – Inverter V_Q biasing monte carlo results

	Process		Mismatch		All	
	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]
No Biasing	355.5	2.64	355.1	0.13	355.2	2.28
Biasing	350.1	0.02	350.1	0.19	350.1	0.18

Source: Author

Table 18 – Inverter I_Q biasing monte carlo results

	Process		Mismatch		All	
	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]	μ_{I_D} [nA]	σ_{I_D}/μ_{I_D} [%]
No Biasing	17.51	28.4	17.59	1.19	17.50	27.2
Biasing	199.6	0.77	199.4	2.56	199.0	2.59

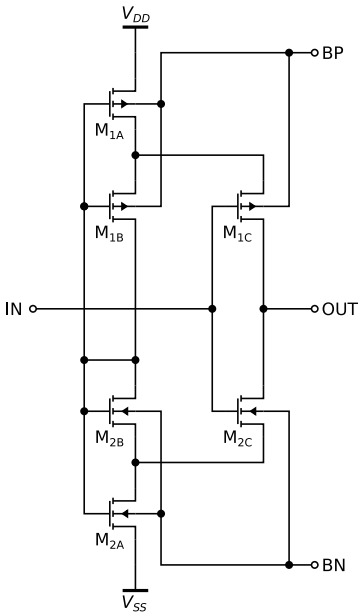
Source: Author

E.3 INVERTER LINEARITY IMPROVEMENT

The transistor gate-to-drain transconductance is highly non-linear, as it has an exponential drain current behavior in weak inversion and a quadratic behavior for strong inversion. Similarly to common-source gate amplifiers, the CMOS inverter transconductance can be linearized by using the source degeneration technique (SHEIKHOLESLAMI, 2014) by using passive resistors between the transistor source and supply voltage terminals. A more efficient technique is to use active source degeneration, as the passive resistors are replaced by active ones implemented with transistors operating in the linear region, as also used in differential pairs (KRUMMENACHER; JOEHL, 1988; KUO; LEUCIUC, 2001).

Figure 56 shows an inverter with active source degeneration. The actual inverter is made of transistors M_{1C} and M_{2C}. Transistors M_{1A} and M_{2B} act as active resistors and while M_{1B} and M_{2B}, which are connected as diodes, force them to operate in the linear region.

Figure 56 – Inverter with active source degeneration



Source: Author

A better comparison can be done by simulating both the conventional inverter INVA, shown in Figure 50, and this proposed linearized inverter INVB, with both using the same biasing circuit shown in Figure 52. Both inverters are made with similar transistor array dimensions, as shown in Table 19, consequently, INVB has three times more area.

Table 19 – Inverter biasing circuit array dimensions

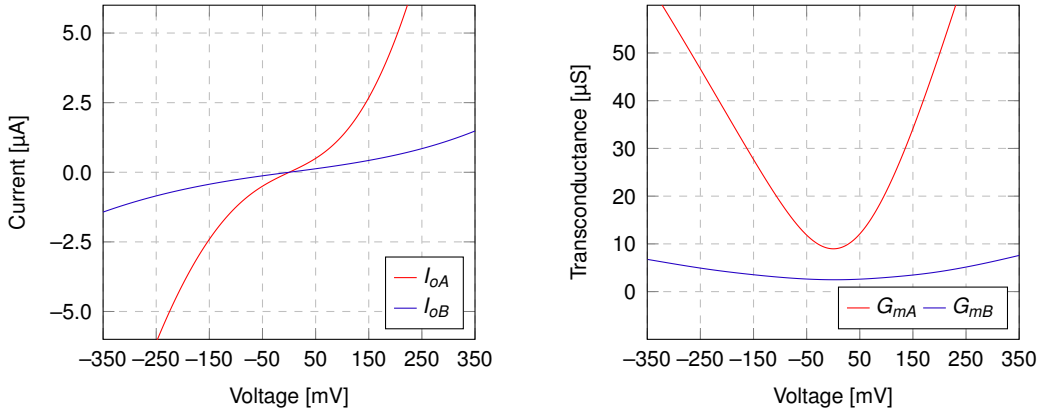
		m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
INVA	M_1	2	8	6.0	0.5	M_2	2	8	1.5	0.5
INVB	$M_{1A\text{-}C}$	2	8	6.0	0.5	$M_{2A\text{-}C}$	2	8	1.5	0.5

Source: Author

Figure 57a shows the inverters INVA and INVB output current for a input voltage V_{IN} varying from V_{SS} = –350 mV to V_{DD} = 350 mV, for a fixed output voltage at 0 V. First of all, INVA output current I_{oA} is much larger than INVB output current I_{oB} for the same input voltages. This translates as a higher transconductance G_{mA}, as shown in Figure 57b.

However, INVA transconductance is much more non-linear. This can be better visualized in Figures 58a and 58b, where the output current and transconductances are normalized by the transconductance value at V_{IN} = 0. INVA transconductance is symmtrical, however, it is highly non-linear, as the transistors operate in weak inversion. INVB normalized transconductance is still non-linear, but is still better. Even better results could be achieved with higher supply voltages, but the resulting transconductance would also increase accordingly.

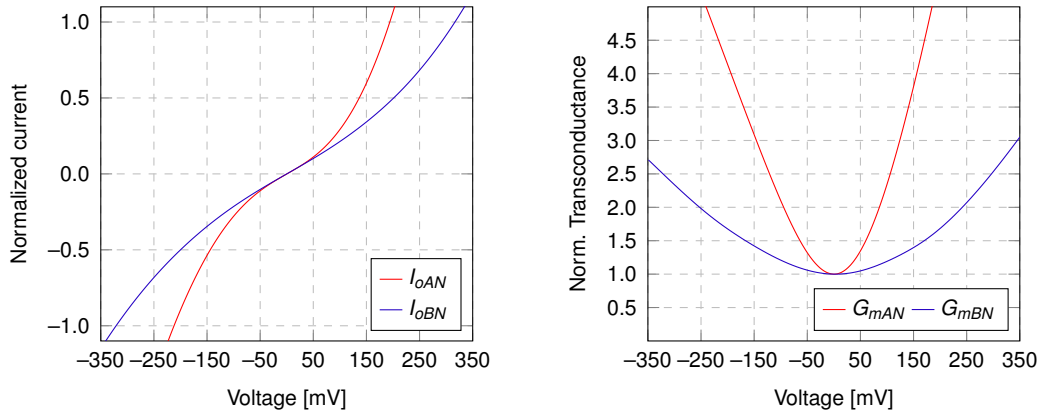
Figure 57 – Inverter current and transconductance



(a) Output current (b) Transconductance

Source: Author

Figure 58 – Inverter normalized current and transconductance



(a) Output current (b) Transconductance

Source: Author

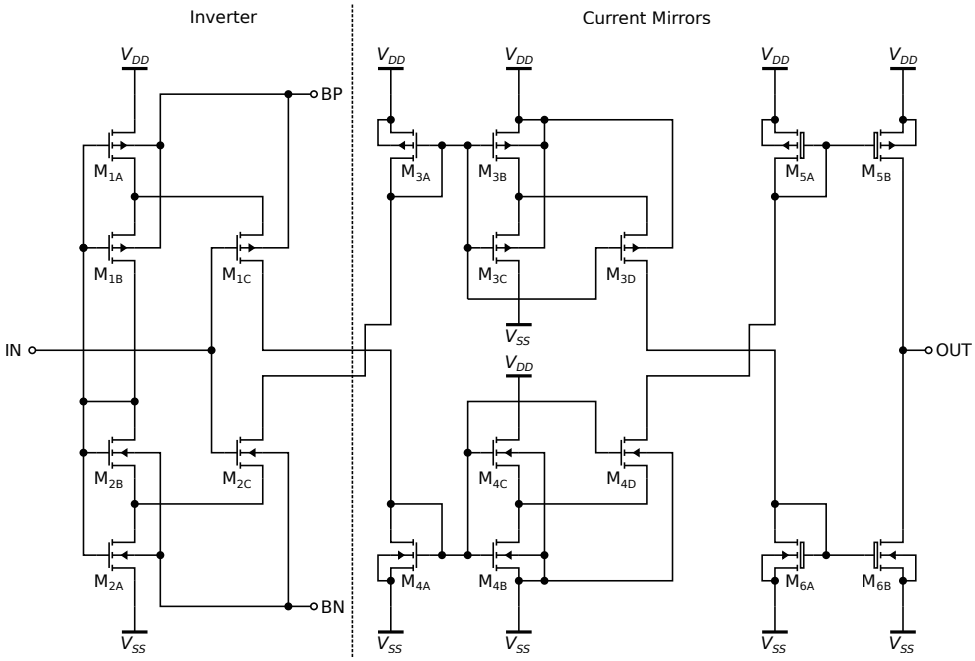
E.4 INVERTER TRANSCONDUCTANCE LOWERING

This thesis proposed artificial mechanoreceptor needs to implement integrated high-pass filters with corner frequencies of a few Hertz. The previous inverter with active source degeneration has a output conductance linear enough for this application, however, it has a minimum transconductance of about 2.5 µS, which would need micro Farad capacitors to implement its filters, while reasonable sized integrated capacitors are in the pico Farad order.

For this reason, the amplifier transconductance must be reduced without compromising its linearity. This can be achieved by using several analog circuit design techniques, but for this work, the inverter-based amplifier with parallel-series current mirrors was chosen. This technique was originally proposed in (KINGET et al., 1992) and further improved in (ARNAUD et al., 2006), by also using active source degenera-

tion (KRUMMENACHER; JOEHL, 1988).

Figure 59 – Ultra-low-transconductance inverter



Source: Author

The parallel-series current mirrors with very large attenuation factors can be placed at the INVB output to achieve a very large transconductance attenuation, as shown in Figure 59. Its transistor array dimensions are shown in Table 20.

Table 20 – Ultra-low-transconductance inverter circuit array dimensions

	m	n	W [µm]	L [µm]		m	n	W [µm]	L [µm]
$M_{1A\text{-}C}$	2	8	6.0	0.5	$M_{2A\text{-}C}$	2	8	1.5	0.5
$M_{3A,C}$	8	1	6.0	0.5	$M_{3B,D}$	2	4	6.0	0.5
$M_{4A,C}$	8	1	1.5	0.5	$M_{4B,D}$	2	4	1.5	0.5
M_{5A}	16	1	6.0	0.5	M_{5B}	2	8	6.0	0.5
M_{6A}	8	2	1.5	0.5	M_{6B}	2	4	1.5	0.5

Source: Author

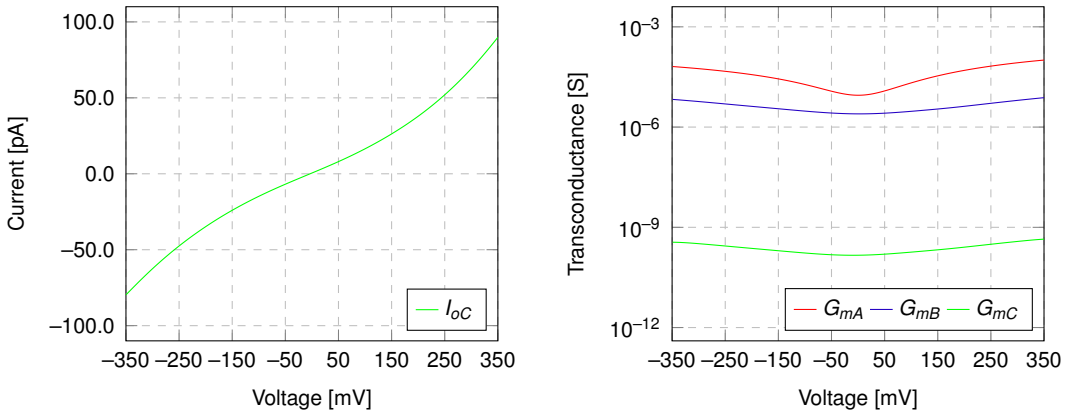
The proposed ultra-low-conductance inverter INVC is made of an inverter stage and two current mirror stages. The first stage is a parallel-trapezoidal current mirror with current splitting (RODOVALHO et al., 2021), as explained in Appendix C. The second current mirror stage is the parallel-series current mirror (FIORELLI et al., 2004).

The first stage current mirrors invert the input signal once, so it needs a second current mirror stage to invert the output signal again. It is important to notice that the second current mirror stage current magnitudes are so low that different transistors with higher threshold voltages were used, otherwise, the transistors would began operating in the linear region and the current mirror would not work. Additionally, by using two

current mirror stages, the current attenuation technique can be used twice, further lowering the inverter transconductance. And, since the signal is inverted only three times and the output node impedance is very large compared to the inner nodes, this circuit is still inherently stable.

Figure 60a shows the resulting INVC output current. It has the exact same shape of INVB, however, its magnitude is in the pico ampere range. Consequently, INVC transconductance at V_{IN} = 0 V is about 146 pS, which is approximately 16000 times less than INVB transconductance at the same operation conditions.

Figure 60 – Ultra-low-transconductance inverter output current and transconductance comparison



(a) Output current (b) Transconductance

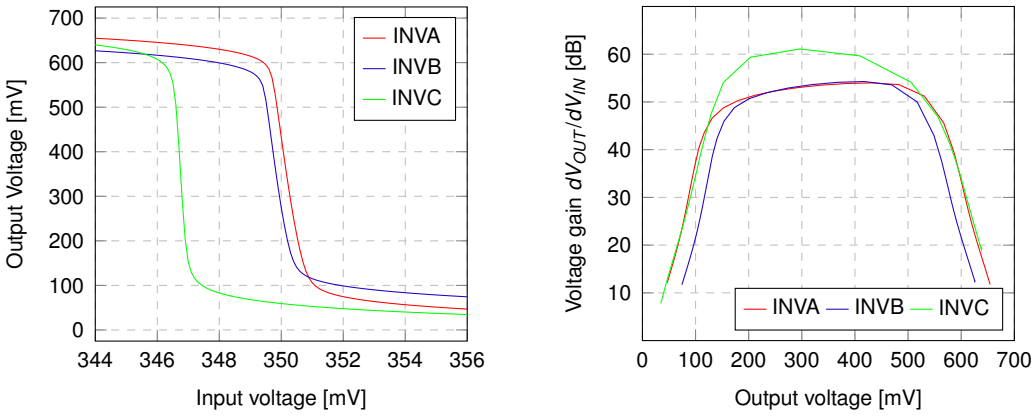
Source: Author

Figure 61a shows the each inverter characteristic curve. As can be seen, INV voltage output excursion is slightly smaller than INVA, due to its active source degeneration. INVC has a characteristic curve slightly displaced, indicating that the biasing circuit does not work perfectly, as V_Q is about 347 mV. However, as can also be seen in Figure 61b, which shows the voltage gain versus output voltage, which was derived from the same characteristic curve, INVC voltage gain is also bigger and its output voltage excursion is similar to INVA. This happens because INVC output does not have source degeneration.

This technique also has its disadvantages. INVB not only uses a larger area, but it is also very power inefficient, and, since it has a very small transconductance, its input referred noise is considerably large, as can be seen in Figure 62. INVC thermal noise is orders of magnitude larger, since its transconductance is very small. Additionally, its 1/f noise is larger, since it has extra transistors to contribute this kind of noise. Nevertheless, since the bandwidth is very narrow, as the signal maximum frequency is also very low, the total output noise is adequate for its application.

Also, as it has additional transistors, it not only has additional noise sources, as it has additional mismatch sources, so the transistors must be sized properly, whose so-

Figure 61 – Inverter characteristic curves and voltage gain comparison

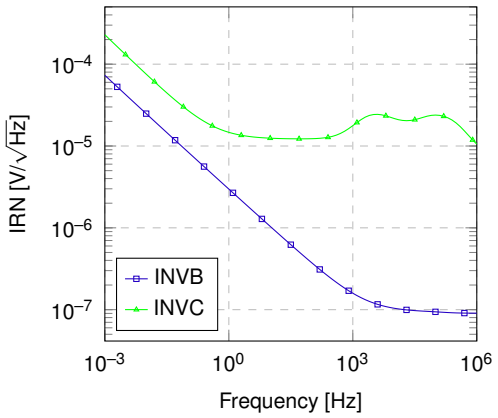


(a) Inverter characteristic curve

(b) Inverter voltage gain

Source: Author

Figure 62 – Inverter noise comparison



Source: Author

lution is a matter of increasing their area. Still, the extra transistor area is compensated by the drastic reduction of the integrated capacitor area.

APPENDIX F – LIST OF PUBLICATIONS

The following papers were published during the doctoral research period

Journal:

- Rodovalho, Luis Henrique. "Push–pull based operational transconductor amplifier topologies for ultra low voltage supplies." Analog Integrated Circuits and Signal Processing (2020): 1-14.
- Rodovalho, Luis Henrique, Orazio Aiello, and Cesar Ramos Rodrigues. "Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors." Electronics 9.9 (2020): 1410.
- Rodovalho, Luis Henrique, Cesar Ramos Rodrigues, and Orazio Aiello. "Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors." Electronics 10.8 (2021): 935.

International Conferences:

- Rodovalho, Luis Henrique, Pedro Toledo, and Sergio Bampi. "A 0.6 V Current Reference Based on the MOSFET Forward-Body-Biased ZTC Condition." 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS). IEEE, 2019.
- Rodovalho, Luis Henrique. "Schmitt Trigger Based Single-Ended Voltage Amplifier with Positive Feedback Control for Ultra-Low-Voltage Supplies." 2020 IEEE Nordic Circuits and Systems Conference (NorCAS). IEEE, 2020.
- Rodovalho, Luis Henrique; Silva, Rafael; Rodirgues, Cesar. "A 1V, 450pS OTA Based on Current-Splitting and Modified Series-Parallel Mirrors". 2021 IEEE 12th Latin American Symposium on Circuits & Systems (LASCAS). [S.l.: s.n.], 2021.