UNIVERSIDADE FEDERAL DE SANTA CATARINA
CENTRO TECNOLÓGICO
PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

FRANCIELE NÖRNBERG

DESIGN OF AN ULTRA-LOW-VOLTAGE DICKSON CONVERTER BASED ON AN LC OSCILLATOR

FLORIANÓPOLIS
2019

Franciele Nörnberg

DESIGN OF AN ULTRA-LOW-VOLTAGE DICKSON CONVERTER BASED ON AN LC OSCILLATOR

Dissertação submetida ao Programa de Pós-Graduação em Engenharia Elétrica para obtenção do grau de "Mestre em Engenharia Elétrica".

Orientador: Prof. Dr. Márcio Cherem Schneider.

Coorientador: Prof. Dr. Márcio Bender Machado.

Florianópolis
2019

Ficha de identificação da obra elaborada pelo autor,
através do Programa de Geração Automática da Biblioteca Universitária da UFSC.

Nörnberg, Franciele
Design of an ultra-low-voltage Dickson converter based on an LC oscillator / Franciele Nörnberg ; orientador, Márcio Cherem Schneider, coorientador, Márcio Bender Machado, 2019.
82 p.

Dissertação (mestrado) - Universidade Federal de Santa Catarina, Centro Tecnológico, Programa de Pós-Graduação em Engenharia Elétrica, Florianópolis, 2019.

Inclui referências.

1. Engenharia Elétrica. 2. Conversores DC-DC elevadores para ultra-baixa-tensão.. 3. Osciladores LC para ultra baixa-tensão.. 4. Circuito de inicialização. 5. Energy harvesting. I. Schneider, Márcio Cherem. II. Machado, Márcio Bender. III. Universidade Federal de Santa Catarina. Programa de Pós-Graduação em Engenharia Elétrica. IV. Título.

Franciele Nörnberg

DESIGN OF AN ULTRA-LOW-VOLTAGE DICKSON CONVERTER BASED ON AN LC OSCILLATOR

O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Eng. Dr. Heider Marconi Madureira
Chipus

Prof. Ph.D Cesar Ramos Rodrigues
UFSC

Prof. Ph.D Carlos Galup Montoro,
UFSC

Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

Bartolomeu Ferreira Uchoa Filho:47636211491
Digitally signed by Bartolomeu Ferreira Uchoa Filho:47636211491
Date: 2019.10.18 16:52:17 -03'00'

Prof. Dr. Bartolomeu Ferreira Uchôa Filho
Coordenador do Programa de Pós-Graduação em Engenharia Elétrica

Marcio Cherem Schneider:08255679987
Assinado de forma digital por Marcio Cherem Schneider:08255679987
Dados: 2019.10.18 14:49:02 -03'00'

Prof. Dr. Márcio Cherem Schneider
Orientador

Florianópolis, 27 de Setembro de 2019.

Dedico esta monografia a minha família pelo apoio incondicional.

Aos amigos pelo convívio em momentos difíceis e alegres.

Aos professores por nortear meu caminho.

A todos que não desistem de seus ideais, seguindo sempre em frente em meio às diversidades.

AGRADECIMENTOS

Agradeço aos meus orientadores Márcio Schneider e Márcio Bender pelo conhecimento compartilhado, pela orientação recebida e pela disposição durante a realização deste trabalho.

Agradeço aos membros da banca examinadora Heider Marconi, César Ramos e Carlos Galup pela disposição em avaliar e enriquecer este trabalho.

Agradeço aos amigos do laboratório LCI, Evandro, Luis Rodovalho, Thiago, Rafael Radin, Rodrigo, Cristina, Rafael, Victoria, Nazide e demais integrantes, com quem compartilhei muitos momentos, muito conhecimento e discussões enriquecedoras.

Agradeço à CAPES, pelo apoio financeiro, e à MOSIS pela fabricação dos circuitos prototipados.

Agradeço aos amigos Luis Otavio, Patricia, Filipe, Palloma, Vitor Couto, Ana Carolina, Joelma, Tuane, Théu, Camila, Michele e Eduarda, por todo apoio nas dificuldades, momentos de descontração e conversas sobre assuntos diversos.

Agradeço a minha família, pelo amor, incentivo e apoio incondicional.

Agradeço a Deus por ter me dado saúde e força para superar as dificuldades.

Nada dura para sempre, nem as dores, nem as alegrias. Tudo na vida é aprendizado. Tudo na vida se supera.

– Caio Fernando Abreu

RESUMO

O presente trabalho de dissertação apresenta a análise e o projeto de conversores DC/DC Dickson operando a partir de ultrabaixa tensão, aplicados para colheita de energia. Os conversores aqui descritos, quando operam em muito baixa tensão, são normalmente utilizados como blocos de inicialização, mas podem também ser utilizados para alimentar diretamente a carga, em aplicações em que a eficiência não seja o principal requisito. Primeiramente, a operação do conversor Dickson como bomba de carga é descrita para aplicações de ultrabaixa tensão. Expressões para a tensão de saída, eficiência na conversão de energia e resistência de entrada em termos dos parâmetros físicos do diodo, da corrente de saída e do número de estágios são derivadas. A operação em ultrabaixa tensão, viabilizada pelo uso de osciladores em anel indutivos e transistores do tipo Zero-VT, é demonstrada em dois protótipos fabricados em tecnologias CMOS de 180 nm e 130 nm. Os dois conversores são totalmente integrados, tendo apresentado funcionamento a partir de 85 mV de tensão de entrada. Para tensões DC de entrada de aproximadamente 120 mV e 150 mV os conversores entregam 1 μW na saída.

Palavras-chave: circuitos integrados CMOS, bomba de carga de Dickson , oscilador em anel indutivo, colheita de energia.

RESUMO EXPANDIDO

Introdução

Os conversores do tipo bomba de carga (do inglês *charge pump*) introduzidos por Dickson [1] foram empregados em uma ampla variedade de aplicações, incluindo, por exemplo, geradores de tensão para polarização de memórias RAM e memórias flash, drivers para diodos emissores de luz e monitores de cristal líquido e conversores de corrente contínua que extraem energia de um sinal de RF [2,3]. No campo de eliminação de energia, a demanda por autonomia energética impulsionou a busca por conversores do tipo *boost* capazes de operar a partir de tensões extremamente baixas. Monitoramento *in vivo* da atividade dos órgãos humanos, por exemplo, eletrocardiograma, eletroencefalograma ou exames de pressão intra-ocular e estimulação de tecidos humanos, que geralmente consomem algumas dezenas de micro watts [4, 5], abriram espaço para uma nova classe de coletores de energia (*energy harvesting*) de ultra-potência (ULP) e ultra-baixa tensão (ULV).

Em geral, a estrutura desses conversores é dividida em dois blocos: um conversor de incialização e outro de alta eficiência [6–10]. O bloco de inicialização, responsável pela operação inicial da conversor, é composto por um oscilador e um *charge pump*. O principal requisito para esse bloco é iniciar a partir de uma voltagem muito baixa, por exemplo, 50 mV ou até menos, enquanto que o oscilador de alta eficiência normalmente é um conversor do tipo boost indutivo.

Com o objetivo de gerar uma tensão DC de inicialização para os conversores *boost* ou fornecer energia para cargas da ordem de micro-watt a partir de baixas tensões, este trabalho apresenta conversores DC/DC construídos com conversores *charge pump* do tipo Dickson (DCP), juntamente com um oscilador em anel indutivo (IRO) ou um oscilador em anel aprimorado (ESRO). São apresentadas as principais equações do DCP, IRO e ESRO, que levam em consideração o acoplamento entre o DCP e o oscilador. Depois disto, os conversores foram projetados, fabricados e testados, sendo dois protótipos totalmente integrados que elevam uma tensão de entrada DC de aproximandamente 100 mV até 1 V.

Objetivos

O principal objetivo desta monografia foi projetar e medir conversores de inicialização totalmente integrados, com base no Dickson *charge pump* e osciladores em anel indutivo operando em tensões muito baixas para inicializar conversores eficientes.

Os objetivos específicos da tese são:

- Apresentar as análises teóricas do DCP em termos de parâmetros do diodo,

número de estágios e corrente de carga para derivar expressões para a tensão de saída, eficiência energética e resistência de entrada, válidas para operação ULV;
- Projetar um IRO e um ESRO para obter uma baixa tensão de inicialização;
- Desenvolver uma metodologia de projeto para projetar os dois blocos principais, a saber, o DCP e o oscilador;
- Analisar numericamente o comportamento dos blocos acoplados, nomeadamente DCP e oscilador;
- Projetar, prototipar e medir os conversores DC/DC.

.

Metodologia

O projeto de um conversor DC-DC tem muitos graus de liberdade, como os parâmetros do oscilador e do *charge pump*. Além disso, o oscilador e o DCP não podem ser projetados independentemente, pois a amplitude do oscilador (V_A) depende de sua carga (R_{in}), a resistência de entrada do DCP, que, por sua vez, depende da amplitude do oscilador. Essa dependência mútua entre os parâmetros dos dois blocos dificulta o projeto manual do conversor.

Para tornar o projeto do conversor Dickson menos dependente do simulador de circuito, uma rotina MatLab foi desenvolvida. A rotina utiliza os parâmetros e equações desenvolvidos para o projeto do oscilador e do *charge pump*. Os parâmetros elétricos dos componentes, nomeadamente transistores, indutores e capacitores, são extraídos do simulador. Todos esses parâmetros são usados para simular o comportamento do conversor no tempo.

A rotina fornece uma visão geral da tensão de saída do conversor para um determinado espaço de projeto composto pelo número de estágios e pela corrente de saturação do diodo empregada no Dickson *charge pump*.

Depois que muitos dos parâmetros foram definidos, os componentes foram introduzidos no simulador para verificar o comportamento elétrico. Assim, ao encontrar a combinação de parâmetros que atende as especificações do projeto, o mesmo é passado para a fase de *layout* e fabricação do protótipo.

Resultados

Foram implementados dois protótipos do conversor de incialização. O primeiro conversor, chamado de design DCP com IRO, foi fabricado utilizando a tecnologia CMOS 180 nm da TSMC, enquanto que o segundo, chamado de design DCP com ESRO, foi integrado na tecnologia CMOS 130 nm da IBM.

O conversor DCP com IRO apresentou tensão média de inicialização das amostras igual a 84 mV, para o conversor sem carga. Como o conversor foi projetado para suprir uma carga de 500 mV/200 nA, um resistor de 2,5 M Ω foi usado para emular a carga. Nesta condição, o conversor inicia em $V_{TEG} = 85$ mV e atinge a saída de 500 mV quando $V_{TEG} = 94$ mV. Alterando a carga do conversor para um resistor de $R_L = 1$ M Ω, o conversor entrega $V_L = 1$ V quando $V_{TEG} = 120$ mV.

O conversor DCP com ESRO apresentou tensão média de inicialização das amostras medidas igual a 78,75 mV para o conversor sem carga. A tensão de entrada

necessária para atingir $V_L = 1$ V é 150,5 mV para $R_L = 1$ M Ω.

Para tensões DC de entrada de aproximadamente 120 mV e 150 mV os conversores entregam 1 μW na saída.

Considerações Finais

As características das arquiteturas de conversores, usando um IRO ou um ESRO, apresentaram características semelhantes. Para as tecnologias empregadas, o fator de baixa qualidade dos indutores parece limitar fortemente a eficiência dos conversores. Apesar das limitações dos osciladores LC totalmente integrados que foram empregados neste trabalho, os dois conversores projetados neste documento podem ser muito úteis para iniciar um conversor eficiente.

Também apresentamos um modelo preciso do Dickson *charge pump*, que inclui a resistência de entrada do DCP com dependência explícita dos parâmetros do diodo, corrente de carga e número de estágios. A expressão derivada para a resistência de entrada é de grande valor, pois deve ser considerada no design do oscilador, pois afeta diretamente a tensão de inicialização do oscilador.

A análise computacional do conversor, que inclui a resistência de entrada do DCP, é uma ferramenta muito útil para projetar o oscilador, pois leva em consideração a influência do DCP no oscilador. Como resultado, a solução numérica assim obtida para os parâmetros DCP fornece uma entrada inicial para o simulador muito próxima da solução ótima pesquisada.

ABSTRACT

This thesis presents the analysis and design of Dickson charge pump converters operating from low-voltage supply, for energy harvesting applications. The DC/DC converters described herein, when operating at very low voltage, are commonly used as startup blocks, but can also be used to directly supply the load in applications in which efficiency is not of major concern. Firstly, the operation of the Dickson charge pump for ultra-low voltage is described. Expressions for the output voltage, power conversion efficiency and input resistance in terms of the diode physical parameters, the output current, and the number of stages are derived. The low-voltage operation, made feasible through the use of inductive ring oscillators and zero-VT transistors, is demonstrated via two prototypes fabricated in 180 nm and 130 nm CMOS technologies. Both converters are fully integrated and started up from around 85 mV of input voltage. For input voltages of around 120 mV and 150 mV the two converters deliver 1 μW to the load.

Keywords: Dickson Charge Pump, Inductive Ring Oscillator, Energy Harvesting.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Abbreviation	**Description**
AC	Alternating Current
ACM	Advanced Compact MOSFET Model
CMOS	Complementary MOS
DC	Direct Current
DCP	Dickson Charge Pump
ESRO	Enhanced Swing Ring Oscillator
IRO	Inductive Ring Oscillator
LC	Inductive-Capacitive oscillator
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOSIS	Metal-Oxide-Semiconductor Implementation Service
NMOS	N-Channel MOS
PCE	Power Converter Efficiency
PMOS	P-Channel MOS
RO	Ring Oscillator
TEG	Thermoelectric Generator
T3LVT	Triple-Well Low Voltage Threshold
ULP	Ultra Low Power
ULV	Ultra Low Voltage
WI	Weak Inversion
ZVT	Zero Voltage Threshold

LIST OF SYMBOLS AND ACRONYMS

Symbol	Description	Unity
C_{db}	Drain-bulk capacitance	[F]
C_{gb}	Gate-bulk capacitance	[F]
C_{gs}	Gate-source capacitance	[F]
C_{jd}	Drain junction capacitance	[F]
C_{db}	Drain-bulk capacitance	[F]
C'_{ox}	Oxide capacitance per unit area	[F/m^2]
C_p	Parasitic capacitance	[F]
f_{osc}	Oscillation frequency	[Hz]
g_m	Gate transconductance	[A/V]
g_{mb}	Bulk transconductance	[A/V]
g_{md}	Drain transconductance	[A/V]
g_{ms}	Source transconductance	[A/V]
G_P	Inductor parallel conductance	[S]
G_o	Load conductance	[S]
I_0	Modified Bessel function of the first kind of order zero	—
I_1	Modified Bessel function of the first kind of order one	—
I_D	Drain current	[A]
i_f	Forward normalized current	—
I_F	Forward saturation current	[A]
i_r	Reverse normalized current	—
I_R	Reverse saturation current	[A]
I_{sat}	Diode saturation current	[A]
I_S	Specific current (normalization current)	[A]
k	Boltzmann's constant (1,38 x 10^{-23})	[J/K]
L	channel length	[m]
n	Transistor slope factor	—
n	Diode ideallity factor	—
N	Number of stages	—
P_D	Diode power dissipated	[W]
P_{in}	Input power	[W]
P_{loss}	Power loss due to the diodes of the DCP	[W]

P_{out}	Output power	[W]
q	Electronic charge (1,6 x 10^{-19})	[C]
Q	Inductor quality factor	—
R_{in}	Dickson input resistance	[Ω]
r_{in}	Dickson normalized input resistance	—
R_S	Inductor series resistance	[Ω]
R_{TEG}	Thermoelectric generator resistance	[Ω]
T	Absolute Temperature	[K]
v_a	Peak amplitude normalized of a sine signal	—
V_A	Peak amplitude of a sine signal	[V]
V_B	Bulk voltage	[V]
V_d	Diode forward voltage drop	[V]
V_D	Voltage across the diode	[V]
V_D	Drain voltage	[V]
V_{DD}	Supply voltage	[V]
V_{DS}	Drain-Source voltage	[V]
V_ϕ	Sine signal	[V]
V_G	Gate voltage	[V]
V_L	Load Voltage	[V]
V_{in}	Input voltage	[V]
V_{out}	Output voltage	[V]
V_P	Pinch-off voltage	[V]
V_S	Source voltage	[V]
V_{T0}	Threshold voltage	[V]
V_{TEG}	Thermoelectric generator voltage	[V]
W	Channel width	[m]
ϕ_t	Thermal voltage	[V]
ω	Angular frequency	[rad/s]

CONTENTS

1. INTRODUCTION

The charge pump converters introduced by Dickson [1] have been employed in a wide variety of applications, including, for example, bias generators for dynamic random access memories and flash memories, drivers for light emitting diodes and liquid crystal displays, and AC-DC converters that harvest energy from a RF signal [2,3]. In the energy scavenging field, the demand for energy autonomy has driven the search for boost converters able to operate from extremely low voltages. *In vivo* monitoring of human organs activity, *e.g.* electrocardiogram, electroencephalogram, or intraocular pressure examinations, and stimulation of human tissues, which generally consume some dozens of micro-watts [4, 5], open space for a new class of ultra-low-power (ULP) and ultra-low-voltage (ULV) energy harvesters.

Solar cells in dark environments [11], wearable thermoelectric generators [6] and implantable glucose fuel cells [12], which typically generate less than 100 mV, are appealing choices to power the electronics of sensor networks and biomedical appliances. However, given the ULV levels generated by these energy harvesters, a boost converter is required to power conventional electronics which, in general, demands supply voltages around 1 V.

In the past decade, in an attempt to reduce the minimum voltage required to start up converters, many researchers have presented solutions employing schematics based on charge pumps or inductive boost converters. A challenge in the design of converters powered from voltages below 50 mV is the start-up stage, due to the low efficiency of devices operating at ULV and the need to generate oscillatory signals from such a low voltage.

In [4], a body sensor node is powered from a supply voltage of 30 mV of a thermoelectric harvester, but wireless RF power is provided for the kick start. In [13], a boost converter that works at minimum voltage of 30 mV, requires at least 50 mV to starts up. In [14], a 35 mV boost converter is presented; nevertheless, it requires a mechanical switch for the kick start of the converter. All these converters use off-chip inductors to start up. A start-up converter of 80 mV is presented in [15], but it requires a threshold-voltage-tuned oscillator in order to decrease the minimum start-up voltage. In recent publications [16–18], fully integrated solutions with no tuning processes are proposed, but they operate from around 100 mV.

In order to deal with the conflicting requirements of very low voltage for the converter start-up and the high power conversion efficiency, the use of a hybrid configuration composed of two converters, similar to that shown in Fig. 1.1, has been widely employed [6–10]. Reference [6] reports a thermoelectric energy harvester which starts up from 65 mV. In [7], an on-chip transformer-based LC oscillator starts up at an open-circuit-voltage of 160 mV . [8] reports a DC-DC converter that operates from a 7 mV supply voltage, but requires a minimum self-start voltage of

210 mV. In [9], a start-up converter based on a ring oscillator and a charge pump starts up at 60 mV. In the converter of [10], an inductor of the start-up Colpitts oscillator is reused in the main boost converter to minimize the number of off-chip components, but it starts up from a minimum of 40 mV.

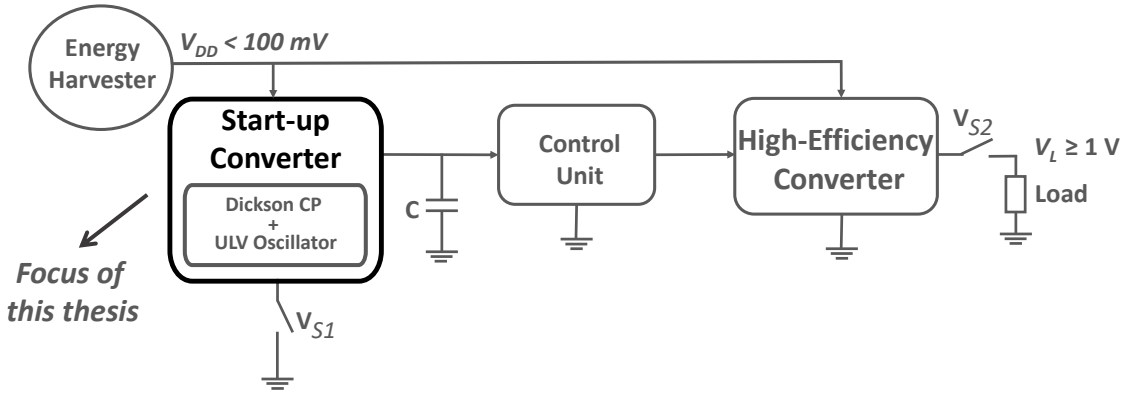


Figure 1.1: Hybrid configuration composed of two voltage converters.

The main characteristics of these converters are summarized in Table 1.1. All of them, which use a hybrid topology implemented in CMOS technology, have a boost converter as the main converter.These converters use a thermoelectric generator (TEG) as a voltage source and employ some off-chip components. V_{DD} is the source voltage, V_{out} is the load voltage and PCE is the Power Conversion Efficiency of the full converter.

Table 1.1: Main characteristics of converters that use hybrid topology and a TEG as a voltage source.

Reference	V_{DD}	V_{out}	PCE (end-to-end)	Process	Off-Shelf
Rozgic (2017)	65 mV	1.8 V	68 % @ 200 mV	65 nm	inductor + capacitor
Qian (2018)	160 mV	1.5 V	74 % @ 200 mV	180 nm	oscillator + regulator
Luo (2018)	45 mV	1.5 V	41 % @ 240 mV	65 nm	inductor
Dezyani (2018)	60 mV	1.0 V	47 % @ 300 mV	180 nm	inductor + capacitor
Lim (2018)	40 mV	1.1 V	75 % @ 150 mV	65 nm	inductors

In general, the start-up converter, responsible for the initial operation of the harvester, is composed of an oscillator and a charge pump. The main requirement for this block is to start up from a very low voltage, *e. g.* 50 mV or even less. Power conversion efficiency is not the primary concern for the start-up block, since it can be turned off after the voltage on capacitor C has reached the minimum voltage required to operate the high-efficiency converter, as can be seen in Fig. 1.1. To kick start the circuit at extremely low voltages, a charge pump has been commonly used, as shown in Table 1.2. In the table, V_{DD} is the start-up voltage and IRO and RO mean Inductive Ring Oscillator and (conventional) Ring Oscillator, respectively.

Aiming at the generation of a DC voltage to kick-start boost converters or directly supply micro-watt loads from low voltages, this thesis presents DC/DC

Table 1.2: Main characteristics of start-up converters based on charge pump.

Reference	V_{DD}	Oscillator	Charge Pump (CP)
Rozgic (2017)	65 mV	IRO	8-stage Dynamic CTS
Qian (2018)	160 mV	LC	10-stage CP
Luo (2018)	210 mV	RO	3-stage Pelliconi CP
Dezyani (2018	60 mV	RO	40-stage Dickson CP
Lim (2018)	40 mV	Colpitts	10-stage Voltage Multiplier

converters built with the Dickson charge pump (DCP) along with either an IRO or an Enhanced Swing Ring Oscillator (ESRO). The main equations of the DCP, IRO and ESRO, which take into account the coupling between the DCP and the oscillator, are presented . After all, the converters were designed and two fully integrated prototypes that convert a DC input voltage from down to 100 mV up to 1 V were fabricated and tested.

1.1. Main and specific goals

The main goal of this thesis has been to design and measure fully integrated start-up converters, based on Dickson charge pump and inductive ring oscillators operating at very low voltages in order to start up efficient converters.

Specifics goals of the thesis are:

- To present the theoretical analyses of the DCP in terms of the diode parameters, the number of stages, and the load current in order to derive expressions for the output voltage, power efficiency and input resistance, valid for ULV operation;
- To design both an IRO and an ESRO in order to achieve a low start-up voltage;
- To develop a design methodology to design the two main blocks, namely the DCP and the oscillator;
- To analyze numerically the behavior of the coupled blocks, namely DCP and oscillator;
- To design, prototype and measure the DC/DC converters.

1.2. Thesis organization

The thesis is organized as follows. The ULV model of the Dickson charge pump is developed in Chapter 2. Chapter 3 presents the analyses of the ULV oscillators . A computational analysis of the converter is shown in Chapter 4. In the following, Chapter 5 presents the design and experimental results of the DC/DC converters. Chapter 6 concludes the thesis.

2. DICKSON CHARGE PUMP

2.1. Introduction

The Dickson charge pump is an DC-DC converter, based on the voltage multiplier concept first presented by Heinrich Greinacher [19], in which the nodes of a diode chain are coupled to the AC inputs via capacitors, as shown in Fig. 2.1 [1].

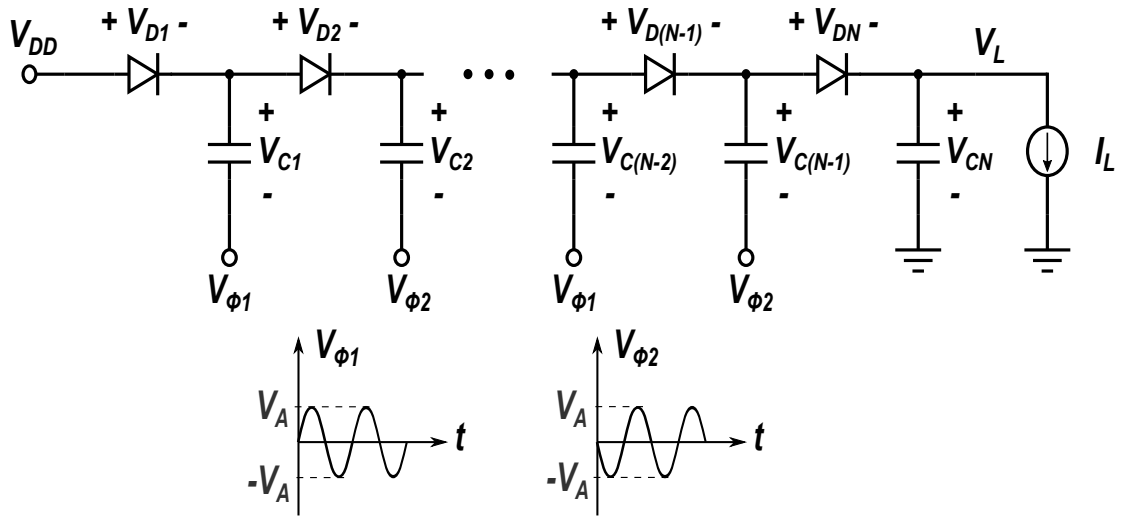


Figure 2.1: DC-DC Dickson charge pump.

The Dickson charge pump shown in Fig. 2.1 requires two out-of-phase clocks, $V_{\phi 1}$ and $V_{\phi 2}$, but it can also operate from a single-phase generator. Briefly, looking the circuit shown in Fig. 2.1, assuming steady state and that the forward voltage drop across each diode is the same [1], the Dickson output voltage is given by

$$V_{L,ideal} = V_{DD} + (N-1)2V_A - NV_D \tag{2.1}$$

in which N is the number of stages, V_D is the diode voltage drop and V_A is the peak voltage of V_ϕ. Here, ideal means that the stray capacitances from the intermediate nodes to ground are negligible and the voltage ripple in the capacitors is very small. This approach gives a good approximation of the Dickson output voltage. However, the diode forward voltage drop was not made explicit in terms of the circuit parameters in [1]. As we shall see in the following, an appropriate estimate of the value of V_D is essential for the calculation of the output voltage, especially for ultra-low-voltage converters.

2.2. Dickson Charge Pump for ULV

To analyze the DCP down to input voltages of the order of dozens of mV, its model should consider that the forward voltage drop across the diodes is not constant and is dependent on both the diode physical parameters and the load current. In [16, 20], the output voltage of the Dickson charge pump was analyzed for a square wave as the oscillatory signal. Based on this previous work, we have modeled the DCP's output voltage, power converter efficiency and input resistance for a sinusoidal wave, as shown in Fig. 2.1.

Firstly, the diode is modeled by the Shockley equation [16, 20, 21] below

$$I_D = I_{sat}\left(e^{\frac{V_D}{n\phi_t}} - 1\right) \tag{2.2}$$

in which I_{sat} is the diode saturation current, n is the diode ideality factor, and ϕ_t is the thermal voltage (kT/q).

Secondly, in steady state the diode average current is equal to the load current, I_L, *i. e.*

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_{sat}\left(e^{\frac{V_D}{n\phi_t}} - 1\right) d\theta \tag{2.3}$$

These assumptions are applied in the next sections in order to model the DCP. These equations are summarized in a recent paper [22].

2.2.1. Output Voltage of the DCP - V_L

Figure 2.2 shows the DCP schematics and the voltage drop across the diodes and capacitors under steady state operation. The voltage waveforms of the leftmost and rightmost diode behave differently from the intermediate diodes, because both D_1 and D_N have one terminal connected to a DC voltage (V_{DD} and V_L, respectively). Therefore, the average voltage across D_1 and D_N are the same, $\overline{V_{D1}} = \overline{V_{DN}}$, while, for the other diodes, the average voltage across them are equal, *i.e.* $\overline{V_{D2}} = ... = \overline{V_{D(N-1)}}$ [16, 20].

Hence, the DCP output voltage (2.1) is rewritten as

$$\begin{aligned} V_L &= V_{DD} - \overline{V_{D1}} - \overline{V_{D2}} - ... - \overline{V_{D(N-1)}} - \overline{V_{DN}} \\ V_L &= V_{DD} - 2\overline{V_{D1}} - (N-2)\overline{V_{D2}} \end{aligned} \tag{2.4}$$

The diode voltages V_{D1} and V_{D2} are calculated for steady state operation and constant load output voltage and current. Furthermore, it is assumed that $V_{\phi 1} = -V_{\phi 2} = V_A cos\theta$ and that the capacitors are high enough to keep the voltage constant.

From Fig. 2.1, the voltage across D_1 is

$$V_{D1} = V_{DD} - V_{C1} - V_A \cos\theta \tag{2.5}$$

The substitution of V_{D1} of (2.5) into (2.3) gives

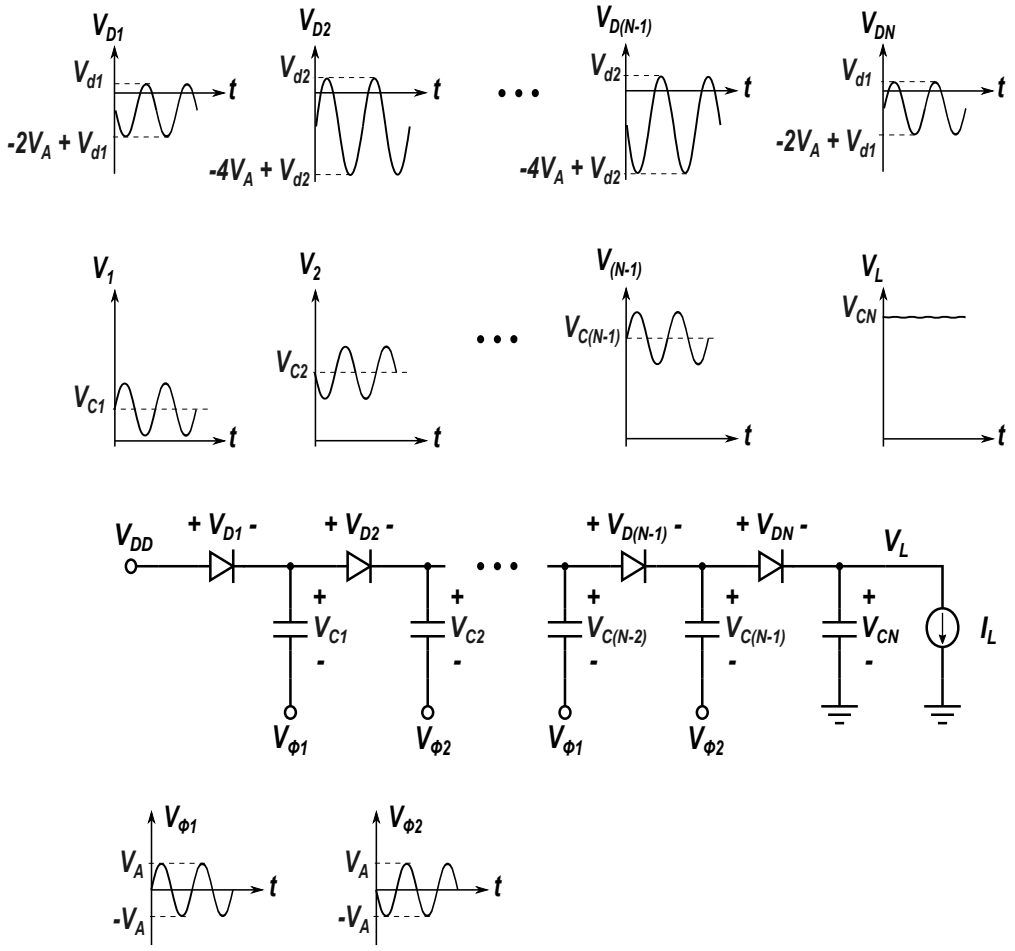


Figure 2.2: Dickson charge pump schematic and voltage across the diodes and capacitors.

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S \left[e^{\frac{V_{DD}-V_{C1}-V_A\cos\theta}{n\phi t}} \right] d\theta \tag{2.6}$$

Solving (2.6) for the voltage stored in C_1 and substituting the resulting value into the voltage drop across D_1 gives, respectively,

$$V_{C1} = V_{DD} + n\phi_t \ln\left[\frac{I_0\left(v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] \tag{2.7}$$

$$V_{D1} = -V_A\cos\theta - n\phi_t \ln\left[\frac{I_0\left(v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] \tag{2.8}$$

where $v_a = V_A/n\phi_t$ is the normalized magnitude of the oscillator output voltage and $I_0(z) = \frac{1}{\pi}\int_0^{\pi} e^{zcos\theta}d\theta$ is the modified Bessel function of the first kind of order zero [23].

The voltage across D_2 is

$$V_{D2} = V_{C1} - V_{C2} + 2V_A\cos\theta \tag{2.9}$$

Replacing V_D of (2.9) into (2.3) gives

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S\left[e^{\frac{V_{C1}-V_{C2}-2V_A\cos\theta}{n\phi t}}\right]d\theta \tag{2.10}$$

Solving (2.10) for the voltage of C_2 and substituting the resulting value of V_{C2} into the voltage drop across D_2 gives, respectively,

$$V_{C2} = V_{DD} + n\phi_t \ln\left[\frac{I_0\left(v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] + n\phi_t \ln\left[\frac{I_0\left(2v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] \tag{2.11}$$

$$V_{D2} = 2V_A\cos\theta - n\phi_t \ln\left[\frac{I_0\left(2v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] \tag{2.12}$$

Replacing the average values $\overline{V_{D1}}$ and $\overline{V_{D2}}$ of (2.8) and (2.12), respectively, into (2.4) gives the DCP output voltage for N stages.

$$V_L = V_{DD} + 2n\phi_t \ln\left[\frac{I_0\left(v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] + (N-2)n\phi_t \ln\left[\frac{I_0\left(2v_a\right)}{1+\frac{I_L}{I_{sat}}}\right] \tag{2.13}$$

Assuming $v_a > 3$, the Bessel function $I_0(z)$ can be approximated by $e^z/\sqrt{2\pi z}$ [23], with an error of less than 5%. For such a case, Eq. (2.13) reduces to

$$V_L = V_{DD} + 2(N-1)V_A - Nn\phi_t \ln\left[\sqrt{2\pi 2v_a}\left(1+\frac{I_L}{I_{sat}}\right)\right] + n\phi_t \ln(2) \tag{2.14}$$

The simplified equation (2.14) presents an error less than 2% when compared to the full equation (2.13), which is a very acceptable error, since the last equation does not make use of the Bessel function.

Figure 2.3 shows V_L from (2.14) (solid line) and electric simulated (symbols) output voltage of a DCP for N ranging from 3 to 11, $V_{DD} = 30$ mV, $V_A = 80$ mV, $\phi_t = 25.9$ mV, and diode parameters $I_{sat} = 1$ μA and $n = 1.05$.

2.2.2. Power Conversion Efficiency - *PCE*

The power conversion efficiency of the DCP is the ratio of the output power to the input power.

$$PCE = \frac{P_{out}}{P_{in}} \tag{2.15}$$

Since the output voltage is given by Eq. (2.13), the converter output power $P_{out} = I_L V_L$ becomes

$$P_{out} = I_L\left[V_{DD} + 2n\phi_t \ln\left(\frac{I_0\left(v_a\right)}{1+\frac{I_L}{I_{sat}}}\right) + (N-2)n\phi_t \ln\left(\frac{I_0\left(2v_a\right)}{1+\frac{I_L}{I_{sat}}}\right)\right] \tag{2.16}$$

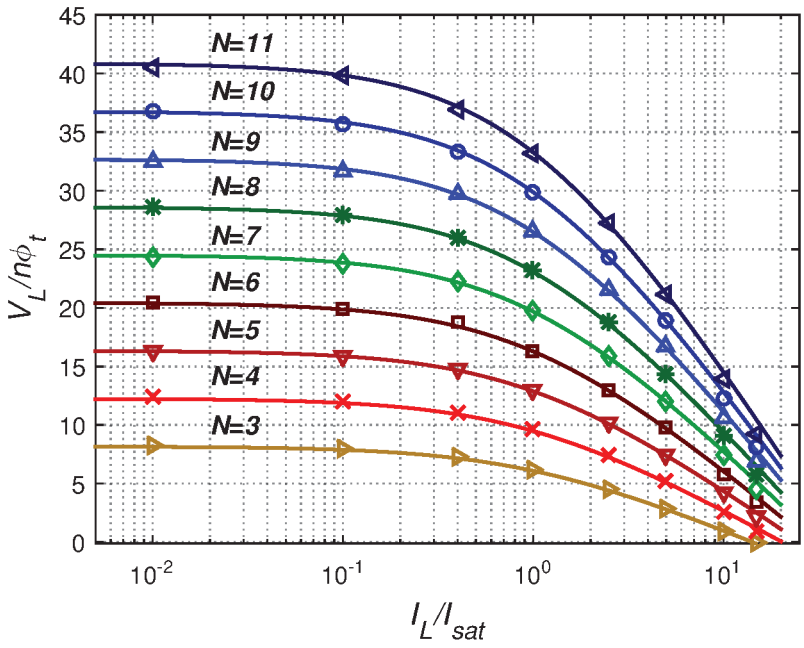


Figure 2.3: Calculated - Eq. (2.14) - (solid line) and electric simulated (symbols) output voltage (V_L) *vs.* load current normalized to the saturation current (I_L/I_{sat}), for N ranging from 3 to 11, V_{DD}=30 mV and V_A=80 mV.

The input power is the output power plus the diode power loss, P_{loss}, where $P_{loss} = 2P_{D1} + (N-2)P_{D2}$, in which P_{D1} is the power loss of the leftmost and rightmost diodes, while P_{D2} is the power loss of the inner diodes. The average power P_D dissipated in a diode is

$$P_D = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_D I_D dt \tag{2.17}$$

Since the diode current follows the Shockley's equation and the voltage drops across the diodes are given by (2.8) and (2.12), the power losses in the diodes are, respectively,

$$P_{D1} = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{D1} I_{D1} d\theta = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{D1} I_{sat}\left(e^{\frac{V_{D1}}{n\phi_t}} - 1\right) d\theta \tag{2.18}$$

$$P_{D2} = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{D2} I_{D2} d\theta = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{D2} I_{sat}\left(e^{\frac{V_{D2}}{n\phi_t}} - 1\right) d\theta \tag{2.19}$$

The solutions of (2.18) and (2.19) yield

$$P_{D1} = (I_{sat} + I_L)2V_A\frac{I_1(v_a)}{I_0(v_a)} - I_L n\phi_t \ln\left(\frac{I_0(v_a)}{1+\frac{I_L}{I_{sat}}}\right) \tag{2.20}$$

$$P_{D2} = (I_{sat} + I_L)2V_A\frac{I_1(2v_a)}{I_0(2v_a)} - I_L n\phi_t \ln\left(\frac{I_0(2v_a)}{1+\frac{I_L}{I_{sat}}}\right) \tag{2.21}$$

where $I_1(z) = \frac{1}{\pi}\int_0^{\pi}\cos\theta e^{z\cos\theta}d\theta$ is the modified Bessel function of the first kind of order one.

From equations (2.20), (2.21), and (2.16), P_{in} becomes

$$P_{in} = I_L \left[V_{DD} + \left(1 + \frac{I_{sat}}{I_L}\right) 2V_A \left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\frac{I_1(2v_a)}{I_0(2v_a)} \right] \right] \tag{2.22}$$

Once the input and output power of the charge pump are known, the power conversion efficiency, PCE, becomes

$$PCE = \frac{V_{DD} + 2n\phi_t \ln\left(\frac{I_0(v_a)}{1+\frac{I_L}{I_{sat}}}\right) + (N-2)n\phi_t \ln\left(\frac{I_0(2v_a)}{1+\frac{I_L}{I_{sat}}}\right)}{V_{DD} + \left(1 + \frac{I_{sat}}{I_L}\right) 2V_A \left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\frac{I_1(2v_a)}{I_0(2v_a)}\right]} \tag{2.23}$$

Even though the DCP efficiency is not the main goal of this work, it can be employed as a criterion to choose among a set of parameters that reaches the required output voltage. Fig. 2.4 shows PCE and $V_L/n\phi_t$ for $v_a = 2$, 4, 6 and 10 . For all cases the efficiency has a peak [24] which, for $V_{DD} = 0$ V, is achieved for the following condition

$$\frac{V_L}{Nn\phi_t} = \frac{I_L}{I_{sat}} \tag{2.24}$$

Note that, in general, the DC input voltage (V_{DD}) does not have an important contribution to the load voltage, since, usually, $V_{DD} << V_L$.

Equation (2.14), for the output voltage, and (2.24), for maximizing the PCE are useful for calculating the values of N and I_{sat} for a given magnitude V_A of the clock signal.

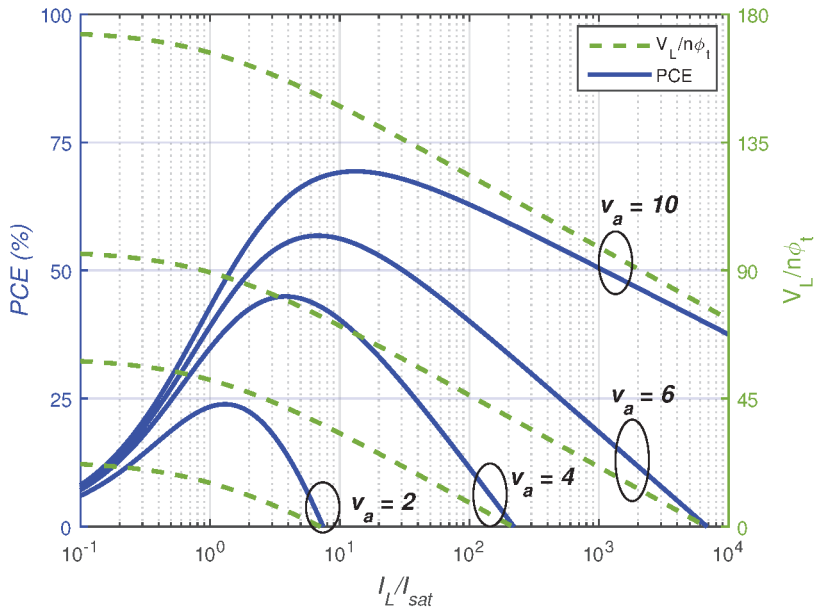


Figure 2.4: PCE and normalized output voltage of an eleven-stage Dickson converter (for $V_{DD} = 0$ V) *vs.* normalized peak voltages $v_a = 2$, 4, 6 and 10.

2.2.3. DCP Input Resistance - R_{in}

Let us now calculate the charge pump input resistance, R_{in}, which loads the oscillator output, as shown in Fig. 2.5. For a sine wave oscillator, the value of R_{in} can be expressed as

$$R_{in} = \frac{V_A^2/2}{P_{in}^*/2} = \frac{V_A^2}{2P_{D1} + (N-2)P_{D2} + P_{out}} \tag{2.25}$$

$$R_{in} = \frac{V_A}{2(I_{sat} + I_L)\left[\dfrac{I_1(v_a)}{I_0(v_a)} + (N-2)\dfrac{I_1(2v_a)}{I_0(2v_a)}\right]} \tag{2.26}$$

where P_{in}^* is the total input power delivered by ϕ_1 and ϕ_2 to the charge pump.

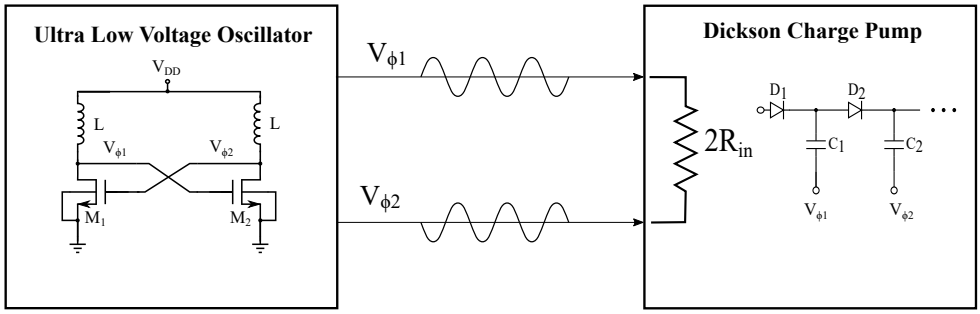


Figure 2.5: Model of the equivalent resistance of the charge pump seen by the oscillator.

When $v_a << 1$, the modified Bessel functions of the first kind reduce to $I_0(z) \approx 1$ and $I_1(z) \approx z/2$ [23]; thus,

$$R_{in,L} = \frac{n\phi_t}{(I_L + I_{sat})(2N-3)} \tag{2.27}$$

On the other hand, when $v_a >> 1$, the modified Bessel functions of the first kind are approximately equal, *i. e.* $I_0(z) \approx I_1(z)$; thus, the normalized input resistance becomes

$$R_{in,H} = \frac{v_a n\phi_t}{(I_L + I_{sat})(2N-2)} \tag{2.28}$$

Using the results of the prior two equations, the normalized input resistance $r_{in} = R_{in}(I_L + I_{sat})/n\phi_t$ can be approximated as

$$r_{in} \approx \sqrt{\left(\frac{1}{2N-3}\right)^2 + \left(\frac{v_a}{2N-2}\right)^2} \tag{2.29}$$

Fig. 2.6 shows the DCP input resistance variation with number of stages for $v_a = 0.4$, 1, 2, and 4. Equation (2.29) (dashed line) has the benefit of simplicity, at the expense of a maximum error of 6.2%, as compared to (2.26) (continuous line), which uses Bessel functions.

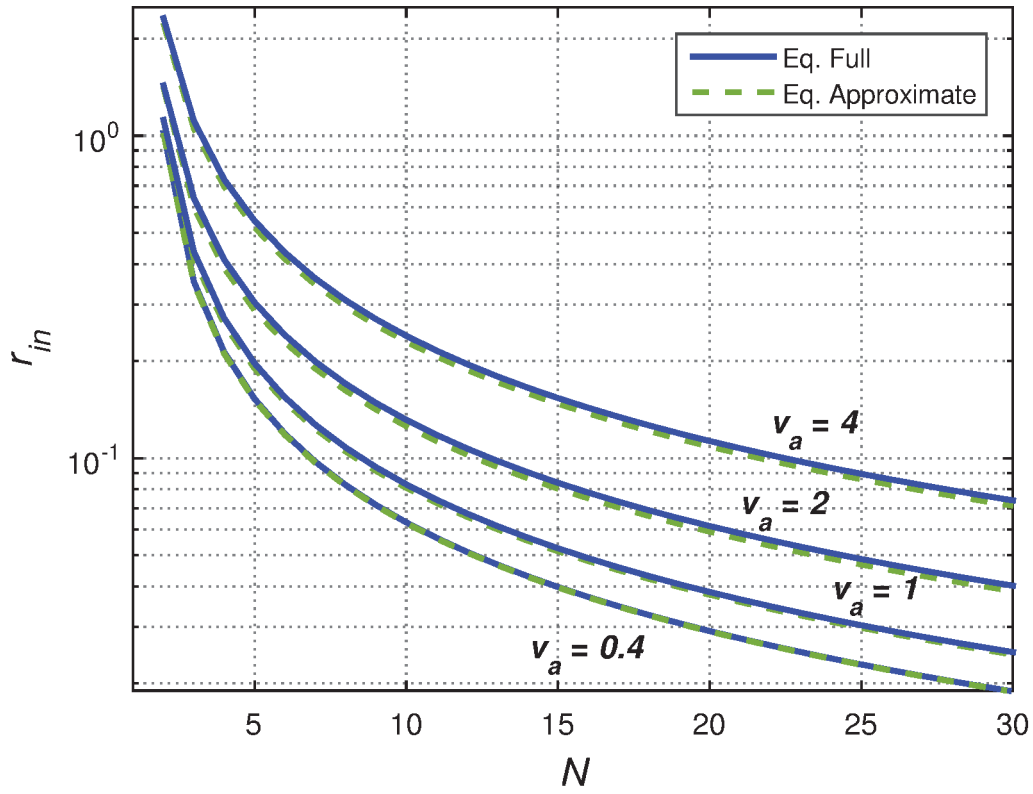


Figure 2.6: DCP input resistance using (2.26), full equation (solid line) and (2.29), approximate equation (dashed line).

2.2.4. DCP Coupling Capacitor - C

The judicious choice of the coupling capacitors is important as regards ripple and transient time. Large capacitors reduce ripple, but, on the other hand, increase the settling time time as well as consume a large area of the integrated circuit.

Let us assume, for the sake of simplicity, that all capacitors are equal. In this case, the relationship between the capacitor C and the voltage fluctuation V_{ripple} at the output node is given approximately by

$$C = \frac{N(I_L + I_{sat})}{2fV_{ripple}} \tag{2.30}$$

In order to avoid both the converter settling time to be high and the waste of silicon area, the capacitance value C should be around the value calculated in the previous equation.

2.2.5. DCP Stray Capacitor - C_s

The DCP suffers from the influence of the stray capacitors C_s shown in Fig. 2.7. The effect of the stray capacitance on the DCP can be calculated from

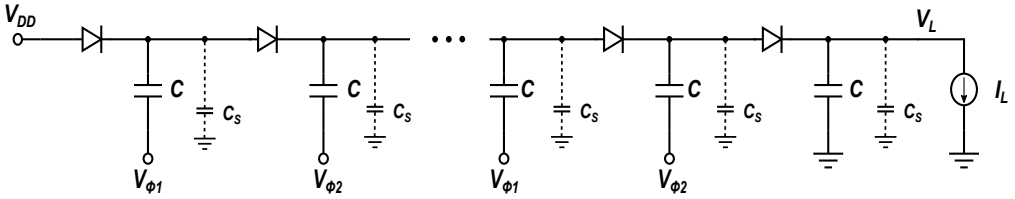


Figure 2.7: Schematic of the Dickson charge pump including the stray capacitances.

$$V'_\phi = \left(\frac{C}{C + C_s}\right) V_\phi \tag{2.31}$$

in which V'_ϕ is the effective oscillator voltage at the internal nodes of the DCP .

For the previous DCP equations, V_L, PCE, R_{in}, the influence of stray capacitors can be taken into account by simply including the attenuation factor of Eq. (2.31). For example, in the 180 nm CMOS technology, the relative value of stray capacitances of MIM (Metal-Insulator-Metal) capacitors varies from 1 % to 12 % when the MIM capacitance changes from 1.8 pF down to 54 fF, as shown in Table A.4 of Appendix A.4.

2.3. Design Equations

In this chapter the main equations of the Dickson charge pump were derived and simplified, as shown in Table 2.1. Equations (2.14) and (2.24) are used to define the number of stages (N) and the diode saturation current (I_{sat}) of a charge pump

Table 2.1: Dickson charge pump equations.

V_L - Full (2.13)
$V_L = V_{DD} + 2n\phi_t \ln\left[\frac{I_0(v_a)}{1+\frac{I_L}{I_{sat}}}\right] + (N-2)n\phi_t \ln\left[\frac{I_0(2v_a)}{1+\frac{I_L}{I_{sat}}}\right]$
V_L - Approximation (2.14)
$V_L \approx V_{DD} + 2(N-1)V_A - Nn\phi_t \ln\left[\sqrt{2\pi 2v_a}\left(1+\frac{I_L}{I_{sat}}\right)\right] + n\phi_t \ln(2)$
PCE (2.23)
$PCE = \frac{V_{DD} + 2n\phi_t \ln\left(\frac{I_0(v_a)}{1+\frac{I_L}{I_{sat}}}\right) + (N-2)n\phi_t \ln\left(\frac{I_0(2v_a)}{1+\frac{I_L}{I_{sat}}}\right)}{V_{DD} + \left(1+\frac{I_{sat}}{I_L}\right)2V_A\left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\frac{I_1(2v_a)}{I_0(2v_a)}\right]}$
Peak Efficiency (2.24)
$\frac{V_L}{Nn\phi_t} = \frac{I_L}{I_{sat}}$
R_{in} - Full (2.26)
$R_{in} = \frac{V_A}{2(I_S+I_L)\left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\frac{I_1(2v_a)}{I_0(2v_a)}\right]}$
R_{in} - Approximation (2.29)
$R_{in} \approx \frac{I_L + I_{sat}}{n\phi_t}\sqrt{\left(\frac{1}{2N-3}\right)^2 + \left(\frac{v_a}{2N-2}\right)^2}$
Coupling Capacitor (2.30)
$C = \frac{N(I_L + I_{sat})}{2fV_{ripple}}$

with high efficiency, while Eq. (2.29) gives the value of the input resistance of the DCP, which is going to be used as the oscillator load. In the next chapter two inductive oscillators topologies are discussed.

3. LOW-VOLTAGE LC OSCILLATORS

3.1. Introduction

The Dickson charge pump we are dealing with requires two oscillatory signals out of phase. These oscillatory signals could be generated, *e.g.* by a conventional ring oscillator (RO). However, conventional ROs do not start up with a DC input lower than of approximately 100 mV.

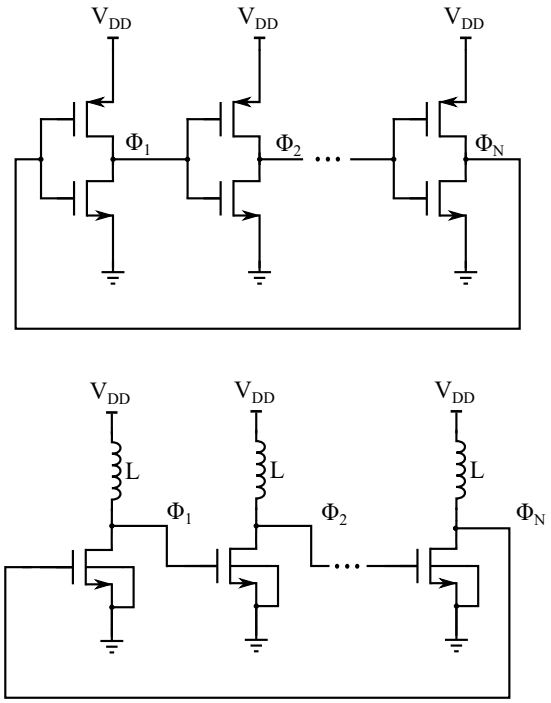


Figure 3.1: Configurations of a conventional ring oscillator and of an inductive ring oscillator .

To overcome this issue, one can use the inductive ring oscillator (IRO) shown in Fig. 3.1, in which the inductor replaces the PMOS transistor. The IRO oscillator is theoretically capable of starting up with a DC voltage lower than that of the standard RO and to provide an oscillation amplitude of around twice the DC input voltage. The inductive ring oscillators to be presented next are based on the work previously published in [25] . For the sake of completeness, the main equations of two types of 2-stage inductive ring oscillators are derived in the next sections .

3.2. Inductive Ring Oscillator - IRO

The 2-stage oscillator presented here is commonly referred to as LC cross-coupled oscillator, but in here it is going to be simply designated as IRO. Next, the frequency of oscillation, minimum transistor gain for oscillation and start-up voltage are derived.

3.2.1. Frequency of oscillation

Fig. 3.2 presents the small-signal model for a single stage of the IRO. g_m and g_{md} are the gate and drain transconductances,, respectively, C is the sum of all parasitic capacitances between the drain node and the AC ground, G_P models the inductor losses, and G_o is the load conductance.

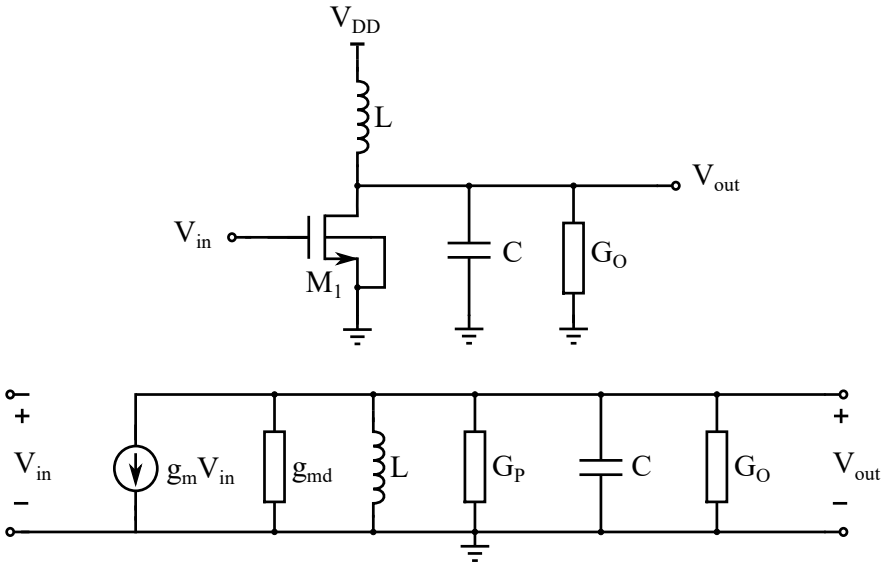


Figure 3.2: A single stage of the inductive ring oscillator and its equivalent small-signal model.

From the small-signal model in Fig. 3.2, in which a negligible gate to drain capacitance has been assumed, KCL gives

$$g_m V_{in} + G V_{out} + \frac{1}{sL} V_{out} + sC V_{out} = 0 \tag{3.1}$$

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{G + \frac{1}{sL} + sC} \tag{3.2}$$

where $G = g_{md} + G_P + G_o$. Replacing s with $j\omega$ the voltage gain becomes

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{G} \frac{1}{1 - j \tan\phi} \tag{3.3}$$

$$\tan\phi = \frac{1 - \omega^2 LC}{\omega LG} \tag{3.4}$$

in which ϕ is the phase shift between the input and output signals.

The Barkhausen criteria says that, for a circuit to oscillate, the phase shift between input and output needs to be a multiple of 2π and the gain should be higher than one [26]. Since the oscillator has two stages, the phase shift of each stage needs to be π; thus, from (3.3) and (3.4), we have

$$\omega = \frac{1}{\sqrt{LC}} \tag{3.5}$$

The influence of the gate-to-drain capacitance, C_{gd}, on the oscillation frequency can be determined by simply substituting $C_P = C + 4C_{gd}$ for C in (3.5) [27]. The extraction of transistor capacitances is shown in Appendix A.1.

3.2.2. Minimum transistor gain for start-up

According to Barkhausen, the loop gain needs to be equal to or slightly higher than unity, *i.e.*

$$\frac{g_m}{g_{md}} \frac{1}{1 + \dfrac{G_P + G_o}{g_{md}}} \geq 1 \tag{3.6}$$

Therefore, the transistor *strength* g_m/g_{md} must be high enough to compensate both the integrated inductor losses (G_P) and the DCP load (G_o).

Using $g_m = (g_{ms} - g_{md})/n$, Eq. (3.6) becomes

$$\frac{g_{ms}}{g_{md}} \geq 1 + n\left(1 + \frac{G_P + G_o}{g_{md}}\right) \tag{3.7}$$

The extraction of the transistor transconductances is shown in Appendix A.1.

3.2.3. Minimum start-up voltage

The minimum voltage required to start up the oscillator can be calculated using the MOSFET model described in Appendix A.1. The drain-source voltage of MOSFET transistor as a function of the transconductances is written below.

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S}\left(g_{ms} - g_{md}\right) + \ln\frac{g_{ms}}{g_{md}} \tag{3.8}$$

Since $V_{DS} = V_{DD}$, replacing (3.7) in (3.8) yields

$$V_{DD} \geq \frac{{\phi_t}^2}{2I_S} g_{md}\left[1 + n\left(1 + \frac{G_P + G_o}{g_{md}}\right)\right] + \phi_t \ln\left[1 + n\left(1 + \frac{G_P + G_o}{g_{md}}\right)\right] \tag{3.9}$$

For an unloaded IRO oscillator, lossless inductors and transistor operation in weak inversion, the minimum start-up voltage is

$$V_{DD,min} = \phi_t \ln\left(1 + n\right) \tag{3.10}$$

Assuming $n = 1$, the limit of (3.10) is 18 mV at room temperature. This limit shows that this oscillator can theoretically operate with half of Meindl limit for digital circuits, which for a CMOS inverter is 36 mV at room temperature [28].

3.3. Enhanced Swing Ring Oscillator - ESRO

Fig. 3.3 shows the ESRO schematics. The connection of each stage to the other via an inductor allows a voltage swing higher than in the case of the IRO [25].

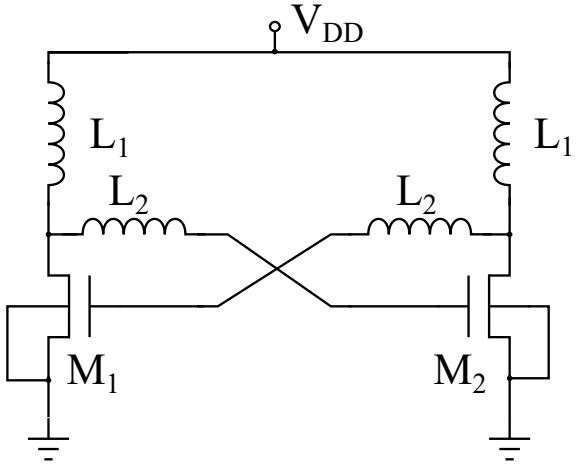


Figure 3.3: Two-stage enhanced swing ring oscillator.

The oscillation frequency of the two-stage ESRO is given [27] by

$$\omega = \frac{1}{\sqrt{[L_1 + L_2 + L_1 R_{S2}(g_{md} + G_{P1})]C}} \tag{3.11}$$

in which R_{S2} is the series resistance of L_2, G_{P1} is the parallel conductance of L_1, C is the capacitance between gate and ground, and g_m and g_{md} are the gate and drain transconductances, respectively.

Applying the Barkhausen criteria, the ESRO starts up when the gain is higher than unity or, equivalently

$$\frac{g_{ms}}{g_{md}} \geq 1 + n\left[\left(1 + \frac{G_{P1}}{g_{md}}\right)(1 - L_2 C\omega^2) + \frac{R_{S2}C}{L_1 g_{md}}\right] \tag{3.12}$$

The DC voltages of the transistors are $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. Using (3.8) in weak inversion, the $V_{DD,min}$ to start up the oscillator [27] is

$$V_{DD,min} = \phi_t \ln\left(1 + n\frac{L_1}{L_1 + L_2}\right) \tag{3.13}$$

Even though the ESRO can enhance the oscillation magnitude, its design has more variables and, thus, is more complex than the design of the IRO. Also, integrated inductors demand too much area. For example, using the 180 nm CMOS technology, an inductance of around 20 nH characterized by the technology requires silicon area larger than 600 μm x 600 μm. In general, since the ESRO demands too much area as compared to the IRO and offers insignificant or almost no benefit, the latter is generally recommended for integration.

Chapter 5 presents the design of two Dickson converters, one of which uses an ESRO in a 130 nm technology, while the other uses an IRO in a 180 nm technology.

4. COMPUTATIONAL ANALYSES

The design of a DC-DC step-up converter has many degrees of freedom, namely the oscillator and charge pump parameters. Also, the oscillator and the DCP cannot be designed independently since the oscillator amplitude (V_A) is dependent of its load (R_{in}), the input resistance of the DCP, which, in turn, is dependent on the oscillator amplitude. This mutual dependence between parameters of the two blocks complicates the hand design of the converter.

In order to make the Dickson converter design less dependent of the circuit simulator, a MatLab routine was developed. The routine uses the parameters and equations developed for the design of both the oscillator and the charge pump. The electrical parameters of components, namely transistors, inductors and capacitors are extracted from the simulator. All these parameters are used to simulate the time behavior of the converter.

The routine outputs an overview of the converter output voltage for a given design space composed of the number of stages and the diode saturation current employed for the Dickson charge pump.

4.1. Initial Conditions

Initially, the unloaded oscillator is simulated, aiming at starting up at the lowest voltage. The integrated inductors present a very small range of inductance values as well as low quality factors, as shown in Appendix A.3. Therefore, the design space of inductors is very small.

Appendix A.3 presents the inductor model and parameters for a set of inductors that can be integrated in the 180 nm technology.

After knowing the features of the inductors available for design, it is necessary to find the transistors for the oscillators. First, the expected gate capacitance of the transistor is chosen using (3.5), for the required oscillation frequency. This frequency should be chosen in order to allow the quality factor of the inductor to be high.

Appendix A.2.3 explains how the gate capacitance was extracted from the dc simulation.

Some combinations of inductors and transistors were tested in order to find the combination which provides the lowest input voltage for starting up the oscillator.

Once the oscillator components have been defined, the main physical parameters of both the inductor and the transistor were extracted by the electrical simulator and transferred to the MatLab routine.

After the oscillation frequency and the components parameters have been known, the oscillator performance was analyzed having the R_{in} of the DCP as the oscillator load.

4.2. Time analyses

Fig. 4.1 shows the oscillator schematic powered by a thermoelectric generator source and loaded with the DCP, represented by its input resistance, R_{in}. The thermoelectric generator (TEG) is represented by an ideal DC voltage source, V_{TEG} and a series resistance, $R_{TEG} = 5\ \Omega$. R_P is the inductor parallel resistance while C_P is the capacitance seen from the transistor gate.

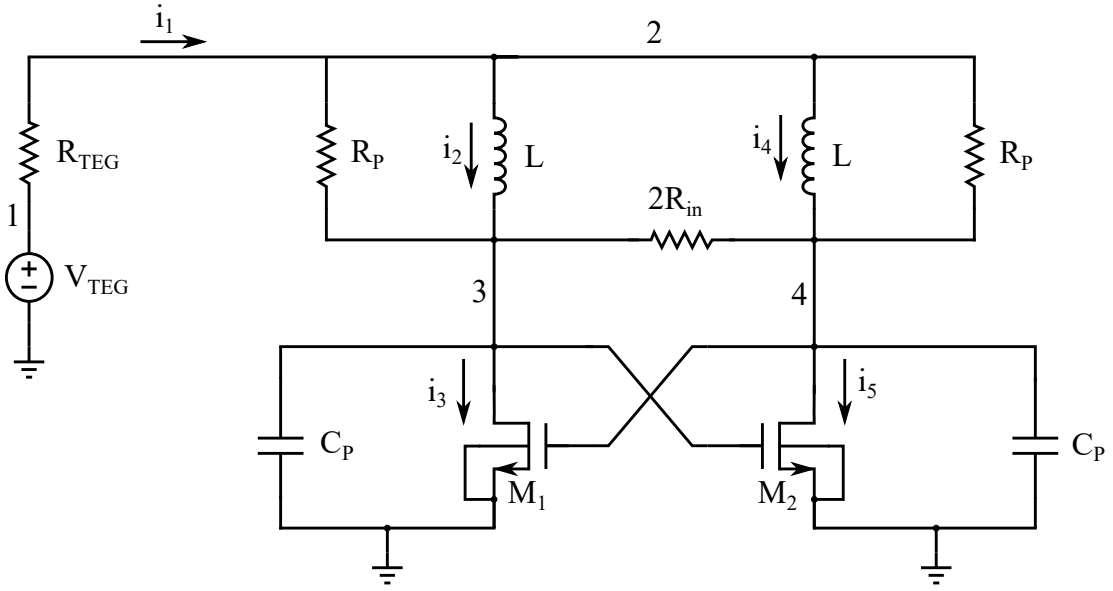


Figure 4.1: Startup schematic.

The circuit behavior over time is achieved using i-v relationships for the capacitor, inductor and resistor , shown below, along with the transistor equation for the current.

$$i_C = C \times \frac{dv_C}{dt} \tag{4.1}$$

$$v_L = L \times \frac{di_L}{dt} \tag{4.2}$$

$$i_R = \frac{v_R}{R} \tag{4.3}$$

The current (I_D) can be calculated using the transistor model described in Appendix A.1. The DC equations are

$$I_D = I_F - I_R \tag{4.4}$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln(\sqrt{1 + i_{f(r)}} - 1) \tag{4.5}$$

$$V_P = \frac{V_G - V_B - V_T}{n} \tag{4.6}$$

where

$I_{F(R)}$ - forward (reverse) current for weak inversion
I_S - specific current extracted using the g_m/I_D method
V_P - pinch off voltage
V_T - threshold voltage extracted using g_m/I_D method
V_D, V_S, V_G, V_B, - drain, source, gate, and bulk voltages
ϕ_t - thermal voltage
$i_{f(r)} = I_{F(R)}/I_S$ is the forward (reverse) inversion level of the transistor.

4.3. MatLab routine

A MatLab routine was developed for solving the circuit shown in Fig. 4.1 . This routine simulates the time behavior of the oscillator, using the current and voltage equations of the circuit. In order to start up the oscillator simulation, the introduction of an initial condition was necessary; in our case, we applied a voltage difference between nodes 3 and 4, $\Delta V = 30$ mV. Once the oscillation steady state is reached, the routine calculates the frequency (f) and the amplitude (V_A) of oscillation.

Another variable parameter is the input resistance of the charge pump, R_{in}, which is dependent on V_A, I_{sat} and N. Each time either I_{sat} or N changes, R_{in} changes and, consequently, V_A also changes. Thus, some iterations, typically three of them, must be run in order to have the correct values of R_{in} and V_A.

Figure 4.2 presents two rounds of simulation for $I_{sat} = 900$ nA, $N = 27$ and $V_{TEG} = 52$ mV. In this case, the value of R_{in} for initialization is $10^{20}\Omega$. For the following iterations, R_{in} is the input resistance of the previous combination of the DCP parameters. As shown in Table 4.1 the values of R_{in} and V_A do not change more than 1 percent from the third to the fourth iteration. For the new set of I_{sat} and N, the last value of R_{in} is taken as the first guessed value, and the iterations are repeated, as shown in the flowchart.

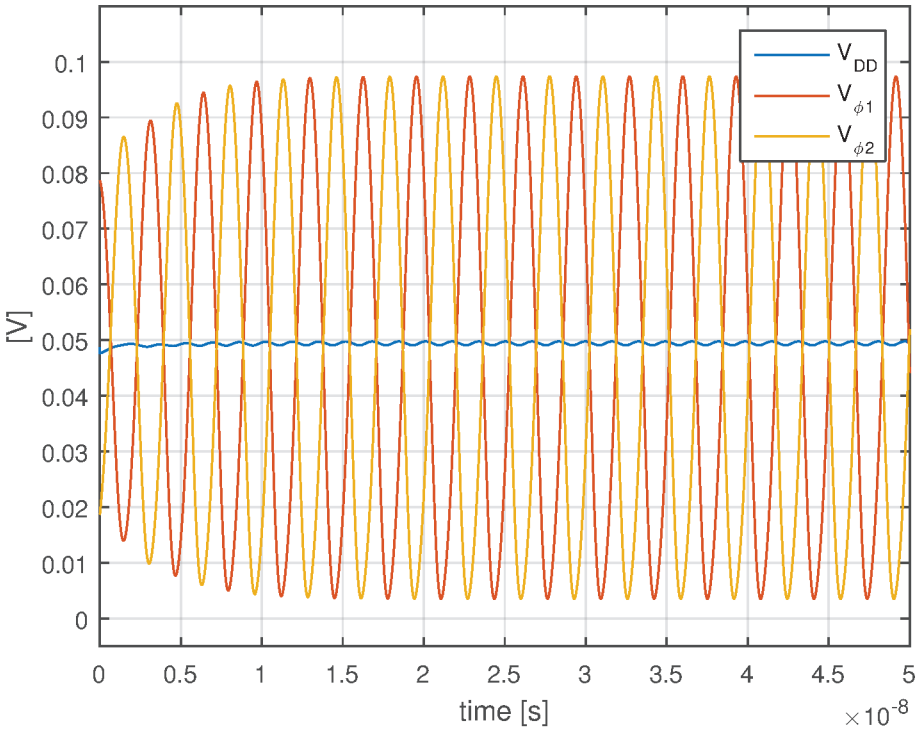
Table 4.1: R_{in} and V_A variation over 4 iterations for $I_{sat} = 900$ nA, $N = 27$ and $V_{TEG} = 52$ mV.

Iteration	R_{in}	V_A
1	10^{20} Ω	97.3 mV
2	1.057 kΩ	92.0 mV
3	0.998 kΩ	91.5 mV
4	0.995 kΩ	91.5 mV

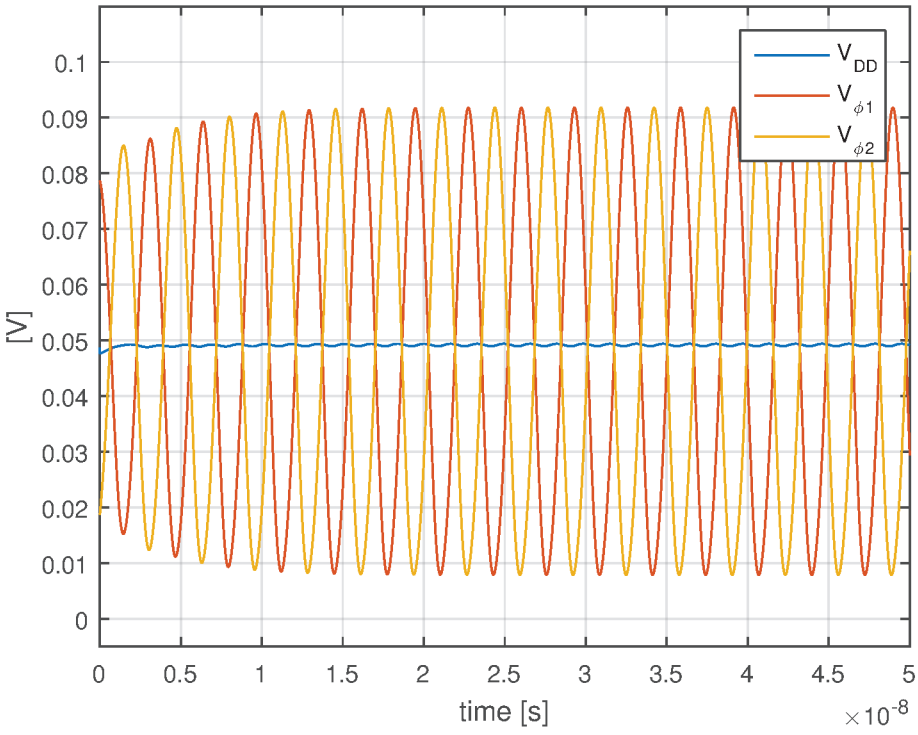
Figure 4.3 shows a sequence of steps that have been followed in order to obtain the time behavior of the startup circuit for different DCP parameters. The * means that, for the very first set of DC parameters, R_{in} is an open circuit.

4.4. Converter design space

Using the flowchart with the oscillator specifications shown in Table 4.2 and load ($I_L = 200$ nA and $V_L = 500$ mV), one can find a set of charge pump parameters



(a)



(b)

Figure 4.2: a) First iteration - $R_{in} = 10^{20}\Omega$. b) Second iteration - $R_{in} = 1.057k\Omega$, both for $I_{sat} = 900$ nA, $N = 27$ and $V_{TEG} = 52$ mV.

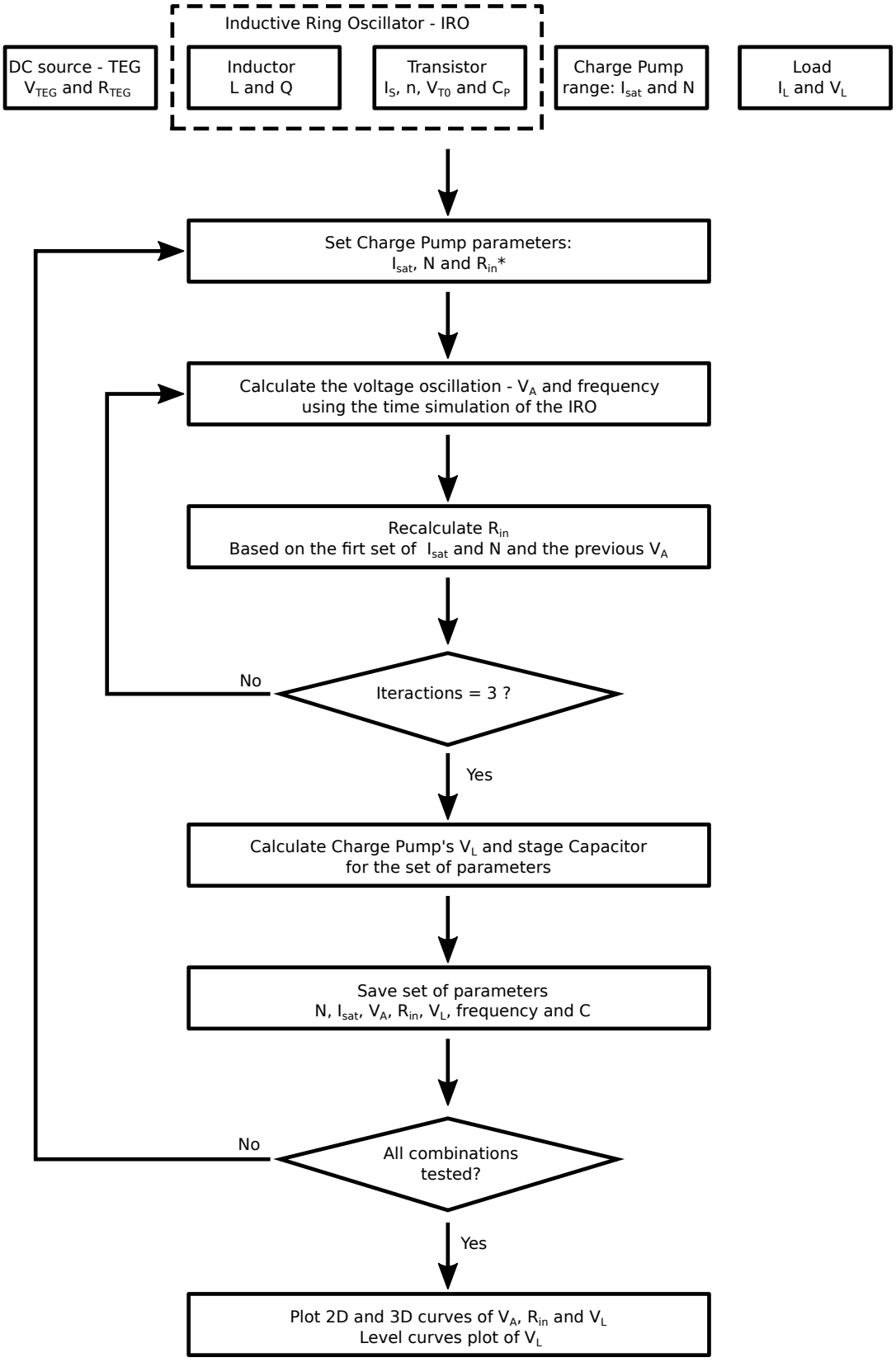


Figure 4.3: Flowchart of the Matlab routine employed for finding the values of I_{sat} and N.

for achieving the minimum start-up voltage, after repeating this routine for a few times.

Table 4.2: Oscillator parameters

Oscillator		
Inductor	Native Transistor	
$L = 18$ nH	$I_S = 1.57$ mA	$n = 1.27$
$Q \simeq 9^*$	$W = 40$ x 4 x 22 μm	$L_{MOS} = 500$ nm
	$V_{T0} = 143.14$ mV	$C_P = 21$ pF

* At oscillation frequency equal to 255 MHz.

The design space for a given DC input voltage is shown either as the DC output voltage in terms of I_{sat} and N, as in Fig. 4.4a, or as a set of level curves, as in Fig. 4.4b.

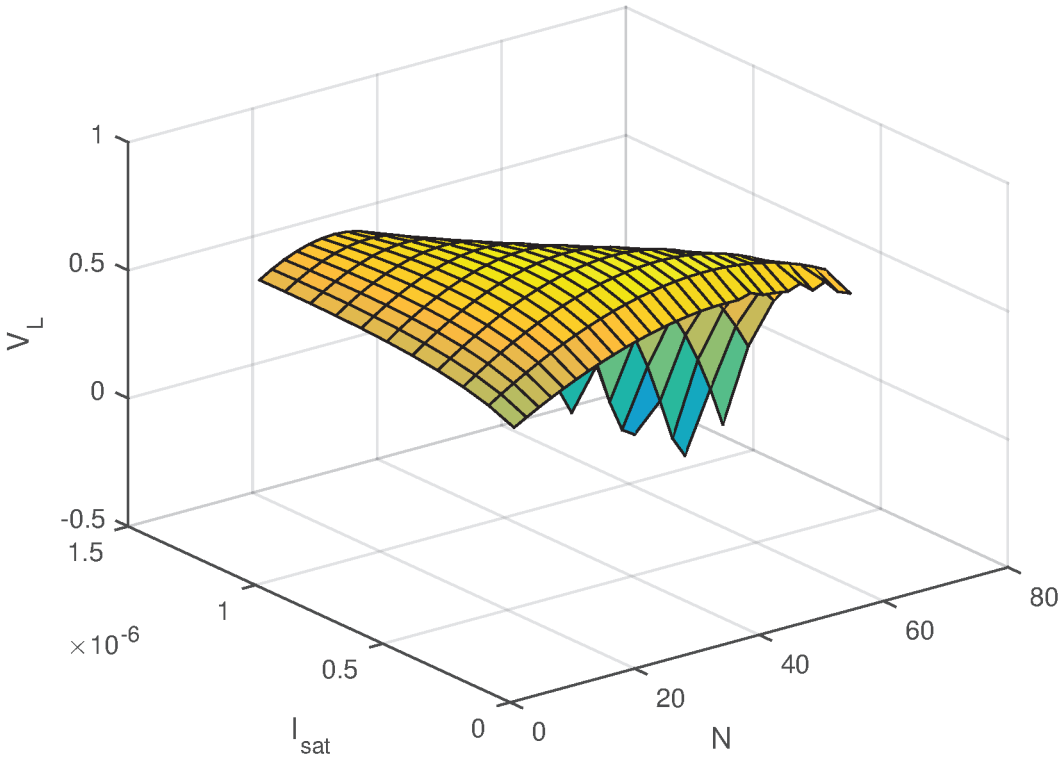
As expected, for fixed I_{sat}, the output voltage increases and, then decreases with the number of DCP stages. This is a consequence of the decrease of the input resistance R_{in} of the DCP as the number of stages increases. The decrease in R_{in} is responsible for the reduction of V_A which, in turn, contributes to reduce the output voltage, which is no longer compensated by the increase of N. The same reasoning applies for the variation of I_{sat} with a fixed value of N.

Figure 4.5a shows the DCP input resistance for the same range of N and I_{sat} as in Fig. 4.4a. R_{in} decreases and, consequently, V_A also decreases for increasing N and I_{sat}. The level curves of V_A are shown in Fig. 4.5b.

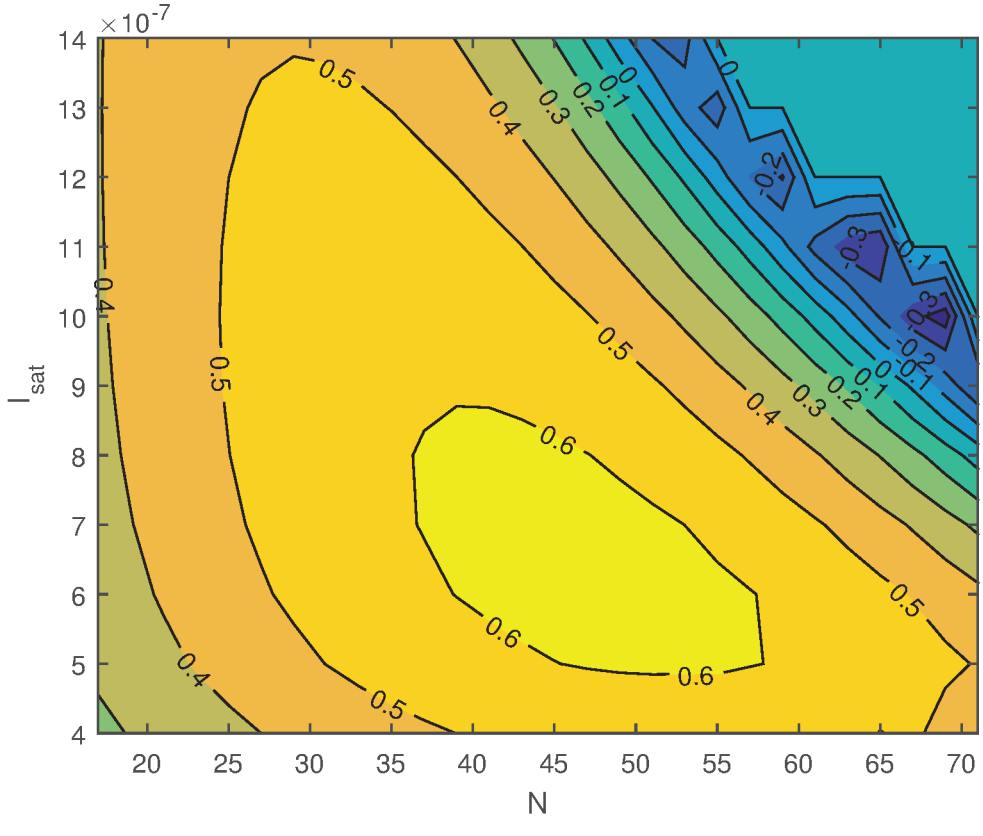
Curves of V_A and V_L for variation of either N or I_{sat}, obtained from the MatLab routine are shown in Fig. 4.6a and Fig. 4.6b, respectively

Using the results provided by the computational analysis shown in figure 4.4b, we found that the best combination of parameters N and I_{sat} is 27 and 900 nA, respectively. Since I_{sat} is a parameter which is dependent onn the voltage applied to the diode-connected transistor due to the connection of the substrate to ground, it may change along the diode chain. We found that N equal to 27 achieves 500 mV at the converter output even if the value of I_{sat} changes from 900 nA to 700 nA.

After most of the parameters have been defined, the components were introduced into the simulator in order to check the schematics behavior. The diode-connected transistor was designed for $I_{sat} = 900$ nA. After the diode has been designed, the diode chain was tested; it was expected that 27 stages would make the output voltage achieve 500 mV for $I_L = 200$ nA; since this condition was attained, the circuit was laid out for further simulation and fabrication.

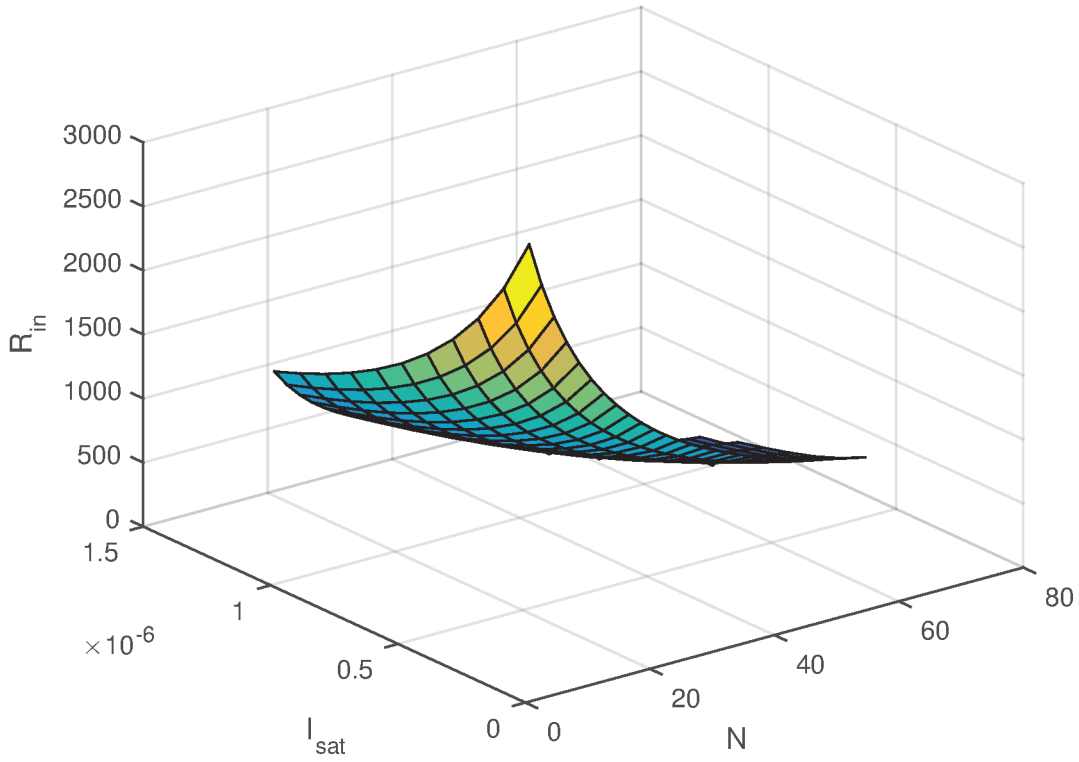


(a)

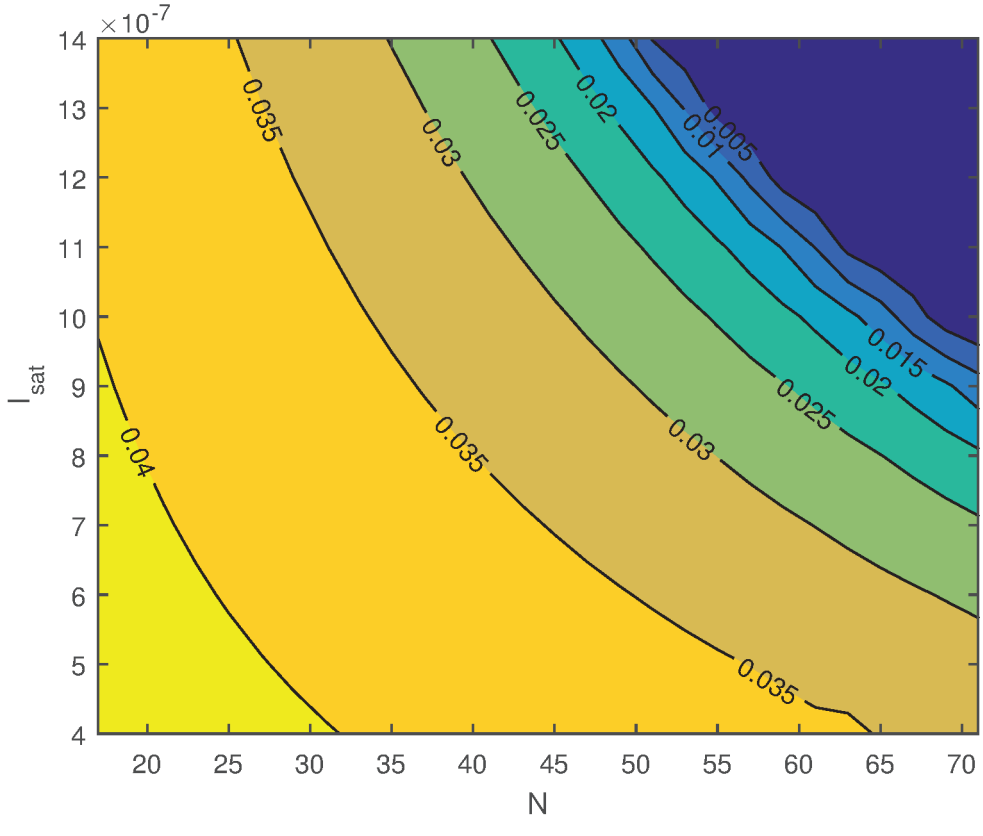


(b)

Figure 4.4: a) Converter output voltage and b) Level curves of V_L for N varying from 3 to 70, I_{sat} ranging from 0.4 μA to 1.4 μA and $V_{TEG} = 52$ mV.

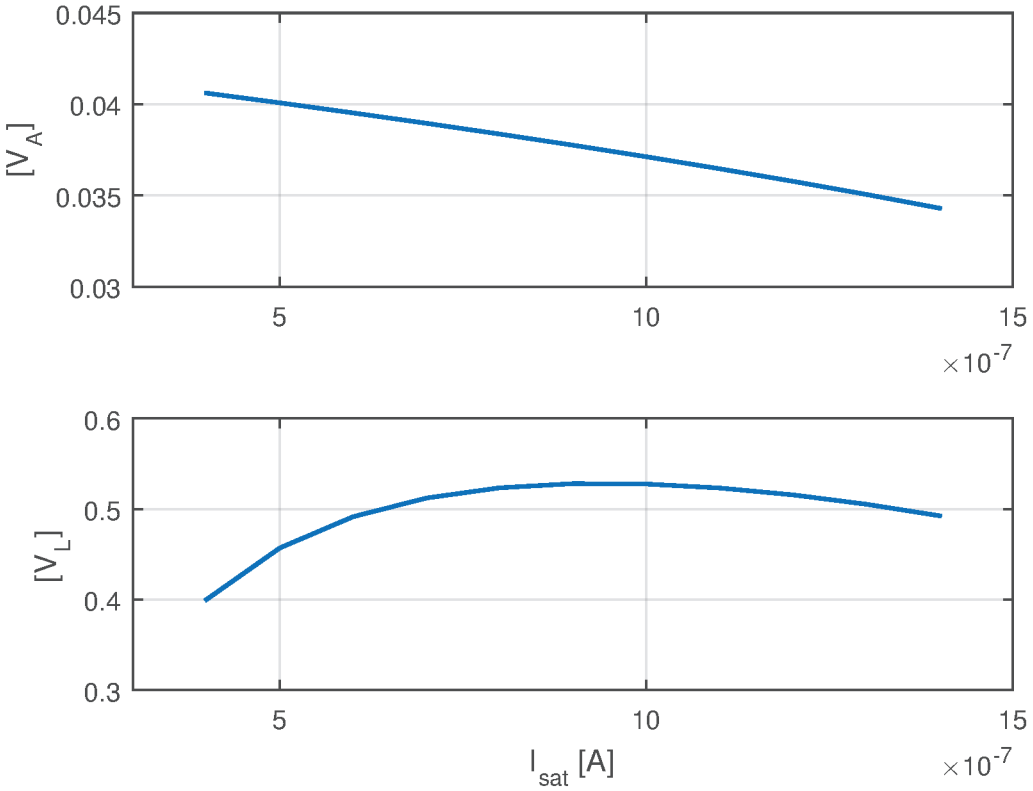


(a)

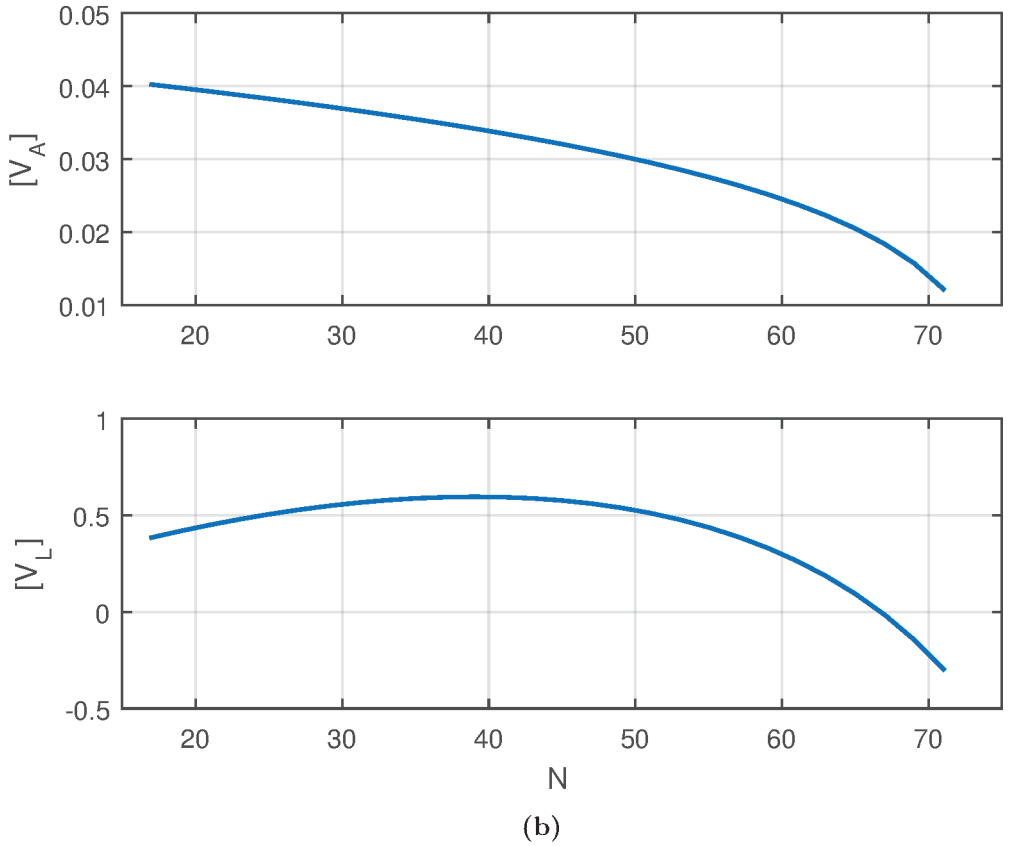


(b)

Figure 4.5: a) Input resistance of the Dickson charge pump and b) Level curves of the oscillator voltage amplitude, for N varying from 3 to 70, I_{sat} ranging from 0.4 μA to 1.4 μA and $V_{TEG} = 52$ mV.



(a)



(b)

Figure 4.6: Oscillator and DCP output voltage variation for $V_{TEG} = 52$ mV. a) V_A and V_L versus I_{sat} for $N = 27$. and b) V_A and V_L versus N for $I_{sat} = 900$ nA.

5. DESIGN AND EXPERIMENT

In this chapter, designs and tests of two Dickson converters are shown and discussed. The first converter, called DCP design with IRO, was fabricated in a TSMC 180 nm CMOS technology, while the second, called DCP design with an ESRO, was integrated in a IBM 130 nm CMOS technology.

The IBM 130 nm technology has 8 layers of metal available for this project. The back end of line is 323, where it means 3 thin, 2 thick, and 3 top metals. The TSMC 180 nm technology has 6 layers.

5.1. DCP design with IRO

To design this DCP converter the MatLab routine was very helpful since it gives the DCP parameters very close to the envisaged solution, thus reducing considerably the number of simulations to be run in the electrical simulator. In the following subsections, details about the design and experimental results are presented.

5.1.1. Schematic Simulation and Layout

The oscillator was simulated using the Virtuoso Analog Design Environment version IC6.1.7, without load in order to find the combination of inductor and transistor that reaches the lowest startup voltage. The first parameter defined was the inductor. Appendix A.3 shows a list of inductors with their quality factors for a set of track width ranging from 3 μm to 30 μm for fixed both number of turns and inner radius and guard ring distance equal to 5.5, 150 μm and 50 μm, respectively.

Inductors with high quality factor (around 10) require a considerable amount of silicon area. As an example, the standard inductor with maximum dimensions (last inductor specified in Table A.3) characterized by the technology requires a silicon area of 790 μm x 790 μm. Due to the small area, 1.5 mm x 1.5 mm, available to our design, the size of inductors is very limited. The transistors dimensions were chosen such that the transistor capacitance leads to an oscillation frequency where the quality factor of the inductor is acceptable for the oscillator. Having also taking into account limitations of silicon area, the characteristics of the inductor and transistor for the IRO are shown in Table 5.1. In schematic simulation the unloaded oscillator starts up at $V_{TEG} = 45$ mV. After schematic simulation of the oscillator, the MatLab routine gives the starting point for the DCP parameters. According to Fig.4.4b, the 27-stage DCP can deliver 500 mV for I_{sat} ranging from 600 nA to 1.1 μA.

After some iterations between MatLab routine and Virtuoso simulator the final parameters of the Dickson converter (Fig. 5.1) shown in Table 5.1 were found.

Table 5.1: Dickson design with IRO Oscillator parameters.

Inductive Ring Oscillator - 2 stages		
Inductor	Native NMOS Transistor	
$L = 18$ nH	$I_S = 1.57$ mA	$n = 1.27$
$Q \simeq 9$	$W^* = 40$ x 4 x 22 μm	$L = 500$ nm
$f = 255$ MHz	$V_{T0} = 143.14$ mV	$C_P = 21$ pF
Dickson Charge Pump - 27 stages		
Capacitor	Diode-Connected Transistor	
$C = 0.80$ pF	$I_{sat} = 900$ nA	$n = 1.55$
$W = L = 20$ μm	$W^{**} = 5$ x 3.2 μm	$L = 500$ nm

* Parallel combination of interdigitaded transistor with 4 fingers.
** Interdigitaded transistor with 5 fingers.

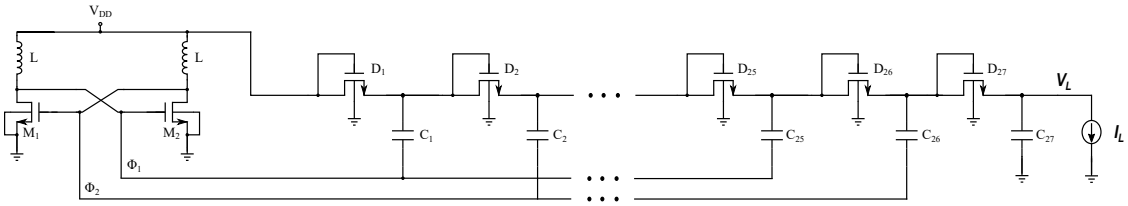


Figure 5.1: Schematics of the Dickson design with IRO.

Post-layout simulations showed that the converter starts up with $V_{TEG} = 55$ mV, but reaches the load conditions only for $V_{TEG} = 63$ mV. Fig 5.2 shows V_{DD} and a) oscillator phases and b) Output voltage of the DCP loaded with a resistor $R_L = 2.5$ MΩ ($V_L = 500$ mV / $I_L = 200$ nA). At this point the oscillator frequency was 250 MHz.

5.1.2. Experimental Results

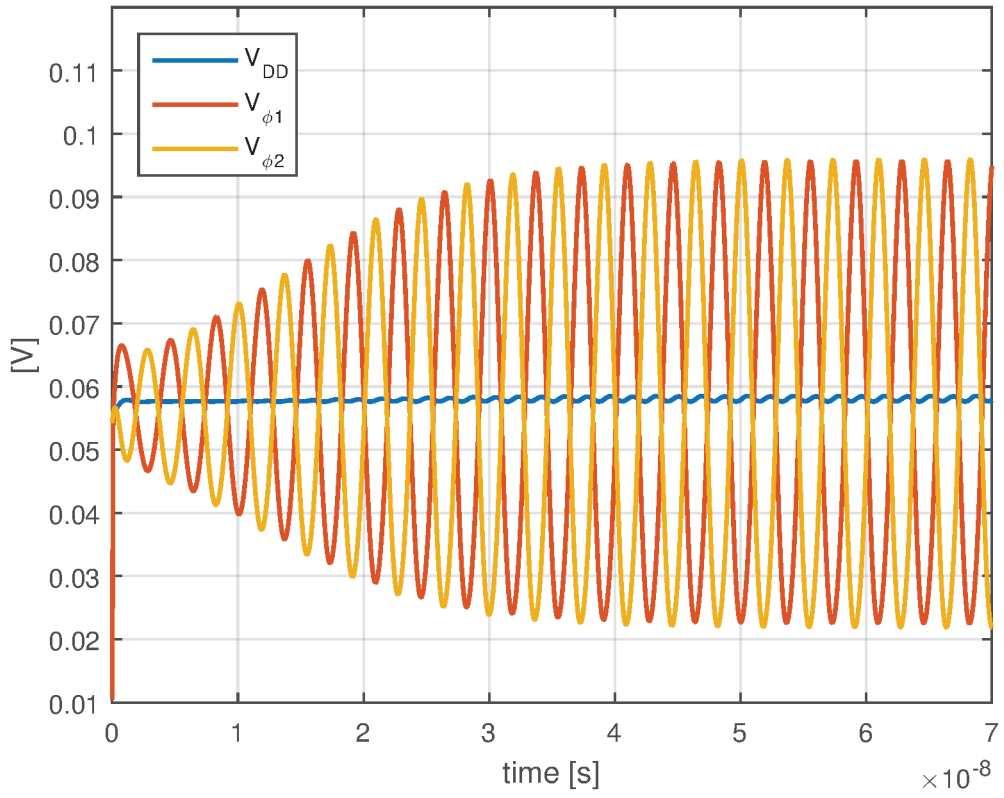
After the design has been concluded, the converter was fabricated through the MOSIS program. The chip micrograph is presented in Fig. 5.3a, while Fig. 5.3b is a zoom of the chip showing the Dickson charge pump.

5.1.2.1. Converter Output Voltage

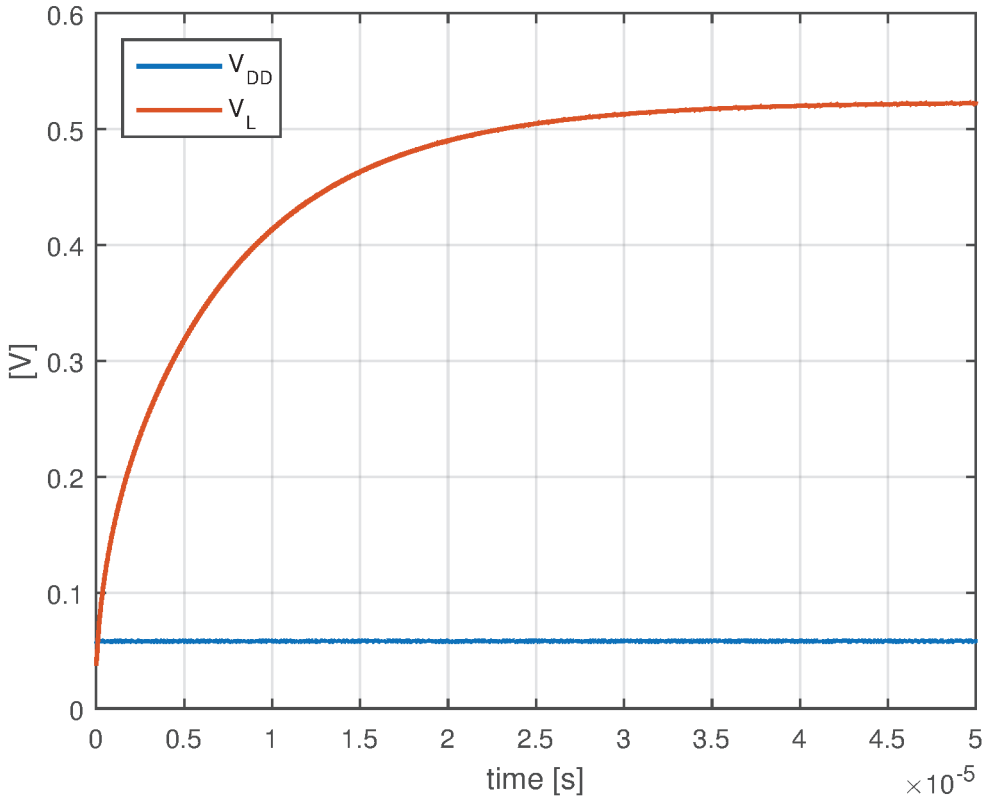
For measuring the converter prototype, the Keithley 2401 SourceMeter was used to emulate the TEG and measure the current sunk by the converter. The DC source voltage (V_{TEG}) was increased gradually from 60 to 140 mV with steps of 1 mV and the R_{TEG} is equal to 5 Ω. The Agilent 34401A digital multimeter, with input resistance higher than 10 GΩ, measured the converter output voltage. The measurement setup is shown in Fig. 5.4.

Firstly, the startup voltage of the converter loaded with the multimeter probe only was measured . Table 5.2 shows the results of four chips. The average start-up voltage and input power are 84 mV and 86.1 μW, respectively.

Since the converter was designed to supply a load of 500 mV / 200 nA, a 2.5 MΩ resistor was used to emulate the load. For this load, the converter starts up at $V_{TEG} = 85$ mV and reaches the 500 mV output for $V_{TEG} = 94$ mV. Here the start

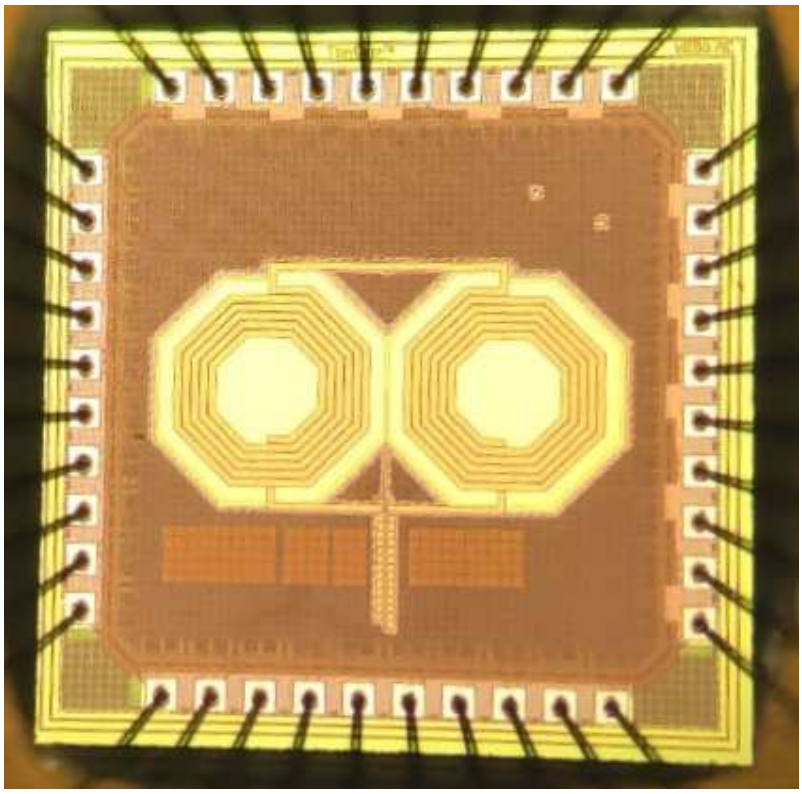


(a)

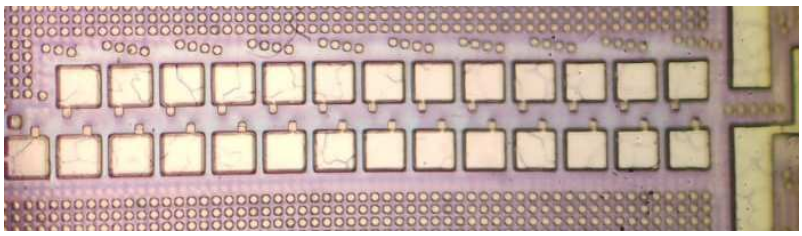


(b)

Figure 5.2: (a) V_{DD} and oscillator output voltages; (b) Converter output voltage. $V_{TEG} = 63$ mV and $R_{TEG} = 5\ \Omega$. The converter load is $R_L = 2.5$ MΩ.



(a)



(b)

Figure 5.3: (a) Micrograph of the chip of the Dickson converter using IRO; (b) Detail of the micrograph showing the Dickson charge pump.

Table 5.2: Startup voltage for the converter loaded with the multimeter probe (R_{in} > 10 GΩ).

	Startup		
	V_{TEG} (mV)	I_{TEG} (mA)	P_{in} (μW)
Chip A	84	1.03	86.52
Chip B	84	0.96	80.64
Chip C	84	1.09	91.56
Chip D	84	1.02	85.68
Average	84.00	1.03	86.10

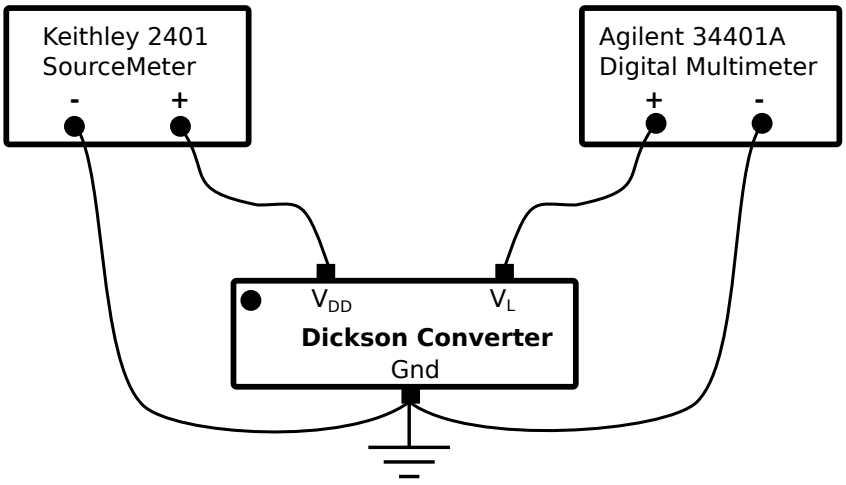


Figure 5.4: Measurement setup of the DC/DC converter.

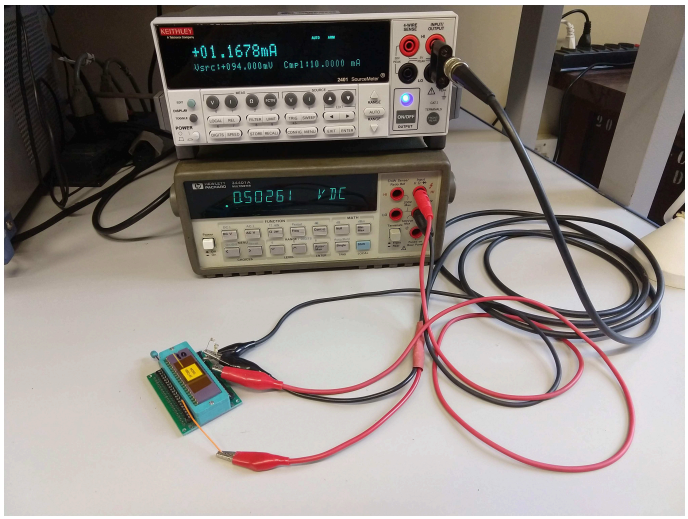


Figure 5.5: Setup for measuring the converter output voltage.

up conditions is when the output voltage changes more then 10 mV for each mV variation at the input. The measurement setup is shown in Fig. 5.5. Tables Table 5.3, Table 5.4 and Table 5.5 show results of the DC/DC converter for I_L = 200 nA, 500 nA and 1 μA, respectively. The power converter efficiency ($PCE_{conv} = P_{out}/P_{in}$) is also presented for each case. Note that the PCE_{conv} is very low, but this is caused by having a fully-integrated solution that starts up at a low voltage.

The measurements showed a startup input voltage of the order of 50% higher than that of post-layout simulation. This discrepancy may be caused by several factors, such as the influence of other circuits around the converter, the pads employed for measurements, poor inductor and transistor modeling, among others less significant. Another important characteristic of the converter is that an increase of around 10 % in V_{TEG} of startup makes the output voltage double. The modeling and characterization of the diode-connected native transistors used in this design are shown in Appendix A.2.4.

Table 5.3: Converter input voltage (V_{TEG}) and current (I_{TEG}) for I_L = 200 nA and V_L equal to 500 mV and 1 V.

I_L = 200 nA				
	V_L = 500 mV		V_L = 1 V	
	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)
Chip A	94	1.17	103	1.28
Chip B	95	1.11	104	1.22
Chip C	94	1.23	104	1.36
Chip D	95	1.17	104	1.28
Average	94.50	1.17	103.75	1.29
PCE_{conv}	0.09 %		0.15 %	

Table 5.4: Converter input voltage (V_{TEG}) and current (I_{TEG}) for I_L = 500 nA and V_L equal to 500 mV and 1 V.

I_L = 500 nA				
	V_L = 500 mV		V_L = 1 V	
	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)
Chip A	101	1.27	110	1.38
Chip B	102	1.21	111	1.32
Chip C	101	1.33	110	1.44
Chip D	101	1.26	111	1.38
Average	101.25	1.27	110.50	1.38
PCE_{conv}	0.19 %		0.33 %	

Table 5.5: Converter input voltage (V_{TEG}) and current (I_{TEG}) for I_L = 1 μA and V_L equal to 500 mV and 1 V.

I_L = 1 μA				
	V_L = 500 mV		V_L = 1 V	
	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)
Chip A	109	1.39	120	1.53
Chip B	110	1.32	121	1.46
Chip C	109	1.45	119	1.57
Chip D	110	1.39	120	1.52
Average	109.50	1.39	120.00	1.52
PCE_{conv}	0.33 %		0.55 %	

5.2. DCP design with ESRO

This DCP was designed using the ESRO, which requires two inductors per stage. The 130 nm CMOS node allowed the design of this converter in a much smaller area than in the 180 nm node, since the available inductors require less silicon area. Another difference is that this converter was designed to deliver $V_L =$ 1 V and $I_L = 1$ μA.

5.2.1. Schematics Simulation and Layout

For the design of this DCP we have not run the MatLab routine, but the remaining design steps of the previous DCP were followed. Through circuit simulation in Cadence, we first found the unloaded ESRO that started at the lowest input voltage. The ratio of inductances L_2/L_1 was chosen equal to three. Then, using the amplitude voltage obtained from the Cadence simulator, the Dickson charge pump was designed. Using the output voltage equation, the number of stages and the diode widths were determined and, following next, the oscillator was simulated again using a resistor as the load. This resistor represents the input resistance of the charge pump. Some iterations later, the DCP parameters were found. The final values used in the Dickson converter are shown in Table 5.6, while its schematic diagram is shown in Fig. 5.6. Fig. 5.7 shows the DCP and ESRO layouts.

Table 5.6: Converter parameters

Enhanced Swing Ring Oscillator - 2 stages		
Inductors	Transistor ZVT	
$L_1 = 22$ nH $L_2 = 66$ nH	$I_S = 225.7$ μA	$n = 1.06$
$Q \simeq 8$	$W = 20$ x 25 μm	$L = 420$ nm
$f \simeq 400$ MHz	$V_{T0} = 62.6$ mV	$C_P = 1.55$ pF
Dickson Charge Pump - 13 stages		
Capacitor	Diode-Connected LVT3T Transistor	
$C = 0.90$ pF	$I_{sat} = 650$ nA	$n = 1.4$
$W = L = 11$ μm	$W = 14$ μm	$L = 700$ nm

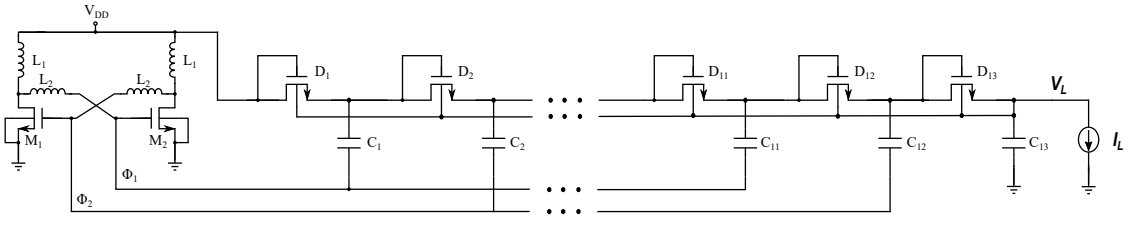


Figure 5.6: Schematics of the converter, ESRO followed by the DCP.

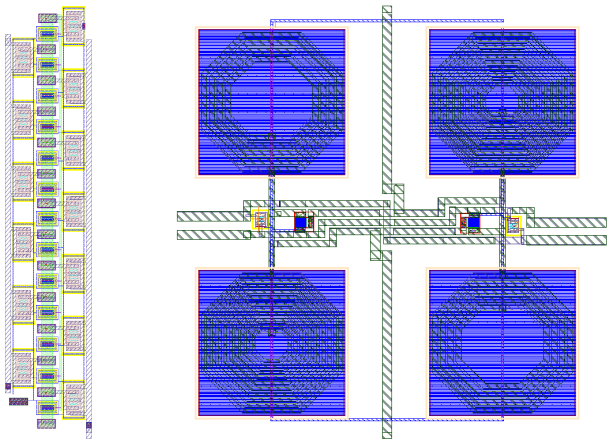


Figure 5.7: DCP (left) and ESRO (right) layouts, not drawn to scale.

5.2.2. Experimental Results

Figure 5.8 depicts the full chip micrograph, in which the main blocks and components of the converter are highlighted.

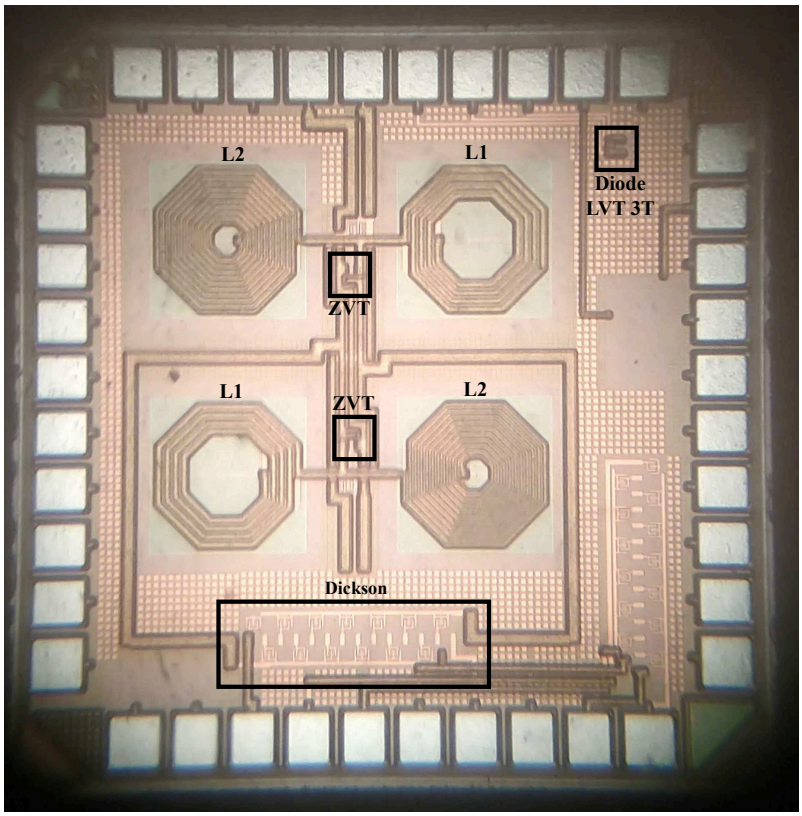


Figure 5.8: Chip micrograph of the DCP that uses the ESRO.

Once again, the Keithley 2401 Source Meter was used to emulate the TEG and measure the current sunk by the converter. The Agilent 34401A digital multimeter, with input resistance higher than 10 GΩ, measured the converter output voltage.

The DC source voltage (V_{TEG}) was increased gradually from 50 mV to 170 mV, with steps of 1 mV and $R_{TEG} = 5\ \Omega$. A 1 MΩ resistor emulated the load.

The average startup voltage of the measured samples is 78.75 mV for the unloaded converter. The input voltage required to achieve $V_L = 1$ V is 150.5 mV for $R_L = 1$ MΩ.

Different resistive loads were attached to the converter, as shown in Table 5.7. For $R_L = 5$ MΩ and 200 kΩ, the input voltages V_{TEG} required for achieving 1 V at the output were 118 mV and 227 mV, respectively. The converter efficiency is lower than 1 %, as shown in Table 5.8.

Table 5.7: DC source voltage (V_{TEG}) and measured current (I_{TEG}) for unloaded and loaded converter.

	Startup No Load		$V_L = 1$ V $R_L = 5$ MΩ		$R_L = 1$ MΩ		$R_L = 200$ kΩ	
	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)	V_{TEG} (mV)	I_{TEG} (mA)
Chip A	80	0.87	119	1.20	150	1.56	226	2.51
Chip B	77	0.78	115	1.16	148	1.55	224	2.50
Chip C	82	0.82	122	1.23	156	1.63	233	2.60
Chip D	76	0.77	115	1.15	148	1.54	224	2.49
Average	78.75	0.81	117.75	1.19	150.50	1.57	226.75	2.53

Table 5.8: Converter PCE and input power from the DC input source for three loads value.

	$P_{out} = 0.2\ \mu$W		$P_{out} = 1\ \mu$W		$P_{out} = 5\ \mu$W	
	P_{in} (μW)	PCE (%)	P_{in} (μW)	PCE (%)	P_{in} (μW)	PCE (%)
Chip A	142.80	0.14	234.00	0.43	567.26	0.88
Chip B	133.40	0.15	229.40	0.44	560.00	0.89
Chip C	150.06	0.13	254.28	0.39	605.80	0.83
Chip D	132.25	0.15	227.92	0.44	557.76	0.90
Average	139.63	0.14	236.40	0.42	572.71	0.87

The relatively high start-up voltage and low efficiency of the DC/DC converter are mainly due to the low quality factor of inductors and the losses in the diodes of the DCP. From post-layout simulation the oscillator frequency was equal to 350 MHz for the designed load.

The characterization of the diode-connected transistor employed in the DCP is shown in Appendix A.

5.3. Discussion

The characteristics of the converter architectures, either using an IRO or an ESRO, presented similar features. For the technologies employed, the low quality factor of the inductors seems to strongly limit the converters efficiency. A question

could be posed here: Are fully integrated LC oscillators competitive with transistor-only ring oscillators for the generation of AC signals? Standard ring oscillators operating from low supply voltages can start up from voltages of the order of 50 mV. However, standard ROs generally oscillate at much lower frequencies than LC oscillators. Therefore, capacitors of the DCP driven by ROs would be much higher than those driven by LC oscillators to achieve the same ripple voltage. Despite the limitations of the fully-integrated LC oscillators that have been employed in this work, the two converters designed herein can be very useful for starting up an efficient converter.

6. CONCLUSION

This thesis presented two fully-integrated start-up oscillators (IRO and ESRO) to drive a Dickson charge pump. Due to the low-quality factor of the integrated inductors along with the transistor voltage gain needed for oscillation, the minimum DC input for starting up the unloaded converters is around 84 mV for the IRO+DCP and 79 mV for the ESRO+DCP. The advantage of the ESRO over the IRO as regards the start-up voltage is not as significant as it could be in the case when using off-the-shelf inductors. The low Q-factor of the integrated inductors explains why the advantage of the ESRO over the IRO as regards the minimum start-up voltage is not significant. We have also presented an accurate model of the Dickson charge pump, which includes the input resistance of the DCP with explicit dependence on the diode parameters, load current, and number of stages. The expression derived for the input resistance is of great value because it must be considered in the oscillator design, since it directly affects the oscillator start-up voltage.

The computational analysis of the converter in chapter 4, which includes the input resistance of the DCP, is a very helpful tool for designing the oscillator, since it takes into account the influence of the DCP on the oscillator. As a result, the numerical solution thus obtained for the DCP parameters provides an initial input to the simulator which is very close to the *optimum* solution searched for.

6.1. Future Work

As regards the start-up oscillator, it would be very useful to evaluate with more detail the influence of transistor size on the minimum start-up voltage and oscillation frequency, as well as on the converter efficiency. For the technologies we have used in this work, it seems that LC oscillators do not offer any advantage over inverter-based ring oscillators as regards the start-up voltage. However, the values of the coupling capacitors of the DCP driven by LC oscillators can be usually much smaller than those driven by standard ROs due to the usually much higher oscillation frequency of the LC oscillators.

A main efficient boost converter can be designed making use of the start-up converter designed in this work, which can be turned off after the operation of the main converter has been initialized. A high-efficiency voltage regulator may be added to the main converter to output a constant voltage.

REFERENCES

1 DICKSON, J. F. On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. **IEEE Journal of Solid-State Circuits**, v. 11, n. 3, p. 374–378, June 1976. ISSN 0018-9200.

2 TANZAWA, T. Innovation of switched-capacitor voltage multiplier: Part 3: State of the art of switching circuits and applications of charge pumps. **IEEE Solid-State Circuits Magazine**, v. 8, n. 3, p. 63–73, Summer 2016. ISSN 1943-0582.

3 SADAGOPAN, K. R.; KANG, J.; RAMADASS, Y.; NATARAJAN, A. A cm-scale 2.4-GHz wireless energy harvester with nanoWatt boost converter and antenna-rectifier resonance for WiFi powering of sensor nodes. **IEEE Journal of Solid-State Circuits**, IEEE, v. 53, n. 12, p. 3396–3406, 2018. ISSN 00189200.

4 ZHANG, F.; ZHANG, Y.; SILVER, J.; SHAKHSHEER, Y.; NAGARAJU, M.; KLINEFELTER, A.; PANDEY, J.; BOLEY, J.; CARLSON, E.; SHRIVASTAVA, A.; OTIS, B.; CALHOUN, B. A batteryless 19μW MICS/ISM-band energy harvesting body area sensor node SoC. In: **2012 IEEE International Solid-State Circuits Conference**. [S.l.: s.n.], 2012. p. 298–300. ISSN 2376-8606.

5 ETHIER, S.; SAWAN, M. Exponential current pulse generation for efficient very high-impedance multisite stimulation. **IEEE Transactions on Biomedical Circuits and Systems**, v. 5, n. 1, p. 30–38, Feb 2011. ISSN 1932-4545.

6 ROZGIć, D.; MARKOVIć, D. A miniaturized 0.78-mW/cm^2 autonomous thermoelectric energy-harvesting platform for biomedical sensors. **IEEE Transactions on Biomedical Circuits and Systems**, v. 11, n. 4, p. 773–783, Aug 2017. ISSN 1932-4545.

7 QIAN, Y.; LU, D.; HE, J.; HONG, Z. An on-chip transformer-based self-startup hybrid SIDITO converter for thermoelectric energy harvesting. **IEEE Transactions on Circuits and Systems II: Express Briefs**, IEEE, v. 65, n. 11, p. 1673–1677, 2018. ISSN 15497747.

8 LUO, Z.; ZENG, L.; LAU, B.; LIAN, Y.; HENG, C. A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 65, n. 5, p. 1744–1757, May 2018. ISSN 1549-8328.

9 DEZYANI, M.; GHAFOORIFARD, H.; SHEIKHAEI, S.; SERDIJN, W. A. A 60 mV input voltage, process tolerant start-up system for thermoelectric energy harvesting. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 65, n. 10, p. 3568–3577, Oct 2018. ISSN 1549-8328.

10 LIM, B.; SEO, J.; LEE, S. A Colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency. **IEEE Journal of Solid-State Circuits**, v. 53, n. 11, p. 3293–3302, Nov 2018. ISSN 0018-9200.

11 VULLERS, R.; SCHAIJK, R. V.; DOMS, I.; HOOF, C. V.; MERTENS, R. Micropower energy harvesting. **Solid-State Electronics**, Elsevier Ltd, v. 53, n. 7, p. 684–693, 2009. ISSN 00381101.

12 RAPOPORT, B. I.; KEDZIERSKI, J. T.; SARPESHKAR, R. A glucose fuel cell for implantable brain–machine interfaces. **PLoS ONE**, v. 7, n. 6, 2012.

13 WENG, P.-S.; TANG, H.-Y.; KU, P.-C.; LU, L.-H. 50 mV-input bateryless boost conveter for thermal energy harvesting. **IEEE Journal of Solid-State Circuits**, v. 48, n. 4, Apr 2013.

14 RAMADASS, Y. K.; CHANDRAKASAN, A. P. A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage. **IEEE Journal of Solid-State Circuits**, v. 46, n. 1, p. 333–341, Jan 2011. ISSN 0018-9200.

15 CHEN, P.; ZHANG, X.; ISHIDA, K.; OKUMA, Y.; RYU, Y.; TAKAMIYA, M.; SAKURAI, T. An 80 mV startup dual-mode boost converter by charge-pumped pulse generator and threshold voltage tuned oscillator with hot carrier injection. **IEEE Journal of Solid-State Circuits**, v. 47, n. 11, p. 2554–2562, Nov 2012. ISSN 0018-9200.

16 MACHADO, M. B.; SCHNEIDER, M. C.; SAWAN, M.; GALUP-MONTORO, C. Fully-integrated 86 mV - 1 V step-up converter for energy harvesting applications. In: **2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)**. [S.l.: s.n.], 2014. p. 452–455.

17 FUKETA, H.; O'UCHI, S.; MATSUKAWA, T. Fully integrated, 100-mV minimum input voltage converter with gate-boosted charge pump kick-started by LC oscillator for energy harvesting. **IEEE Transactions on Circuits and Systems II: Express Briefs**, v. 64, n. 4, p. 392–396, April 2017. ISSN 1549-7747.

18 JAYAWEERA, H. M.; MUHTAROG̃ğLU, A. Design optimization of a fully integrated charge-pump with LC tank oscillator for ultra-low voltage energy harvesting. **Microelectronics Journal**, v. 59, n. August 2015, p. 33–39, 2017. ISSN 00262692.

19 PAN, F.; SAMADDAR, T. **Charge Pump Circuit Design**. [S.l.]: McGraw-Hill, 2010.

20 MACHADO, M. B.; SAWAN, M.; SCHNEIDER, M. C.; GALUP-MONTORO, C. 10 mV: 1V Step-up Converter for Energy Harvesting Applications. In: **Proceedings of the 27th Symposium on Integrated Circuits and Systems Design - SBCCI '14**. New York, New York, USA: ACM Press, 2014. p. 1–5. ISBN 9781450331562.

21 CARDOSO, A. J.; CARLI, L. G. de; GALUP-MONTORO, C.; SCHNEIDER, M. C. Analysis of the rectifier circuit valid down to its low-voltage limit. v. 59, n. 1, p. 106–112, Jan 2012. ISSN 1549-8328.

22 MACHADO, M. B.; NORNBERG, F.; SAWAN, M.; GALUP-MONTORO, C.; SCHNEIDER, M. C. Analysis and design of the Dickson charge pump for sub-50 mV energy harvesting. **Microelectronics Journal**, Elsevier Ltd, v. 90, n. April, p. 253–259, 2019. ISSN 00262692.

23 ABRAMOWITZ, M.; STEGUN, I. A. **Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables**. [S.l.]: Dover Publications, Inc, 1964. 358-434 p. ISBN 0-486-61272-4.

24 CARDOSO, A. J.; CARLI, L. G. de; GALUP-MONTORO, C.; SCHNEIDER, M. C. Analysis of the rectifier circuit valid down to its low-voltage limit. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 59, n. 1, p. 106–112, Jan 2012. ISSN 1549-8328.

25 MACHADO, M. B.; SCHNEIDER, M. C.; GALUP-MONTORO, C. On the minimum supply voltage for MOSFET oscillators. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 61, n. 2, p. 347–357, Feb 2014. ISSN 1549-8328.

26 SEDRA, A. S.; SMITH, K. C. **Microelectronic Circuits, 2Nd Ed.** Austin, TX, USA: Holt, Rinehart & Winston, 1987. ISBN 0030073286.

27 MACHADO, M. B. **Ultra-Low-Voltage Oscillators With Application to Energy Harvesting Circuits**. 169 p. Tese (Doutorado) — Universidade Federal de Santa Catarina, 2014.

28 MEINDL, J. C.; DAVIS, J. A. The fundamental limit on binary switching energy for terascale integration (tsi). **IEEE Journal of Solid-State Circuits**, v. 35, p. 1515–1516, 2000.

29 SCHNEIDER, M. C.; GALUP-MONTORO, C. **CMOS Analog Design Using All-Region MOSFET Modeling**. [S.l.]: Cambridge University Press, 2010.

30 CUNHA, A.; SCHNEIDER, M.; GALUP-MONTORO, C.; CAETANO, C.; MACHADO, M. Unambiguous extraction of threshold voltage based on the transconductance-to-current ratio. In: **WCM Nanotechnol**. [S.l.: s.n.], 2005. p. 139–141.

31 MACHADO, M. B.; SCHNEIDER, M. C.; GALUP-MONTORO, C. Fully integrated inductive ring oscillators operating at VDD below 2kT/q. In: **Analog Integrated Circuits and Signal Processing**. [S.l.]: Springer US, 2015. v. 82, n. 1, p. 5–15. ISSN 0925-1030.

A. COMPONENTS ANALYSES

A.1. Transistor Model

In this study the MOSFET model is based on the Advanced Compact Model (ACM), which describes the behavior of MOS transistor in all regions of operation. The ACM model gives the drain current (I_D) of the MOSFET transistor in terms of the forward (I_F) and reverse (I_R) components in all the operating regions as

$$I_D = I_F - I_R = I_S \left(i_f - i_r\right) \tag{A.1}$$

in which i_f and i_r are the normalized forward and reverse currents, respectively. I_S is the specific current, defined in (A.2), where, μ is the effective mobility, C'_{ox} is the oxide capacitance per unit area, n is the slope factor, ϕ_t is the thermal voltage and W/L is the aspect ratio of the transistor.

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{A.2}$$

The relation between voltages, referenced to bulk, and currents for all regimes of operation is given by

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)\right] \tag{A.3}$$

$$V_P = \frac{V_G - V_T}{n} \tag{A.4}$$

in which V_P is the pinch-off voltage and V_T is the threshold voltage.

For weak inversion operation, in which $i_{f(r)} < 1$, the drain current relates exponentially with the voltages, as shown below.

$$I_D = 2I_S e^1 e^{\frac{V_P - V_S}{\phi_t}} \left[1 - e^{\frac{-V_{DS}}{\phi_t}}\right] \tag{A.5}$$

The source, drain and gate transconductances are given by

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = 2I_S \left(\sqrt{1 + i_f} - 1\right) \tag{A.6}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = 2I_S \left(\sqrt{1 + i_r} - 1\right) \tag{A.7}$$

$$g_{mg} = g_m = \frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{n} \tag{A.8}$$

From (A.2) and (A.3) the drain-source voltage can be expressed as

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{A.9}$$

Also, V_{DS} can be written in terms of transconductances, substituting (A.6) and (A.7) into (A.9)

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S}\left(g_{ms} - g_{md}\right) + \ln\frac{g_{ms}}{g_{md}} \tag{A.10}$$

which, for weak inversion operation, becomes

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}} \tag{A.11}$$

A.2. Transistor Characterization

A.2.1. Extraction of V_T, I_S and n

The main parameters of MOS transistors (V_T, I_S, and n) were extracted employing the transconductance-to-current ratio procedure (g_m/I_D). Briefly, these parameters are extracted from the I_D vs V_G characteristic of the circuit in Fig. A.1. Details on the extraction are given in [29] and [30].

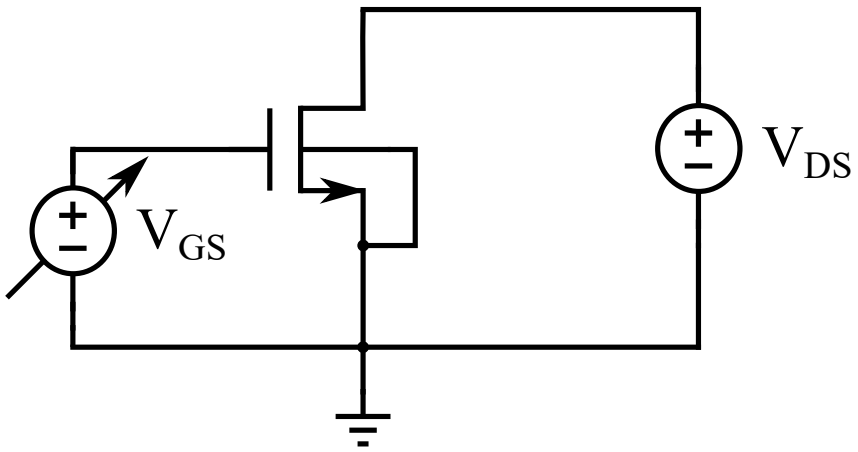


Figure A.1: Circuit configuration for transistor parameter extraction.

In the g_m/I_D vs V_G curve, with $V_{DS} = \phi_t/2$, the point where g_m/I_D drops around half (53.1%) of its peak value is measured. The gate voltage obtained at this point is V_{T0} and the corresponding current is 0.88 I_S. Fig. A.2 shows this method graphically.

The slope factor, n, is determined from the peak of g_m/I_D curve and the temperature, since $(g_m/I_D)_{max} = 1/n\phi_t$. In this study n is assumed to be independent of V_G.

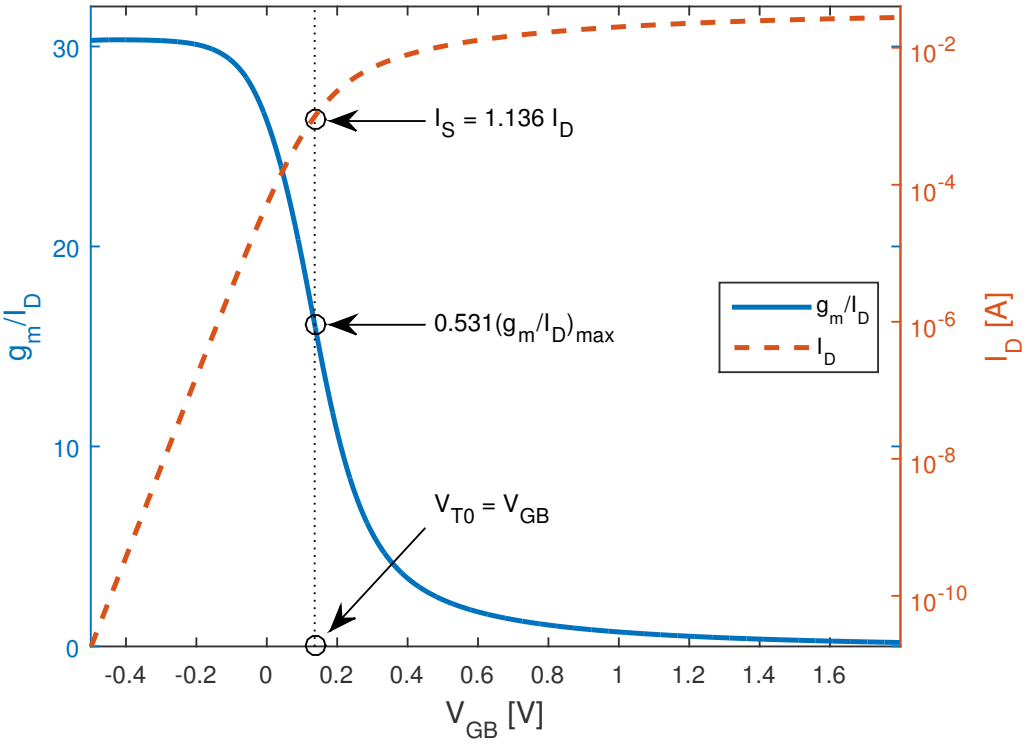


Figure A.2: Transconductance-to-current ratio and drain current vs. gate voltage of a native NMOS with $W/L = 2496\ \mu$m/500 nm, for $V_{DS} = \phi_t/2$.

A.2.2. Extraction of the Transconductances

The drain and source transconductances can be extracted using the I_D x V_D curve measured from the circuit in Fig. A.3.

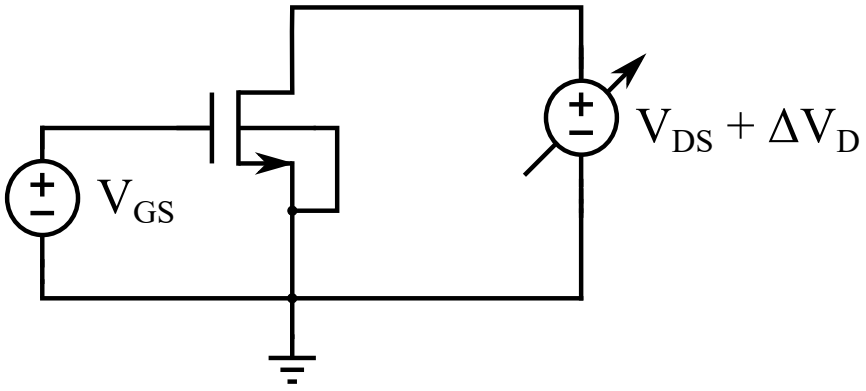


Figure A.3: Circuit configuration for transistor transconductances extraction.

For the extraction of g_{md}, the gate and drain voltages are equal to the DC source of the oscillator, $V_{GS} = V_{DS} = V_{DD}$, and ΔV_D is equal to 1 mV around V_{DD}.

On the other hand, g_{ms} was extracted for $V_{GS} = V_{DD}$ and $V_{DS} = 0$ V, because $g_{ms} = g_{md}|_{V_{DS}=0}$ due to transistor symmetry.

Following this procedure, the extracted drain and source transconductances of the native transistor used in the IRO oscillator are shown in Fig. A.4.

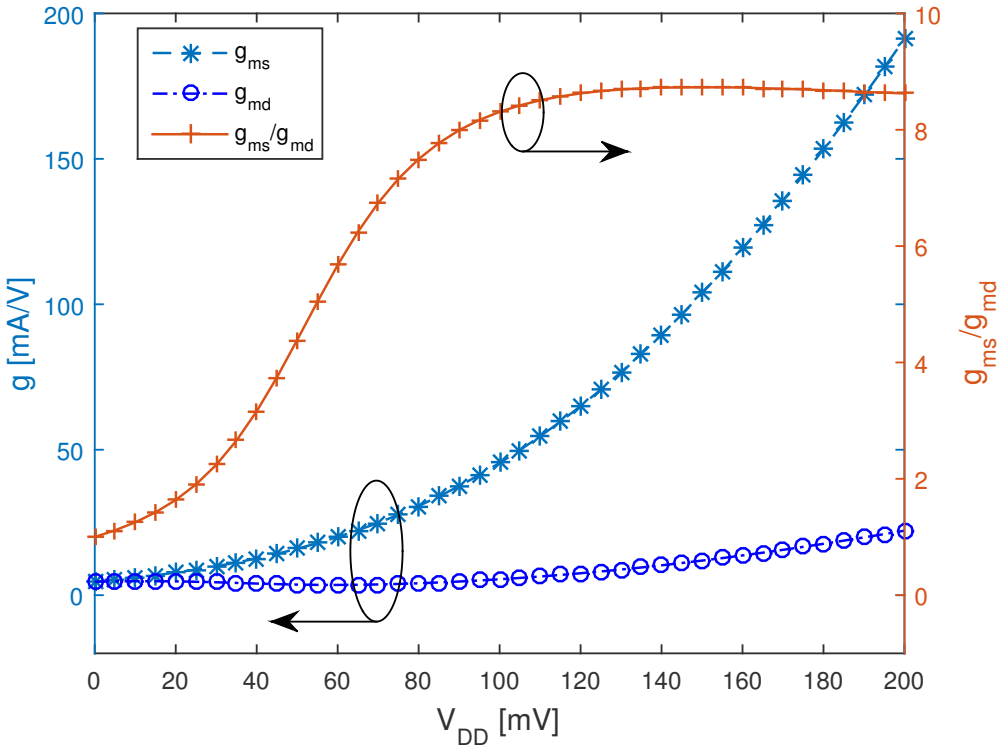


Figure A.4: Drain and source transconductances, and their ratio, for the native NMOS transistor of the 180 nm technology, with $W/L = 2496$ μm/500 nm, for V_{DD} = 0 to 200 mV.

A.2.3. Extraction of the Parasitic Capacitance

The gate capacitance C_P is one of the factors that determines the oscillation frequency. In this study, C_P, given by

$$C_P = C_{gs} + C_{gb} + C_{db} + C_{jd} + 4C_{gd} \tag{A.12}$$

was extracted via the operating point of the simulation.

This approach is specific for an oscillator with 2 stages. Further information for inductive ring oscillators with more than two stages is given in [31].

A.2.4. Diode-Connected Transistor

The equations for the DCP assume that the diode-connected transistor behaves according to Shockley's equation. Thus, the diode characterization consists in fitting

its current with Shockley's equation. Aiming at characterizing the diode in the -250 mV to 250 mV range and knowing that the DC voltage will change from the first to the last stage of the charge pump, the circuit configuration shown in Fig. A.5 was used to characterize the transistor, setting the V_{IN} according to the expected voltage in that stage and sweeping V_{DC} to cover the V_D range.

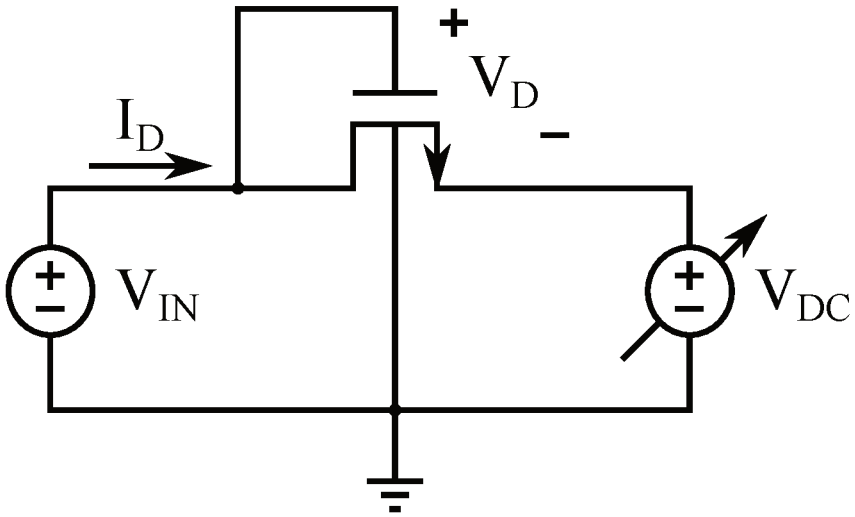


Figure A.5: Circuit configuration for the extraction of the diode parameters.

Fig. A.6 shows the fitting of the diode-connected native transistor, $W = 16\ \mu m$ and $L = 500\ nm$, which present $I_{sat} = 900$ nA and $n = 1.6$ according to Shockley's equation.

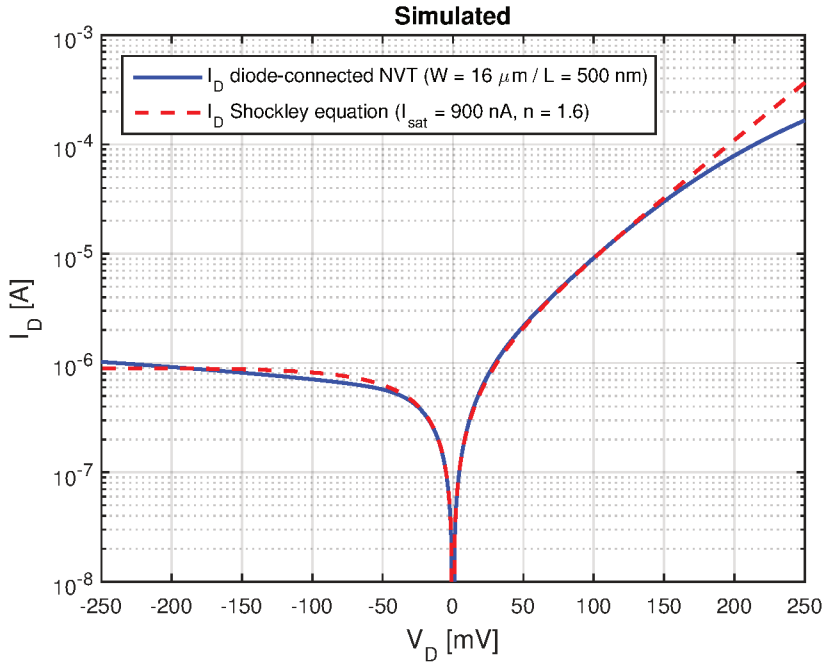


Figure A.6: I_D current fitting by Shockley equation with V_{IN}= 50 mV.

A.2.4.1. Diode Characterization - 180 nm CMOS

The diode-connected native transistor, available on the 180 nm CMOS technology, was characterized using the Agilent 4156C Precision Semiconductor Parameter Analyzer along with the 16442B Test Fixture Module. The measured I_D x V_D curve as well as the Shockley equation used to model the diode-connected transistor are shown in Fig. A.7 . A reverse current not as flat as expected is caused by the forward current of the diode-connected transistor of the ESD protection.

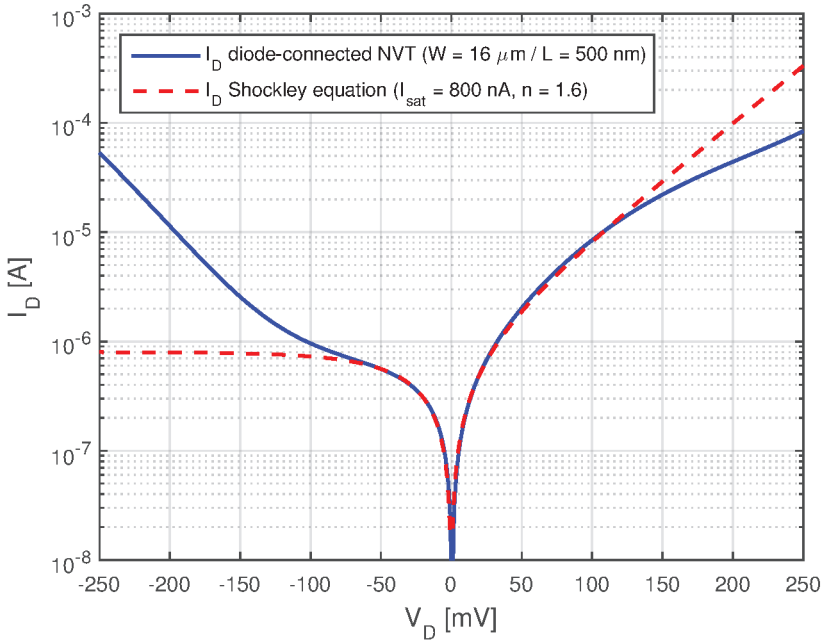


Figure A.7: Measured I_D current of diode-connected native transistor on chip C and fitting by Shockley equation.

Table A.1 shows the average values of I_{sat} and n, equal to 725 nA and 1.6, respectively, which are very close to the expected values of 900 nA and 1.6.

Table A.1: Diode-connected native transistor characterization.

	I_{sat} (nA)	n
Chip A	700	1.6
Chip B	700	1.6
Chip C	800	1.6
Chip D	700	1.6
Average	725	1.6

A.2.4.2. Diode Characterization - 130 nm CMOS

In order to characterize the diode-connected transistor LVT-3T of the 130 nm CMOS technology, the same setup of the previous section was used. Fig. A.8 shows the measured diode current and its fitting by the Shockley equation for Chip A.

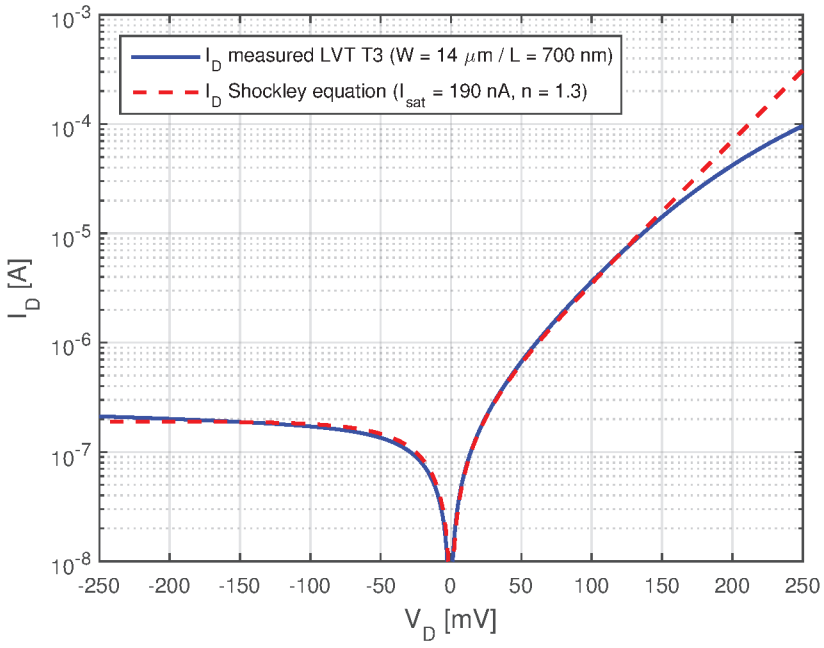


Figure A.8: Fitting of measured diode current by Shockley equation (dashed line).

Values of the saturation current and ideality factor that provide a good fitting to the Shockley's equation, for chips A, B, C and D, are shown in Table A.2.

Table A.2: Diode measured parameters.

	Isat	n
Chip A	190	1.3
Chip B	170	1.3
Chip C	190	1.3
Chip D	170	1.3
Average	180	1.3

A.3. Inductor Model

The inductor losses are represented by the parallel resistance, R_P, according to Fig. A.9

The parallel resistance is related to the quality factor Q as

$$R_P = Q\omega_0 L = Q(2\pi f_0)L \tag{A.13}$$

in which f_0 is the work frequency of the inductor.

For the 180 nm technology, inductors can be standard, symmetric or symmetric with center tap. An inductance range from hundreds of pH to some tens of nH are achieved through choice of number of turns, spacing between turns, inner radius, track width and distance between inductor and guard ring. Fig. A.10 shows the inductance and quality factor of a standard inductor with 5.5 turns, spacing between turns equal to 3 μm, track width of 24 μm, inner radius equal to 150 μm and distance

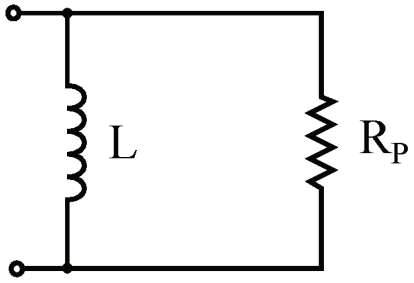


Figure A.9: Inductor equivalent circuit.

to guard ring of 50 μm. The resulting inductance of 19.17 nH has a maximum quality factor of 10.85 at 479 MHz .

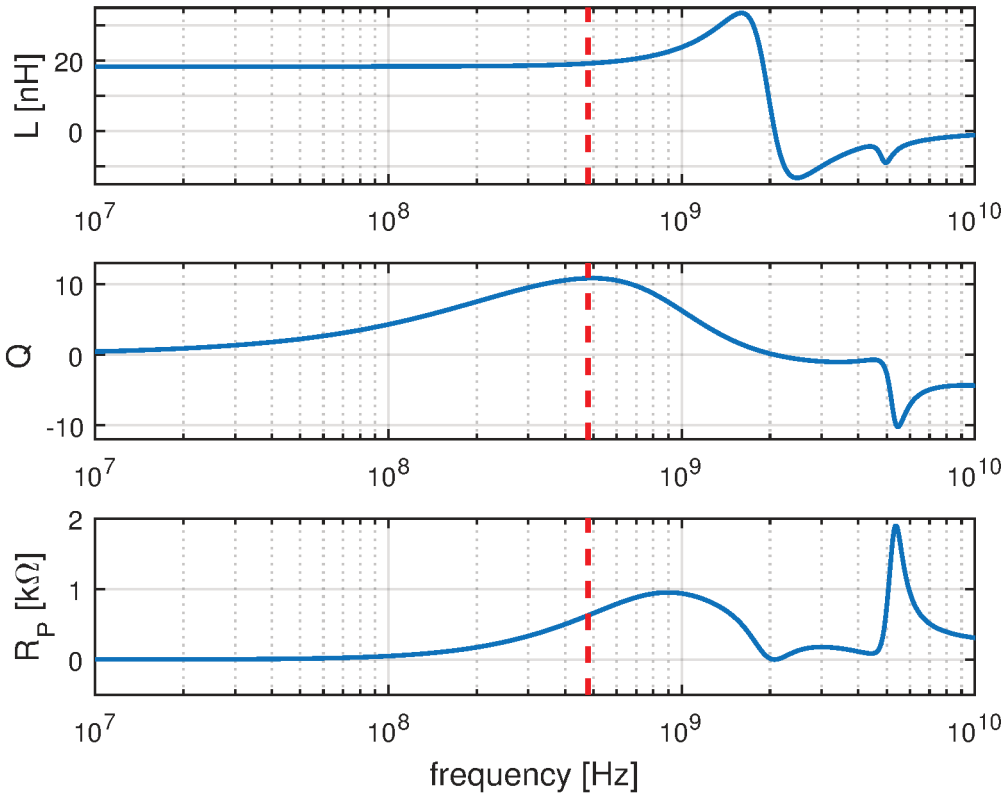


Figure A.10: Inductance and quality factor versus frequency.

Setting the maximum distance between inductor and guard ring will minimize the influence of external circuits in the inductor and keep the inductor quality factor close to the designed one.

Table A.3 presents electrical characteristics of some inductors, for track widths ranging from 3 μm to 30 μm and fixed parameters of number of turns $N = 5.5$, inner radius = 150 μm, spacing between turns = 3 μm and guard ring distance = 50 μm.

Table A.3: Set of inductors for track widths ranging from 3 μm to 30 μ, for fixed $N = 5.5$, inner radius = 150 μm, spacing between turns = 3 μm and guard ring distance = 50 μm.

W [μm]	Q_{max}	$L(Q_{max})$ [nH]	$f(Q_{max})$ [GHz]
3	8.30	23.62	1,333.52
4.5	9.97	22.56	1,122.02
6	10.98	21.83	988.55
7.5	11.56	21.22	891.25
9	11.84	20.71	822.24
10.5	11.90	20.20	758.58
12	11.82	19.72	691.83
13.5	11.71	19.65	653.13
15	11.59	19.55	616.60
16.5	11.47	19.47	588.84
18	11.36	19.41	568.85
19.5	11.27	19.33	549.54
21	11.10	19.18	537.03
22.5	10.98	19.20	512.86
24	10.85	19.25	495.45
25.5	10.72	19.29	478.63
27	10.58	19.33	462.38
28.5	10.44	19.36	446.68
30	10.29	19.43	436.52

A.4. Capacitor model

The 180 nm CMOS technology offers two options of linear capacitors, namely the Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM) capacitors. The MIM capacitor was our choice due to its higher capacitance density over the MOM capacitor. The MIM capacitor is composed of Metal 6 (top layer of metal) and Metal 5 separated by an insulator.

Table A.4 shows some capacitance values for square capacitors of sides equal to 5, 10, 20 and 30 μm and their stray capacitances for two ground positions. In position 1 the bottom plate is connected to ground and top plate to the AC voltage level, while for position 2 the opposite connection stands.

Table A.4: Capacitors and their respective stray capacitances considering ground connected to the bottom (position 1) and top (position 2) plate of the capacitors.

Capacitors MIMCAP (m x n)			
Dimensions $m = n$	Capacitance	Stray Capacitance position 1	Stray Capacitance position 2
30 μm	1.79 pF	9.85 fF	16.85 fF
20 μm	803.55 fF	8.11 fF	9.65 fF
10 μm	206.28 fF	6.94 fF	7.06 fF
5 μm	54.28 fF	6.51 fF	6.54 fF

B. MATLAB ROUTINE

In here the main functions implemented are shown.

The IRO function is used to simulate the time behavior of an IRO represented on Fig. 4.1. The Initial Conditions presents all the parameters needed to simulated IRO and DCP.

B.1. IRO function

Summarizing this function simulates the IRO considering that the inductor losses are represented by its parallel resistance, the transistor NMOS work in weak, moderate and string inversion and the DCP load are represented by R_{in}.

The function receives the parameters specified in right side and return the parameters of left side.

function $[VA, freqm, vdd, v]$ = iro transient ACM$(L, Q, Is, n, Vth, Cp, freq,$
$Rteg, Vteg, vss, Rin, dt, t, Tc)$

% Calculus of ACM vn and il relation
$il = 10.^(-7 : 0.01 : 5)$;
vn = ACM array(il);
$Rp = Q * 2 * pi * freq * L$; % Eq. A.13
$v(1,1) = Vteg$; % positive supply voltage
$v(5,1) = vss$; % negative supply voltage

% considering Rp in parallel with Rin
$Req = Rp * Rin/(Rp + Rin)$;

% calculates dc solution for initialization of the oscillator
$f0 = @(vx)(Vteg-vx)/Rteg-2*$nmos ACM$(vx,vx,v(5,1),v(5,1), Is, n, Vth, vn, il, Tc)$;
$vx = fzero(f0,Vteg)$;
$v(2,1) = vx$;

% inserts initial oscillator state
$delta = 30e-3$; % This is the difference voltage between the stages
$v(3,1) = vx + delta$;
$v(4,1) = vx - delta$;
$c(1,1) = (v(1,1) - v(2,1))/Rteg$; % source current
$c(2,1)$ = nmos ACM$(v(2,1),v(4,1),v(5,1),v(5,1), Is, n, Vth, vn, il, Tc)$; % inductor 1 current
$c(3,1)$ = nmos ACM$(v(2,1),v(4,1),v(5,1),v(5,1), Is, n, Vth, vn, il, Tc)$; % transistor 1 current
$c(4,1)$ = nmos ACM$(v(2,1),v(3,1),v(5,1),v(5,1), Is, n, Vth, vn, il, Tc)$; % inductor 2 current

$c(5,1) = \text{nmos ACM}(v(2,1),v(3,1),v(5,1),v(5,1), Is, n, Vth, vn, il, Tc)$; % transistor 2 current
$c(6,1) = (v(2,1) - v(3,1))/Req$; % Rp 1 current
$c(7,1) = (v(2,1) - v(4,1))/Req$; % Rp 2 current

% time simulation loop
for $i = 2{:}\text{length}(t)$
$c(2,i) = c(2,i-1) + (dt/L) * (v(2,i-1) - v(3,i-1))$;
$c(6,i) = (v(2,i-1) - v(3,i-1))/Req$;
$c(4,i) = c(4,i-1) + (dt/L) * (v(2,i-1) - v(4,i-1))$;
$c(7,i) = (v(2,i-1) - v(4,i-1))/Req$;
$c(1,i) = c(2,i) + c(6,i) + c(4,i) + c(7,i)$;
$v(1,i) = Vteg$;
$v(2,i) = v(1,i) - c(1,i) * Rteg$;
$v(3,i) = v(3,i-1) + (c(2,i-1) + c(6,i-1) - c(3,i-1)) * dt/Cp$;
$v(4,i) = v(4,i-1) + (c(4,i-1) + c(7,i-1) - c(5,i-1)) * dt/Cp$;
$c(3,i) = \text{nmos ACM}(v(3,i),v(4,i),v(5,i),v(5,i), Is, n, Vth, vn, il, Tc)$;
$c(5,i) = \text{nmos ACM}(v(4,i),v(3,i),v(5,i),v(5,i), Is, n, Vth, vn, il, Tc)$;
$v(5,i) = vss$;
end
% Oscillator frequency from voltage wave
$x = v(3,:) - v(4,:)$;
$y(find(x < 0)) = -1$;
$y(find(x >= 0)) = 1$;
$z = find(diff(y) == -2)$;
$p = diff(t(z))$;
$tp = t(z(2:end))$;
$f = 1./p$;
$freqm = \text{mean}(f(\text{floor(end/2):end}))$;
% Voltage amplitude of oscillation
$vmax = \max(v(3,\text{floor(end/2):end}))$;
$vmin = \min(v(3,\text{floor(end/2):end}))$;
$VA = (vmax - vmin)/2$;
% Voltage amplitude of oscillation
$vddmax = \max(v(2,\text{floor(end/2):end}))$;
$vddmin = \min(v(2,\text{floor(end/2):end}))$;
$delta = (vddmax - vddmin)$;
$vdd = vddmax - delta/2$;
end

B.2. nmos ACM function

This function calculates the drain current of NMOS transistor, considering the equations (4.4) and (4.6).

function $id = \text{nmos ACM}(vd, vg, vs, vb, Is, n, Vth, vn, il, Tc)$
$q = 1.6021e - 19$;

$k = 1.38e-23$;
$Tk = Tc + 273.15$;
$phit = k * Tk/q$; % thermal voltage
$vp = (vg - vb - Vth)/n$; % pinch-off voltage (4.6)
if = interp1(vn,il,(($vp - vs + vb$)/($phit$)),'pchip');
ir = interp1(vn,il,(($vp - vd + vb$)/($phit$)),'pchip');
$id = Is * (if - ir)$;
end

B.3. Initial Conditions

Here is all the initial conditions and parameters of the componentes of IRO and DCP.

% Temperature and time parameters
$Tc = 27$; % Celsius temperature
$dt = 1e-11$;
$t = 0 : dt : 50e-9$;
% TEG parameters
$Rteg = 5$; % source resistance
$Vteg = 0.052$;
$Vss = 0$; % ground
% IRO Oscillator parameters
% Transistor
$Is = 1.15e-3$; % Specific current
$n = 1.27$; % slope factor
$Vth = 136.5e-3$; % threshold voltage
$Cp = 14.5e-12$; % node capacitance of transistor
% Inductor
$L = 18.58e-9$; % inductance
$Q = 9.5$; % inductor quality factor at freq
$freq = 1/(2 * pi * sqrt(L * Cp))$;
% Dickson Charge Pump
$Nvector = 3 : 2 : 71$; % number of Dickson stages
$Rin = 1e20$; % DCP* input resistance (almost infinity)
% Diode parameters
$nd = 1.55$; % diode ideality factor
$Isatvector = 1e-9 * [200 : 50 : 1100]$; % A - reverse saturation current
$af = 0.95$; % VA attenuation factor given by (2.31)
% Load
$ILoad = 200e-9$;
$VLoad = 0.5$;
$ripple = 2$; % V_L ripple

C. PAPER ACCEPTED TO ELSEVIER MICROELECTRONICS JOURNAL

Microelectronics Journal 90 (2019) 253–259

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Analysis and design of the Dickson charge pump for sub-50 mV energy harvesting

Marcio Bender Machado [a], Franciele Nornberg [b,*], Mohamad Sawan [c,d], Carlos Galup-Montoro [b], Marcio Cherem Schneider [b]

[a] Federal Institute of São Paulo, Brazil
[b] Federal University of Santa Catarina, Brazil
[c] École Polytechnique de Montréal, Canada
[d] School of Engineering, Westlake University, Hangzhou, China

ARTICLE INFO

Keywords:
Dickson charge pump
Ultra-low voltage
Ultra-low power
Energy harvesting
Zero-VT MOSFET

ABSTRACT

This paper presents the analysis and design of a DC/DC boost converter operating from supply voltages around the thermal voltage (26 mV at room temperature), for energy harvesting applications. The boost converter described herein is aimed at starting up DC/DC converters, but its use can be extended to a conventional DC/DC converter in which the power conversion efficiency is not of major concern. Firstly, the operation of the Dickson charge pump for ultra-low voltage is described. Expressions for the output voltage, power conversion efficiency and input resistance are derived. The extremely low voltage operation, made feasible through an enhanced-swing ring oscillator and zero-VT transistors, is demonstrated via a prototype fabricated in 130 nm CMOS technology. For an input voltage of 17 mV, the converter delivers an output current of 10 nA at 1 V output and provides a current of 1 μA at a DC output of 1 V from an input voltage of 23 mV.

1. Introduction

Charge pump converters introduced by Dickson [1] have been employed in a wide variety of applications, including bias generators for dynamic random access memory and flash memory, drivers for light emitting diodes and liquid crystal displays, and AC-DC converters that harvest energy from an RF signal [2]. In the energy scavenging field, the demand for energy autonomy has driven the search for boost converters able to operate from extremely low voltages. *In vivo* monitoring of the activity of human organs (*e.g.* through electrocardiograms, electroencephalograms, or intraocular pressure examinations) and the stimulation of human tissue, which generally consume some dozens of micro-watts [3,4], could lead to a new class of ultra-low-power (ULP) and ultra-low-voltage (ULV) energy harvesters.

Solar cells in dark environments [5], wearable thermoelectric generators [6–8] and implantable glucose fuel cells [9], which typically generate less than 100 mV, are appealing choices to power the electronics of sensor networks and biomedical appliances. However, given the ULV levels generated by these energy harvesters, a boost converter is required to power conventional electronics which, in general, needs supply voltages of around 1 V. In the past decade, in an attempt to reduce the minimum voltage required to start up converters, many researchers have presented solutions employing schematics based on charge pumps or inductive boost converters. A challenge in the design of converters powered from voltages below 50 mV is the start-up stage, due to the low efficiency of devices operating at ULV and the need to generate oscillatory signals from such a low voltage.

In Ref. [3], a body sensor node is powered from a supply voltage of 30 mV of a thermoelectric harvester, but wireless RF power is provided for the kick start. In Ref. [10], a boost converter that uses off-chip inductors starts up at a minimum voltage of 50 mV. In Ref. [11], a 35 mV boost converter is presented; however, it requires a mechanical switch for the kick start of the converter. A start-up converter of 80 mV is presented in Ref. [12], but it requires a threshold-voltage-tuned oscillator in order to decrease the minimum start-up voltage. In recent publications [13–15], fully integrated solutions with no tuning processes are proposed, but they operate from around 100 mV.

In order to deal with the conflicting requirements of very low voltage for the converter start-up and the high power conversion efficiency, the use of a hybrid configuration composed of two converters, similar to

* Corresponding author.
E-mail address: francielefnornberg@gmail.com (F. Nornberg).

https://doi.org/10.1016/j.mejo.2019.06.009
Received 12 April 2019; Received in revised form 7 June 2019; Accepted 17 June 2019
Available online 20 June 2019

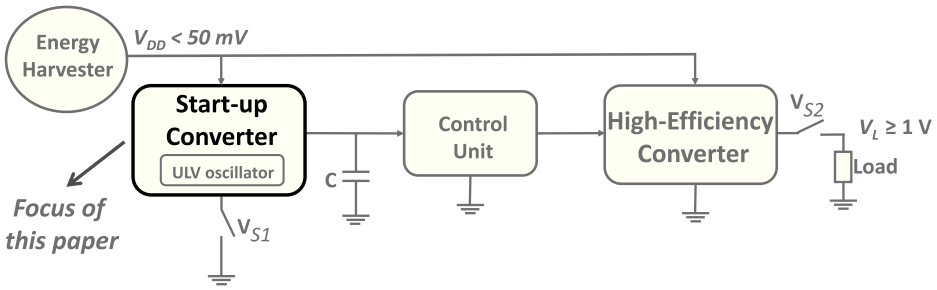


Fig. 1. Hybrid configuration composed of two voltage converters.

that shown in Fig. 1, has been widely employed [6,7,14,16–19]. Reference [6] reports a thermoelectric energy harvester which starts up from 65 mV. In Ref. [7], an on-chip transformer-based LC oscillator starts up at an open-circuit-voltage of 160 mV. [14] presents a converter which starts up from 100 mV. [16] reports a DC-DC converter that operates from a 7 mV supply voltage, but requires a minimum self-start voltage of 210 mV. In Ref. [17], a start-up converter based on a ring oscillator and a charge pump starts up at 60 mV. In the converter of [18], an inductor of the start-up Colpitts oscillator is reused in the main boost converter to minimize the number of off-chip components, but it starts up from a minimum of 40 mV.

In general, the start-up converter, responsible for the initial operation of the harvester, is composed of an oscillator and a charge pump. The main requirement for this block is to start up from a very low voltage, *i. e.* 50 mV or even less. Power conversion efficiency is not the primary concern for the start-up block, since it can be turned off after the voltage on capacitor C has reached the minimum voltage required to operate the high-efficiency converter. To kick start the circuit at extremely low voltages, a charge pump has been commonly used.

Aiming at the generation of a DC voltage to kick-start boost converters or directly supply micro-watt loads from extremely low voltages, this paper presents an analysis of the Dickson charge pump (DCP), which includes the forward voltage drop across the diodes in terms of the diode parameters, the number of stages, and the load current. Expressions for the output voltage, power efficiency and input resistance, valid for ULV operation, are derived. Using an enhanced swing ring oscillator, together with a DCP, we designed and tested a prototype built with zero-VT transistors and high quality factor inductors, aimed at converting DC input voltages of the order of 20 mV to 1 V.

The paper is organized as follows. Section 2 presents the ULV model of the DCP. The design of the ULV converter prototype is shown in Section 3. Section 4 reports the experimental results for the converter prototype. Section 5 details the conclusion based on the findings reported in this paper.

2. Analysis of the ULV Dickson charge pump

The analysis of the DCP in Ref. [1] includes three terms that contribute to the reduction of the output voltage as compared to the ideal case. These terms are the attenuation of the clock voltage due to the stray capacitances, the voltage ripple on the capacitors, and the forward voltage drop across the diodes. The first two factors are analyzed in Ref. [1], but the voltage drop in the diodes, which is the main degradation factor of the performance of the DCP at ultra-low voltages, was not deduced. This paper reviews the analysis of the forward voltage drop across the diodes as a function of the load current and the diode parameters. We have also expanded the model of [13] to include the efficiency as well as the input resistance of the DCP. The analysis herein assumes that all diodes are identical, the ripple voltage is negligible, and the stray capacitances are much smaller than the coupling capacitances. In this work, similarly to the rectifier analysis described in Ref. [20], the diode parameters I_S, the saturation current, the ideality factor (n) and the load current (I_L) are included to model the DCP down to ultra-low voltages.

For the N-stage Dickson converter in Fig. 2, one can calculate the steady state DC output voltage with the following simplifying assump-

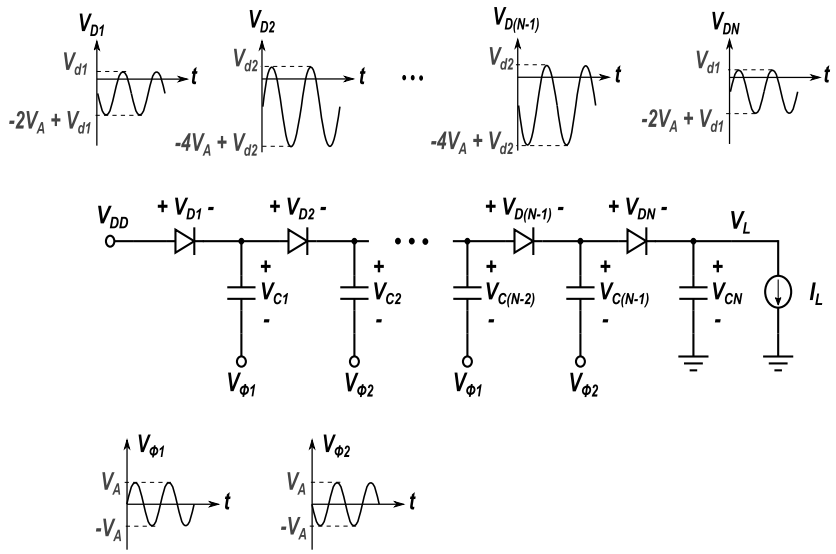


Fig. 2. Schematic showing N-stage Dickson charge pump and voltage drop across the diodes.

tions: (i) $V_{\phi 1} = -V_{\phi 2} = V_A \cos\theta$; (ii) the capacitors are high enough to preclude any significant variation in the voltages across them; and (iii) the diodes are modeled by the Shockley equation, written below.

$$I_D = I_S \left[\exp\left(\frac{V_D}{n\phi_t} \right) - 1 \right] \tag{1}$$

where ϕ_t is the thermal voltage (kT/q) and V_D is the voltage waveform across the diodes.

2.1. Output voltage

For the sake of completeness, we summarize in this subsection and in Appendix A the derivation of the output voltage presented in Ref. [13]. The schematic of the Dickson charge pump, along with the voltage waveforms across the diodes is shown in Fig. 2. The voltage drop across diodes D_1 and D_N differs from that across the other diodes, since one of the terminals of both D_1 and D_N is connected to DC nodes (V_{DD} and V_L, respectively). Noting that $V_{d1} = V_{dN}$, while $V_{d2} = \ldots = V_{d(N-1)}$, the DC output voltage (V_L) is given by

$$V_L = V_{DD} + (N-1)2V_A - 2V_{d1} - (N-2)V_{d2} \tag{2}$$

Using the diode forward voltage drop derived in Appendix A, the converter output voltage becomes

$$V_L = V_{DD} + 2n\phi_t \ln\left[\frac{I_0(v_a)}{1 + I_L/I_S} \right] + (N-2)\, n\phi_t \ln\left[\frac{I_0(2v_a)}{1 + I_L/I_S} \right] \tag{3}$$

Here, $v_a = V_A/n\phi_t$ is the normalized magnitude of the oscillator output voltage, and $I_0(z)$ is the modified Bessel function of the first kind of order zero. V_A, the magnitude of the oscillator output voltage, is a function of the DC input voltage and the DCP equivalent input impedance (R_{in}). Simulation of the converter in our design indicated that, for $V_{DD} = 24$ mV and an 11-stage DCP, the value of the oscillator amplitude V_A is less than 100 mV and the output voltage is 1 V for a load of 1 μA.

Expression (3), which is graphically shown in Fig. 3 for the particular case of $V_A = 80$ mV, is an important tool for the design of charge pumps operating from low voltages. For a given value of v_a one can find a combination of the number of stages and the saturation current that satisfies the design specifications (V_L and I_L).

For $v_a > 3$, $I_0(v_a)$ can be approximated by $exp(v_a)/\sqrt{2\pi v_a}$ with an error below 5% [21] and Eq. (3) reduces to

$$V_L = V_{DD} + 2(N-1)V_A - Nn\phi_t \ln\left[\sqrt{\frac{2\pi 2V_A}{n\phi_t}} \left(1 + \frac{I_L}{I_S} \right) \right] + n\phi_t \ln 2 \tag{4}$$

For the example of Fig. 3, Eq. (4) presents an error of 2% when compared to Eq. (3), which is affordable considering its simplicity.

2.2. Power conversion efficiency

The power conversion efficiency (*PCE*) of the DCP is $PCE = P_{out}/P_{in}$, where P_{in} is the output power plus the power dissipated in the diodes.

Using the power loss in the diodes derived in Appendix A yields

$$PCE = \frac{V_{DD} + 2n\phi_t \ln\left[\frac{I_0(v_a)}{1+I_L/I_S} \right] + (N-2)\, n\phi_t \ln\left[\frac{I_0(2v_a)}{1+I_L/I_S} \right]}{V_{DD} + \left(1 + \frac{I_S}{I_L} \right) 2V_A \left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\, \frac{I_1(2v_a)}{I_0(2v_a)} \right]} \tag{5}$$

in which $I_1(z)$ is the modified Bessel function of the first kind of order one.

Fig. 4 shows the variation of both the output voltage and the *PCE* of an eleven-stage DCP in terms of I_L/I_S. For a given magnitude applied to the DCP, the *PCE* reaches, for the case $V_{DD} = 0$, a maximum given [20] by

$$\frac{V_L}{Nn\phi_t} = \frac{I_L}{I_S} \tag{6}$$

Note that, in general, the DC input voltage (V_{DD}) does not have an important contribution to the load voltage, since, usually, $V_{DD} << V_L$.

Equation (3), for the output voltage, and equation (6), for maximizing the PCE are useful for calculating the values of N and I_S for a given V_A at the DCP input.

2.3. Input resistance

Let us now calculate the charge pump input resistance, R_{in}, which loads the oscillator output signals ϕ_1 and ϕ_2. For a sine wave oscillator, the value of $R_{in} = (V_A^2/2)/(P_{in}/2)$ is expressed as

$$R_{in} = \frac{V_A}{2(I_S + I_L)\left[\frac{I_1(v_a)}{I_0(v_a)} + (N-2)\frac{I_1(2v_a)}{I_0(2v_a)} \right]} \tag{7}$$

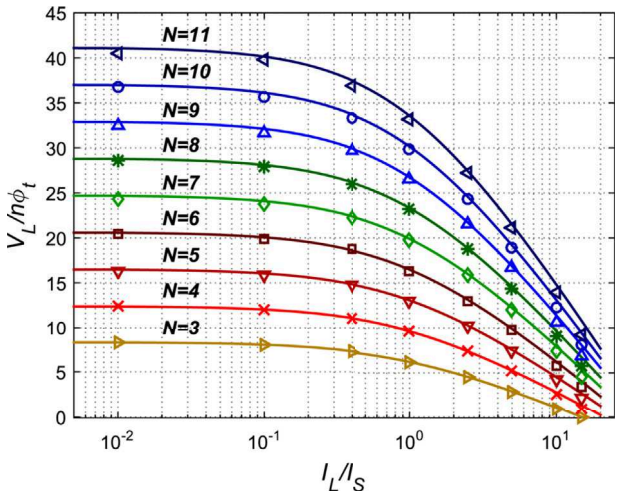


Fig. 3. Calculated (solid line) and simulated (symbols) output voltage normalized to thermal voltage ($V_L/n\phi_t$) *vs.* load current normalized to the saturation current (I_L/I_S), for N ranging from 3 to 11, $V_{DD} = 30$ mV, $V_A = 80$ mV, and $n\phi_t = 27.1$ mV.

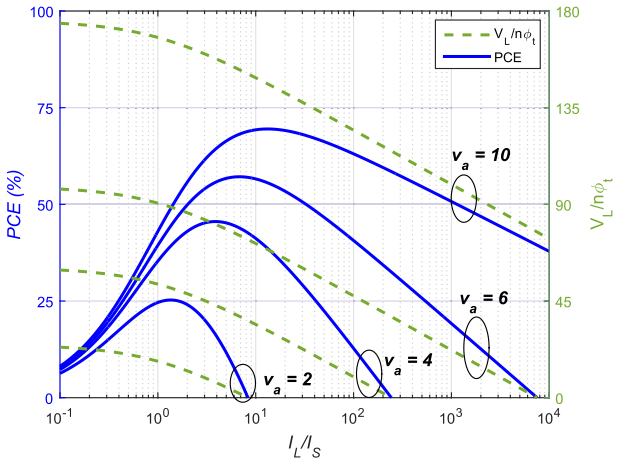


Fig. 4. *PCE* and normalized output voltage of the eleven-stage Dickson converter (for $V_{DD} = 0$) *vs.* normalized load current for normalized peak voltages $v_a = 2$, 4, 6, and 10.

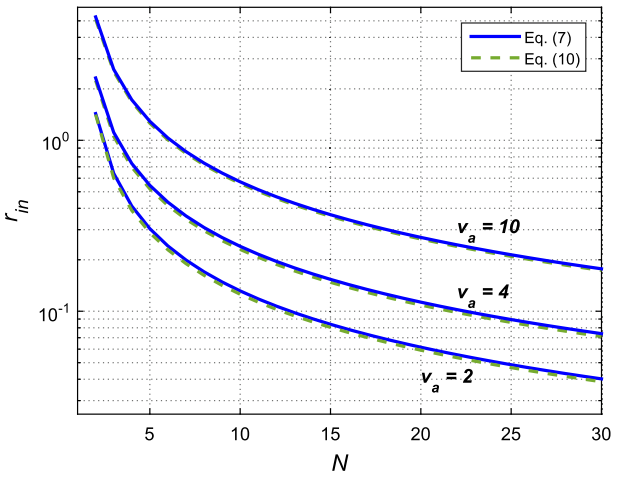


Fig. 5. Normalized input resistance of the Dickson converter using Eq. (7) (continuous line) and approximate Eq. (10) (dashed line).

in which P_{in} is the total input power delivered by ϕ_1 and ϕ_2 to the charge pump.

When $v_a << 1$, the modified Bessel functions of the first kind reduce to $I_0(v_a) \approx 1$ and $I_1(v_a) \approx v_a/2$ [21]; thus,

$$R_{in,L} = \frac{n\phi_t}{(2N-3)(I_S+I_L)} \tag{8}$$

On the other hand, when $v_a >> 1$, the modified Bessel functions of the first kind are $I_0(v_a) \approx I_1(v_a)$ [21] and the input resistance, becomes

$$R_{in,H} = \frac{v_a n\phi_t}{(2N-2)(I_S+I_L)} \tag{9}$$

Using the results of the prior two equations, the normalized input resistance $r_{in} = R_{in}(I_S+I_L)/n\phi_t$ can be approximated as

$$r_{in} \approx \sqrt{\left(\frac{1}{2N-3}\right)^2 + \left(\frac{v_a}{2N-2}\right)^2} \tag{10}$$

Fig. 5 shows the normalized input resistance of the Dickson charge pump versus the number of stages, for $v_a = 2$, 4, and 10. Equation (10) (dashed line) has the benefit of simplicity, at the expense of a maximum error of 6.2%, as compared to Eq. (7) (continuous line), which uses Bessel functions.

3. Design of the ULV converter

The goal of developing the prototype was to demonstrate the feasibility of the converters operating from very low voltages. The target of the designed converter was to give a DC output of 1 V from a DC input voltage of a few tens of mV. The schematic diagram of the converter is shown in Fig. 6.

In order to reduce the prototype area and the losses resulted from the connections between the chip and the external inductors, the chip was wire-bonded to the board substrate using gold wires with a length of 1.5 mm. Fig. 7 shows a photograph of the board employed to test the chip.

Some design details of both the oscillator that generates the complementary signals and the DCP are presented in the following subsections.

3.1. The ULV enhanced-swing ring oscillator

The design of the enhanced-swing ring oscillator (ESRO) follows the guidelines presented in Refs. [13,22]. In order to design a step-up converter able to start-up with V_{DD} of the order of 20 mV, the oscillator was built with high quality off-the-shelf inductors and native transistors. The inductance values are $L_1 = 220$ nH, $L_2 = 595$ nH, both with

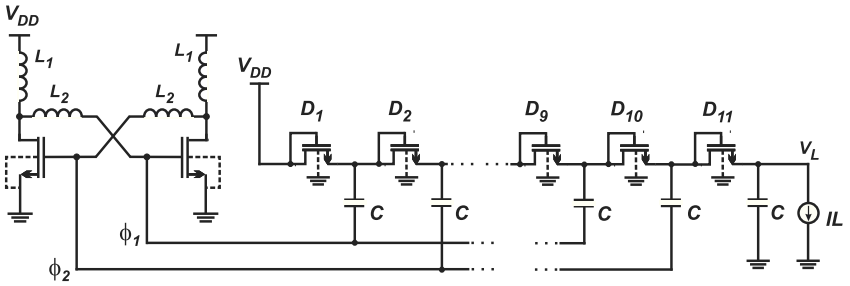


Fig. 6. Schematic diagram of the boost converter showing both the ESRO and the DCP.

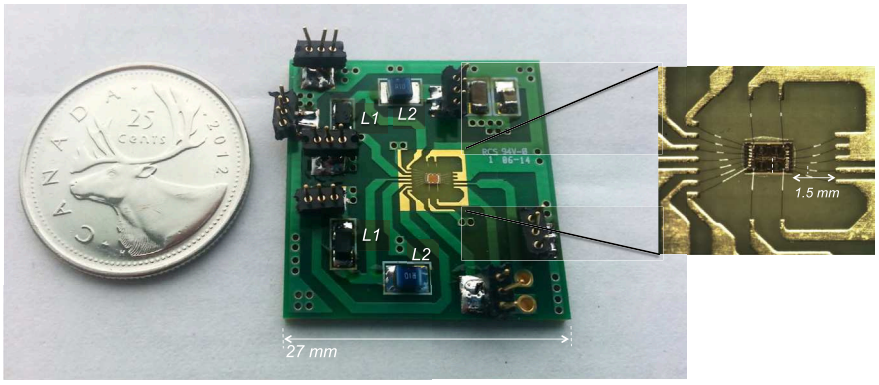


Fig. 7. Photograph of the wire-bonded prototype implemented to test the step-up converter.

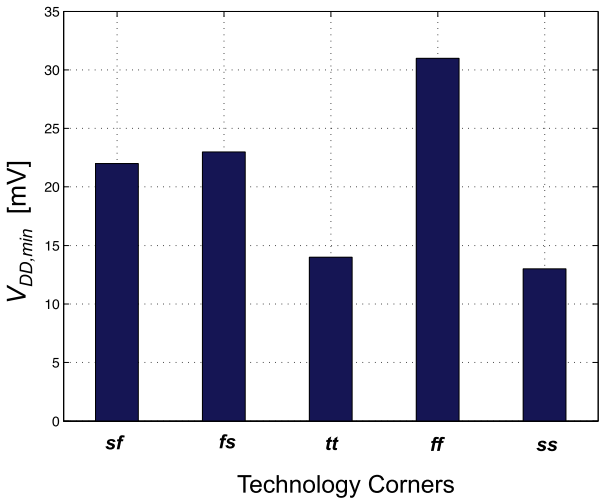


Fig. 8. Post-layout simulation of the minimum supply voltage required to start up the converter with $I_L = 0$, for the technology corners.

Q values of around 60 at 50 MHz, which is the approximate value of the oscillation frequency. The dimensions of inductors L_1 and L_2 are 3.2 mm × 1.6 mm x 1.8 mm and 2.5 mm × 2 mm x 1.6 mm, respectively. The zero-VT transistors are composed of a parallel association of 400 MOSFETs, each of them with an aspect ratio of 5 µm/0.42 µm.

The minimum supply voltage to start up the converter ($I_L = 0$), simulated for the corners of the technology, is shown in Fig. 8. On comparing the simulations run using the typical parameters (tt) with the experiments, the results match very closely.

3.2. ULV Dickson charge pump

The DCP parameters were determined from equations (3) and (6) for the maximum *PCE*. Considering the ESRO designed, the load specifications ($V_L = 1$ V and $I_L = 1$ µA) and expression (6), we found that the number of stages N and the normalized load current I_L/I_S that lead to the lowest supply voltage for starting up the oscillator are around 11 and 2.5, respectively. After some tuning through simulation, the requirements for the output voltage and load current were achieved using diode-connected zero-VT transistors in the charge pump, with $W/L = 4.2$ µm/0.42 µm, which corresponds roughly to $I_S = 550$ nA.

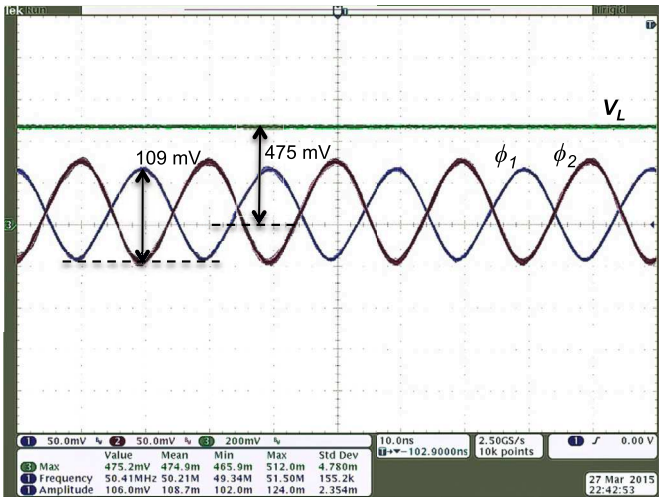


Fig. 9. Waveforms of the step-up converter for $V_{DD} = 21.8$ mV and $I_L = 48$ nA. Measurements at the oscillator outputs were taken with 10 MΩ probes.

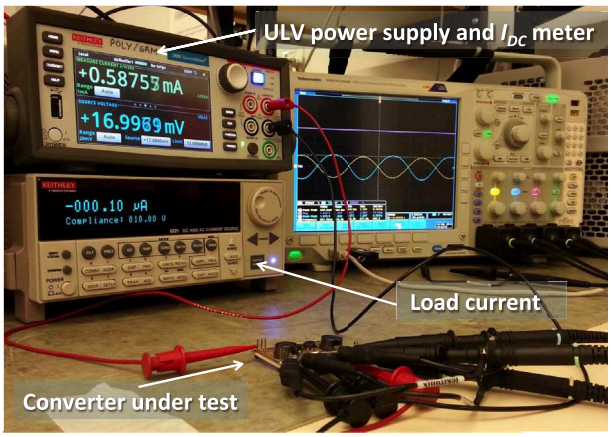


Fig. 10. Setup employed to measure the characteristics of the step-up converter.

Coupling capacitors of 2 pF were employed based on the analysis of the ripple voltage, similarly to that described in Refs. [1,20].

4. Experimental results and discussion

The prototype was simulated and experimentally characterized. The complementary oscillator outputs (peak-to-peak voltage of around 110 mV and frequency of 50 MHz) as well as the converter output ($V_L = 475$ mV) for $V_{DD} = 21.8$ mV are shown in Fig. 9.

The measurements were taken with the output loaded by the oscilloscope probe, for which R = 10 MΩ and C = 3.3 pF. In order to supply the very small voltage at the converter input, we used the high resolution Keithley 2450 source meter, which gives accurate voltage and measures the DC current. The output voltage was measured using a high impedance voltmeter (Agilent 34411A). To emulate the load current, a Keithley 6221 current source was employed. Fig. 10 shows the setup employed to measure the characteristics of the step-up converter.

The transient of the converter is illustrated in Fig. 11, for $V_{DD} = 24$ mV and $I_L = 100$ nA. The upper trace is the output voltage of the DCP while the bottom traces are the oscillator outputs.

The output voltage of the DC-DC converter in terms of the input voltage for a 10 MΩ load resistance is shown in Fig. 12. For increasing V_{DD}, the converter starts up at $V_{DD} \approx 17$ mV, giving an output of approximately 750 mV. For decreasing V_{DD}, the converter delivers an output voltage of the order of 400 mV for an input of around 16 mV.

The reason for the difference between the time for the increasing or the decreasing of the supply voltage is that for the increasing V_{DD},

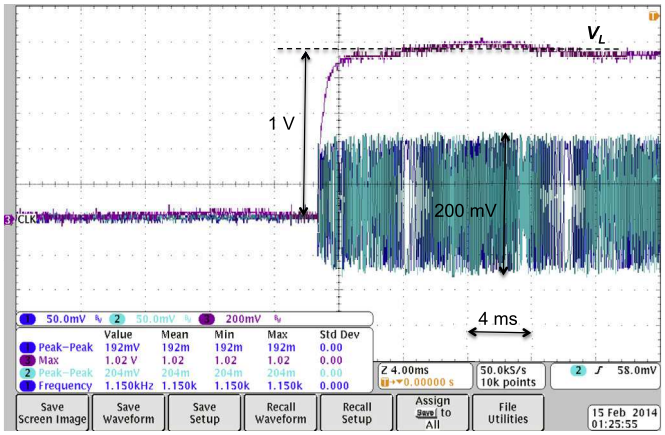


Fig. 11. Load voltage V_L and oscillator outputs, loaded with two 10 MΩ probes, of the converter prototype for $V_{DD} = 24$ mV and $I_L = 100$ nA.

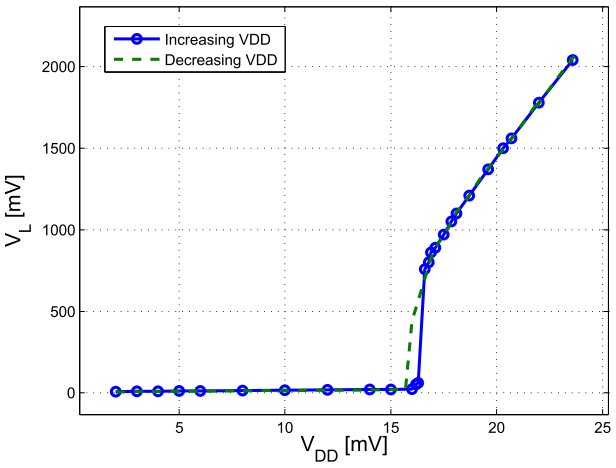


Fig. 12. Output voltage of the boost converter associated with increasing and decreasing input voltage. The load resistance is 10 MΩ.

the oscillator has to provide some energy to charge the capacitors in addition to other amounts of energy to compensate the (very small) losses in the diodes. On the other hand, in relation to the decreasing V_{DD}, since the capacitors have already been charged, the amount of energy the oscillator must provide to the charge pump is smaller than that required for the increasing V_{DD}. As the input voltage decreases below 16 mV, the output voltage suddenly vanishes, indicating that the oscillator stops running.

Other experimental results are shown in Fig. 13. The circuit starts up with $V_{DD} = 16$ mV (at $I_L = 10$ nA), a value very close to the result of 14 mV obtained from post-layout simulation using typical parameters. The condition $I_L = 1$ μA and $V_L = 1$ V is attained at $V_{DD} = 23$ mV. With $V_{DD} = 37.7$ mV the converter can supply a load current of 5 μA with $V_L = 1$ V. The efficiency of the DCP is greatly reduced for low oscillator voltages. As can be seen in Fig. 13 (b), the maximum *PCE* is around 10% for an output voltage of 1 V. Also, there is an optimum I_L/I_S ratio that maximizes the converter efficiency. For the converter under test, the peak of the overall efficiency is achieved for $I_L = 4$ μA, corresponding to $I_L/I_S = 7.3$ ($I_S = 550$ nA).

In addition to the measurements, the start-up converter was simulated for different temperatures. Fig. 14 shows that, for a load resistance equal to 100 MΩ, the converter reaches 1 V, for $V_{DD} \approx 20$ mV, in the temperature range from −20 to 20 °C, and to approximately 21.5 mV

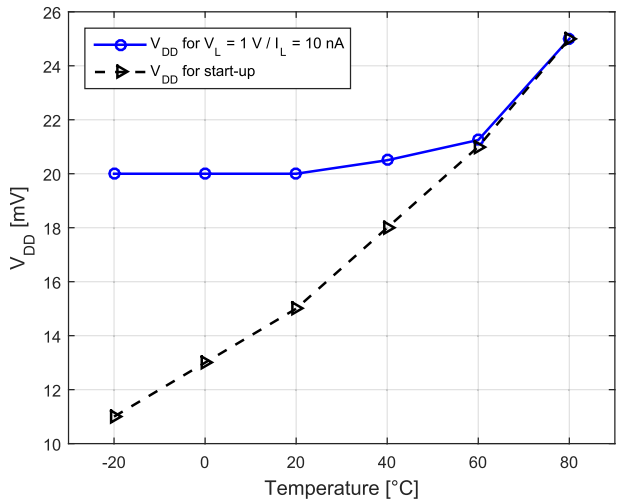


Fig. 14. Simulated results of V_{DD} required for start-up and for nominal output voltage (1 V) with a load resistance of 100 MΩ, in terms of temperature (°C).

when the temperature equals 60 °C. The start-up voltage here means that the output voltage of the charge pump is 100 mV, at least. Fig. 14 shows that the converter start-up is strongly influenced by the temperature, as expected [22].

5. Conclusions

In summary, we have presented an accurate model of the Dickson charge pump, including output voltage, power conversion efficiency, and input resistance. With explicit dependence on the diode parameters, load current, and number of stages, the model is valid from extremely low voltages. A simple expression derived for the input resistance is of great value because it must be considered in the oscillator design, since it directly affects the oscillator start-up voltage.

A converter prototype composed of an enhanced-swing ring oscillator and a Dickson charge pump built in a 130 nm CMOS technology, able to start up from 16 mV, was designed and tested. The analysis presented in this paper offers potential for the design of energy harvesting circuits operating from extremely low voltages, as low as or even less than the thermal voltage.

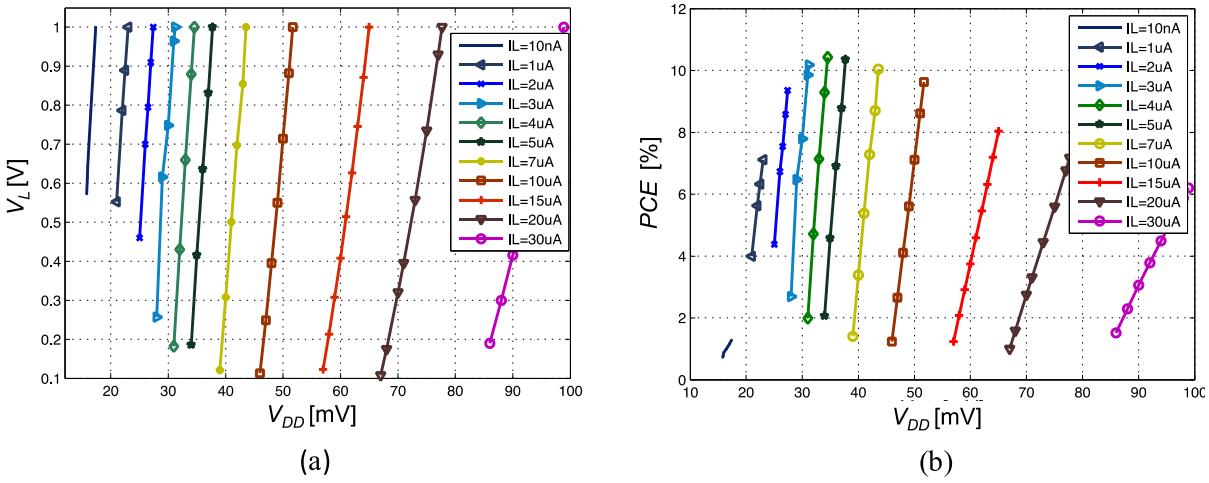


Fig. 13. Experimental results for the step-up converter: (a) DC output voltage and (b) power converter efficiency, in terms of the supply voltage (V_{DD}). The maximum measured output voltage was limited to 1 V.

Acknowledgment

The authors are grateful to CMC Microsystems and MOSIS for providing access to integration and to the Brazilian research agencies CAPES, Finance Code 001, and CNPq, for partially funding this study. The authors thank L. Mouden for assembling the samples used in this study.

Appendix A. Diode forward voltage drop and power losses

The average value of the diode current over a complete cycle of the oscillating signal is equal to the load current I_L [20].

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_D d\theta \tag{A.1}$$

Applying (A.1) for both D_1 and D_2 gives

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S\left[\exp\left(\frac{V_{DD} - V_{C1} - V_A\cos\theta}{n\phi_t}\right)\right] d\theta \tag{A.2}$$

$$I_L = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S\left[\exp\left(\frac{V_{C1} - V_{C2} - 2V_A\cos\theta}{n\phi_t}\right)\right] d\theta \tag{A.3}$$

where V_{C1} and V_{C2} are the DC voltages of the leftmost and second capacitors in Fig. 2. The solution of (A.2) and (A.3) results in

$$V_{d1} = V_A - n\phi_t \ln\left[\frac{I_0(v_a)}{1 + I_L/I_S}\right] \tag{A.4}$$

$$V_{d2} = 2V_A - n\phi_t \ln\left[\frac{I_0(2v_a)}{1 + I_L/I_S}\right] \tag{A.5}$$

where V_{d1} is the forward voltage drop across diodes D_1 and D_N, V_{d2} is the forward voltage drop across the remaining diodes and $I_0(z) = \frac{1}{\pi}\int_0^{\pi} e^{z\cos\theta} d\theta$ is the modified Bessel function of the first kind of order zero.

The average power dissipated in the diodes is

$$P_{d1} = (I_S + I_L)\, V_A \frac{I_1(v_a)}{I_0(v_a)} - I_L n\phi_t \ln\left[\frac{I_0(v_a)}{1 + I_L/I_S}\right] \tag{A.6}$$

$$P_{d2} = (I_S + I_L)\, 2V_A \frac{I_1(2v_a)}{I_0(2v_a)} - I_L n\phi_t \ln\left[\frac{I_0(2v_a)}{1 + I_L/I_S}\right] \tag{A.7}$$

where P_{d1} is the power dissipation in diodes D_1 and D_N, P_{d2} is the power dissipation in the remaining diodes and $I_1(z) = \frac{1}{\pi}\int_0^{\pi} \cos\theta e^{z\cos\theta} d\theta$ is the modified Bessel function of the first kind of order one.

References

[1] J.F. Dickson, On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique, IEEE J. Solid State Circuits 11 (1976) 374–378, https://doi.org/10.1109/JSSC.1976.1050739.
[2] T. Tanzawa, Innovation of switched-capacitor voltage multiplier: Part 3: state of the art of switching circuits and applications of charge pumps, IEEE Solid-State Circuits Mag. 8 (2016) 63–73, https://doi.org/10.1109/MSSC.2016.2573998.
[3] Y. Zhang, F. Zhang, Y. Shakhsheer, J.D. Silver, A. Klinefelter, M. Nagaraju, J. Boley, J. Pandey, A. Shrivastava, E.J. Carlson, A. Wood, B.H. Calhoun, B.P. Otis, A batteryless 19 W MICS/ISM-band energy harvesting body sensor node SoC for ExG applications, IEEE J. Solid State Circuits 48 (2013) 199–213, https://doi.org/10.1109/JSSC.2012.2221217.
[4] S. Ethier, M. Sawan, Exponential current pulse generation for efficient very high-impedance multisite stimulation, IEEE Trans. Biomed. Circuits Syst. 5 (2011) 30–38, https://doi.org/10.1109/TBCAS.2010.2073707.
[5] R. Vullers, R. Van Schaijk, I. Doms, C. Van Hoof, R. Mertens, Micropower energy harvesting, Solid State Electron. 53 (2009) 684–693, https://doi.org/10.1016/j.sse.2008.12.011.
[6] D. Rozgi, D. Markovi, A miniaturized 0.78-mW/cm^2 autonomous thermoelectric energy-harvesting platform for biomedical sensors, IEEE Trans. Biomed. Circuits Syst. 11 (2017) 773–783, https://doi.org/10.1109/TBCAS.2017.2684818.
[7] Y. Qian, D. Lu, J. He, Z. Hong, An on-chip transformer-based self-startup hybrid SIDITO converter for thermoelectric energy harvesting, IEEE Trans. Circuits Syst. II: Express Briefs 65 (2018) 1673–1677, https://doi.org/10.1109/TCSII.2017.2773564.
[8] S. Yoon, S. Carreon-Bautista, E. Sanchez-Sinencio, An area efficient thermal energy harvester with reconfigurable capacitor charge pump for IoT applications, IEEE Trans. Circuits Syst. II: Express Briefs 65 (2018) 1974–1978, https://doi.org/10.1109/TCSII.2018.2794299.
[9] B.I. Rapoport, J.T. Kedzierski, R. Sarpeshkar, A glucose fuel cell for implantable brain-machine interfaces, PLoS One 7 (2012) e38436https://doi.org/10.1371/journal.pone.0038436.
[10] P.-S. Weng, H.-Y. Tang, P.-C. Ku, L.-H. Lu, 50 mV-input batteryless boost converter for thermal energy harvesting, IEEE J. Solid State Circuits 48 (2013) 1031–1041, https://doi.org/10.1109/JSSC.2013.2237998.
[11] Y.K. Ramadass, A.P. Chandrakasan, A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage, IEEE J. Solid State Circuits 46 (2011) 333–341, https://doi.org/10.1109/JSSC.2010.2074090.
[12] P. Chen, X. Zhang, K. Ishida, Y. Okuma, Y. Ryu, M. Takamiya, T. Sakurai, An 80 mV startup dual-mode boost converter by charge-pumped pulse generator and threshold voltage tuned oscillator with hot carrier injection, IEEE J. Solid State Circuits 47 (2012) 2554–2562, https://doi.org/10.1109/JSSC.2012.2210953.
[13] M.B. Machado, M.C. Schneider, M. Sawan, C. Galup-Montoro, Fully-integrated 86 mV - 1 V step-up converter for energy harvesting applications, in: 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), 2014, pp. 452–455, https://doi.org/10.1109/NEWCAS.2014.6934080.
[14] H. Fuketa, S. Ouchi, T. Matsukawa, Fully integrated, 100-mV minimum input voltage converter with gate-boosted charge pump kick-started by LC oscillator for energy harvesting, IEEE Trans. Circuits Syst. II: Express Briefs 64 (2017) 392–396, https://doi.org/10.1109/TCSII.2016.2573382.
[15] H.M. Jayaweera, A. Muhtaroglu, Design optimization of a fully integrated charge-pump with LC tank oscillator for ultra-low voltage energy harvesting, Microelectron. J. 59 (2017) 33–39, https://doi.org/10.1016/j.mejo.2016.10.010.
[16] Z. Luo, L. Zeng, B. Lau, Y. Lian, C. Heng, A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting, IEEE Trans. Circuits Syst. I: Reg. Pap. 65 (2018) 1744–1757, https://doi.org/10.1109/TCSI.2017.2757505.
[17] M. Dezyani, H. Ghafoorifard, S. Sheikhaei, W.A. Serdijn, A 60 mV input voltage, process tolerant start-up system for thermoelectric energy harvesting, IEEE Trans. Circuits Syst. I: Reg. Pap. 65 (2018) 3568–3577, https://doi.org/10.1109/TCSI.2018.2834312.
[18] B. Lim, J. Seo, S. Lee, A Colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency, IEEE J. Solid State Circuits 53 (2018) 3293–3302, https://doi.org/10.1109/JSSC.2018.2863951.
[19] K.R. Sadagopan, J. Kang, Y. Ramadass, A. Natarajan, A cm-scale 2.4-GHz wireless energy harvester with nanoWatt boost converter and antenna-rectifier resonance for WiFi powering of sensor nodes, IEEE J. Solid State Circuits 53 (2018) 3396–3406, https://doi.org/10.1109/JSSC.2018.2875465.
[20] A.J. Cardoso, L.G. de Carli, C. Galup-Montoro, M.C. Schneider, Analysis of the rectifier circuit valid down to its low-voltage limit, IEEE Trans. Circuits Syst. I: Reg. Pap. 59 (2012) 106–112, https://doi.org/10.1109/TCSI.2011.2161366.
[21] M. Abramowitz, I.A. Stegun, Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables, Dover Publications, Inc, 1964.
[22] M.B. Machado, M.C. Schneider, C. Galup-Montoro, On the minimum supply voltage for MOSFET oscillators, IEEE Trans. Circuits Syst. I: Reg. Pap. 61 (2014) 347–357, https://doi.org/10.1109/TCSI.2013.2278344.