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Isolated Bidirectional DC-DC Converter Based on the Integration of the Full-Bridge ZVS-PWM and Current-Fed Push-Pull Converter for DC Microgrid Applications

Florianópolis, Santa Catarina - Brazil
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Orientador: Prof. Ivo Barbi, PhD

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

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Florianópolis, Santa Catarina - Brazil, 29 de Novembro de 2019.

Este trabalho é dedicado aos meus pais e ao meu irmão.

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“Somewhere, something incredible is waiting to be known.”
(Carl Sagan, 1977)

RESUMO

Esta dissertação de mestrado apresenta a proposta de um Conversor CC-CC Bidirecional Isolado baseado na integração dos conversores CC-CC *ZVS-PWM* Ponte Completa e *Push-Pull* alimentado em corrente, grampeado com um conversor *Buck*. A energia acumulada na indutância de dispersão do transformador ocasiona sobretensões nos *MOSFETs* do estágio *Push-Pull*, essas tensões são reguladas pelo conversor Buck. Assim, a energia que seria dissipada em grampeadores passivos usuais é parcialmente regenerada pelo conversor de grampeamento. De maneira geral, o conversor proposto serve como solução para a aplicação em uma microrrede CC, conectando um banco de baterias de íons de lítio a um barramento CC principal de distribuição de energia. Portanto, a revisão do estado da arte abrange microrrede CC, módulos fotovoltaicos, baterias de íon de lítio, técnicas de controle de transferência de energia como controle por droop e principalmente conversores CC-CC bidirecionais isolados. Ademais, a análise matemática, dimensionamento e resultados experimentais de um protótipo de 2000 W serviram para atestar todas as teorias apresentadas neste trabalho. Finalmente, o conversor projetado apresentou uma eficiência máxima de 95,1% quando as baterias estão sendo carregadas e 91,8% quando estão sendo descarregadas. Além disso, estudos teóricos como ganho estático parametrizado, características de saída, técnica de modulação, modelagem e controle de corrente das baterias são demonstrados para enriquecer o conteúdo científico desse trabalho na área de eletrônica de potência e servir como base para o estudo de conversores CC-CC bidirecionais isolados na aplicação de microrredes CC.

Palavras-chave: Bidirecional. *Buck*. CC. Baterias. Íons de Lítio. Microrrede. Ponte Completa. *Push-Pull*. *ZVS*. *PWM*.

RESUMO EXPANDIDO

Introdução

Primeiramente, a necessidade da busca por fontes de energia limpas e renováveis é citada para levantar questões e desafios importantes sobre a implementação de microrredes de corrente contínua, tais como sua importância no atual sistema elétrico, os componentes implementados como fontes e cargas, o gerenciamento do fluxo de potência, os controles necessários e principalmente a necessidade dos conversores estáticos para fazer as conversões de tensão e corrente, conectando todo sistema. A implementação de um conversor CC-CC bidirecional isolado é então proposto para carregar e descarregar baterias de íons de Lítio no barramento CC da microrrede. Desta maneira, esta dissertação de Mestrado apresenta a proposta de um Conversor CC-CC Bidirecional Isolado baseado na integração dos conversores CC-CC ZVS-PWM Ponte Completa e Push-Pull alimentado em corrente, grampeado com um conversor Buck.

Objetivos

O objetivo geral deste trabalho é iniciar um projeto de pesquisa que visa construir um microrrede de corrente contínua no Laboratório Fotovoltáica/UFSC. Assim, o estado da arte sobre a aplicação e necessidades de microrredes de corrente contínua foi estudado. Além disso, os principais objetivos específicos dessa pesquisa são o estudo, simulação e análise de topologias de conversores CC-CC bidirecionais isolados de alto ganho para a aplicação no carregamento de baterias de íons de lítio em uma microrrede de corrente contínua. Diversas estruturas serão comparadas, e por fim, será proposto a montagem de um protótipo para verificar a funcionalidade do mesmo. Será também comparada a nova estrutura a outras estruturas já estudadas. Finalmente, outro objetivo a ser cumprido é a divulgação e incentivo de mais linhas de pesquisas na área microrredes CC, mostrando sua importância à sociedade.

Metodologia

Para realização da dissertação de Mestrado a seguinte metodologia foi adotada. Primeiramente, é realizada uma introdução e contextualização sobre microrrede CC assim como a apresentação dos objetivos e metodologias utilizadas. Então, é apresentado uma revisão da literatura sobre possíveis arquiteturas e componentes da microrrede, como os módulos fotovoltaicos e seu conversor CC-CC unidirecional para operar na máxima potência, baterias de íon de lítio e seu conversor CC-CC bidirecional isolado, o inversor bidirecional e a rede. Além disso, outros aspectos como o fluxo de potência e os controles necessários para funcionamento estável da microrrede são estudados. Em seguida, são estudados os conversores CC-CC Ponte Completa *ZVS-PWM* e *Push-Pull* alimentado em corrente para formar o conversor CC-CC bidirecional isolado proposto, bem como a modulação de autoria própia. Finalmente, a obtenção da função transferência necessária para o controle de corrente das baterias do conversor proposto, assim como o projeto e dimensionamento do mesmo são demonstrados. Com isso, um protótipo de 2000 W foi construído físicamente, com tensão do barramento

CC em 400 V e tensão das baterias em 48 V. Sendo que todo os cálculos realizados para a construção do protótipo se encontram nos Apêndices.

Resultados e Discussão

De maneira geral, a aplicação de uma microrrede CC pode gerenciar e distribuir energia entre várias fontes e cargas, com segurança e estabilidade. As tecnologias existentes no mercado foram exploradas para entender as necessidades de controle e compartilhamento de energia. Portanto, foi verificado nesta pesquisa, a necessidade de projetar um conversor CC-CC bidirecional isolado para conectar o banco de baterias de íons de lítio ao barramento CC. Finalmente, o conversor bidirecional proposto com base na integração Conversores Ponte Completa *ZVS-PWM* e *Push-Pull* alimentado em corrente, grampeado com o conversor *Buck*, apresentou uma eficiência máxima de 95,1% para o fluxo de potência positivo e 91,8% para o fluxo de energia negativo, sendo que a operação no fluxo positivo está acima de 90% de eficiência para qualquer faixa de potência. Assim, este conversor pode ser aplicado em microrredes CC para carregar e descarregar banco de baterias de íons de lítio com o barramento CC, já que os resultados experimentais confirmaram a operação e características do conversor.

Considerações Finais

O conversor proposto se mostrou estável e eficiente nos testes em potência nominal. Ao comparar os resultados obtidos com os resultados encontrados na literatura, o conversor CC-CC bidirecional isolado proposto se apresenta como uma excelente solução para conversores de alta eficiência e ganho estático, aplicados em alta potência. Porém, trabalhos futuros visam melhorar as vantagens desse conversor. Por exemplo, o projeto de outro conversor para ser usado como regulador de tensão para comparar sua eficiência com o Conversor *Buck* implementado um controle de tensão eficaz. Estudar e aplicar comutação suave para o fluxo de potência negativo para otimizar a eficiência do conversor. Assim como verificar a influência da indutância magnetizante do transformador na operação do conversor e a influência dos atrasos nos sinais de comando entre os dois estágios do conversor.

Palavras-chave: Bidirecional. *Buck*. CC. Baterias. Íons de Lítio. Microrrede. Ponte Completa. *Push-Pull*. *ZVS*. *PWM*.

ABSTRACT

This master thesis presents the proposal of an Isolated Bidirectional DC-DC Converter based on the integration of a DC-DC Full-Bridge ZVS-PWM and Current-Fed Push-Pull converters, clamped with a Buck Converter to regenerate energy stored in the transformer leakage inductance that is normally dissipated in passive snubber circuits. The converter was design to be applied in a DC microgrid connecting a Lithium-ion battery bank with the DC bus. Therefore, this thesis presents a review in the state of the art about DC microgrid, photovoltaic modules, Lithium-ion batteries, power transfer control techniques such as droop control and isolated bidirectional DC-DC converters. Moreover, the mathematical analysis, sizing and experimental results of a 2000 W prototype are developed to attest all theories presented in this paper. The designed converter presented a maximum efficiency of 95.1% when the batteries are being charged and 91.8% when they are being discharged. In addition, theoretical analysis about the proposed converter like the parameterized static gain, output characteristics, modulation technique, converter modeling and the battery current control are demonstrated to enrich the scientific content of this work in the power electronics field, so the designed converter can be reference in the study of isolated bidirectional DC-DC converters in DC microgrid applications.

Keywords: Bidirectional. Buck. DC. Full-Bridge. Batteries. Lithium-ion. Microgrid. Push-Pull. ZVS. PWM.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternate Current
BESS	Battery energy storage system
BMS	Battery Management System
DAB	Dual Active Bridge
DAROPF	Dynamic active-reactive optimal power flow
DC	Direct Current
EMI	Electromagnetic interference
FACTS	Flexible Alternating Current Transmission System
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated-gate bipolar transistor
I-V	Current-Voltage
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPPT	Maximum power point tracker
PCB	Printed Circuit Board
PLL	Phase locked loop
PV	Photovoltaic
P-V	Power-Voltage
PWM	Pulse Width Modulation
SoC	State of Charge
STATCOM	Static synchronous compensator
SVC	Static VAR compensator
THD	Total Harmonic Distortion
UPFC	Unified power flow controller
USPTO	United States Patent and Trademark Office
VSI	Voltage Source Inverter
ZVS	Zero Voltage Switching

CONTENTS

1 INTRODUCTION

Due to climate change, government of all countries and media have increased the pressure on companies to develop and provide sustainable technologies, including the usage of renewable and clean energy. Sources of renewable energy have low environment impact when compared to traditional energy. Wind, solar, biomass, hydro and geothermal are sources of energy available non-exhaustively in nature.

There are many ways to use those fonts of energy. Photovoltaic cells take advantage of sun rays by converting solar in electrical energy (UPASANI; PATIL, 2018). Since this kind of energy is intermittent, a Battery Energy Storage System (BESS) must be coupled to allow the usage of energy at anytime.

In recent years, the prices of photovoltaic panels and storage systems have been steadily falling and their efficiencies increasing, becoming more competitive in the energy market (UPASANI; PATIL, 2018). Thus, the presence of photovoltaic modules connected to the electricity distribution network has increased over the years in Brazil as shown in the national energy balance of 2018 (BRASIL, 2018), although this amount is still small, as shown in the Figure 1.

Therefore, distributed generation with solar energy would diversify the Brazilian energy sources, which is ideal for the national connected system reliability. Moreover, the implementation of this technology would decrease the environmental impact of energy consumption compared to conventional energy sources. Also, the finance in this area would open new industrial and research field in Brazil that create new jobs and boost the economy with sustainable development.

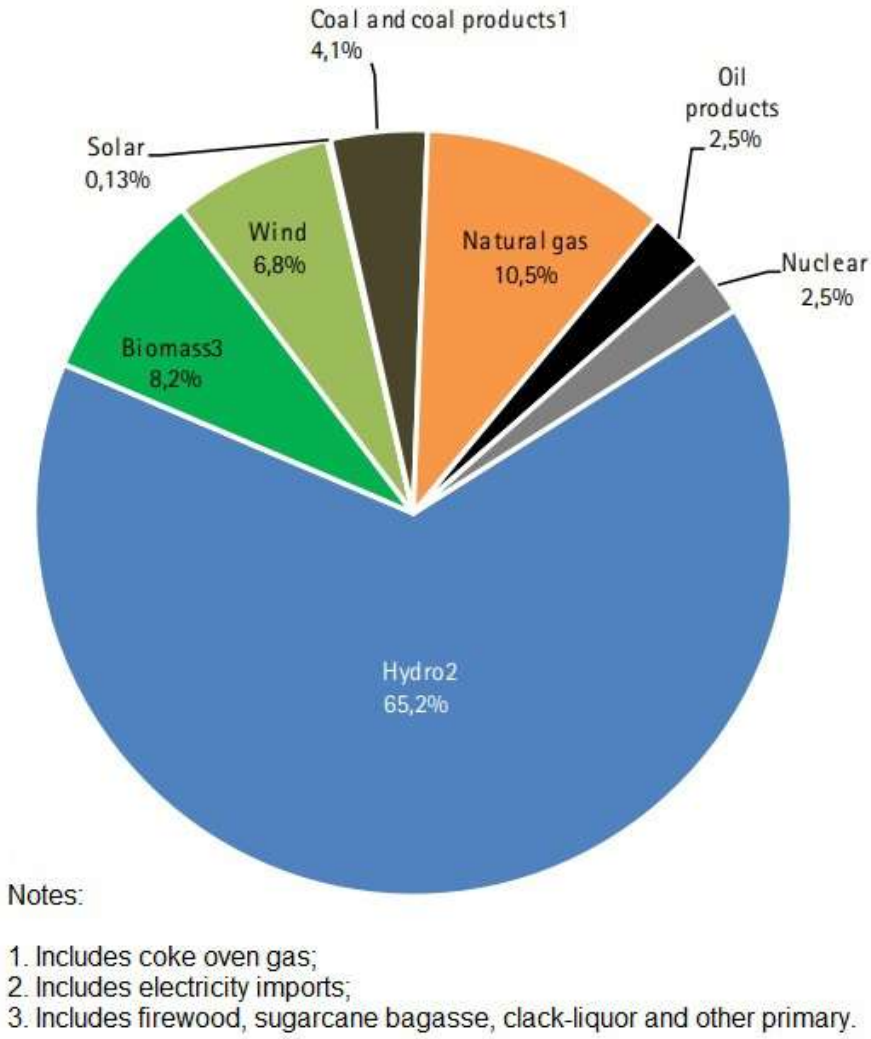
1.1 MICROGRID

Microgrid is a small-scale power grid that can operate individually or in partnership with the main power grid. A microgrid is normally integrated with photovoltaic systems that require static converters to operate at their maximum power point and to keep the voltage or current levels steady at the output. Furthermore, in a microgrid an energy storage system is very important to balance the power flow and manage the energy distribution (UPASANI; PATIL, 2018). Therefore, the BESS is a valuable solution.

A Battery energy storage system (BESS) consists of a battery bank, usually Lithium-ion technology (due to its efficiency) and a converter or inverter. Then, the BESS can be connected to a Direct Current (DC) or Alternate Current (AC) bus, it actually depends on the desired microgrid connection.

Since the majority of the house loads are electronic devices, a low DC voltage-fed house (48 V) could increase the global electrical efficiency of the house and be safer to the user. Therefore, a DC bus is more attractive for this kind of application.

Figure 1 – Solar energy in Brazil



Source: Adapted from (BRASIL, 2018)

The BESS must maintain the balance of power between the source and the load, absorbing or providing energy when necessary, since the source is intermittent. To perform this power flow control, the BESS controls the bidirectional converter of the batteries, observing their state of charge and equalizing their power. The sizing of the BESS is extremely important either, it guarantee a high reliability of the structure, since the greater is the battery pack, the greater is power that it can accumulate.

Furthermore, these systems can also be connected to the grid, in order to guarantee a greater reliability in the supply of energy to the local load, to prevent the system to collapse if there is no energy available, and to export surplus energy.

In conclusion, the DC microgrid presents itself as a challenge for the operation of intermittent power sources feeding a local load, connected to the grid, with a BESS. In other words, the control system applied into the power electronic field is very complex

and its implementation analyzing the efficiency of the microgrid is extremely hard. The microgrid must apply reliable converters to perform the control and power management, so this application requires specific converters design according to the microgrid's functionalities. In fact, the microgrid study is performed only to identify the converter necessities and functionalities, as the main research focus is to study and develop an Isolated Bidirectional DC-DC Converter for this application.

1.2 MARKET TECHNOLOGIES

Most of the products on the market that make the connection between all the mentioned sources and loads, manage and control the power flow do not have their studies published for academic society, which makes this implementation a challenge.

Some manufacturer catalogs show the wiring diagrams, efficiency, and general electrical characteristics of their products, but they do not mention which are the converters, algorithms, controls and methods used to make the system operate stabilized and balanced.

In fact, most manufacturers do not specify if the battery bank is plugged into a DC or AC bus, as in (KYOCERA, 2015) and (ELECTRIC, 2018). Although the battery bank connected to the AC bus presents as a good architecture as cited in (SMA, 2016), this work will follow a model similar to (BOSCH, 2014), which the batteries are connected to the DC bus through a DC-DC bidirectional converter.

The controls necessary to ensure system's stability, balance and power management will be studied further in this dissertation thesis as they have a relevant importance and are not provided by the manufacturers.

1.3 MICROGRID OPERATION

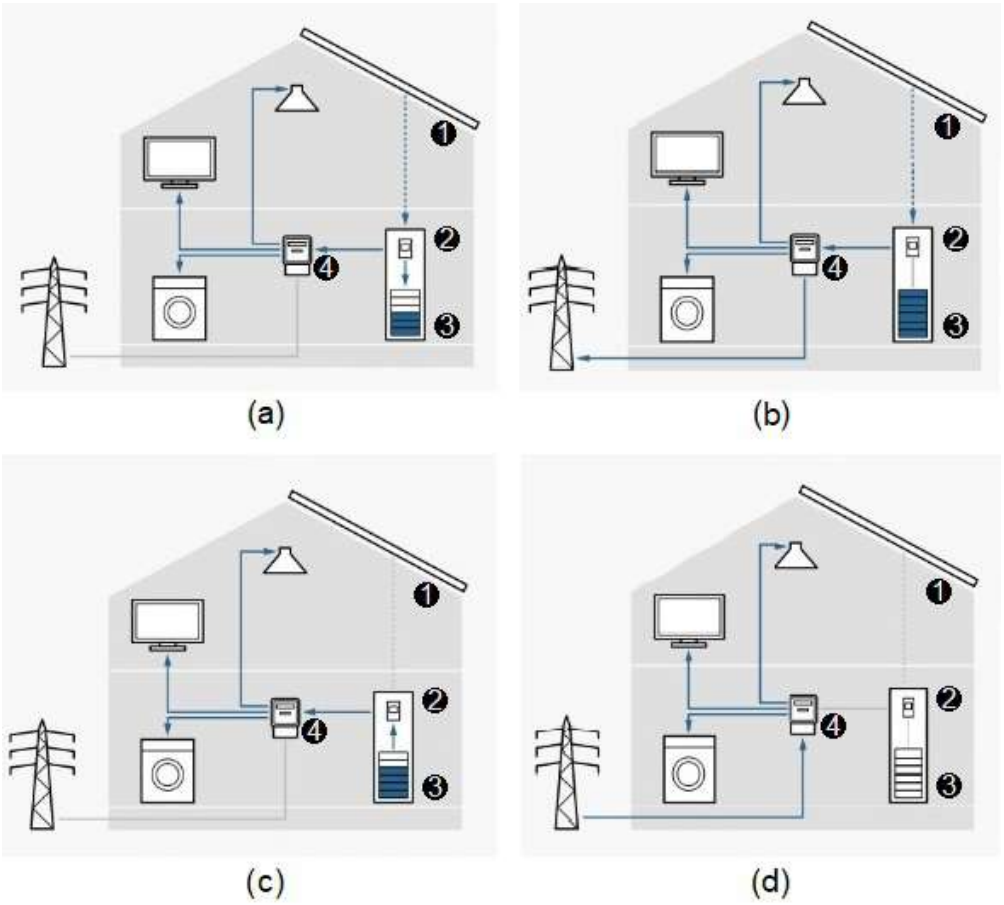
A general microgrid is composed of the following parts:

1. PV modules;
2. PV modules' DC-DC converter, batteries' bidirectional DC-DC converter and DC bus capacitors;
3. Lithium-ion batteries or other energy storage system;
4. Bidirectional voltage inverter, filters, microcontrollers and auxiliary circuits to implement, measure, control and manage the power flow.

This parts are represented in the Figures 2 (a), (b), (c) e (d), so it is possible to analyze the system's behavior during day and night periods.

First, in the morning the photovoltaic modules generate energy used to feed the local load. The excess power is used to charge the Lithium-ion batteries as shown in Figure 2 (a).

Figure 2 – (a) - Microgrid operation at morning, (b) - Microgrid operation at afternoon, (c) - Microgrid operation at night, (d) - Microgrid operation at dawn



Source: (BOSCH, 2014)

In the afternoon, if the batteries are fully charged, any excess power is transferred to the grid and measured as shown in Figure 2 (b).

When the sun goes down, the battery system will function as a power source supplying the local load, as shown in Figure 2 (c).

Finally, late at night if the capacity of the batteries is insufficient to supply power to the load, the electrical grid provides the power to balance the system, as shown in Figure 2 (d).

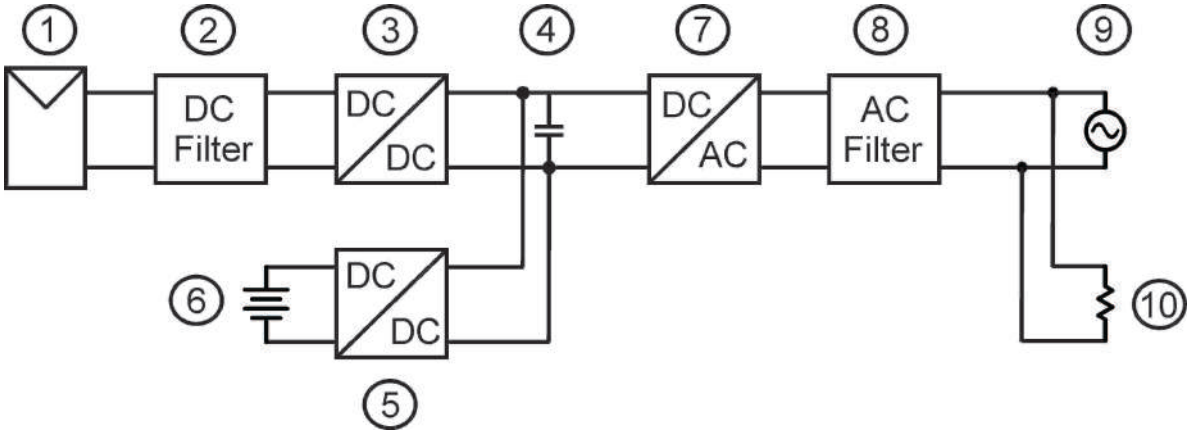
1.4 PROPOSED MICROGRID

Thus, the previously microgrid that was analyzed must be able to connect the sources and loads, making all the necessary controls to keep the system stable and

balanced, respecting safety standards, something similar to what is presented in the market so far.

Many works such as (UPASANI; PATIL, 2018), (KARSTENSEN; MANEZ; ZHANG, 2018), (ALMAZROUEI; HAMID; SHAMSUZZAMAN, 2018) and (KHAWAJA et al., 2017) show the connection scheme between sources and loads through static converters. Based on these references, the power circuit connection diagram shown in the Figure 3 illustrates the proposed microgrid and the DC-DC converter that should be developed in this thesis. Note that the system will not present others power sources such as wind turbines and DC load in order to simplify the analysis of the microgrid.

Figure 3 – Power circuit connection diagram of the proposed grid-tied DC Microgrid



Source: Own elaboration

Which:

1. Photovoltaic modules;
2. DC filter to connect the DC-DC converter;
3. Unidirectional DC-DC converter responsible for the maximum point tracking and to regulate the voltage level in the DC-Bus;
4. Capacitors responsible to maintain stability and voltage of the DC-Bus in 400 V, it also slows the system dynamic;
5. Bidirectional Isolated DC-DC Converter responsible for energy management using droop control, observing the state of charge of the batteries;
6. Lithium-ion battery bank (48 V);
7. Bidirectional voltage inverter responsible for connecting the DC-Bus with a AC load (if necessary) and the network, maintaining the stability of the system and the power management of the microgrid;

8. AC filter to connect the grid and load;
9. Electricity distribution network (220 V);
10. AC load.

The microgrid have voltage and power limits as presented in the market and must comply with safety and quality standards. Also, the system is presented as a complex power network, so it will not focus in the study of the whole microgrid's operation, but implement an efficient solution for items 4, 5 and 6 from Figure 3.

1.4.1 Microgrid control

A control system is required for a stable operation of the proposed network. As it has a lot of controllable variables, the control will be divided into three levels of hierarchy, which the first one has the lowest priority and the third has highest, as follows:

1. Control of the DC-DC converters to perform Maximum power point tracker (MPPT), control of the AC-DC Inverter implementing some modulation technique, single-phase or three-phase Phase locked loop (PLL) to make a synchronous connection to the grid and applying an anti-islanding method;
2. DC bus voltage control, State of Charge (SoC) control and battery equipotentialization;
3. Power management control using concepts such as droop control to maintain system static and dynamic stability.

The first control level is well-known in the literature, but the other two are presented as a challenge in the state of the art for this type of application. Nevertheless, these control techniques are widespread when applied separately. For instance, the droop control is a widespread technique used in the market to connect sources and loads to the network, as shown by (MOUSSAOUI et al., 1996), (YU et al., 2016), (ALAM et al., 2016) e (LUO et al., 2013). Although it is a simple and old method of power sharing, it is hard to find a study that applies this technique in microgrids' applications.

In a power electronics system, the droop control can be performed using the output current to adjust reference voltages for the equivalent circuit of each converter or inverter.

1.5 OBJECTIVES

1.5.1 General objectives

- Develop a part of the microgrid that integrates, control and manage the connection between Photovoltaic (PV) modules, batteries, grid and a local load;

- Contribute to the Brazilian academic society with knowledge and new technology development in the country;
- Propose an efficient Isolated Bidirectional DC-DC Converter that presents a single modulation technique for both power flows.

1.5.2 Specific objectives

- Search the products in the market;
- Search for the best cost-benefit converter and inverter architectures and topologies;
- Search the control techniques for power management and system stability;
- Study and propose an Isolated Bidirectional DC-DC Converter to connect the DC bus and the batteries;
- Model and simulate the proposed system;
- Design, build and debug a small scale prototype;
- Analyze the experimental results;
- Document and publish the acquired knowledge.

1.6 METHODOLOGY

The master thesis is divided into nine chapters, the first is an introduction and contextualization about microgrid, the thesis' proposal and the objectives. Thus, the second chapter supports the thesis goal with a literature review of possible microgrid architectures and each component of the network such as the photovoltaic modules and their DC-DC converter to operate in the maximum power point, Lithium-ion batteries, bidirectional DC-DC converter and the inverter used to connect the system to the grid. Subsequently in the same chapter, a study of the microgrid power flow and some control techniques used for the stable operation of the network is done.

Then, the next chapters proposes a isolated bidirectional DC-DC converter to be applied in the item 5 of Figure 3 based on the integration of the DC-DC Full-Bridge ZVS-PWM and Current-Fed Push-Pull Converters with a voltage regulation done by a buck converter, so this topology is responsible to transfer power between the Lithium-ion battery bank to the DC bus. Thus, the main goal will be study the topology through the topological states, modulation technique, waveforms, output characteristics, static gain, commutation, voltage and current stresses in the components, model, control and simulation.

As the proposed converter have a complex operation, it will be divided into some chapters to better analyze its functioning. So, chapter three presents the study of the DC-DC Full-Bridge ZVS-PWM stage, which is a well-know topology and then chapter four shows the study of the Current-Fed Push-Pull stage to further analyze the connection between these two topologies to have a bidirectional one. So, the Isolated Bidirectional DC-DC Converter is studied in chapter five.

Moreover, since the converter will be applied into a microgrid it is necessary to get the converter's transfer functions to further control it, so chapter six presents the small-signal modeling of the current of the proposed topology.

Chapter seven presents the design of a 2 kW prototype to prove the theoretical studies and to analyze the efficiency and operation of the proposed converter to be applied in a DC microgrid and chapter eight analyze the experimental results acquired in practical experience.

Finally, chapter 9 presents the main conclusions about the research and futures studies that could be done to improve the converter's efficiency and implement it on a DC microgrid.

2 STATE OF THE ART

This chapter presents a literature review about microgrids, since this theme has attracted new researches by companies, technological centers and universities, which generated a lot of publishes in scientific conferences, patents and thesis.

The bibliographic research will be divided into four sections, which the first demonstrates the architectures of the system with the all the necessary converters and inverters to connect the elements of the network such as panels and batteries. The second section study each microgrid component individually. The third defines the power flow management of each architecture studied in section one. Finally, the fourth section refers to the control strategies used to keep the system stable.

The major sources of this research include the Institute of Electrical and Electronic Engineers (IEEE) online platform, the United States Patent and Trademark Office (USPTO) online platform, master thesis, doctoral thesis and product manufacturer catalogs similar to the proposed theme. So, this research aims to analyze the relationship between the theoretical publications and the current market's products.

2.1 DC MICROGRID ARCHITECTURE

In the proposed microgrid, the photovoltaic modules can be represented by a DC source, the power grid by an AC source, the loads can be fed by AC or DC bus and the battery bank can be represented as a DC source or load.

Analyzing this context in the Power Electronics area, it is possible to realize the necessity of static converters and inverters to build the DC microgrid because it is necessary to connect sources and loads at different voltage levels.

There are many examples in the literature about architectures relating converters and inverters for the connection of all mentioned sources and loads. Thus, some possible connections will be presented.

Basically, the possible architectures are divided in relation to the battery bank connection on the DC or AC bus, as proposed by (CHUNG; KANG; PARK, 2018). This work refers to these two microgrid connections as the DC and AC system.

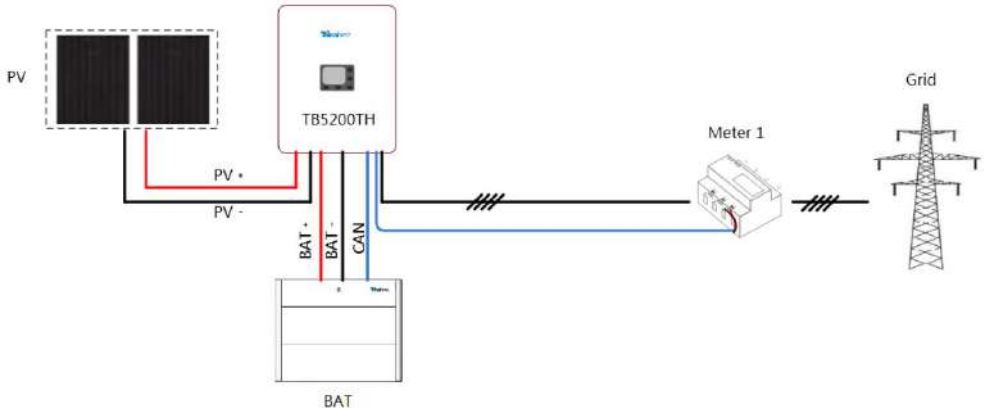
Patents and published researches of architectures for the connection of this type of system correspond to the reality of what is implemented by manufacturers worldwide. Although most manufacturers provide information like voltage, current and power levels of the connections, they do not provide a technical study of the converter's topologies.

Some manufacturer catalogs such as (KYOCERA, 2015), (ELECTRIC, 2018), (SMA, 2016), (BOSCH, 2014), (PANASONIC, 2017), (E-GEAR, 2015), (TRINABESS, 2018) and (INGETEAM, 2016) provide specifications of the equipment and sometimes the simplified diagram of the equipment's connection. For example, some recognized companies that offer solutions for PV modules and BESS such as TrinaBESS, Tabuchi

Electric, Kyocera and Ingeteam contribute with a comprehensive catalog of equipment in this regard, such as the power flow direction between panels, batteries, loads and the network.

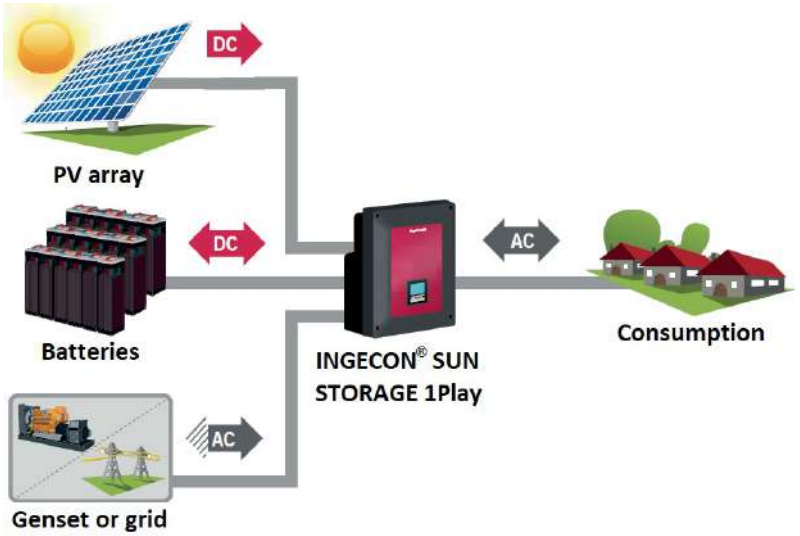
However, these manufacturers do not describe the control techniques employed, nor the converter's topologies. In addition, the wiring diagram of their products, illustrated in the Figures 4 and 5 do not provide any technical information about the power electronics technologies used to connect their microgrid, it only shows the power flow direction.

Figure 4 – Diagram of the TrinaBESS company's commercial product



Source: Adapted from (TRINABESS, 2018)

Figure 5 – Diagram of the Ingeteam company's commercial product



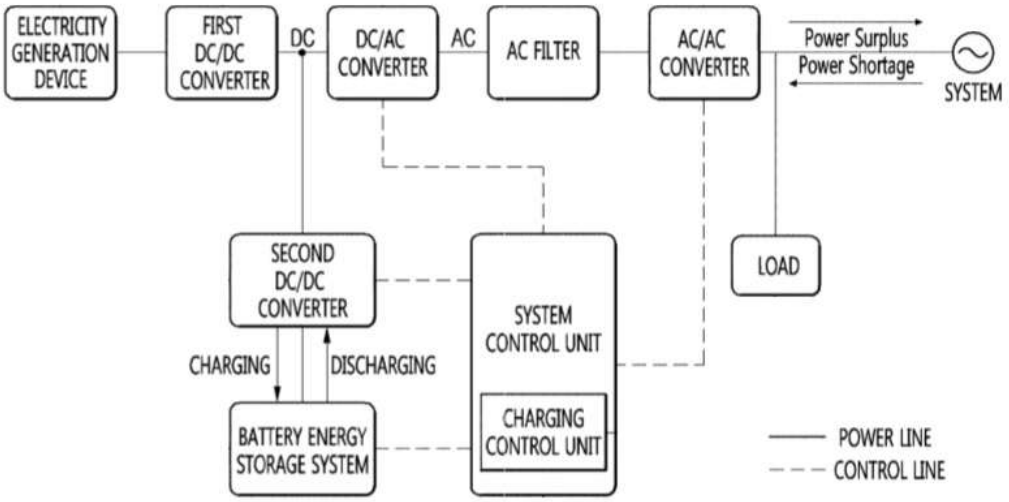
Source: Adapted from (INGETEAM, 2016)

In addiion, some patents are more specific about the power electronics involved

in the block diagrams. The DC microgrid converters necessary to connect sources and loads are shown in Figure 6. The first DC-DC converter has to do the MPPT of the photovoltaic modules and to increase the output voltage at the same level of the DC bus voltage defined in the project.

Control the bus voltage to maintain its level within the limits required by the standard is a very important task, since the DC bus is connected to the inverter input, which directly affect the quality of the output voltage and current that is connected to the grid and load. In addition, DC loads could be connected to this bus through unidirectional DC-DC converters.

Figure 6 – DC microgrid architecture scheme



Source: (CHUNG; KANG; PARK, 2018)

The charging control unit will be responsible for determining if the load is requiring power, otherwise the excess power generated by the panels should charge the batteries depending on their SoC, or export this power to the grid. In addition, the system control unit must decide when it is necessary to discharge the batteries to keep the power system balanced and stable with or without the power generated by the PV modules. Thus, the required control actions are entered into this control unit that gates a bidirectional DC-DC converter and the DC-AC inverters.

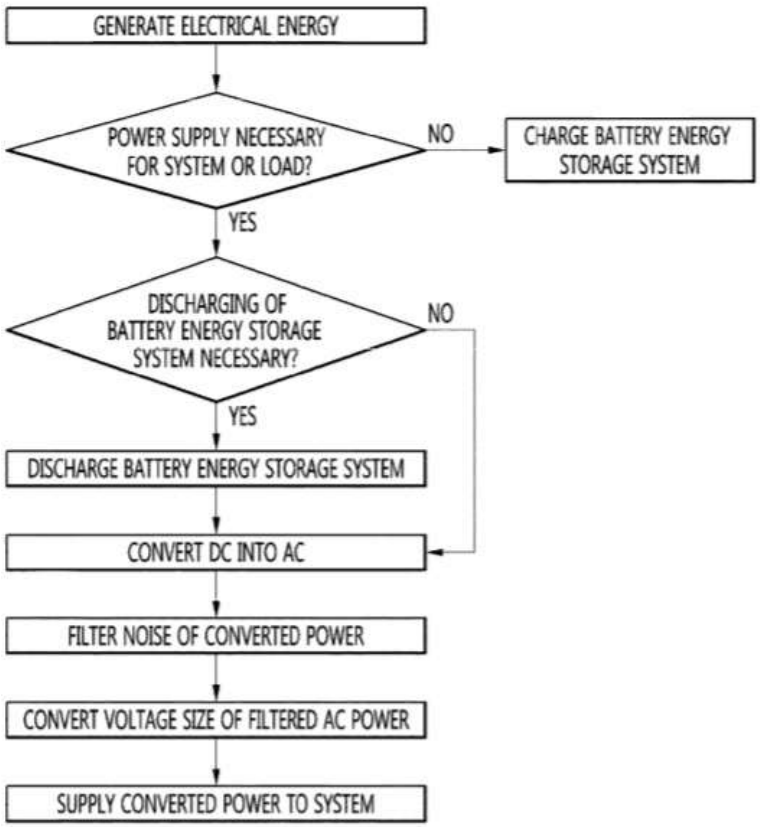
The DC-AC inverter is responsible for converting the DC bus voltage into AC voltage to make the connection with the local AC load and electrical grid. Furthermore, to increase the microgrid life time this inverter may be designed to endure a 10% to 30% greater power than the rated power.

An AC filter is required at the inverter output to reduce the high frequency components generated by inverter modulation. Thus, a more sophisticated modulation techniques or even multilevel inverters are interesting strategies to reduce Total Har-

monic Distortion (THD) which decreases the filter's size, what makes the system lighter and more compact. In contrast, a multilevel inverter would require more Insulated-gate bipolar transistor (IGBT), which significantly increases the project's cost. Finally, an AC-AC converter or transformer suits the voltage and current levels to connect the load and the grid, which can be omitted if the levels are already equal.

In addition, to manage the system power flow, the control unit must follow a pre-established algorithm, as shown in the Figure 7.

Figure 7 – Block diagram of the DC microgrid control



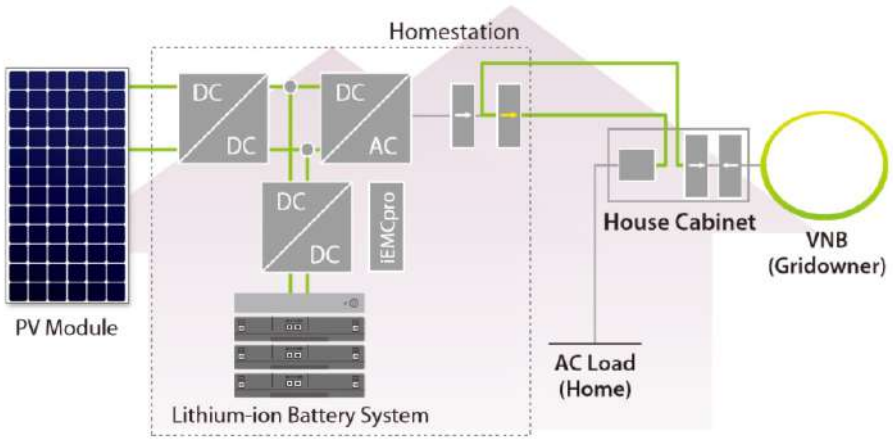
Source: (CHUNG; KANG; PARK, 2018)

An example of a DC bus architecture on the market is the Panasonic system. It offers an alternative to solve the problem of intermittent photovoltaic panels, storing energy at times when the panels are generating more power than the load consumes and providing power when the modules stop generating. Therefore, the system reduces the use of the grid to feed the load, which reduces the consumer's electricity bill.

In addition, the manufacturer provides the internal connection of the static converters, as shown in Figure 8. Photovoltaic panels and batteries are connected to a DC bus via unidirectional and bidirectional DC-DC converters, respectively. The DC bus is

connected to the input of a voltage inverter to connect the microgrid with the electrical grid and a local AC load.

Figure 8 – Block diagram of Panasonic's product



Source: (PANASONIC, 2017)

The similarity between a patented architecture and the architecture of a product on the market can be observed in Figures 6 and 8. In addition, no control information and specific topology of each converter are provided.

2.2 MICROGRID COMPONENTS

The microgrids have several components necessary for their operation. The sources and loads are usually projected for a designed necessity. For example, in this dissertation the sources will be represented by photovoltaic modules, a stationary Lithium-ion battery bank and the electric distribution grid, while the loads will also be represented by the same battery bank, the grid and laboratory loads.

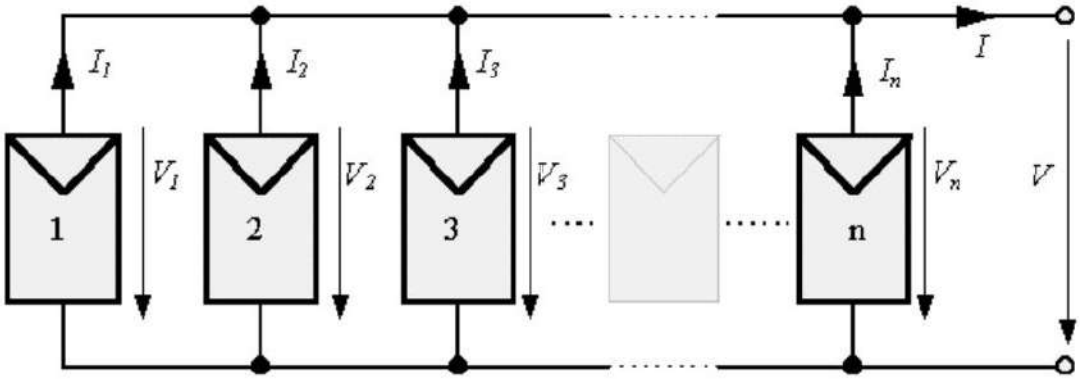
Although some components are well-know in the literature, their study is necessary for a comprehensive understanding of the whole microgrid operation.

In addition, other components such as converters and inverters used for this type of application may not be so trivial to find as it is a boundary knowledge, but it is necessary to build a microgrid.

2.2.1 Photovoltaic modules

Photovoltaic module is a set of cells connected in series, parallel or both, as shown in (AMARAL et al., 2016). By connecting the cells in parallel, the currents are summed and the voltage is the same as the initial cell voltage, as shown in the Figure 9.

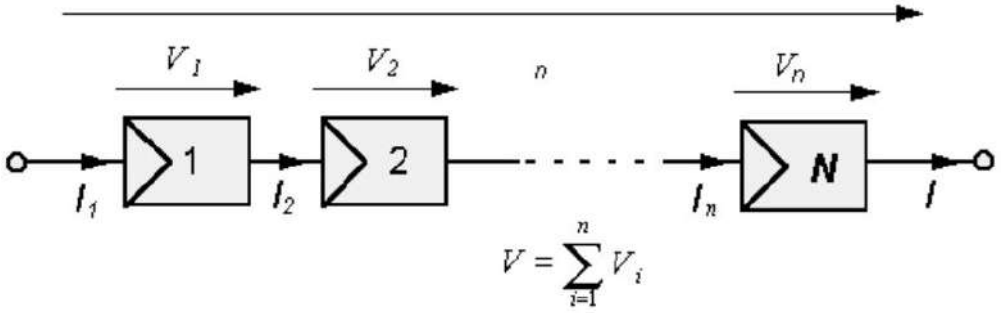
Figure 9 – Photovoltaic modules in parallel



Source: (BRITO, 2006)

When the cells are connected in series, the voltages are summed and the initial current remains the same, as shown in the Figure 10. Thus, for some applications it is interesting to use the series-parallel combination to increase both the voltage and current of the PV array, especially for applications that requires high power (AMARAL et al., 2016).

Figure 10 – Photovoltaic modules in series



Source: (BRITO, 2006)

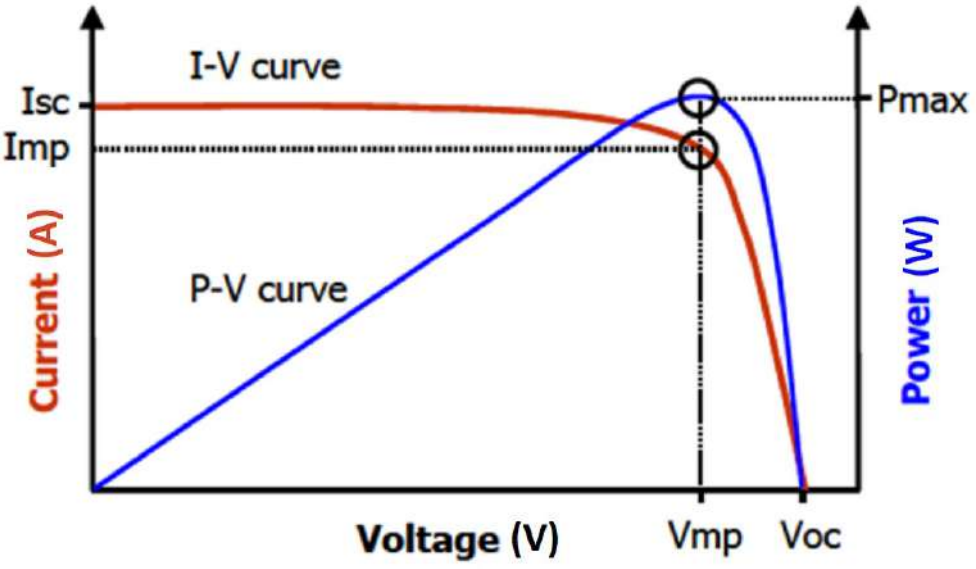
When a cell in a module is shaded, the output power drops sharply, compromising the entire module operation. Thus, to reduce the current module limitation, a bypass diode is used in parallel with the photovoltaic module to be used as an alternative current path. Normally this diode is placed in a range of cell because it is cheaper, though the ideal scenario for efficiency is one diode for each cell, as shown in (AMARAL et al., 2016).

Another constraint is a negative current through the cells due to the connection with batteries. This current can cause a cell efficiency drop and even disconnect it from the array causing a total module power loss. To avoid these problems, a blocking diode

is used in series with the module that prevents the flow of reverse currents.

Among all characteristics that can be extracted from a photovoltaic module, the Current-Voltage (I-V) and Power-Voltage (P-V) curves shown in Figure 11 are the most important ones.

Figure 11 – I-V and P-V curves of a photovoltaic module



Source: Adapted from (SINGH; GOSWAMI, 2018)

Through the I-V and P-V curves of the photovoltaic panels, the electrical parameters that characterize the modules can be determined as shown by (PINHO; GALDINO, 2014) and (SINGH; GOSWAMI, 2018).

Which:

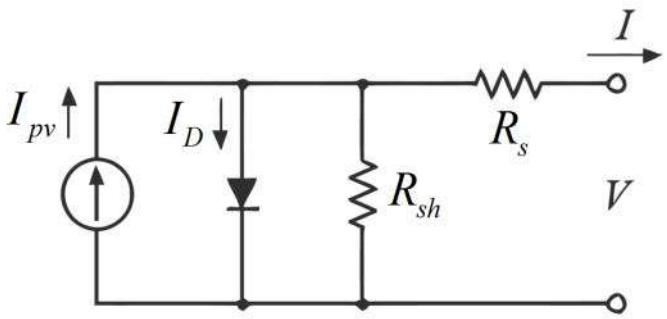
- **Open Circuit Voltage (Voc):** Voltage between the terminals of the PV module when the output terminals are opened so there is no current. It can be measured with a voltmeter at the opened module terminals.
- **Short circuit current (Isc):** Maximum current that can be obtained by the panels, measured when the voltage at their terminals is zero or short circuited. It can be measured with an ammeter by short circuiting the module's terminals.
- **Maximum Power Point (MPP):** The maximum power point that panels can provide corresponds to the point of the curve which the product of current and voltage is maximum.

In addition, environmental factors change the appearance of the module's curves. The result of a change in irradiation intensity is a variation in output current and the

main effect caused by the increase in the module's temperature is a reduction of its output voltage.

So, to model the I-V curve the equivalent static circuit presented in Figure 12 and the Shockley diode equation are necessary.

Figure 12 – Equivalent static circuit of a PV module



Source: (CUBAS; PINDADO; DE MANUEL, 2014)

I_{pv} is the current generated by the solar irradiation, I_{pD} is the diode current, R_s is the series resistor, R_{sh} is the shunt resistor, I_o is the reverse saturation current, V_t is the diode thermal voltage, q is the elementary charge of the electron ($q = 1,602 \times 10^{-19} C$), I_0 is the inverse saturation current, k is the Boltzmann constant ($k = 1,381 \times 10^{-23} \frac{J}{K}$), T is the temperature in the p-n junction of a diode, α is a ideality factor of the diode and N_S is the number of modules, as shown in (CUBAS; PINDADO; DE MANUEL, 2014).

With these circuit and the Shockley diode equation, it is possible to get the equation 1.

$$I = I_{pv} - I_o \left[e^{\frac{V + R_s I}{\alpha N_S V_t}} - 1 \right] - \frac{V + R_s I}{R_{sh}} \tag{1}$$

Which:

$$V_t = \frac{kT}{q} \tag{2}$$

Finally, with the experimental results, the photovoltaic module manufacturer's specifications, the previous equations and a circuit analysis in Figure 12 for different cases, it is possible to simulate I-V and P-V curves and acquire some data that is not provided by the manufacturers such as the value of the resistances of the circuit presented in Figure 12, as determined in (UPASANI; PATIL, 2018).

The approach of modeling the photovoltaic panels is enough to design them as the source that fed the loads in the proposed microgrid.

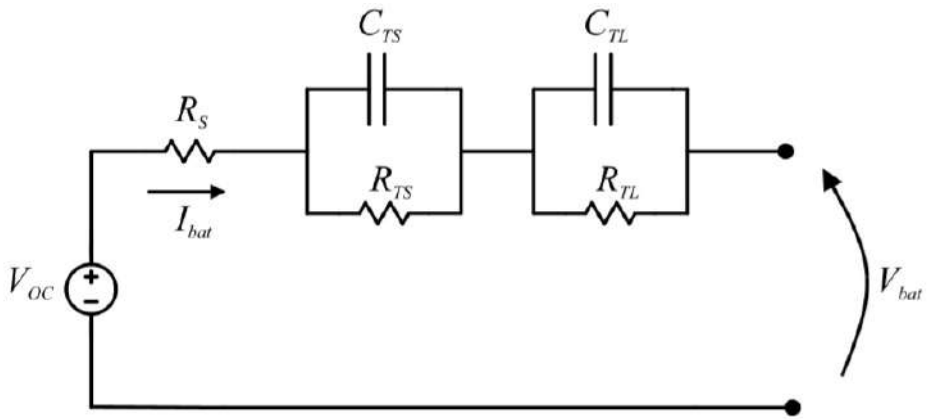
2.2.2 Battery energy storage system

The battery energy storage system or BESS is composed of a Lithium-Ion battery bank capable of supplying the load for a specific time and a bidirectional converter. In addition, a control unit is necessary to satisfy the batteries' state of charge, equalize their energy and manage the power demand.

Lithium-Ion batteries have a high energy density, high output currents and a high efficiency compared to other technologies. A battery is a device that stores energy in a nonlinear waveform through a complex electrochemical process that is different for charging and discharging.

In addition, the batteries can be represented by the dual polarization equivalent circuit presented in (LIMA, 2019), as shown in Figure 13.

Figure 13 – Equivalent circuit of the Lithium-Ion battery



Source: (LIMA, 2019)

Which:

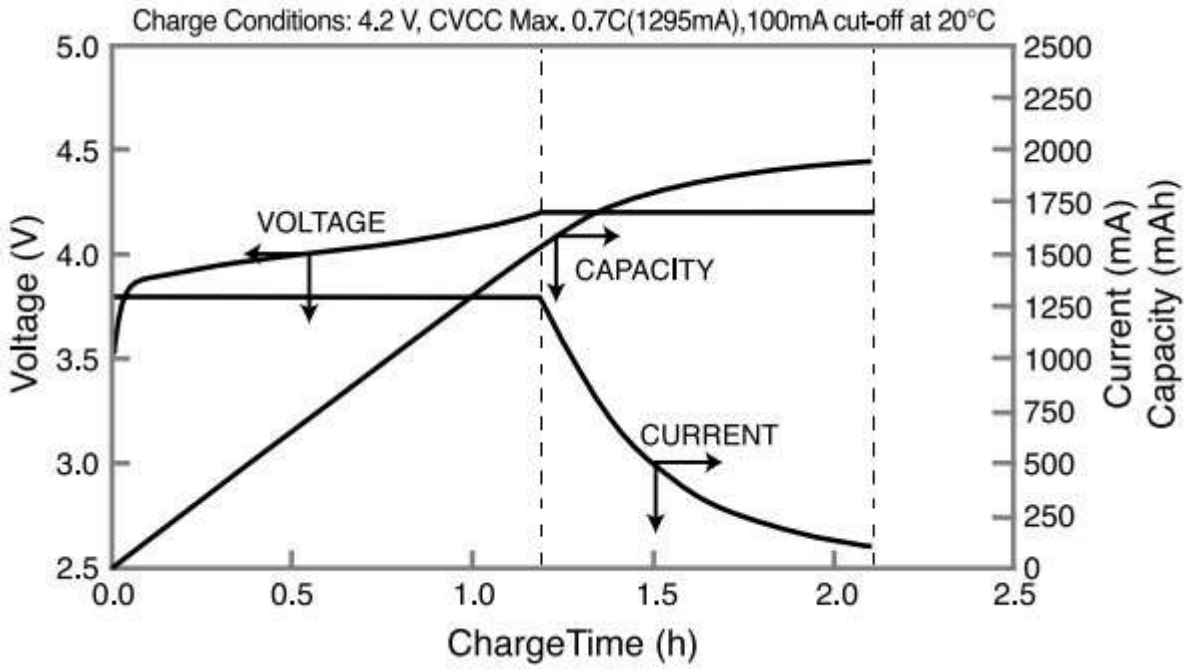
- V_{oc} is the internal open circuit voltage (V);
- V_{bat} is the terminal voltage (V);
- R_S is the series resistance responsible for instantaneous voltage drop of the step response (Ω);
- $R_{TS}C_{TS}$ is responsible for modeling short-time constant (s);
- $R_{TL}C_{TL}$ is responsible for modeling long-time constant (s).

However, the Lithium-Ion batteries also have disadvantages, especially regarding their shortened life due to improper charge and discharge. Thus, it is necessary to use a Battery Management System (BMS) to check and protect battery cells by measuring temperature, voltages and current.

The BMS should perform the analysis to estimate SoC, as it is necessary that the cells are in equilibrium in terms of SoC, so that the difference between each one is smaller, equalizing their powers (KWANG-SEOB KIM; HYUN, 2012). In general, BMS is the part of BESS responsible for its control and protection.

Thus, the process of charging the battery bank and SoC estimation are critical tasks that can be implemented through different methods, as shown by (KWANG-SEOB KIM; HYUN, 2012), (HAN, 2016), (TOPAN et al., 2016) and (THOMAS; STIENEKER; DE DONCKER, 2013). All methods use a constant current and voltage mode to estimate the battery SoC, as shown in Figure 14.

Figure 14 – Lithium-Ion battery characteristics



Source: (KWANG-SEOB KIM; HYUN, 2012)

This method is also presented in (THOMAS; STIENEKER; DE DONCKER, 2013) and it shows that in the first interval, the batteries are charged with a constant current until the maximum voltage is reached. In the second interval, the voltage is kept constant, however, as the state of charge increases the battery current decreases until it reaches a certain value. So, the battery is considered fully charged and the process is done.

Using this technique it is possible to charge batteries faster and extend their lifetime because these methods reduces the time batteries are subjected to high current and voltage levels at its terminals (KAWAKAMI et al., 2014).

2.2.3 Unidirectional DC-DC converter

Photovoltaic applications must use an unidirectional DC-DC converter at the output of the PV array. The converter has the functions of implement a MPPT algorithm so that the converter operates at its maximum power point and control the output voltage of the converter to match the voltage levels of the DC bus.

There are several converters in the literature that can be applied in Photovoltaic modules. Commercial converters such as buck, boost, buck-boost, flyback and their derivations are common examples in the market, depending on the PV array and DC bus voltage levels.

The MPPT techniques are consolidated in the literature through dissertations, theses and articles. A widely referenced method in the literature is the incremental conductance method, so it should be implemented within the closed-loop control of the unidirectional DC-DC converter. This method is based on the calculation of the derivative of power to voltage of the photovoltaic system. Thus, the algorithm uses the values to adjust the step size of MPPT.

If the derivative value is greater than zero, then the greatest power point is in the right side of the curve. If the derivative value is smaller than zero, then the maximum power point is in the left side of the curve. So, the maximum point is found when the derivative value is zero. A disadvantage is the requirement of current and voltage sensors.

There are many other effective methods that do not require these sensors and others efficient converters too. However, the focus of this dissertation does not involve the implementation of these converters or advanced algorithms since there are many studies in the literature that could applied in the microgrid development.

2.2.4 Bidirectional DC-AC inverter

The main objective of the inverter is to transform the DC bus into AC to connect the system to the grid and the local load. However, this application requires some control technique to manage the power flow of the microgrid and keep the network stable.

The inverter could use droop control, a method that requires to check the power levels of the batteries and the local load needs, being responsible for exporting or importing power from the distribution network to balance the power flow. Thus, the inverter is a key part of system reliability and balance.

Some robust inverter that can be found in researches and the market are the single-phase and three-phase Voltage Source Inverter (Voltage Source Inverter (VSI)), each one depending on the power of the system (RODRÍGUEZ et al., 2004). This inverter is used when the DC source is a voltage source, as presented in the microgrid

since the source will be the DC bus itself composed of a capacitor bank that must keep a constant voltage.

Thus, this inverter transforms the input continuous voltage into a 60 Hertz sinusoidal voltage by triggering the IGBTs with a modulation technique that has many levels to decrease the filter size and volume.

Therefore, the inverter's output requires the implementation of a passive filter to improve THD on both grid and load. The higher the number of output voltage levels, the smaller the filter will be to keep THD in compliance with the standards, so the use of multilevel inverters has been a good alternative for microgrid applications.

2.2.5 Isolated Bidirectional DC-DC converter

To charge and discharge the batteries within the microgrid DC bus many publications show the necessity of a bidirectional DC-DC converter, since it has less components than apply two individual unidirectional DC-DC converters for each power flow.

In addition, the galvanic isolation between the DC bus and the batteries increase user's protection and the converter static gain.

Since the focus of this Master thesis is the application of a bidirectional DC-DC converter to connect the Lithium-ion battery bank with the DC bus, some isolated topologies will be presented to understand their advantages and disadvantages compared with the proposed topology.

There are many examples in the state of the art about isolated bidirectional DC-DC converters that can be applied in DC microgrid applications.

2.2.5.1 Modified DAB bidirectional DC-DC converter

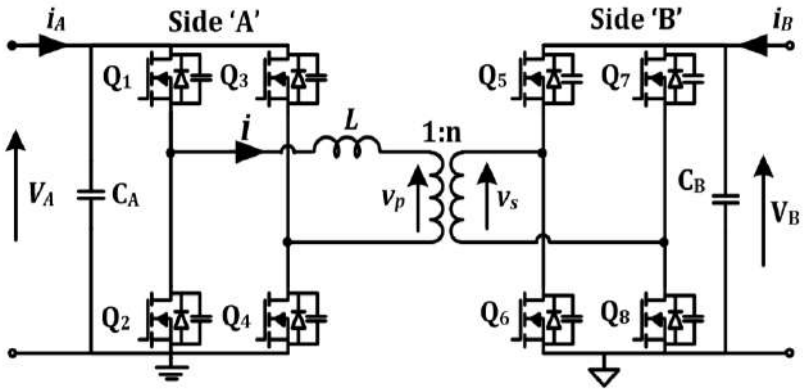
Among the isolated bidirectional soft switching converters, the Dual Active Bridge (DAB) converter is one of most common choises to use in high power applications, presented in Figure 15. However, the converter presets a narrow soft switching range, which decreases its efficiency. Furthermore, the DAB converter suffer a problem of high current ripple in the low voltage side, which represents the batteries.

Therefore, the converter proposed in (DANESHPAJOOH; BAKHSHAI; JAIN, 2012) was designed to address some problems metioned for conventional DAB converters along with a modulation technique. The modified dual active bridge converter is shown in Figure 16.

Different from traditional current fed converters, the modified DAB converter have inductors connected into the center pole of the bridge legs instead of the DC bus. In this topology, the inductors are responsible to smooth the DC bus current ripple and help soft switching.

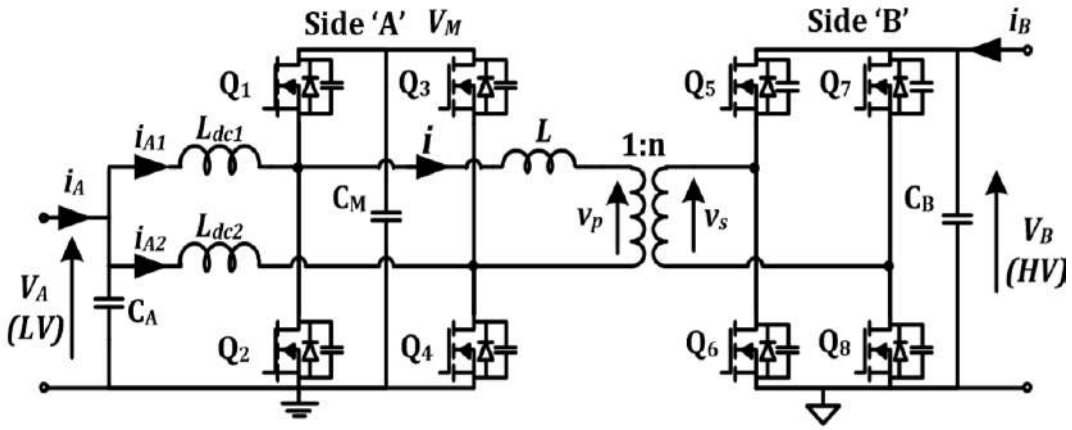
Moreover, the basic energy transfer principles is similar to the conventional DAB converter. So, the energy transfer is based on the phase shift modulation technique.

Figure 15 – Conventional Dual Active Bridge Converter



Source: (DANESHPAJOOH; BAKHSHAI; JAIN, 2012)

Figure 16 – Modified Dual Active Bridge Converter



Source: (DANESHPAJOOH; BAKHSHAI; JAIN, 2012)

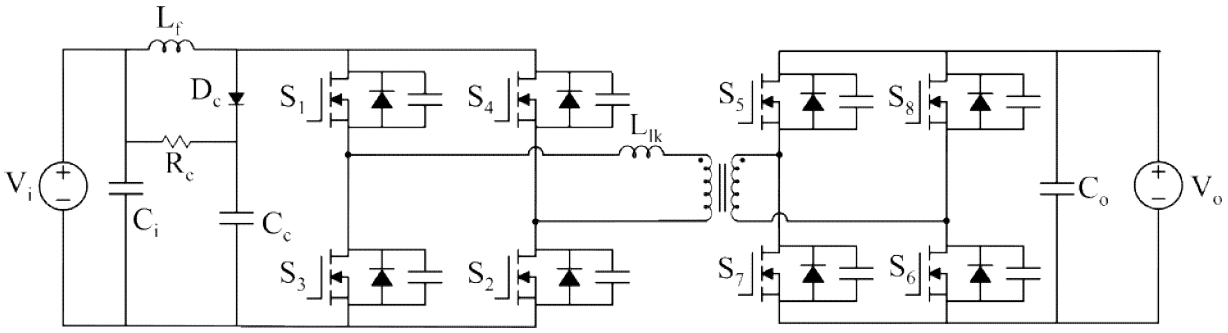
2.2.5.2 Isolated bidirectional Boost Full-Bridge DC-DC converter

The converter proposed in (ZHU, 2006) is a high power isolated bidirectional DC-DC converter to control the direct current flow between a voltage bus and an energy storage device to provide stable power to a DC load. Therefore, it is mentioned the importance of a Galvanic isolation for flexibility of system reconfiguration and meeting safety standards.

The proposed converter is presented in Figure 17. The converter is composed by two stage. The first stage is an current-fed inverter driven as a boost converter, which presents some high voltage spike across the current-fed switches because of the leakage inductance of the transformer. The second stage is a Full-Bridge ZVS-PWM.

The proposed converter was presented in 2004. Although it was not tested in

Figure 17 – Isolated Boost Full-Bridge ZVS-PWM DC-DC bidirectional converter



Adapted from: (ZHU, 2006)

both power flow direction, some concepts cited by the author are still applicable, such as the importance of separating the commutation mode from the energy transferring mode to avoid load power flowing into the snubber circuit.

Furthermore, it can be notice in this article a disadvantage of the topology when the power is increased. In high power operation the boost inductor current exceeds the preset leakage inductance current. The mismatch current shows up when the commutation occurs, which modifies the converter waveforms and cause some current and voltage spikes across the converter's components.

2.2.5.3 Isolated bidirectional Half-Bridge DC-DC converter

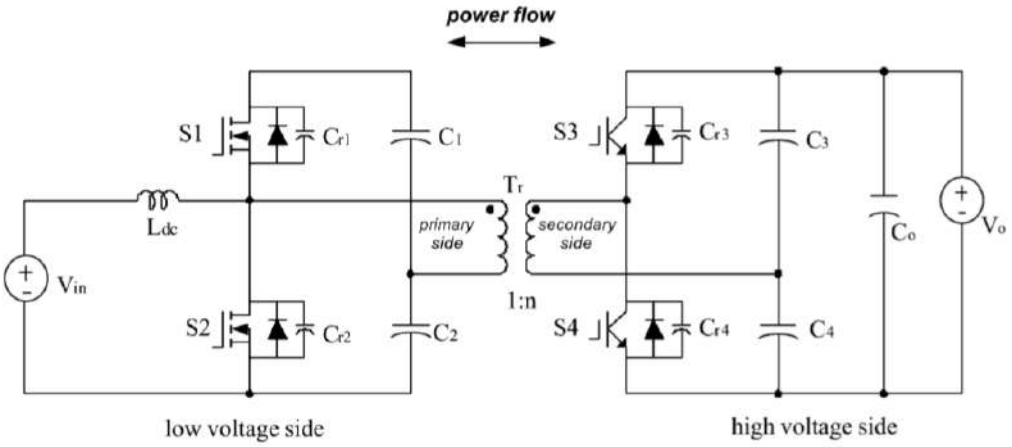
The converter proposed by (PENG et al., 2004) is based on a dual half-bridge topology. The topology shown in Figure 18 has a minimum number of components. So, it is a good alternative to high power and low cost applications.

The circuit consists of an inductor (L_{dc}) on the battery side and two half-bridges each placed on each side of the main transformer. Also, the switches present parallel capacitor for soft switching.

The converter presents two power flow directions. The boost mode is when the power flow from the low voltage side to the high voltage side. The other power flow direction the converter works in buck mode to recharge the battery. The switches of the high voltage side are implemented with IGBTs and the low voltage side are implemented with MOSFETs.

The article provides the simplified modulation technique implemented, the converter topological states, some characteristics and the experimental results for the 1.6 kW prototype. In addition, the efficiency for load power range chart shown in the article indicates the maximum converter efficiency of 92.5%.

Figure 18 – Isolated Soft-Switched Bidirectional Half-Bridge DC-DC converter



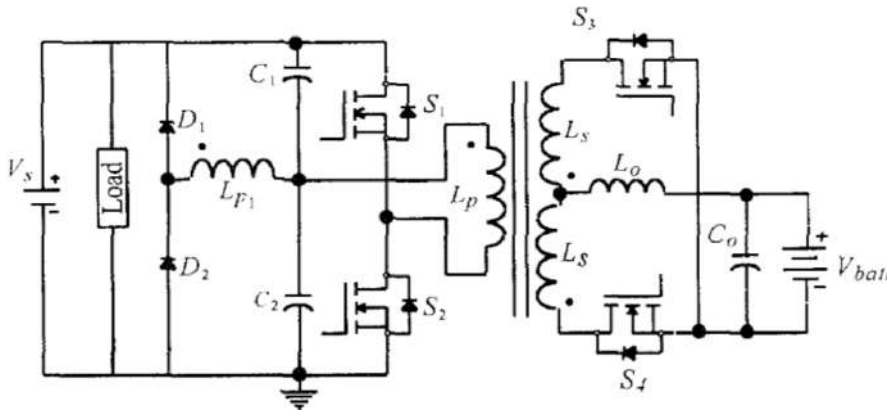
Source: (PENG et al., 2004)

2.2.5.4 Isolated bidirectional DC-DC converter based on the integration of the Half-Bridge and current-fed Push-Pull converts

The converter proposed in (JAIN; DANIELE; JAIN, 2000) presents some advantages such as reduced part count due to power flow in either direction through the same component, low stresses across the switches, galvanic isolation and low ripple current.

Furthermore, Figure 19 shows the converter proposed. The power circuit topology presents a half-bridge converter connected to the DC bus and a current-fed push-pull converter connected to the battery. The converter uses the body diodes of the bidirectional switches for rectification, instead of the usual fast recovery diodes.

Figure 19 – Half-Bridge/Push-Pull Isolated bidirectional DC-DC Converter



Source: (JAIN; DANIELE; JAIN, 2000)

Moreover, the converter have two modes of operation. In the charging mode, the

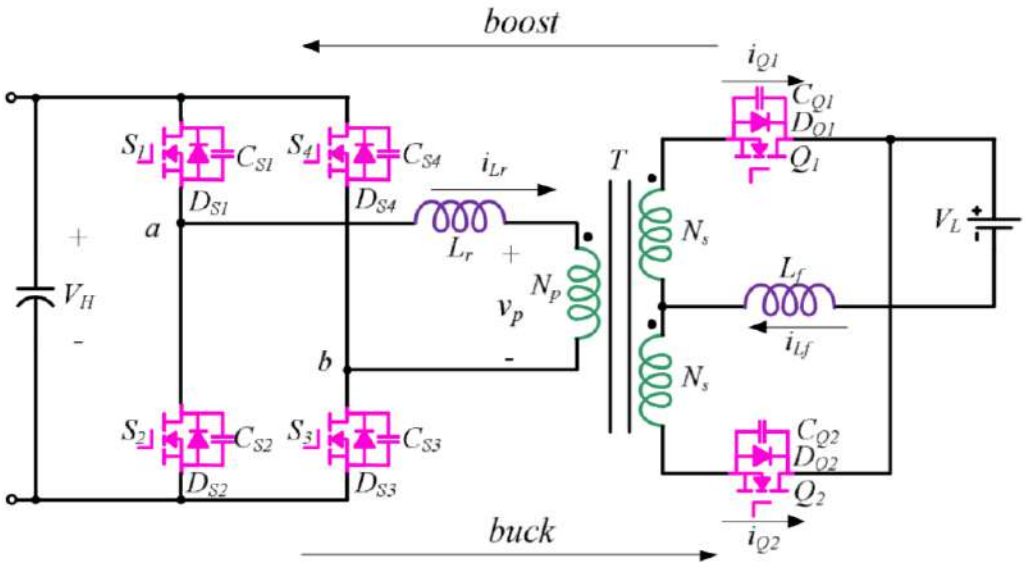
DC bus charges the battery. So, the switches S_1 and S_2 on the half-bridge are gated on and the body diodes of S_2 and S_4 provide load rectification. In the current-fed mode, the battery discharges over the DC bus. Therefore, the switches S_3 and S_4 are gated on and the body diodes of S_1 and S_3 provide rectification.

In addition, the article provides the efficiency curves from experimental setup with a 190 W prototype that presented the maximum efficiency of 90.5% in the current-fed mode and 86.6% in the charging mode.

2.2.5.5 Isolated bidirectional DC-DC converter based on the integration of the Full-Bridge and current-fed Push-Pull converts

There are some publications about the integration of the Full-Bridge Converter with the Current-Fed Push-Pull Converter, such as (DADIALLA; HARDAS, 2017), (INCORPORATED, 2015) and (CHEN et al., 2014). The converter is shown in Figure 20.

Figure 20 – Full-Bridge/Push-Pull Isolated bidirectional DC-DC Converter



Source: (CHEN et al., 2014)

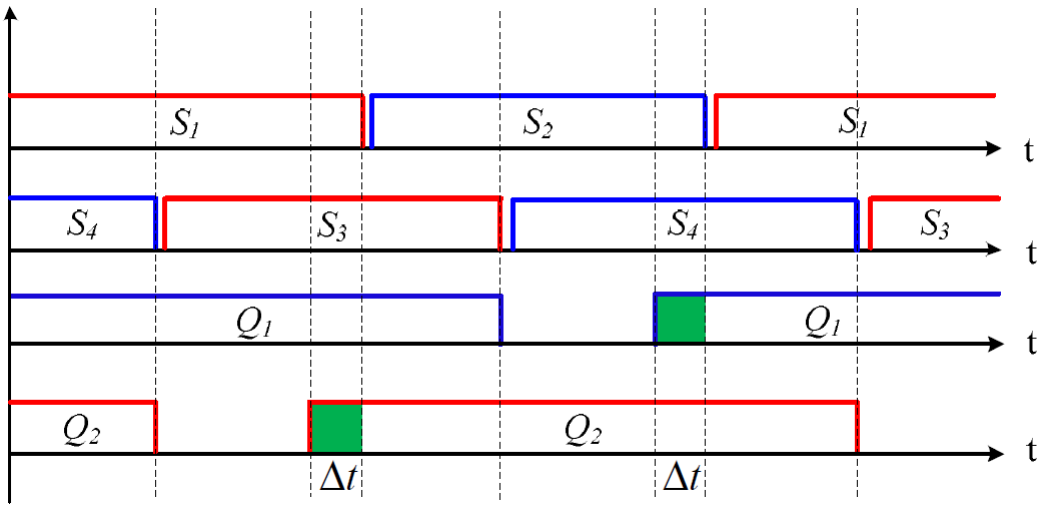
The modulation technique presented in (DADIALLA; HARDAS, 2017) and (INCORPORATED, 2015) is applied to have synchronous rectification in the Push-Pull Stage. In addition, the anti-parallel diodes with the MOSFET in the Full-Bridge Stage is used to provide rectification, when the power flow discharges the battery. In addition, the clamping circuits are dissipative snubber circuits.

Furthermore, the converter proposed in (INCORPORATED, 2015) presents a 300 W prototype from Texas Instruments (TIDM-BIDIR-400-12). Finally, the converter's efficiency was obtained with the maximum of 88% for the buck mode and 80% for the

boost mode. Note that the buck mode represents the battery charging and the boost mode represents the battery discharging.

In addition, the modulation technique proposed in (CHEN et al., 2014) offers a single modulation technique for both the boost and buck mode. The modulation is presented in Figure 21.

Figure 21 – Modulation scheme for Full-Bridge/Push-Pull Isolated bidirectional DC-DC Converter



Source: (CHEN et al., 2014)

The experimental results of the converter implementing the modulation scheme was obtained for a 1kW prototype. Although the author mentioned the reduced spike voltage for the modulation strategy, the converter still needs snubber circuits. Moreover, the efficiency results were not obtained.

2.3 MICROGRID POWER FLOW

The microgrid can present several states according to the variation of the source's generation and load's consumption. So, the study of the power flow will allow to find the microgrid control needs and present an algorithm that can be used in the power management control.

In addition, to study the power flow of the DC microgrid, table 1 compares some pertinent parameters of products sold in the market and the prototype that should be built in this Master Thesis. Some characteristics such as the power rating, the DC and AC bus voltage and the battery ideal state of charge are presented in this table.

Some parameters like the output frequency, battery technology, connection type and technology have been omitted as they are similar for all products, which are 50 or

Table 1 – Technology examples

Company	**Power (kW)**	**DC bus (V)**	**AC bus (V)**	**SoC (%)**
Bosch	5	240-940	230	25-75
Kyocera	4,6	100-600	230	8-88
Tabuchi	5,5	80-600	240	-
SMA	2,5	180-280	230	8-88
TrinaBess	18	250-800	400	5-95
Ingecon	3	300-480	230	-
E-Gear	5	42-58	240	5-95
Panasonic	2	-	230	-
Master Thesis	2	400	220	20-80

Source: Own elaboration

60 Hz, Lithium-ion and single-phase inverters without transformer, respectively. Only the technologies presented in E-Gear and Ingecon feature products with transformer.

2.3.1 DC microgrid

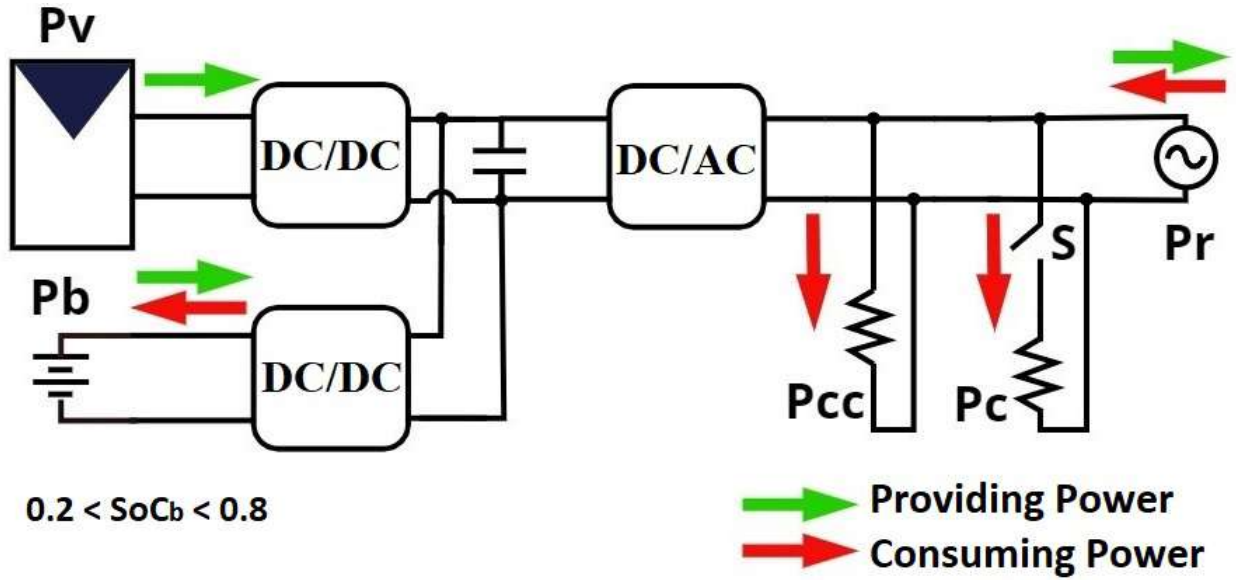
So, to manage the power distribution of the network, the basic techniques used in power systems are the Kirchhoff's law and power balance methods. In general, the power generated must be equal to the power consumed to have a source-load equilibrium. So, the battery bank and the grid may behave as generator or consumer of energy when necessary to stabilize the system.

A DC microgrid can have a power flow as shown in Figure 22, in this configuration the DC bus to battery DC-DC converter and the DC-bus to grid DC-AC inverter must be bidirectional.

Which:

1. P_v is the power generated by photovoltaic modules;
2. P_b is the power stored in the batteries;
3. P_{cc} is the critical local defined by the user that should always be charged, such as lighting circuit;
4. P_c is the local load;
5. P_r is the power grid;
6. S_{on} and S_{off} represent whether the S switch is closed or open, respectively;
7. SoC_b is the battery state charge.

Figure 22 – DC microgrid's power flow



Source: Own elaboration

Some loads could be connected to the DC bus without further analysis, since the DC-AC inverter on this configuration must be bidirectional to keep the DC bus voltage stable.

With the power values obtained through voltage and current sensors, a logical algorithm with all the microgrid's state should be applied the control its power flow. So, to simplify the analysis, the power generated and consumed are represented for positive and negative values, respectively. Additionally, the SoC_b should not be smaller than 0.2 or greater than 0.8 to optimize the battery's lifetime.

The states can occur when only the critical load is connected (S_{off}) or when both loads are being fed (S_{on}). Therefore, when S is open (S_{off}) the microgrid can present a lot of states, so they will be enumerated and explained through a cause and consequence format, as follows:

1. If $P_v = -(P_{cc})$.

   P_v provides power to P_{cc}, P_b remain constant regardless the SoC_b value.

2. If $P_v > -(P_{cc})$ and $SoC_b < 0.8$.

   P_v provides power to P_{cc} and the excess charges the battery (P_b).

   So $P_v = -(P_{cc} + P_b)$.

3. If $P_v > -(P_{cc})$ and $SoC_b > 0.8$.

   P_v provides power to P_{cc} and the excess is transferred to the grid (P_r).

   So $P_v = -(P_{cc} + P_r)$.

4. If $P_v < -(P_{cc})$, $SoC_b < 0.2$.

   P_v and P_r provide power to P_{cc} and P_b.

   So $P_v + P_r = -(P_{cc} + P_b)$.

5. If $P_v < -(P_{cc})$, $SoC_b > 0.2$.

   P_v and P_b provide power to P_{cc}.

   So $P_v + P_b = -(P_{cc})$.

6. If $P_v = 0$, $SoC_b < 0.2$.

   P_r provides power to P_{cc} e P_b.

   So $P_r = -(P_{cc} + P_b)$.

7. if $P_v = 0$, $SoC_b > 0.2$.

   P_b provides power to P_{cc}.

   So $P_b = -(P_{cc})$.

8. If $P_v > -(P_{cc})$, $SoC_b > 0.8$ and $P_r = 0$.

   The unidirectional DC-DC converter leaves the maximum power point and keep the batteries charged, also it is necessary to open the grid's connection through the inverter. If the critical load was connected to the DC bus, it could be fed by the panels and batteries, which is an advantage of the DC microgrid.

   So $P_v + P_b = -(P_{cc})$.

9. If $P_v > -(P_{cc})$, $SoC_b < 0.8$ and $P_r = 0$.

   Open the grid terminal for protection via the DC-AC inverter, leaving the critical load without power. So, the modules charge the battery.

   So $P_v = -(P_b)$.

   However, if the critical load was connected to the DC bus, it could be fed by the panels.

So $P_v = -(P_{cc} + P_b)$.

10. If $P_v < -(P_{cc})$, $SoC_b > 0.8$ and $P_r = 0$.

    Open the grid terminal for protection via the DC-AC inverter, leaving the critical load without power. Also, open the PV modules through the unidirectional DC-DC converter, since there are not a load connected to the system.

    Again, if the critical load was connected to the DC bus, it could be fed by the panels.

    So $P_v + P_b = -(P_{cc})$.

11. If $P_v < -(P_{cc})$, $SoC_b < 0.8$ and $P_r = 0$.

    Open the grid terminal for protection via the DC-AC inverter, leaving the critical load without power.

    So $P_v = -(P_b)$.

    If the critical load was connected to the DC bus, it could be fed through the panels.

    So $P_v = -(P_{cc} + P_b)$.

12. If $P_v = 0$, $0.2 < SoC_b < 0.8$ and $P_r = 0$.

    Leave the critical load without power. If the load was connected on the DC bus, it may be powered by the batteries until their charge state is greater than 20%.

    So $P_b = -(P_{cc})$.

In fact, the DC microgrid should have an autonomy of some hours feeding these loads. At the end of the autonomy the system should shut down until the PV or grid generation is reestablished.

When S is closed (S_{on}) the microgrid has the following states:

1. If $P_v = -(P_{cc} + P_c)$.

   P_v provides power to P_{cc} and P_c while P_b remain constant regardless the SoC_b value.

2. If $P_v > -(P_{cc} + P_c)$ and $SoC_b < 0.8$.

   P_v provides power to P_{cc}, P_c and the excess charges the battery (P_b).

   So $P_v = -(P_{cc} + P_c + P_b)$.

3. If $P_v > -(P_{cc} + P_c)$ and $SoC_b > 0.8$.

   P_v provides power to P_{cc}, P_c and the excess is transferred to the grid (P_r).

   So $P_v = -(P_{cc} + P_c + P_r)$.

4. If $P_v < -(P_{cc} + P_c)$, $SoC_b < 0.2$.

   P_v e P_r provide power to P_{cc}, P_c and P_b.

   So $P_v + P_r = -(P_{cc} + P_c + P_b)$.

5. If $P_v < -(P_{cc} + P_c)$, $SoC_b > 0.2$.

   P_v e P_b provide power to P_{cc} and P_c.

   So $P_v + P_b = -(P_{cc} + P_c)$.

6. If $P_v = 0$, $SoC_b < 0.2$.

   P_r provides power to P_{cc}, P_c and P_b.

   So $P_r = -(P_{cc} + P_c + P_b)$.

7. If $P_v = 0$, $SoC_b > 0.2$.

   P_b provides power to P_{cc} and P_c.

   So $P_b = -(P_{cc} + P_c)$.

8. If $P_v > -(P_{cc} + P_c)$, $SoC_b > 0.8$ and $P_r = 0$.

   The unidirectional DC-DC converter leaves the maximum power point and keep the batteries charged, also it is necessary to open the grid terminal for protection via the DC-AC inverter.

   If the critical load was connected to the DC bus, it could be fed through the panels and batteries.

   So $P_v + P_b = -(P_{cc} + P_c)$.

9. If $P_v > -(P_{cc} + P_c)$, $SoC_b < 0.8$ and $P_r = 0$.

   Open the grid terminal for protection via the DC-AC inverter, leaving the load without power.

   So $P_v = -(P_b)$.

If the load was connected to the DC bus, it could be fed through the panels.

So $P_v = -(P_{cc} + P_c + P_b)$.

10. If $P_v < -(P_{cc} + P_c)$, $SoC_b > 0.8$ and $P_r = 0$.

    Open the grid terminal for protection via the DC-AC inverter, leaving the load without power. Also, open the PV modules through the unidirectional DC-DC converter, since there are not a load connected to the system.

    If the load was connected to the DC bus, it could be fed through the panels and batteries.

    So $P_v + P_b = -(P_{cc} + P_c)$.

11. If $P_v < -(P_{cc} + P_c)$, $SoC_b < 0.8$ and $P_r = 0$.

    Open the grid terminal for protection via the DC-AC inverter, leaving the load without power.

    So $P_v = -(P_b)$.

    If the load was connected to the DC bus, it could be fed through the panels.

    So $P_v = -(P_{cc} + P_c + P_b)$.

12. If $P_v = 0$, $0.2 < SoC_b < 0.8$ and $P_r = 0$.

    Leave the critical load without power.

    If the load was connected on the DC bus, it may be powered by the batteries until their charge state is greater than 20%.

    So $P_b = -(P_{cc} + P_c)$.

The system would have an autonomy of some hours feeding these loads. At the end of the autonomy the system would shut down until the PV or grid generation is reestablished.

So, it is possible to observe a great advantage about DC systems that the loads are connected in the DC bus, the loads will always be fed regardless of a power outage of the distribution grid or a null generation of photovoltaic modules, since the batteries have a sufficient state of charge ($SoC_b > 0.2$). So, a well designed battery bank project would offer a stable microgrid operation for any case above with a designed time.

2.4 MICROGRID CONTROL

A well-know concept in the literature is that renewable energy sources such as photovoltaic modules can be used to increase the power system supply. For example, it can lower the peak of the power curve at high power load demands, since the energy will be more distributed.

Thus, energy storage systems become an interesting solution for grid connected applications, especially in conjunction with renewable sources. The system may include some battery banks or other storage devices to store and supply energy at the right time.

The proposed microgrid consists in a connection of photovoltaic modules, BESS, loads and grid into a single DC bus, so a literature review about its control is required to have a stable system. For instance, it is described by (CUTRIGHT et al., 2018) that microgrids require a power flow control method that observes the power generation, consumption and the batteries' state of charge.

Most of the microgrid's controls are already described in patents and articles, so they can be organized as follows:

- Unidirectional DC-DC converter MPPT algorithm;
- Bidirectional DC-AC converter PLL and anti-islanding method;
- DC bus voltage control;
- Battery SoC and equipotentialization control;
- Power flow management control;

As presented by (CUTRIGHT et al., 2018), the microgrid control system should be conFigured to categorize and prioritize the system's power demands, ensuring power availability with effective control of battery state of charge. This control logic can have several modes of operation and variables, as described in the microgrid power flow section. Typically, the device responsible for the power balance is the storage system. Normally, the BESS is accompanied by a control system called BMS to check the charge state of the batteries, provide protection when the operation is not safe, control variables such as temperature and other functions.

Therefore, a literature review of the main control techniques used for managing the microgrid will be presented, as the connection of nonlinear and intermittent sources can cause a problem in the distribution of electricity. So, some control techniques such as droop, optimized, hierarchical and central-unit power flow will be presented as alternative ways to control the DC microgrid (SUAREZ SOLANO et al., 2015).

2.4.1 Droop control

There are several publications in the literature, such as (SHUVRA; CHOWDHURY, 2017), (SUCH; MASADA, 2017), (HAN, 2016) and (GUERRERO; HANG; UCEDA ANTOLÍN, 2008), as well as patents like (HOLVECK; KOCHEROV, 2018) that use droop to control the power between sources, grid and BESS. This concept is well-known in power systems and used in technologies such as voltage regulators.

The main constraints in controlling this type of system is ensuring a similar distribution between storage units to keep their charge states equal, and making power distribution to the load without supervising all batteries.

This control technique is also interesting to stabilize the DC bus voltage by varying the configurable coefficients when the power changes, so it is possible to maintain a constant voltage.

Furthermore, the patent (CHOI; LEE, 2017) uses droop control to charge and discharge a BESS, observing its SoC. Similarly, the control of patent (CUTRIGHT et al., 2018) observes the power demand of the system to control the batteries. Thus, in these patents the apparent power stored in the batteries is controlled by the slope in the curves of the grid's frequency and voltage variation. However, their control seems to fit an AC microgrid, since they need a voltage and frequency references.

In addition, droop control can also be used to maintain the DC bus voltage ripple low, according to the work proposed by (SUZAN et al., 2018). This article uses droop to control the DC bus voltage ripple of an inverter connected to the grid. So, the power is balanced between them. Furthermore, a capacitor bank is necessary to connect the DC bus on the grid, this capacitor inserts a slow dynamic into the system which increases the stability.

2.4.2 Optimized power flow control

In addition, there are some controls that uses mathematical equations to find the ideal operating point for the system power flow, publications such as (JIAN; YUTIAN; GUANNAN, 2016), (MASSIGNAN; MACHADO; BOSCO, 2016), (XIA et al., 2015) and (BUDH; VIRULKAR, 2014) shows some of this methods. For instance, in (BUDH; VIRULKAR, 2014) the author uses a stochastic technique called Dynamic active-reactive optimal power flow (DAROPF) to find the optimal point of system power transfer for time periods.

Stochastic models to solve this kind of problem are very implemented in the field of power systems to find the optimal power flow. This type of control, as shown by (JIAN; YUTIAN; GUANNAN, 2016), requires to model and study the microgrid power flow, so needs a method such as Newton-Raphson.

2.4.3 Hierarchical control system

The hierarchical control has at least two levels that are implemented by its importance, as shown in (SUAREZ SOLANO et al., 2015). This control system is well-known to connect voltage sources in a bus, as represented in (GIRARD; PAPPAS, 2007).

The hierarchy of the system studied in (GUAN et al., 2015) is basically control the output voltage and current of each source that is connected to the DC bus, synchronize the system with the grid through an AC/DC inverter and control the system's power flow. Meanwhile, in the reference (HE et al., 2013), the major priority is given to the synchrony and then the source's output voltage and current control

In conclusion, this control method is very interesting to a reliable microgrid, since the microgrid has a lot of control variables and all these would be organized with different priority levels.

2.4.4 Central unit control system

In the publications (GUI et al., 2015) and (OLALLA et al., 2013), the decisions are made by a controller in a central processing unit.

In general, this unit controls all converters and inverters to add or remove sources and load to keep the voltage stable and the system's power sharing. Similar to optimized power flow control, this control requires an equivalent circuit each system's operations as specified in the Power flow section.

In addition, these central units can be Flexible Alternating Current Transmission System (FACTS) devices, such as a Unified power flow controller (UPFC), a Static synchronous compensator (STATCOM) or a Static VAR compensator (SVC) as shown by (XU et al., 2017).

2.4.5 Other control methods

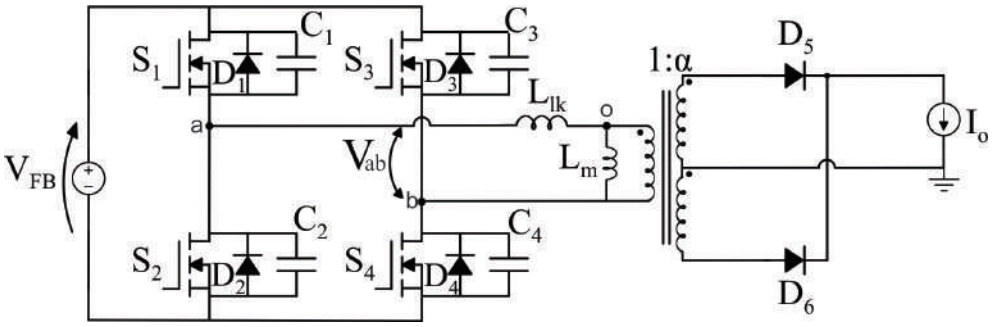
Control is a specific need of each system, and there may be several solutions to the same problem. The methods cited for controlling the microgrid are not the only ways to keep it stable. There are studies such as the harmonic detection control (KUMAR; SINGH, 2017), the peak shaving control (WANG; ZARGHAMI; VAZIRI, 2016) and the hysteresis current control (SUBRAMANYAM; VYJAYANTHI, 2016) that may solve the problem of the microgrid's power sharing.

3 STUDY OF THE DC-DC FULL-BRIDGE ZVS-PWM STAGE

The development of an Isolated Bidirectional DC-DC Converter is necessary to do the power management of the DC microgrid, as studied in the state of the art. Thus, to understand the bidirectional converter proposed in this Master Thesis, it is first necessary to understand each converter stage separately, which will be divided in two stages. Further, the first power stage that is called Full-bridge ZVS-PWM Stage will be used to perform the bidirectional converter.

Therefore, this chapter is an study review of the unidirectional topology known in the literature as Full-Bridge ZVS-PWM converter (BARBI; PÖTTKER, 2019), which Zero Voltage Switching (ZVS) means Zero Voltage Switching and PWM means Pulse-Width-Modulation. The circuit represented in figure 23 is modulated in order to have three voltage levels in V_{ab} and it is connected to a diode bridge in the secondary side. Both sides are isolated galvanically by a high frequency transformer.

Figure 23 – Isolated unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

The major reference for writing this chapter is the book (BARBI; PÖTTKER, 2019) from Professor Dr. Ivo Barbi and Professor Dr. Fabiana Pottker. Furthermore, the converter presents some characteristics, such as:

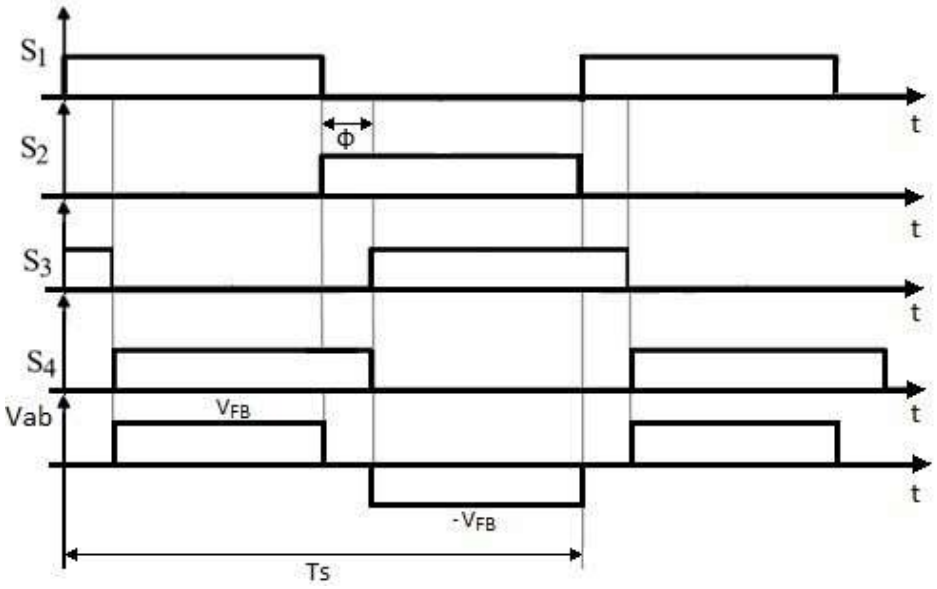
- Voltage input;
- Current output;
- Galvanic isolation between the primary and secondary side of the transformer;

3.1 GATE SIGNALS

In order to understand the operation steps of the mentioned converter, it is necessary to visualize the gate signals of each switch. Thus, as can be seen in figure 24, the control signals of each leg are complementary and consequently the voltage in

the primary side of the transformer (V_{ab}) and the power transferred to the load can be controlled by the lag between the command signals of the lags (ϕ).

Figure 24 – Gate Signals of the switches and Voltage V_{ab}



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

In pulse width modulation the switching frequency is set and the switches of each leg have a duty cycle of 50%. In addition lagging leg is triggered with a lag angle (ϕ) in relation to the leading leg, in order to transfer the power. Therefore, the angle ϕ can vary from 0º to 180º, representing the maximum and zero power transferred to the load.

3.2 CIRCUIT OPERATION

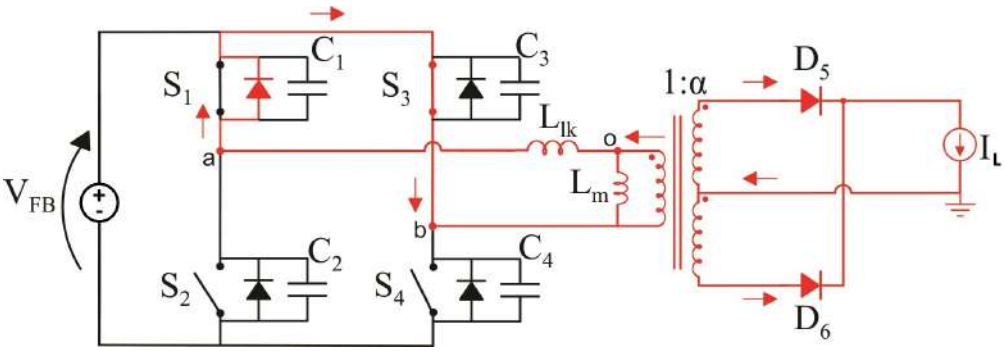
In this first analysis, the converter will be studied with hard switching, so there is still no dead-time between the gate signals of the switches in the same lag.

The transformer leakage inductance (L_{lk}) will be considered. In the next analysis, this inductance will resonate with the capacitors in parallel with the switches in order to realize soft commutation of the switches. Furthermore, other components are considered ideal.

Time interval Δt_1 - At time t_0 the topological state of the converter is represented by figure 25. The current source, which represents the load, is short-circuited by the output rectifier diodes. The current of the leakage inductance L_{lk} circulates through S_3 and D_1.

Time interval Δt_2 - During this time interval, the switch S_4 is turned on and the switch S_3 is turned off, as shown in figure 26. Since the current in the inductor L_{lk}

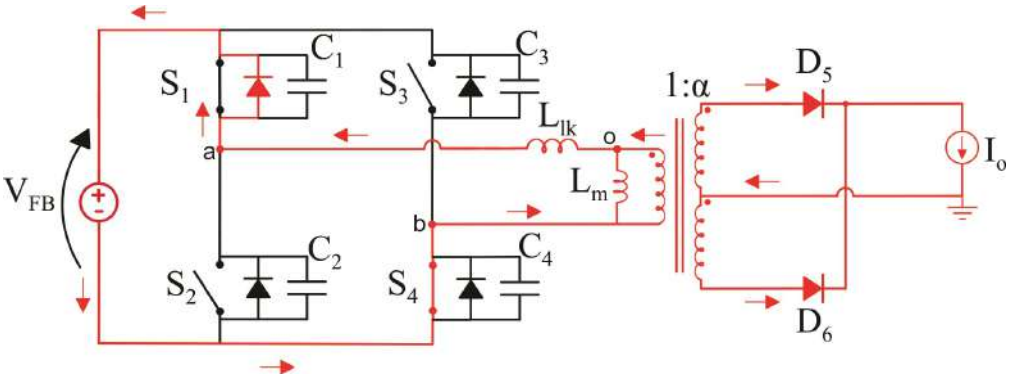
Figure 25 – Topological state of the first stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

remains negative due to the previous step, the current flows through the diodes S_1 and D_4, also it increases linearly until it becomes zero. In this step $V_{ab} = V_{Llk} = V_{FB}$ and the output is short-circuited.

Figure 26 – Topological state of the second stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



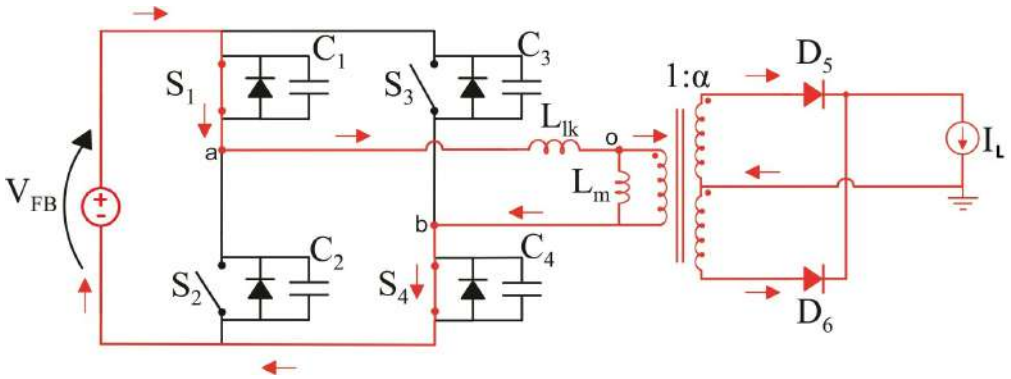
Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Time interval Δt_3 - The topological state representing the third stage of operation is shown in figure 27. This state begins at t_2, when the current in the inductor L_{lk} is fully demagnetized, so it reverses the polarization of the diodes D_1 and D_4.

Also, in this time interval the switches S_1 and S_4 turn on, so they start to drive current in the inductor L_{lk} which increases linearly. Furthermore, $V_{ab} = V_{Llk} = V_{FB}$ and the rectifier is short-circuited.

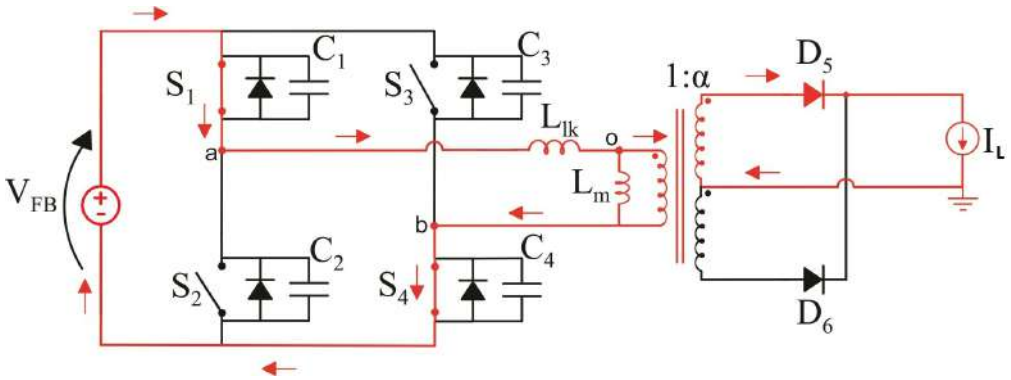
Time interval Δt_4 - The fourth step of operation that starts at $t = t_3$ is shown in figure 28. It begins when the current of the inductor L_{lk} reaches the current of the output I_L reflected to the primary side of the transformer. Since $V_{ab} = V_{FB}$, the diode D_5 is directly polarized and the power is transferred to the load.

Figure 27 – Topological state of the third stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 28 – Topological state of the fourth stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Time interval Δt_5 - The fifth step of operation starts when $t = t_4$, which can be seen in figure 29. During this stage, the switch S_2 is triggered and S_1 is turned off.

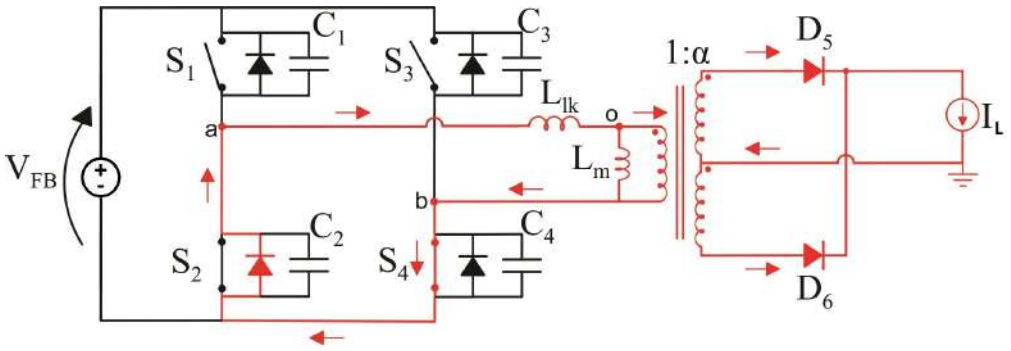
Hence, the output current source is short-circuited in the secondary side of the transformer. Furthermore, the voltage V_{ab} is equals to zero and the current in the inductor L_{lk} flows through the diode D_2 and the switch S_4.

Time interval Δt_6 - The topological state that represents the sixth step of operation is shown in figure 30. It starts at $t = t_5$, when S_3 is gated and S_4 is switched off.

As the current in the inductor stays positive, it flows through diodes D_2 and D_3. Also its value is decreasing linearly from the maximum to zero. In addition, the voltage $V_{ab} = V_{Llk} = -V_{FB}$ and the output is short-circuited.

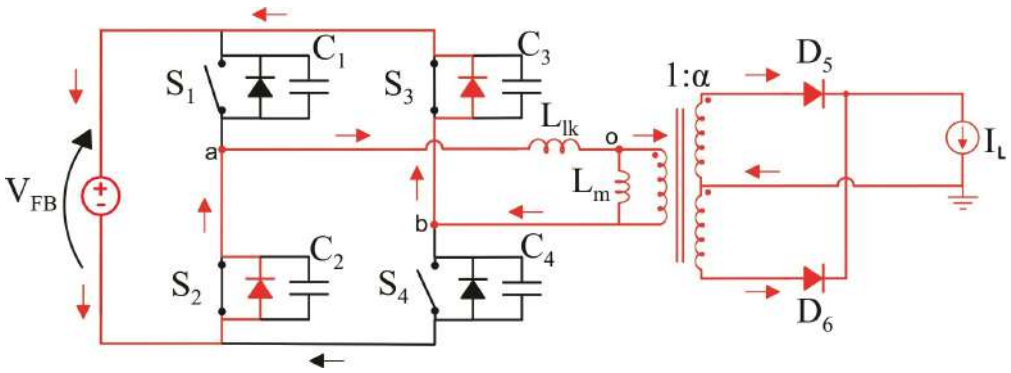
Time interval Δt_7 - The topological state shown in figure 31 represents the

Figure 29 – Topological state of the fifth stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 30 – Topological state of the sixth stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

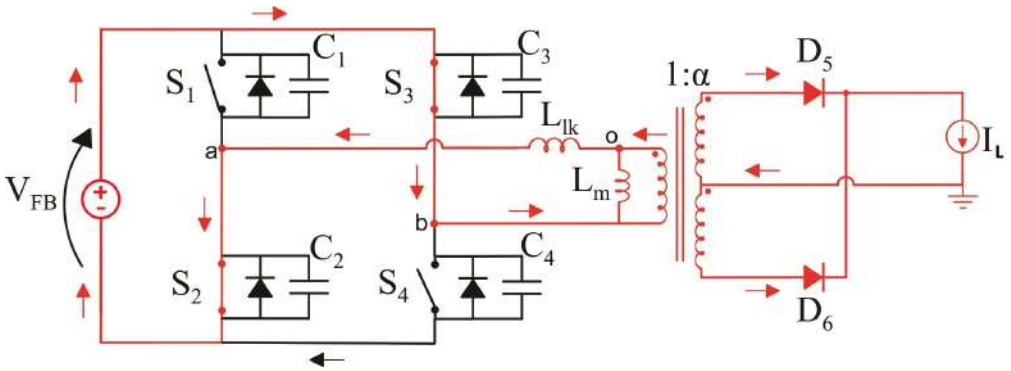
seventh stage of operation. It begins at $t = t_6$ when the current in the inductor L_{lk} is equal to zero.

Therefore, the current that was flowing through the diodes D_2 and D_3 in the previous time interval flows through the switches S_2 and S_3, while the current in the inductor decreases linearly until it reaches the maximum negative value. In addition, during this step $V_{ab} = V_{Llk} = -V_{FB}$ and the output is short-circuited.

Time interval Δt_8 - The eighth step of operation that begins at $t = t_7$ is represented by Figure 32. This stage begins when the current in the inductor L_{lk} reaches the maximum output current's value reflected to the primary ($I_{lk} = \alpha I_L$).

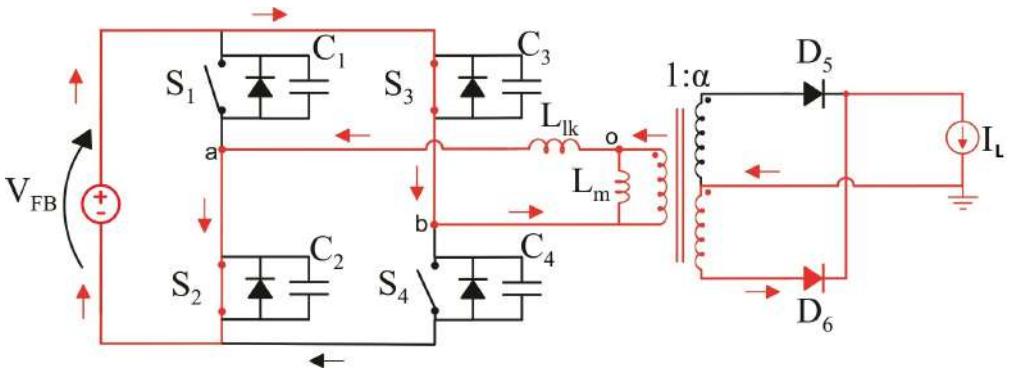
Since the voltage $V_{ab} = -V_{FB}$, the rectifier is no longer short-circuited because and the diode D_6 is directly polarized, so the power is transferred to the load.

Figure 31 – Topological state of the seventh stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 32 – Topological state of the eighth stage of operation of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

3.2.1 Waveforms

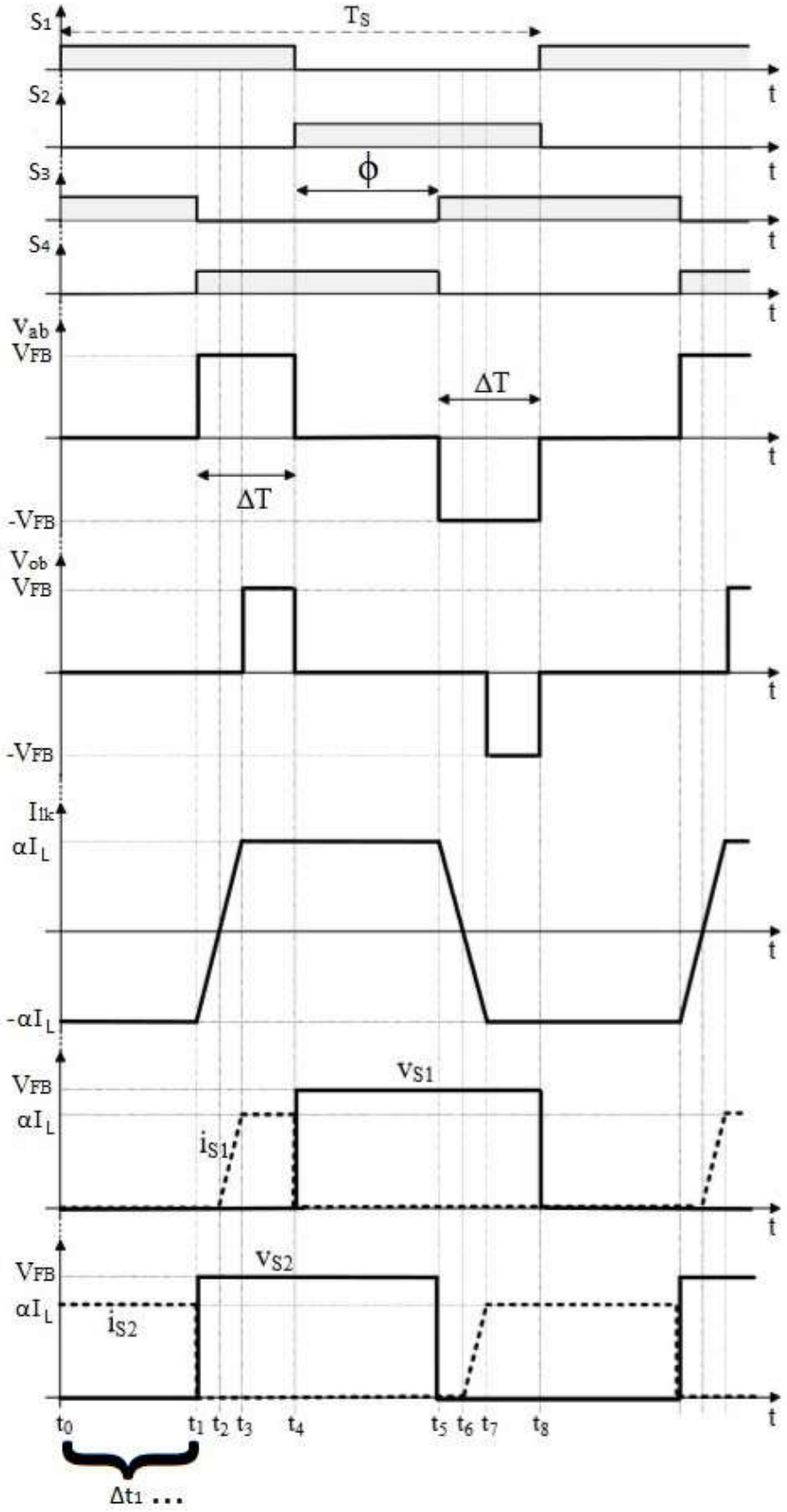
With the topological states defined, the main waveforms of the converter are shown in figure 33.

3.3 COMMUTATION ANALYSIS

In this analysis, the capacitors are added in parallel with the full-bridge switches and a dead-time is introduced between the gate signals of the switches of the legs. Thus, soft commutation can be achieved with four more time intervals for each switching period (T_s). In addition, the mathematical analysis of the capacitance and dead-time necessary to perform a zero-voltage-switching will be performed later.

In the complete full-bridge converter, the inductor L_{lk} provides energy to charge and discharge the switching capacitors at the interval that commutation occurs. Thus,

Figure 33 – Main waveforms of the unidirectional DC-DC Full-Bridge ZVS-PWM converter



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

they can be fully discharged, causing the antiparallel diodes to conduct current before the dead-time finishes. Therefore, for light load conditions, soft commutation may not be achieved as there may not be enough energy stored in the inductor L_{lk} to charge and discharge the capacitors.

So, in order to extend the operating range of the soft switching, the inductance L_{lk} must be increased. However, a large inductance increases the reactive energy circulating in the converter, decreasing its efficiency due to conduction losses and increasing its weight and volume.

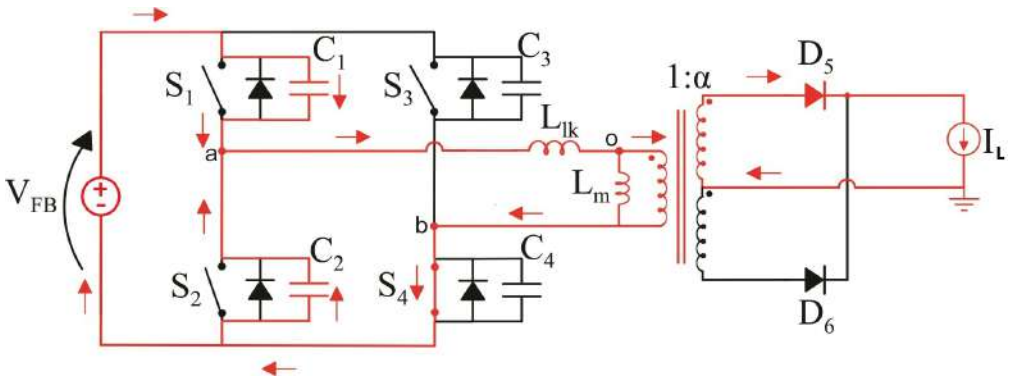
Finally, the converter presents twelve topological states which eight of them are the same as it was presented in this chapter.

3.3.1 Leading leg commutation

The leading leg, composed of S_1 and S_2, switches its states when the secondary output is not short-circuited, then the output current charges and discharges the capacitors of the switches with a linear waveform.

Figure 34 illustrates the switching interval that occurs between periods t_4 and t_5, when switch S_1 is switched off and S_2 is not yet switched on. So, the current in the inductor L_{lk} is equal to the output current's value reflected to the primary side (αI_L) and half of the current flows through each capacitor, charging C_1 from 0 to V_{FB} and discharging C_2 from V_{FB} to 0.

Figure 34 – Topological state of the dead-time implemented when S_1 turns off and S_2 turns on.

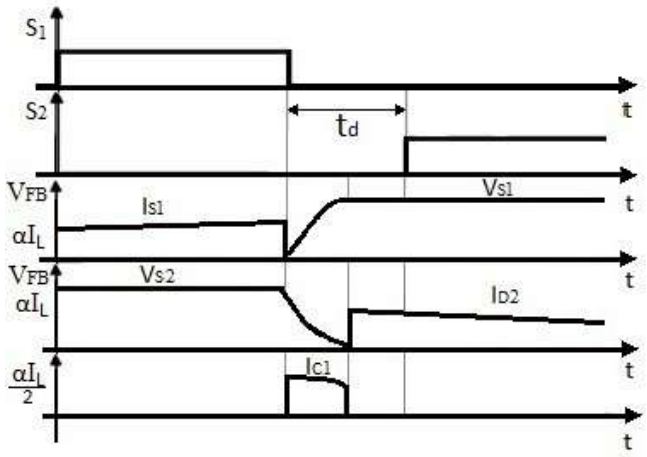


Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

In addition, it can be seen in the waveforms of figure 35 that when the capacitor C_2 is fully discharged, the diode D_2 begins to conduct together with the switch S_4.

Figure 36 illustrates the time interval between periods t_8 and t_1 when S_2 is switched off and S_1 is not yet switched on. Hence, the current in the inductor L_{lk} is equal to the negative output current's value reflected to the primary side ($-\alpha I_L$) and half of

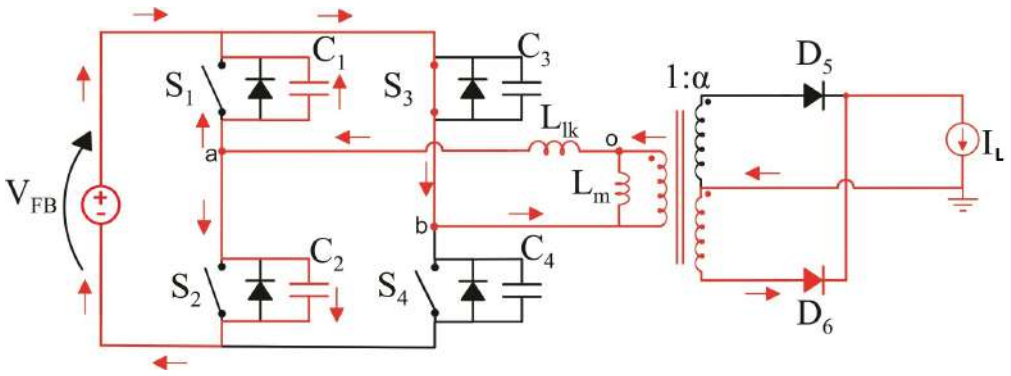
Figure 35 – Main waveforms of the converter with the dead-time implemented when S_1 turns off and S_2 turns on.



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

the current flows through each capacitor, charging C_2 from 0 to V_{FB} and discharging C_1 from V_{FB} to 0.

Figure 36 – Topological state of the dead-time implemented when S_1 turns on and S_2 turns off.

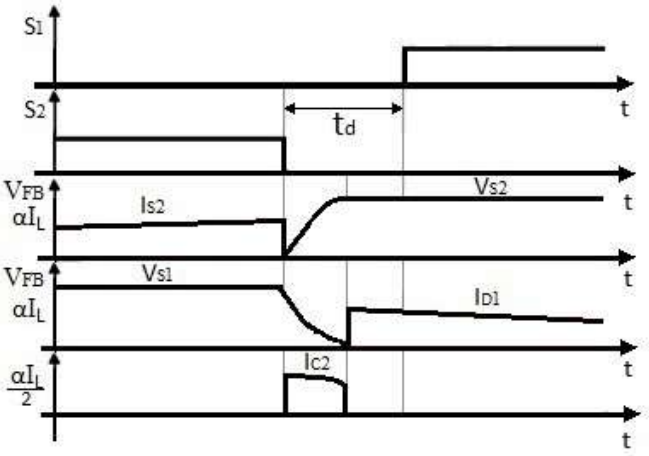


Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

In addition, it can be seen in the waveforms of figure 37 that when the capacitor C_1 is fully discharged, the diode D_1 starts to conduct together with the switch S_3.

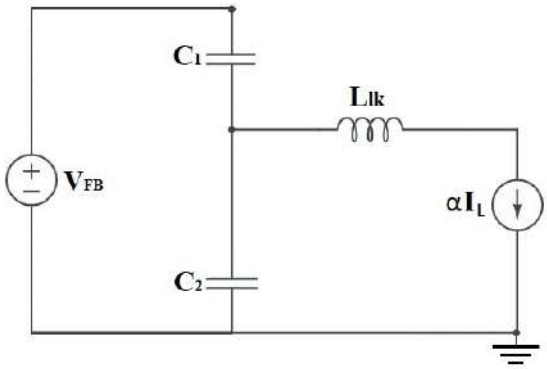
Therefore, it is noticed that the commutation of these switches always occurs when there is a output current present in the circuit, as shown in the equivalent circuit of figure 38. Furthermore, the two commutation periods of this leg have the same equivalent circuit, changing only the direction of the current in each one.

Figure 37 – Main waveforms of the converter with the dead-time implemented when S_1 turns on and S_2 turns off.



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 38 – Equivalent circuit of the leading leg commutation



Source: Own elaboration

Thus, the initial conditions of the circuit is given by the expressions 3, 4 and 5.

$$V_{C1}(0) = 0 \tag{3}$$

$$V_{C2}(0) = V_{FB} \tag{4}$$

$$I_{lk}(0) = \alpha I_L \tag{5}$$

From the equivalent circuit, equations 6 and 7 could be found:

$$\alpha I_L = I_{C1}(t) + I_{C2} \tag{6}$$

$$V_{FB} = V_{C1}(t) + V_{C2} \tag{7}$$

In addition, the currents in the capacitors are defined as:

$$I_{C1}(t) = C_1 \frac{dV_{C1}(t)}{dt} \tag{8}$$

$$I_{C2}(t) = C_2 \frac{dV_{C2}(t)}{dt} \tag{9}$$

Substituting equations 8 and 9 into 6 gives 10.

$$\alpha I_L = C_1 \frac{dV_{C1}(t)}{dt} + C_2 \frac{dV_{C2}(t)}{dt} \tag{10}$$

Since the capacitances are equal to each other, the equation 10 can be rewritten to obtain equation 11.

$$\alpha I_L = 2C \frac{dV_{C1}(t)}{dt} \tag{11}$$

Applying the Laplace transform in equation 11 equations 12 and 13 are obtained.

$$\frac{\alpha I_L}{s} = 2CsV_{C1}(s) \tag{12}$$

$$V_{C1}(s) = \frac{\alpha I_L}{s^2 2C} \tag{13}$$

Applying the inverse Laplace transform in equation 13 gives the expression 14.

$$V_{C1}(t) = \frac{\alpha I_L}{2C} t \tag{14}$$

Thus, by isolating the time in the equation 14 and considering that the capacitor's voltage is equal to the input voltage, equation 15, which represents the minimum dead-time to guarantee ZVS in the leading leg, can be obtained.

$$t_d \geq \frac{2CV_{FB}}{\alpha I_L} \tag{15}$$

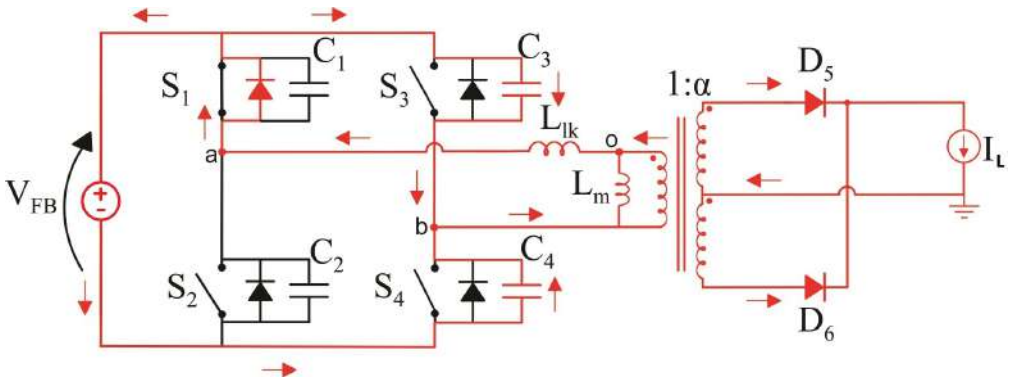
3.3.2 Lagging leg commutation

The lagging leg (S_3 and S_4) change its states when the secondary output is short-circuited, so the charge and discharge of the capacitors in parallel with the switches happens in a resonant way. This leg has a more critical commutation, because only the energy stored in the inductor L_{lk} is available to charge and discharge of the capacitors.

Figure 39 illustrates the time interval between periods t_1 and t_2, when switch S_3 is off and S_4 is not yet switched on. Then, the current in the inductor L_{lk} is equals to the negative output current's value reflected to the primary side ($-\alpha I_L$) and half of the

current flows through each capacitor. Thus, this current charges C_3 from 0 to V_{FB} and discharges C_4 from V_{FB} to 0.

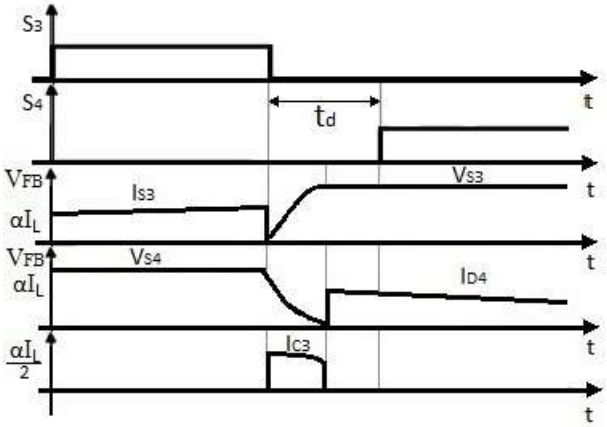
Figure 39 – Topological state of the dead-time implemented when S_3 turns off and S_4 turns on.



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

In addition, it can be seen in the waveforms of figure 40 that when the capacitor C_4 is fully discharged, the diode D_4 begins to conduct together with the switch S_1.

Figure 40 – Main waveforms of the converter with the dead-time implemented when S_3 turns off and S_4 turns on.

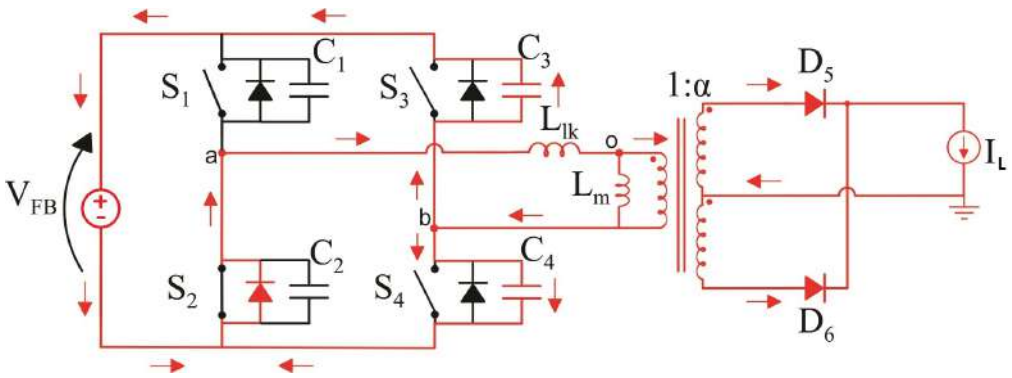


Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 41 illustrates the time interval between instants t_5 and t_6, when switch S_4 is switched off and S_3 is not yet switched on. Therefore, the current in the inductor L_{lk} is equals to the negative output current's value reflected to the primary side ($-\alpha I_L$) and half of the current flows through each capacitor, so it charges C_4 from 0 to V_{FB} and discharges C_3 from V_{FB} to 0.

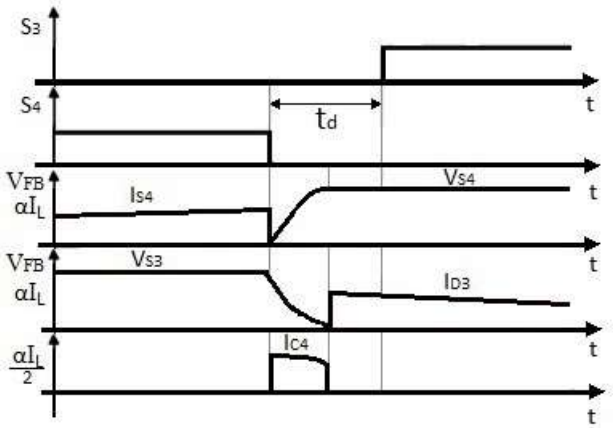
In addition, it can be seen in the waveforms of figure 42 that when the capacitor C_3 is fully discharged, the diode D_3 begins to conduct together with the switch S_2.

Figure 41 – Topological state of the dead-time implemented when S_3 turns on and S_4 turns off.



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

Figure 42 – Main waveforms of the converter with the dead-time implemented when S_3 turns on and S_4 turns off.



Source: Own elaboration based on (BARBI; PÖTTKER, 2019)

The main difference in this leg is that the rectifier is short-circuited, so the only available energy to charge and discharge the capacitors is that stored in the inductor L_{lk}, as shown in the equivalent circuit of figure 43.

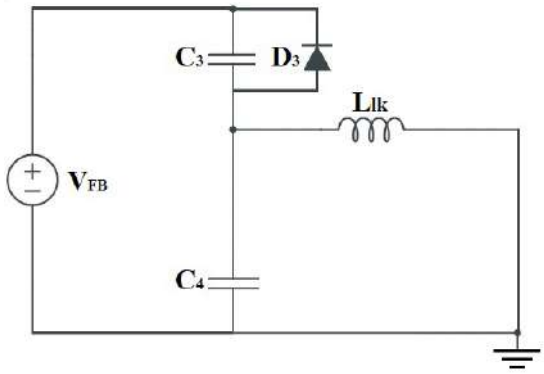
Although the current direction and the diode that will be polarized at the end of this step are different, the analysis can be done for only one of these steps.

The initial conditions of the equivalent circuit shown in figure 43 are given by equations 16, 17 and 18.

$$V_{C3}(0) = 0 \tag{16}$$

$$V_{C4}(0) = V_{FB} \tag{17}$$

Figure 43 – Equivalent circuit of the lagging leg commutation



Source: Own elaboration

$$I_{lk}(0) = \alpha I_L \tag{18}$$

From the electric circuit the following equations can be obtained:

$$I_{lk}(t) = I_{C3}(t) + I_{C4}(t) \tag{19}$$

$$L_{lk}\frac{dI_{lk}(t)}{dt} + V_{C3}(t) - V_{FB} = 0 \tag{20}$$

$$V_{FB} = V_{C3}(t) + V_{C4}(t) \tag{21}$$

Besides, the current in the capacitors can be defined as:

$$I_{C3}(t) = C_3\frac{dV_{C3}(t)}{dt} \tag{22}$$

$$I_{C4}(t) = C_4\frac{dV_{C4}(t)}{dt} \tag{23}$$

By substituting equations 22 and 23 in equation 19, 24 is obtained.

$$I_{lk}(t) = C_3\frac{dV_{C3}(t)}{dt} + C_4\frac{dV_{C4}(t)}{dt} \tag{24}$$

As the capacitances are equal, equation 24 can be rewritten to obtain 25.

$$I_{lk}(t) = 2C\frac{dV_{C3}(t)}{dt} \tag{25}$$

Applying Laplace transform in the equations 25 and 20, equations 26 and 27 are found.

$$I_{lk}(s) = 2sCV_{C3}(s) \tag{26}$$

$$sL_{lk}I_{lk}(s) - L_{lk}\alpha I_L + V_{C3}(s) = 0 \tag{27}$$

If the equation 26 is replaced in 27, 28 can be found.

$$V_{C3}(s)(s^2 2L_{lk}C + 1) = L_{lk}\alpha I_L \tag{28}$$

If the equation 29 is replaced in 28, 30 is obtained.

$$\omega_o = \frac{1}{\sqrt{2L_{lk}C}} \tag{29}$$

$$V_{C3}(s) = L_{lk}\omega_o^2 \frac{\alpha I_L}{(s^2 + \omega_o^2)} \tag{30}$$

The expression 32 is found by replacing the equation 31 into 30 and applying the inverse Laplace transform.

$$z = \sqrt{\frac{L_{lk}}{2C}} \tag{31}$$

$$V_c\,(t) = z\alpha I_L sen\,(\omega_o t) \tag{32}$$

Finally, by replacing the equation 32 in 25, the expression 33 that represents the current of the inductor is found.

$$I_{lk}\,(t) = \alpha I_L cos\,(\omega_o t) \tag{33}$$

In order to find the critical time to have ZVS in the lagging leg, the state plane trajectory that represents the topological state can be used as a tool, as shown in figure 44.

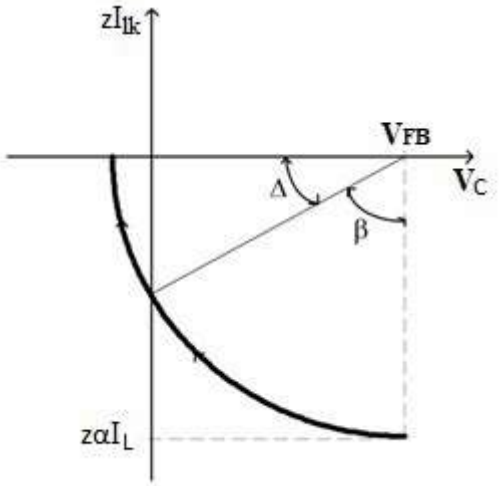
The center of the circle is at (V_{FB}, 0) and the initial current is $-z\alpha I_L$. Thus, the capacitor is resonantly discharged within the angle β. When the trajectory reaches the angle Δ, the voltage in the capacitor is null and the diode starts to conduct in a linear way, causing the remaining current of the inductor to discharge into the power source. Therefore, to ensure soft commutation, the circle has to intercept the y-axis, so the equation 34 is valid.

$$z\alpha I_L \geq V_{FB} \tag{34}$$

If the terms of equations 34 are rearranged, 35 is found.

$$\alpha I_L \geq \sqrt{\frac{2C}{L_{lk}}} V_{FB} \tag{35}$$

Figure 44 – State plane trajectory that represents the equivalent circuit



Source: Own elaboration

Furthermore, as it can be understood from figure 44:

$$\beta + \Delta = \frac{\pi}{2} \tag{36}$$

The time interval that commutation occurs is defined by equation 37.

$$\Delta t = \frac{\beta}{\omega} \tag{37}$$

After some algebraic manipulation the equation 38 is found.

$$\Delta t = \left(\frac{\pi}{2} - \Delta\right) \sqrt{2CL_{lk}} \tag{38}$$

The angle Δ is defined by the expression 39:

$$\Delta = \cos^{-1}\left(\frac{V_{FB}}{\alpha I_L}\sqrt{\frac{2C}{L_{lk}}}\right) \tag{39}$$

Substituting equation 39 in 38 gives 40 which represents the minimum dead-time needed to guarantee soft commutation with a Zero-Voltage-Switching.

$$\Delta t = \left[\frac{\pi}{2} - \cos^{-1}\left(\frac{V_{FB}}{\alpha I_L}\sqrt{\frac{2C}{L_{lk}}}\right)\right] \sqrt{2CL_{lk}} \tag{40}$$

3.4 OUTPUT CHARACTERISTICS

In this analysis, the commutation intervals are disregarded, since they are very small with respect to the other intervals. In addition, the current in the inductor will be considered constant.

Since the converter is symmetrical in a switching period and according to figure 33, the following time intervals are equal: $\Delta t_1 = \Delta t_5$, $\Delta t_2 = \Delta t_6$ and $\Delta t_3 = \Delta t_7$.

In addition, the time interval which V_{ab}=$\pm V_{FB}$ is defined as ΔT, thus the equations 41 and 42 can be written.

$$\Delta T = \Delta t_2 + \Delta t_3 + \Delta t_4 = \Delta t_6 + \Delta t_7 + \Delta t_8 \tag{41}$$

$$\frac{T_S}{2} = \Delta T + \Delta t_5 \tag{42}$$

Moreover, the duty cycle is defined by the expression 43:

$$D = \frac{2\Delta T}{T_S} \tag{43}$$

The current in the inductor L_{lk} evolves linearly in the time intervals Δt_2, Δt_3, Δt_6 and Δt_7, so the output rectifier diodes are short-circuited and the output voltage is zero. Then, the power is transferred to the load only in time intervals Δt_4 and Δt_8.

Furthermore, the effective duty cycle is defined as equation 44

$$D_{ef} = \frac{2\Delta t_4}{T_S} \tag{44}$$

The time intervals Δt_2 and Δt_3 have the same equivalent circuit and the same voltage across the inductor, so these time intervals are described by the equation 45.

$$\Delta t_2 = \Delta t_3 = (D - D_{ef})\frac{T_S}{2} \tag{45}$$

The first time interval is defined as:

$$\Delta t_1 = (1 - D)\frac{T_S}{2} \tag{46}$$

In the third time interval, the current in the inductor can be found by the expression 47:

$$V_{FB} = L_{lk}\frac{dI_{lk}(t)}{dt} \tag{47}$$

Applying Laplace transform the inductor current is found, as it can be seen in equation 48.

$$I_{lk}(s) = \frac{V_{FB}}{s^2 L_{lk}} \tag{48}$$

Finally, when it is applied the inverse Laplace transform in the equation 48, 49 is obtained.

$$I_{lk}(t) = \frac{V_{FB}}{L_{lk}}t \tag{49}$$

This time interval ends when the current in the inductor reaches the nominal value of the output current reflected to the primary(αI_L). The interval Δt_3 can be defined by the equation 50.

$$\Delta t_3 = \frac{\alpha I_L L_{lk}}{V_{FB}} \tag{50}$$

Substituting the equations 44, 45 and 50 in the equation 41, the expression 51 is found.

$$\Delta T = \frac{2\alpha I_L L_{lk}}{V_{FB}} + D_{ef}\frac{T_S}{2} \tag{51}$$

The duty cycle loss due to the voltage drop in the inductance is defined as the parameterized current $\overline{I'_{lk}}$:

$$\overline{I'_{lk}} = \frac{4\alpha I_L L_{lk} f}{V_{FB}} \tag{52}$$

Therefore, the effective duty cycle is defined by equation 53.

$$D_{ef} = D - \frac{4\alpha I_L L_{lk} f}{V_{FB}} \tag{53}$$

Finally, the output voltage with the voltage drop in the inductance is defined by equation 54.

$$V_{op} = D_{ef} V_{FB} \tag{54}$$

Therefore, the transformer turns ratio is defined by equation 55.

$$\alpha = \frac{V_{bat}}{V_{FB} D_{ef}} = \frac{V_{bat}}{V_{op}} \tag{55}$$

4 STUDY OF THE CURRENT-FED PUSH-PULL STAGE

To develop the Isolated Bidirectional DC-DC Converter it is fundamental to study the second power stage that is called the Current-Fed Push-Pull Stage. Further, this stage will be integrated with the DC-DC Full-Bridge ZVS-PWM Stage to develop the desired converter.

Therefore, this chapter is dedicated to the study of the current-fed push-pull converter. First, the idealized converter will be studied to clarify the basic concepts regarding its operation, after that some non-idealities will be added to the circuit to study the real operation of the converter. The main references used in this chapter are the master thesis of Mauro Tavares Peraça (PERAÇA et al., 2002) and Faruk José Nome Silva (SILVA, 1998), both advised by Professor Dr. Ivo Barbi.

The unidirectional isolated DC-DC current-fed Push-Pull converter works with overlapped gate signals of the switches. Thus, it has an operation similar to the isolated symmetrical boost converter, which is largely used in industrial applications. The converter operation is based on the energy storage at the input inductor (L) when both switches (S_5 and S_6) are turned on and the transfer of the energy to the load when one of the switches are turned off.

Although the converter operates in continuous and discontinuous conduction mode (CCM and DCM), it is only usual to operate it in CCM because of its pour efficiency operating in DCM and also it current stresses. Then, the CCM will be deeply discussed in this section and DCM will be studied only to find a critical condition to operate in CCM.

A desirable feature of this topology is basically the high static gain that converts the batteries voltage ($V_{bat} = 48V$) to the DC bus voltage of the microgrid ($V_{FB} = 400V$). Also, there is a current peak limitation in the battery due to the presence of the inductor at the push-pull side, which is perfect to charge and discharge batteries.

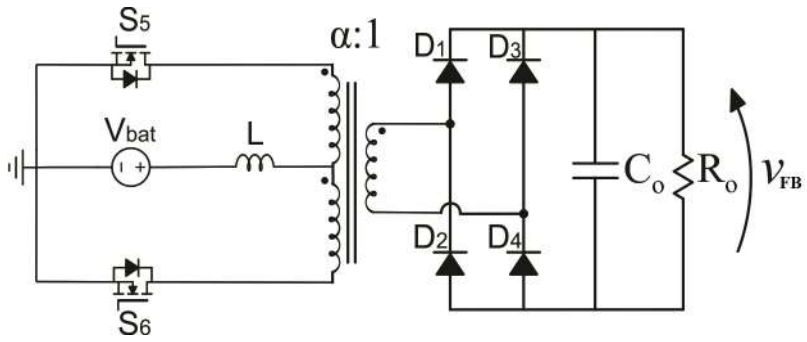
Nevertheless, the converter has some drawbacks that are the high voltage across the switches and the power loss, both due to the leakage inductance of the transformer. So, this disadvantages will be studied and overcome further in the end of this chapter.

4.1 IDEAL UNIDIRECTIONAL ISOLATED DC-DC CURRENT-FED PUSH-PULL CONVERTER

The ideal current-fed Push-Pull stage is shown in Figure 45. This consists of an usual push-pull converter on the primary side of the transformer with an inductor (L) in series with the voltage source (V_{bat}), so the converter operates as a current source. Also, the secondary of the transformer has a diode bridge.

The converter is considered ideal when there are a perfect magnetic coupling

Figure 45 – Ideal unidirectional isolated DC-DC current-fed push-pull converter



Source: Own elaboration

in the transformer and a very high magnetizing inductance, also there are not leakage inductance and parasitic resistances. In addition, the transformer turns ratio (α), shown in Figure 45, modifies the converter's static gain.

4.1.1 Continuous Conduction Mode

The converter is considered to be operating in the continuous conduction mode (CCM) when the current in the push-pull inductor does not reaches zero in a switching period.

This converter operates with constant commutation frequency (f) and a variable duty cycle on two switches located at the primary side. The diode bridge in the secondary side rectifies the voltage which is subsequently filtered by an capacitor (C_o) in order to maintain a low ripple voltage across the load resistor (R_o) that will represents the DC bus (V_{FB}).

4.1.1.1 Gate signals

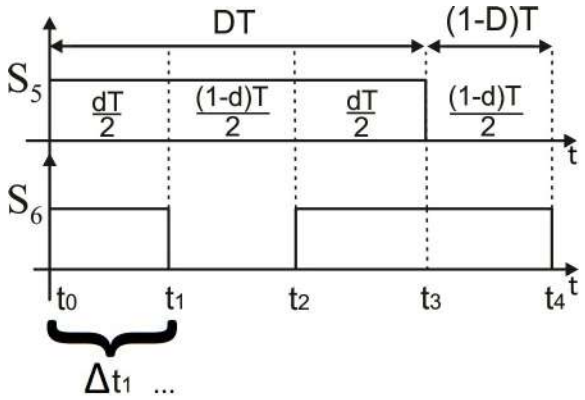
The ideal converter has four stages of operation, so it has four topological states. Also, it operates with a duty cycle (D) that represents the cycle that the input inductor is accumulating energy from the battery. The switches gate-source signals are shown in Figure 46.

The operation shown in Figure 46 illustrates that in steps 1 and 3 the inductor stores energy and in steps 2 and 4 it transfers the stored energy to the load.

4.1.1.2 Circuit operation

The analysis of the circuit presented in Figure 45 applying the modulation of Figure 46 has four operation steps, as it will be presented hereafter.

Figure 46 – Gate signals of the ideal unidirectional isolated DC-DC current-fed push-pull converter - CCM operation

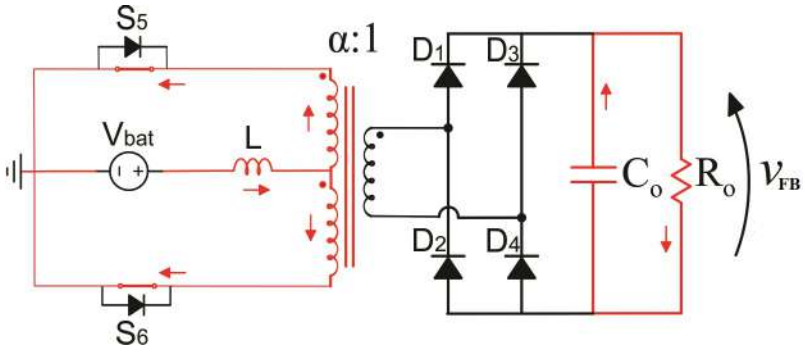


Source: Own elaboration

Time interval Δt_1 - At t_0, the switch S_5 is gated on and then conducts current. So, it assumes half of the average current of the inductor (L), since switch S_6 is already conducting from previous step. Therefore, the voltage in the transformer primary windings is zero, so it does not transfer energy.

Moreover, the current in the inductor increases linearly and the power required from the load is supplied by the capacitor. The first step is illustrated in Figure 47.

Figure 47 – First topological state of the ideal DC-DC current-fed push-pull converter - CCM operation

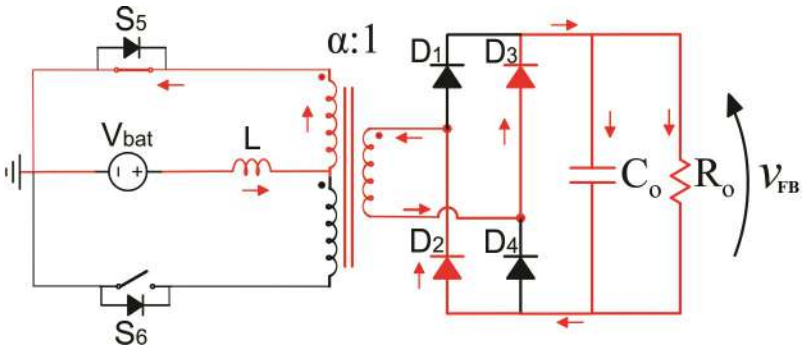


Source: Own elaboration

Time interval Δt_2 - At time t_1, the switch S_6 is turned off, so the diodes D_2 and D_3 are polarized and begin to conduct. During this step, the load is fed by the energy that was accumulated in the inductor and the switch S_5 conducts all the current. The second step is illustrated in Figure 48.

Time interval Δt_3 - At time t_2, the switch S_6 is turned on again and then starts to conduct half of the current from the inductor. This step is identical to the first one and

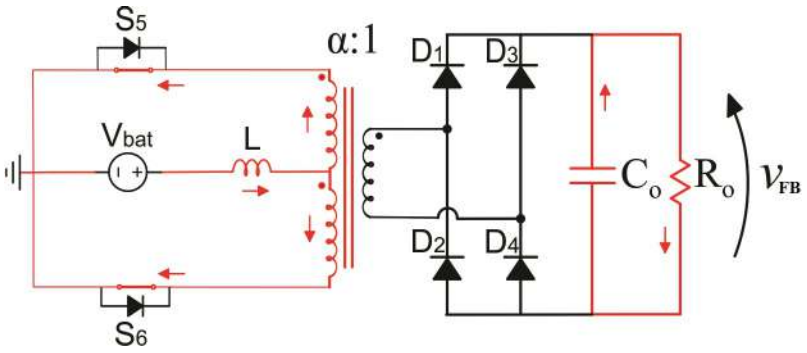
Figure 48 – Second topological state of the ideal DC-DC current-fed push-pull converter - CCM operation



Source: Own elaboration

is illustrated in Figure 49.

Figure 49 – Third topological state of the ideal DC-DC current-fed push-pull converter - CCM operation



Source: Own elaboration

Time interval Δt_4 - Finally, at time t_3, the switch S_5 is gated off, so the transformer windings has a positive voltage and the diodes D_1 and D_4 are direct polarized, so it the energy is transferred to the load as in the second step. The fourth step is illustrated in Figure 50.

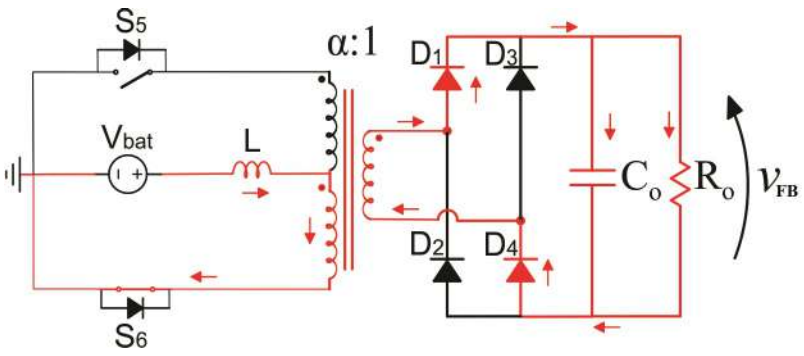
4.1.1.3 Waveforms

The main waveforms of the ideal current-fed Push-Pull converter are shown in Figure 51.

The maximum breakdown voltage across the switches are twice the voltage of the load referred to the push-pull side.

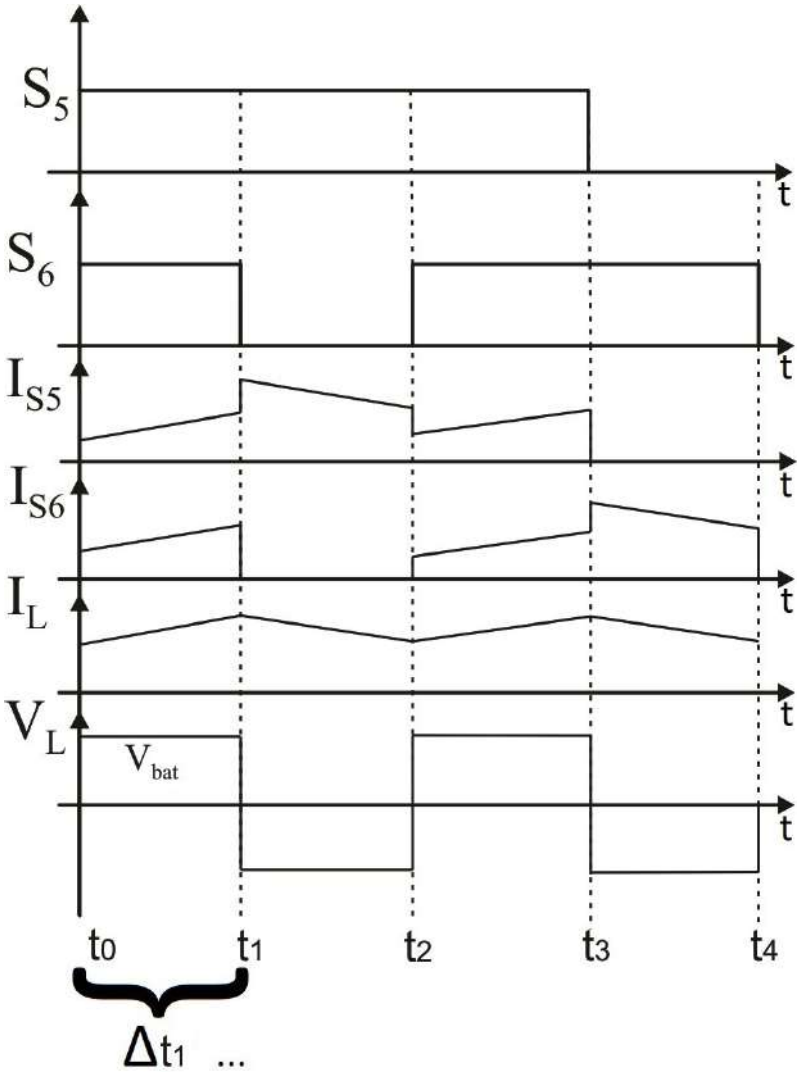
Also, it can be inferred that the waveforms and topological states are symmetrical for half cycle, then in the next analysis for CCM only half period will be demonstrated.

Figure 50 – Fourth topological state of the ideal DC-DC current-fed push-pull converter - CCM operation



Source: Own elaboration

Figure 51 – Main waveforms of the ideal unidirectional isolated DC-DC current-fed push-pull converter - CCM operation



Source: Own elaboration

4.1.1.4 Static Gain

The duty cycle (D) that represents the cycle that each switch is on and the duty cycle of the converter (d) represents the cycle that the inductor is charging.

With the Figure 52, it is possible to define the equation 56.

$$DT = \frac{dT}{2} + \frac{dT}{2} + \left(\frac{(1-d)T}{2}\right) \tag{56}$$

So, this equation can be simplified into equation 57.

$$D = \frac{d+1}{2} \tag{57}$$

Also, the time intervals can also be calculated as shown in equations 58 and 59.

$$\Delta t_1 = t_1 - t_0 = \frac{dT_S}{2} \tag{58}$$

$$\Delta t_2 = t_2 - t_1 = \frac{(1-d)T_S}{2} \tag{59}$$

In order to obtain the static gain and thus the output characteristics of the converter, it is used the fact that the average voltage at the inductor is zero during a period of operation as represented at equation 60.

$$V_{Lmed} = 0 \tag{60}$$

Also, the average voltage across the inductor can be defined as equation 61:

$$V_{Lmed} = \frac{2}{T_S}\left(\int_0^{\Delta t_1} V_{bat}dt + \int_0^{\Delta t_2} (V_{bat} - \alpha V_{FB})dt\right) \tag{61}$$

If equation 60 is replaced in 61, it gives equation 62.

$$0 = \frac{2}{T_S}\left(V_{bat}\frac{dT_S}{2} + (V_{bat} - \alpha V_{FB})\frac{(1-d)T_S}{2}\right) \tag{62}$$

Finally, if equation 62 is algebraically manipulated, the static gain of the converter can be found, as shown in equation 63.

$$q = \frac{V_{FB}}{V_{bat}} = \frac{1}{\alpha(1-d)} \tag{63}$$

The most desirable duty cycle is the one that limits the value of the voltage across the switches and this is represented in equation 64. So, with this equation is possible to assume a switch maximum voltage and calculate the needed duty cycle.

$$d_{max} = 1 - \frac{2V_{bat}}{V_{Smax}} \tag{64}$$

Then, there is a maximum static gain that the duty cycle can provide and this is represented in equation 65.

$$q_d = \frac{1}{1 - d_{max}} \tag{65}$$

Now, different from the equation 55 which α is based on the duty cycle, it is possible to find a relation to α by choosing an admissible drop voltage in the battery terminals, as represented in equation 66.

$$\alpha = \frac{q_d(V_{bat} - V_{drop})}{V_{FB}} \tag{66}$$

Finally, the duty cycle of the converter is defined as shown in equation 67.

$$d = 1 - \frac{V_{bat}}{\alpha V_{FB}} \tag{67}$$

And the turns number of the primary and secondary side of the transformer can be then calculated as shows equation 68.

$$N_P = \alpha N_S \tag{68}$$

In addition, to demagnetize the inductor (L), the voltage from the DC bus referred to push-pull side be higher than the voltage of the batteries, this voltage can be calculated as equation 69 shows:

$$\alpha V_{FB} = \frac{V_{bat}}{1 - d} \tag{69}$$

4.1.1.5 Inductor ripple current

First of all, it is possible to use the formula that represents the inductor voltage as represented in equation 70.

$$V_L = L\frac{di_L(t)}{dt} = L\frac{\Delta i_L}{\Delta t} \tag{70}$$

As Δi_L represents the inductor ripple current, Δt represents the time that the inductor is being magnetized.

$$\Delta t = \frac{dT_S}{2} \tag{71}$$

Also, it is know that:

$$f = \frac{1}{T_S} \tag{72}$$

The voltage across of the inductor is equals to the battery voltage. Then, if 71 be replaced in 70 gives:

$$V_{bat} = 2L\frac{\Delta i_L}{dT_S} \tag{73}$$

Thus, to calculate the inductance (L) of the push-pull converter it is necessary to chose a maximum ripple current and isolate L in the expression 73.

$$L = \frac{V_{bat}d}{2f\Delta i_L} \tag{74}$$

4.1.1.6 DC bus ripple voltage

To calculate the maximum DC bus voltage ripple across the capacitor, a similar approach is used. However, the objective is to size the capacitor. Therefore, the formula of the current in the capacitor is used, as shown in equation 75:

$$I_C = C\frac{dV_C(t)}{dt} = C\frac{\Delta V_C}{\Delta t} \tag{75}$$

Since ΔV_C is the DC bus voltage ripple and Δt is the period which the capacitor is discharged, if 71 be replaced in 75, it gives:

$$\Delta V_C = \frac{I_C dT_S}{2C} \tag{76}$$

Moreover, by isolating the variable d in the expression 63 it is leads to:

$$d = \frac{\alpha V_{FB} - V_{bat}}{\alpha V_{FB}} \tag{77}$$

Finally, if equation 77 be replaced in 76, it is possible to size the capacitance by choosing a maximum voltage ripple at the DC bus ripple, as shown in equation 78.

$$C = \frac{I_C}{2f\Delta V_C} \cdot \frac{\alpha V_{FB} - V_{bat}}{\alpha V_{FB}} \tag{78}$$

4.1.2 Discontinuous Conduction Mode

The operation of the current-fed push-pull converter in the discontinuous conduction mode (DCM) is not common. Notwithstanding, the presentation of the operating steps and the output characteristics of this mode will be important to understand and correctly size the converter.

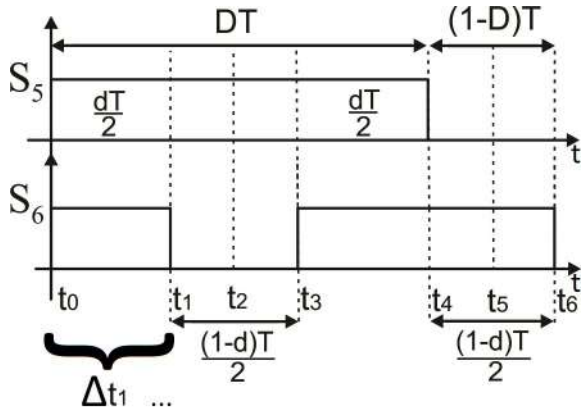
Furthermore, the electrical circuit remains the same as presented in Figure 45.

4.1.2.1 Gate signals

The gate signals of the switches are shown in Figure 52. Although they are not different from the commands in the continuous conduction, there are two more time

intervals and topological states that represents the period which the current at the inductor is zero.

Figure 52 – Gate signals of the ideal unidirectional isolated DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

It can be seen in Figure 52 that steps 1 and 4 represent the energy accumulation in the inductor, steps 2 and 5 represent the energy transfer from the inductor to the load and steps 3 and 6 represent the stationary period which the current at the inductor is zero. Moreover, in steps 3 and 6, only the capacitor supplies power to the load.

An important aspect of the theory on discontinuous conduction mode is the extinction of the inductor current exactly in half of a switching period, which indicates the operation in the critical continuous conduction mode (CCCM), or the boundary between the continuous and discontinuous modes.

In fact, the study of the operation in DCM will be performed only to identify the CCCM, since the converter should not operate in the DCM due to the low performance and large current stresses in the semiconductors.

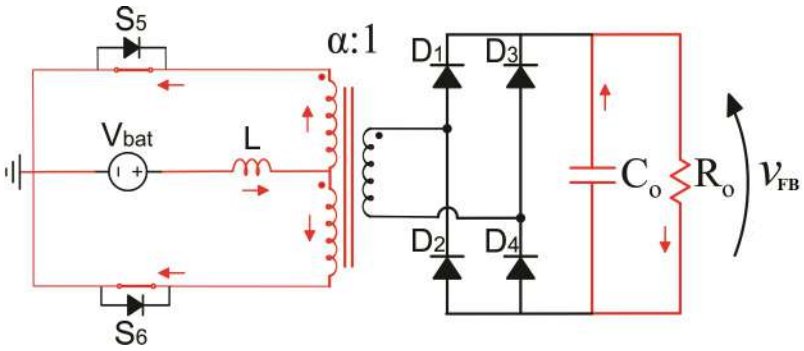
4.1.2.2 Circuit operation

The topological states of the converter operating in DCM are described next.

Time interval Δt_1 - At time t_0 the switch S_5 is gated on and switch S_6 was already on since the previous. This step has the operation equals to first step in CCM, which the inductor is being magnetized. Thus, the magnetic flux at the transformer terminals cancels out, because they have opposite directions. So, there is no energy transfer to the load. The first step is illustrated in Figure 53.

Time interval Δt_2 - At time t_1, the switch S_6 turned off and again the converter behaves equal to the second stage of the continuous conduction mode, which the energy of the inductor is transferred to the load because the diodes D_2 and D_3 are

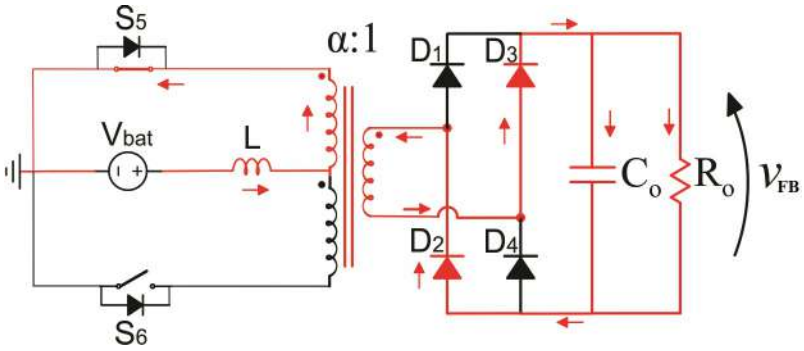
Figure 53 – First topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

directly polarized. Therefore, the current in the inductor is decreases linearly and this step is illustrated in Figure 54.

Figure 54 – Second topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



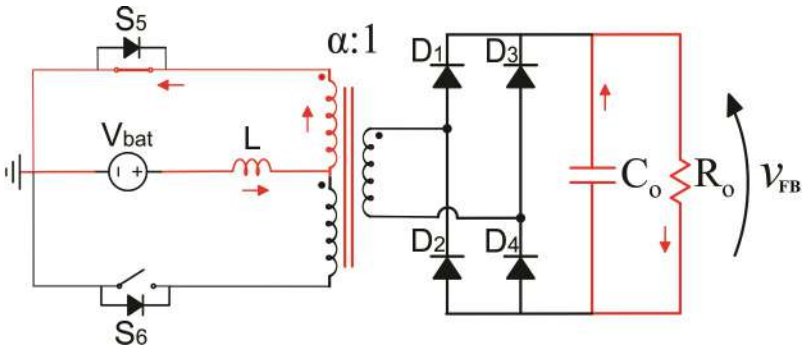
Source: Own elaboration

Time interval Δt_3 - At time t_2, the circuit is the same as in the previous topological state, but the current in the inductor is null. Thus, there is no more energy to be transferred to the output. This step is called the stationary stage and only the filter capacitor at the output provides power to the load. The third step is illustrated in Figure 55.

Time interval Δt_4 - At time t_3, the switch S_6 is gated on and the converter assumes the same configuration as the first stage of CCM, which the inductor is magnetized with a linear current. The fourth step is illustrated in Figure 56.

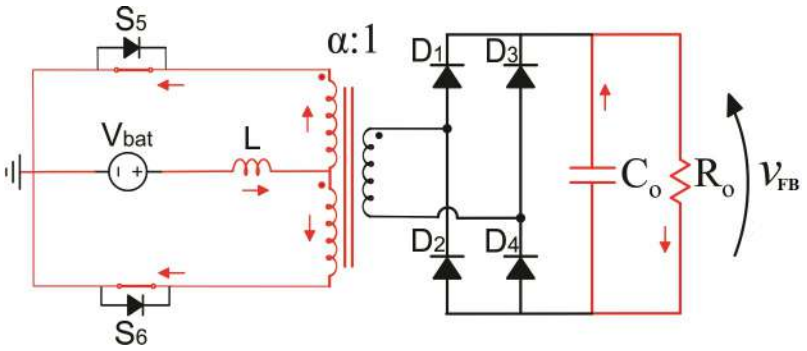
Time interval Δt_5 - At time t_4, the switch S_5 is gated off and then the converter assumes the configuration of the fourth operating stage of CCM, which the inductor is demagnetized with a linear current through diodes D_1 and D_4, providing power to the

Figure 55 – Third topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

Figure 56 – Fourth topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

load. The fifth step is illustrated in Figure 57.

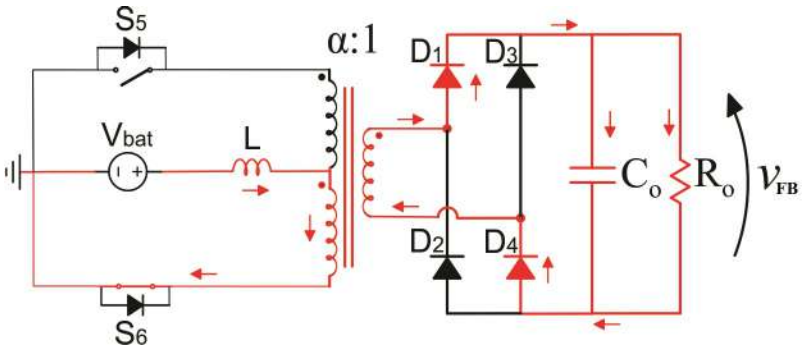
Time interval Δt_6 - At time t_5, the current in the inductor drops to zero. Then, there is no more energy to be transferred, so only the filter capacitor at the output provides power to the load. The sixth step is illustrated in Figure 58.

4.1.2.3 Waveforms

The main waveforms of the ideal current-fed Push-Pull converter operating in DCM are shown in Figure 59.

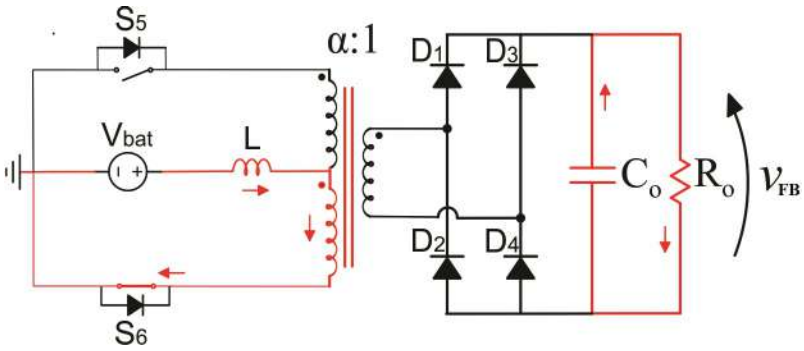
It can be inferred that the waveforms and topological states are symmetrical for half cycle, then in the next analysis for DCM only half period will be demonstrated.

Figure 57 – Fifth topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

Figure 58 – Sixth topological state of the ideal DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

4.1.2.4 Output Characteristics

First of all, in order to find the static gain of the converter operating in the DCM, it will be necessary to obtain the time duration of each topological state. Thus, as the converter presents symmetrical half-periods, only the three initial time intervals have to be analyzed.

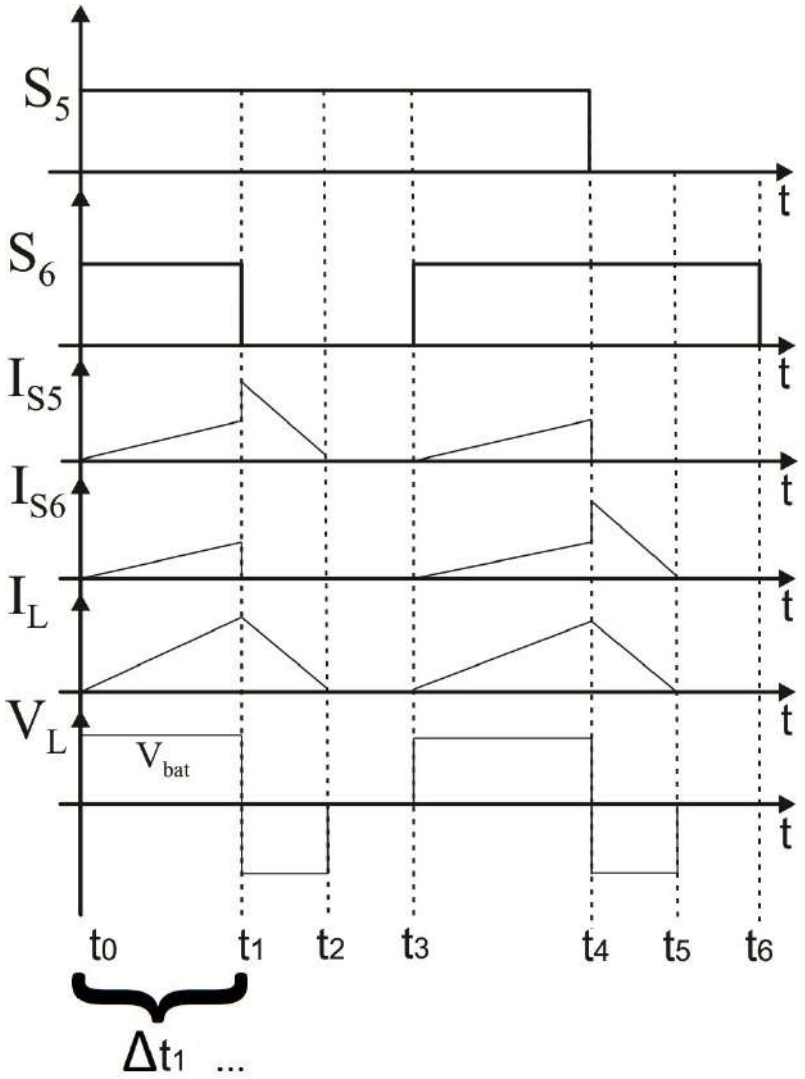
$$\Delta t_1 = \frac{dT_S}{2} \tag{79}$$

$$\Delta t_1 + \Delta t_2 + \Delta t_3 = \frac{T_S}{2} \tag{80}$$

The load current at the output is equal to twice the average current in the output diodes:

$$I_o = 2I_{Dmd} \tag{81}$$

Figure 59 – Main waveforms of the ideal unidirectional isolated DC-DC current-fed push-pull converter - DCM operation



Source: Own elaboration

The current in the output diode can also be found from its waveform.

$$I_{Dmd} = \frac{\alpha I_{L\max} \Delta t_2}{2T_S} \tag{82}$$

In the time interval Δt_1, the inductor is being magnetized, so the current at the end of this step has its maximum value.

$$I_{L\max} = \frac{V_{bat} \Delta t_1}{L} \tag{83}$$

If equation 79 be replaced into 83, it gives:

$$I_{L\max} = \frac{V_{bat} d T_S}{2L} \tag{84}$$

In the time interval Δt_2, the inductor is transferring energy and the current is null at the end of the period, so:

$$I_{L\max} - \frac{(\alpha V_{FB} - V_{bat})\Delta t_2}{L} = 0 \tag{85}$$

If equation 84 be replaced into 85, it gives:

$$\frac{V_{bat} d T_S}{2L} = \frac{(\alpha V_{FB} - V_{bat})\Delta t_2}{L} \tag{86}$$

If Δt_2 be isolated, it leads to:

$$\Delta t_2 = \frac{V_{bat} d T_S}{2(\alpha V_{FB} - V_{bat})} \tag{87}$$

Now, by substituting 83 into 82, it gives:

$$I_{Dmd} = \frac{\alpha V_{FB} \Delta t_1 \Delta t_2}{2 T_S L} \tag{88}$$

Finally, substituting equations 79 and 87 into 88, it gives:

$$I_{Dmd} = \frac{\alpha {V_{bat}}^2 d^2 T_S}{8L(\alpha V_{FB} - V_{bat})} \tag{89}$$

Finally, replacing 89 in 81 gives:

$$I_o = \frac{\alpha {V_{bat}}^2 d^2}{4Lf(\alpha V_{FB} - V_{bat})} \tag{90}$$

Then, substituting the equation 63 in equation 90, the following DCM static gain is found.

$$q_{dcm} = \frac{V_{bat} d^2}{4 f L I_o} + \frac{1}{\alpha} \tag{91}$$

It is possible to analyze that in the expression 91 some characteristics of the converter. First of all, the relation between the static gain and the duty cycle is not directly proportional. In addition, the load current depends on the static gain of the converter.

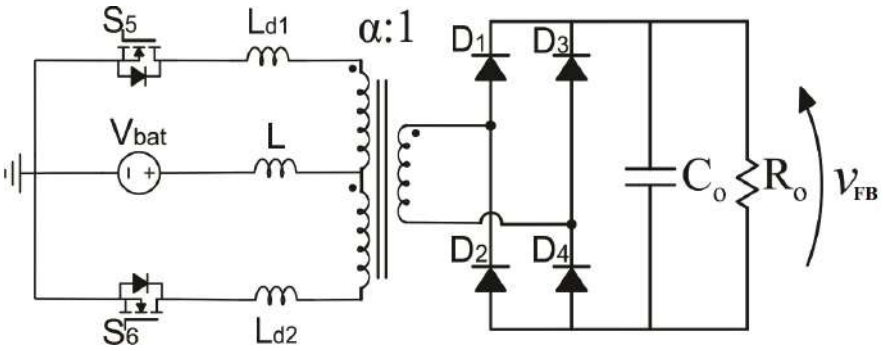
Although in DCM the converter behaves in a non-linear way and that the static gain depends on the load, when the it reaches CCM this characteristic disappears, which is good for the converter because it simplifies the analyze.

4.2 UNIDIRECTIONAL ISOLATED DC-DC CURRENT-FED PUSH-PULL CONVERTER WITH LEAKAGE INDUCTANCE

The non-idealities modifies the current-fed push-pull converter analysis. Thus, the new analysis will be performed by adding the Leakage inductance studied in Chapter

3 (L_{lk}) referred to the push-pull side of the transformer (L_{d1} and L_{d2}) in series with the switches. The converter with leakage inductance is shown in Figure 60.

Figure 60 – Unidirectional isolated DC-DC current-fed push-pull converter with leakage inductance



Source: Own elaboration

Note that these inductances (L_{d1} and L_{d2}) are the inductance from Chapter 3 (L_{lk}) referred to the Current-Fed Push-Pull Stage. The inductance value can be calculated with equation 92

$$L_{d1} = L_{d2} = 2\alpha^2 L_{lk} \tag{92}$$

The leakage inductances in series with the switches S_5 and S_6 store energy during the time interval which the switches are turned on. Then, when these are turned off, the energy soted in the inductance demagnetize over the MOSFET parasitic capacitances, causing a high breakdown voltage across the switches.

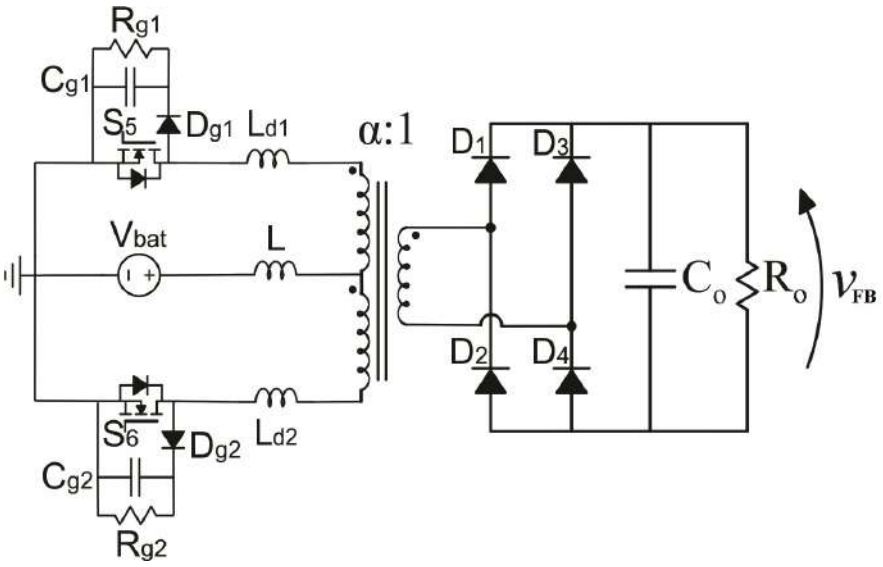
Thus, to analyze the steps of operation of this circuit it is necessary to include a circuit to provide an alternative path for the energy stored in the leakage inductance.

In order to perform voltage limitation, a passive voltage clamping technique can be used to transfer the accumulated energy in the leakage inductance to clamping capacitors (C_{g1} and C_{g2}) through clamping diodes (D_{g1} and D_{g2}), dissipating the energy in the clamping resistors (R_{g1} and R_{g2}). This technique, which prevents high voltage across the switches is represented in Figure 61.

However, this type of clamping circuit decreases the efficiency of the converter, since all the energy accumulated in the leakage inductance are dissipated as heat in the clamping resistors. Thus, one of the objectives of this chapter is to study another technique to improve the efficiency of the converter.

So, a more efficient voltage clamper circuit should be studied. Therefore, a possible solution would be the implementation of an active or regenerative voltage clamper.

Figure 61 – Unidirectional isolated DC-DC current-fed push-pull converter with leakage inductance and passive voltage clamper

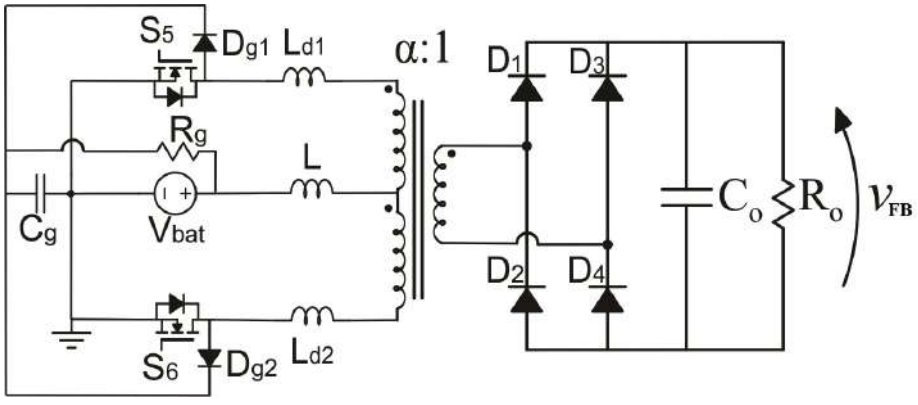


Source: Own elaboration

4.3 UNIDIRECTIONAL ISOLATED DC-DC CURRENT-FED PUSH-PULL CONVERTER WITH LEAKAGE INDUCTANCE AND PARTIALLY REGENERATIVE VOLTAGE CLAMPER

The circuit in Figure 62 illustrates the current-fed Push-Pull converter with the partially regenerative voltage clamper. This topology is similar to the that presented in previous section. The energy accumulated in the leakage inductance is transferred to the clamping capacitor (C_g) through the clamping diodes (D_{g1} and D_{g2}).

Figure 62 – Unidirectional isolated DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper



Source: Own elaboration

However, the energy in the clamping capacitor is partially regenerated to the source and partially dissipated in the clamping resistor (R_g), because the resistance is connected to the source input and not the ground.

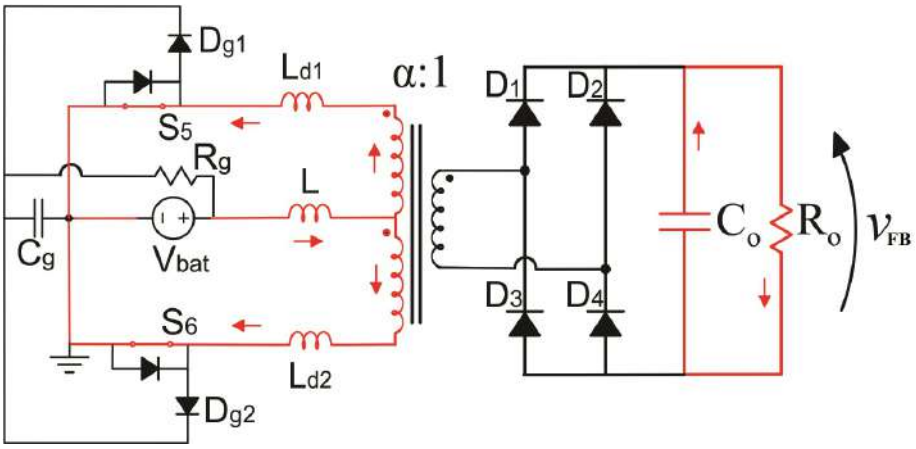
4.3.1 Continuous Conduction Mode

4.3.1.1 Circuit operation

The converter with leakage inductance presents eight topological states when operating in CCM, but half of them are symmetrical for one commutation period. Therefore, only four states will be presented:

Time interval Δt_1 - In this topological state the inductor (L) is being magnetized by the voltage source (V_{bat}). At this state, the switches S_5 and S_6 are turned on. So, the currents that flow through the two winding have the same value and opposite directions. Thus, the magnetic flux nulls the voltage in the secondary side of the transformer. The first operation step is presented in Figure 63.

Figure 63 – First topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - CCM operation

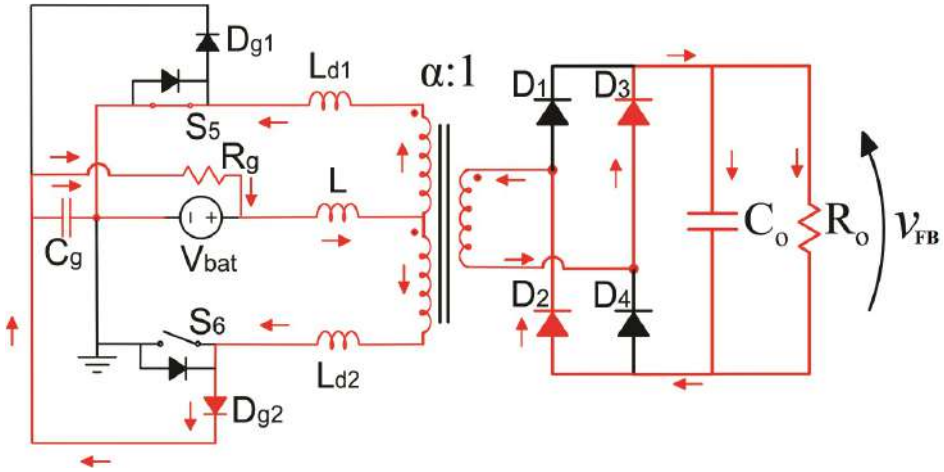


Source: Own elaboration

Time interval Δt_2 - At t_1, the switch S_6 is gated off, so the energy that has been stored in the leakage inductance (L_{d2}) is transferred to he clamping capacitor (C_g) through the diode D_{g2}. This energy is partially transferred to the voltage source and partly dissipated in the clamping resistor (R_g). Furthermore, the energy stored in the inductor L is transferred to the load by the diodes D_2 and D_3. The second operation step is presented in Figure 64.

Time interval Δt_3 - When the energy stored in L_{d2} is null, the diode D_{g2} stops the current flow through the clamping circuit. The energy in the inductor L continues to be transferred to the load and it drops steadily until the next step. Furthermore, there

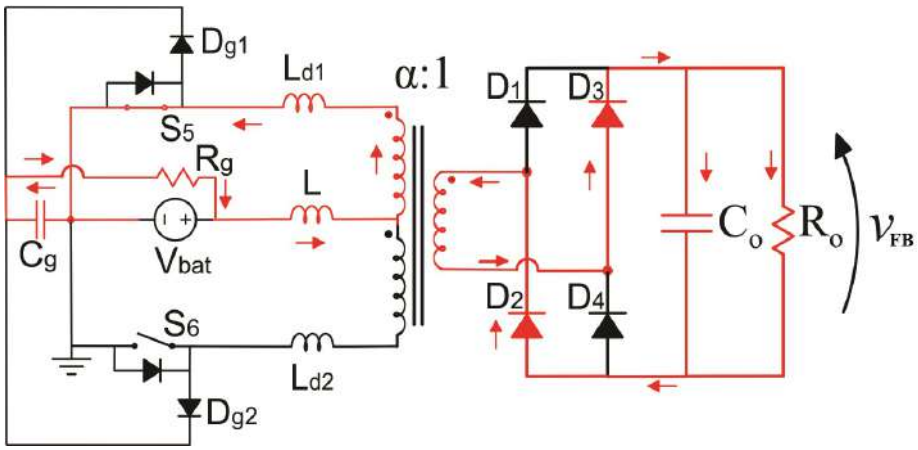
Figure 64 – Second topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - CCM operation



Source: Own elaboration

is a voltage across the clamping capacitor. So, the current that flows through clamping resistor is regenerated to the voltage source. The third operation step is presented in Figure 65.

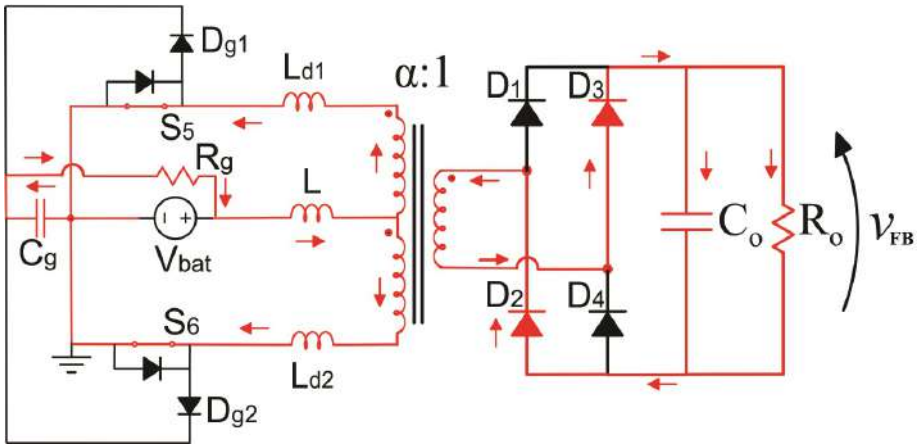
Figure 65 – Third topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - CCM operation



Source: Own elaboration

Time interval Δt_4 - At t_3, the switch S_6 is turned on. While its current increases, the current in S_5 decreases linearly. The current in the inductance and the clamping circuit is transferred to the load through diodes D_2 and D_3 until the currents in the switches are equalized. The fourth operation step is presented in Figure 66.

Figure 66 – Fourth topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - CCM operation



Source: Own elaboration

4.3.1.2 Waveforms

With the topological states, it is possible to represent the circuit operation of the unidirectional isolated DC-DC current-fed push-pull converter with leakage inductance and the partially regenerative voltage clamper operating in continuous conduction mode. The waveforms are shown in Figure 67.

4.3.1.3 Output Characteristics

The output characteristics of the non-ideal converter with a regenerative voltage clamper circuit is more complex, so it should be presented carefully. A mathematical analysis has to be performed in the topological states in order to obtain a operation point and validate the model.

Thus, the output voltage reflected to the primary side (or push-pull side) and the average current in the inductor without the clamping circuit are presented in equations 93 and 94.

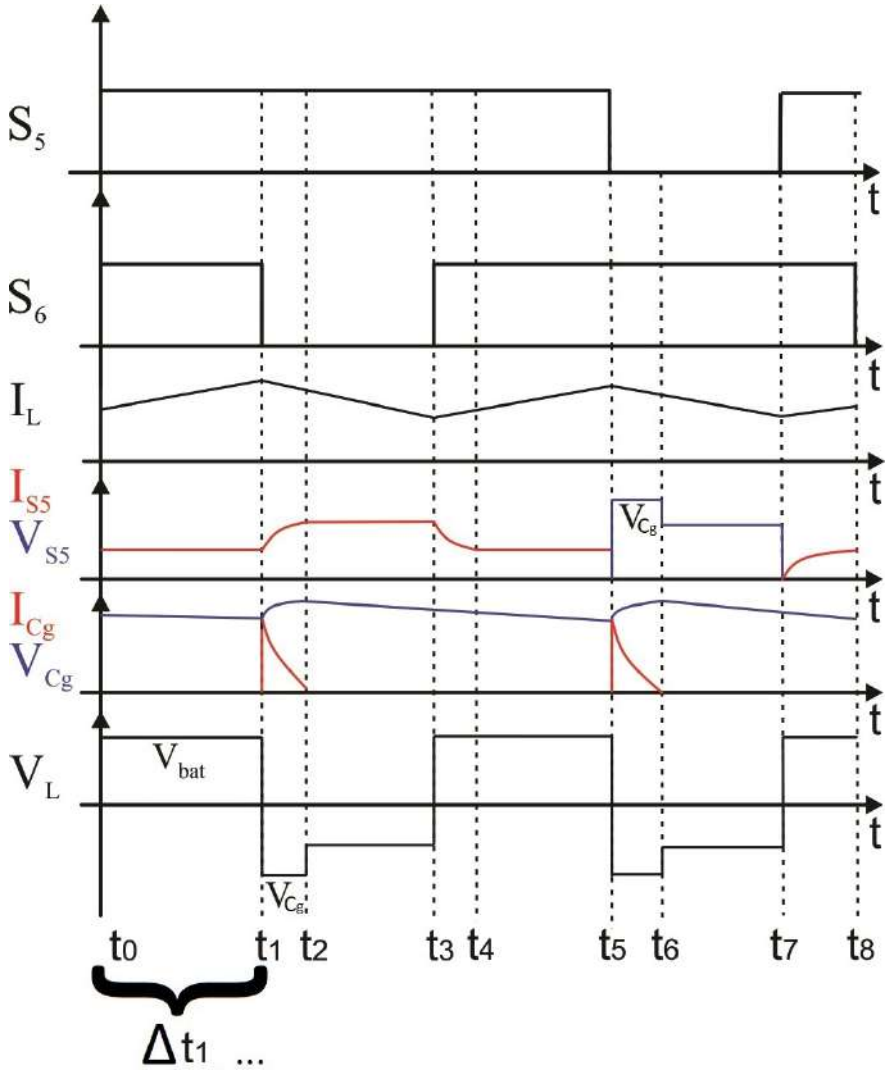
$$V_{op} = \frac{V_{bat}}{1-d} \tag{93}$$

$$I_{Lmd} = \frac{I_o}{\alpha(1-d)} \tag{94}$$

Also, the time steps of each topological state should be calculated.

$$\Delta t_1 + \Delta t_4 = \frac{dT_S}{2} \tag{95}$$

Figure 67 – Main waveforms of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - CCM operation



Source: Own elaboration

$$\Delta t_2 + \Delta t_3 = \frac{(1-d)T_S}{2} \tag{96}$$

The voltage across the leakage inductance is represented in equation 97.

$$V_{Ld} = L_d \frac{\Delta I_{Ld}}{\Delta t} \tag{97}$$

At t_2 the leakage inductance has the following voltage, which V_G is the clamping capacitor voltage:

$$V_{Ld} = \frac{V_G}{2} - V_{op} \tag{98}$$

And at t_4 the leakage inductance has the following voltage:

$$V_{Ld} = V_{op} \tag{99}$$

If 98 and 99 be replaced into 97, it gives equations 100 and 101 respectively.

$$\frac{V_G}{2} - V_{op} = L_d \frac{\Delta I_{Lmd}}{2\Delta t_2} \tag{100}$$

$$V_{op} = L_d \frac{\Delta I_{Lmd}}{2\Delta t_4} \tag{101}$$

Finally, if the times be isolated in equations 100 and 101 and then replaced into equations 95 and 96, the following equations are found:

$$\Delta t_1 = \frac{d}{2f} - \frac{I_o L_d}{2V_{bat}\alpha} \tag{102}$$

$$\Delta t_2 = \frac{I_o L_d}{2\alpha(1-d)\left(\frac{V_G}{2} - \frac{V_{bat}}{1-d}\right)} \tag{103}$$

$$\Delta t_3 = \frac{(1-d)}{2f} - \frac{I_o L_d}{2\alpha(1-d)\left(\frac{V_G}{2} - \frac{V_{bat}}{1-d}\right)} \tag{104}$$

$$\Delta t_4 = \frac{I_o L_d}{2V_{bat}\alpha} \tag{105}$$

It can be noticed in the defined time intervals that they depend on the leakage inductance (L_d) and the clamping voltage (V_G), besides other variables. Therefore, it is fundamental to find a expression for the clamping voltage.

To find this voltage is possible to analyze the average current in the clamping resistor (R_g), which is the sum of the currents in the clamping diodes or a integrate of half cycle.

$$I_{RG} = \frac{1}{T_S} \int_0^{\Delta t_2} \frac{I_{Lmd}}{2} dt \tag{106}$$

By solving the equation 106, 107 is found.

$$I_{RG} = \frac{f I_{Lmd} \Delta t_2}{2} \tag{107}$$

If 94 and 103 be replaced into 107, it gives:

$$I_{RG} = \frac{f L_d}{\left(\frac{V_G}{2} - \frac{V_{bat}}{1-d}\right)} \cdot \left(\frac{I_o}{2\alpha(1-d)}\right)^2 \tag{108}$$

The voltage across the clamping capacitor can be found with electrical circuit analysis.

$$V_G = R_g I_{RG} + V_{bat} \tag{109}$$

By replacing 108 into 109, it leads to:

$$V_G = \frac{R_g f L_d}{\left(\frac{V_G}{2} - \frac{V_{bat}}{1-d}\right)} \cdot \left(\frac{I_o}{2\alpha(1-d)}\right)^2 + V_{bat} \tag{110}$$

With some algebraic manipulations, it is possible to isolated the clamping voltage.

$$V_G = V_{bat}\left[\frac{\alpha(3-d) + I_o\sqrt{\frac{2L_d R_g f}{V_{bat}^2} + \frac{\alpha^2(1+d)^2}{I_o^2}}}{2\alpha(1-d)}\right] \tag{111}$$

Now, it is indispensable to find the average inductance current considering the clamping circuit, in order to obtain the static gain.

First of all, the average current in the output diodes are:

$$I_{Dmd} = \frac{I_o}{2} \tag{112}$$

$$I_{Dmd} = \frac{\alpha I_{Lmd}}{T_S}\left[\Delta t_3 + \left(\frac{\Delta t_2 + \Delta t_4}{2}\right)\right] \tag{113}$$

By replacing 112 into 113, it leads to:

$$I_{Lmd} = \frac{I_o}{\alpha\left[1 - d + f\left(\Delta t_4 - \Delta t_2\right)\right]} \tag{114}$$

Now, replacing equations 103 and 105 in 114, 115 is found.

$$I_{Lmd} = \frac{I_o}{\alpha\left[\frac{I_o L_d f}{2V_{bat}\alpha} - \frac{I_o L_d f}{2\alpha(1-d)\left(\frac{V_G}{2} - \frac{V_{bat}}{1-d}\right)} + 1 - d\right]} \tag{115}$$

Finally, by substituting 111 in 115, it is possible to find a expression for the average current in the inductor.

$$I_{Lmd} = \frac{I_o}{\alpha\left[\frac{I_o L_d f}{2V_{bat}\alpha} + \frac{I_o L_d f}{2\alpha V_{bat}\left(1 + \frac{\alpha(3-d) - I_o\sqrt{\frac{2L_d R_g f}{{V_{bat}}^2} + \frac{\alpha^2(1+d)^2}{{I_o}^2}}}{4\alpha}\right)} + 1 - d\right]} \tag{116}$$

Therefore, it is possible to find the static gain of the converter using the power balance. The power of the batteries (P_{bat}) is equals to the power of the load (P_{out}) and the power loss in the clamping resistor and other elements (P_G).

$$P_{bat} = P_{out} + P_G \tag{117}$$

Furthermore, each power can also be calculated as:

$$P_{bat} = V_{bat}(I_{Lmd} - I_{RG}) \tag{118}$$

$$P_{out} = V_{FB}I_o \tag{119}$$

$$P_G = \frac{(V_G - V_{bat})^2}{R_g} \tag{120}$$

So, by replacing 118, 119 and 120 in 117 gives:

$$V_{bat}(I_{Lmd} - I_{RG}) = V_{FB}I_o + \frac{(V_G - V_{bat})^2}{R_g} \tag{121}$$

Finally, the static gain is defined as:

$$\frac{V_{FB}}{V_{bat}} = \frac{(I_{Lmd} - I_{RG})}{I_o} - \frac{(V_G - V_{bat})^2}{V_{bat}R_gI_o} \tag{122}$$

Therefore, the static gain (q) in function of the project parameters can be found by replacing equations 111 and 116 into 122. Also, the term V_{bat} must be isolated. Then, the static gain found is:

$$q = \frac{V_{FB}}{V_{bat}} = a - b - c \tag{123}$$

Which a, b and c are defined by equations 124, 125 and 126, respectively.

$$a = \frac{1}{\left(\alpha - \alpha d + \frac{I_oL_df\left(\frac{\alpha}{2\alpha - \frac{I_o\sqrt{\frac{2L_dR_gf}{{V_{bat}}^2} + \frac{\alpha^2(1+d)^2}{{I_o}^2}}}{2} + \frac{\alpha(d-3)}{2}} + \frac{1}{2}\right)}{V_{bat}}\right)} \tag{124}$$

$$b = \frac{I_oL_df}{4\alpha^2(d-1)V_{bat}\left(1 + \frac{\alpha(d-3) - I_o\sqrt{\frac{2L_dR_gf}{{V_{bat}}^2} + \frac{\alpha^2(1+d)^2}{{I_o}^2}}}{4\alpha}\right)} \tag{125}$$

$$c = \frac{V_{bat}}{I_o R_g}\left[1 - \frac{\alpha(3-d) - I_o\sqrt{\frac{2L_d R_g f}{{V_{bat}}^2} + \frac{\alpha^2(1+d)^2}{{I_o}^2}}}{2\alpha(d-1)}\right]^2 \tag{126}$$

Moreover, it is possible to calculate the ideal static gain of the push-pull by considering the leakage inductance equals to zero. Thus, equation 123 is simplified into equation 127.

$$q_{ideal} = \frac{1}{\alpha(1-d)} - \frac{V_{bat}(1-\frac{2}{1-d})}{I_o R_g} \tag{127}$$

4.3.1.4 Parameterization

First of all, some variables must be defined to interpolate the curves around an operation point. Therefore, the following variables are defined as shown in table 2

Table 2 – Parameterization Variables

Variable	**Value**
Leakage inductance referred to the Push-Pull Stage (L_d)	1.108 μH
Battery Voltage (V_{bat})	48 V
Tranformer turns ratio (α)	0.185
Switching frequency (f)	40 kHz
Duty Cylcle (d)	0.352
Clamping resistance (R_g)	320 Ω
Push-Pull Stage inductance (L)	43.2 μH

Source: Own elaboration

Now it is possible to parameterize the static gain in order to have a dimensionless variable. Note that the duty cycle and clampling resistance values will not be used when the charts represent duty cycle variation and clamping resistance variation, respectively.

So, the parameterized resistance (γ) and the parameterized output current (I_{op}) are defined.

$$\gamma = \frac{R_g}{f L_d} \tag{128}$$

$$I_{op} = \frac{I_o f L_d}{V_{bat}} \tag{129}$$

If 128 and 129 be replaced in 124, 125 and 126, the parameterized static gain is found, as shown is equations 130, 131, 132 and 133,

$$q(\alpha, d, \gamma, I_{op}) = \frac{V_{FB}}{V_{bat}} = a - b - c \tag{130}$$

Which:

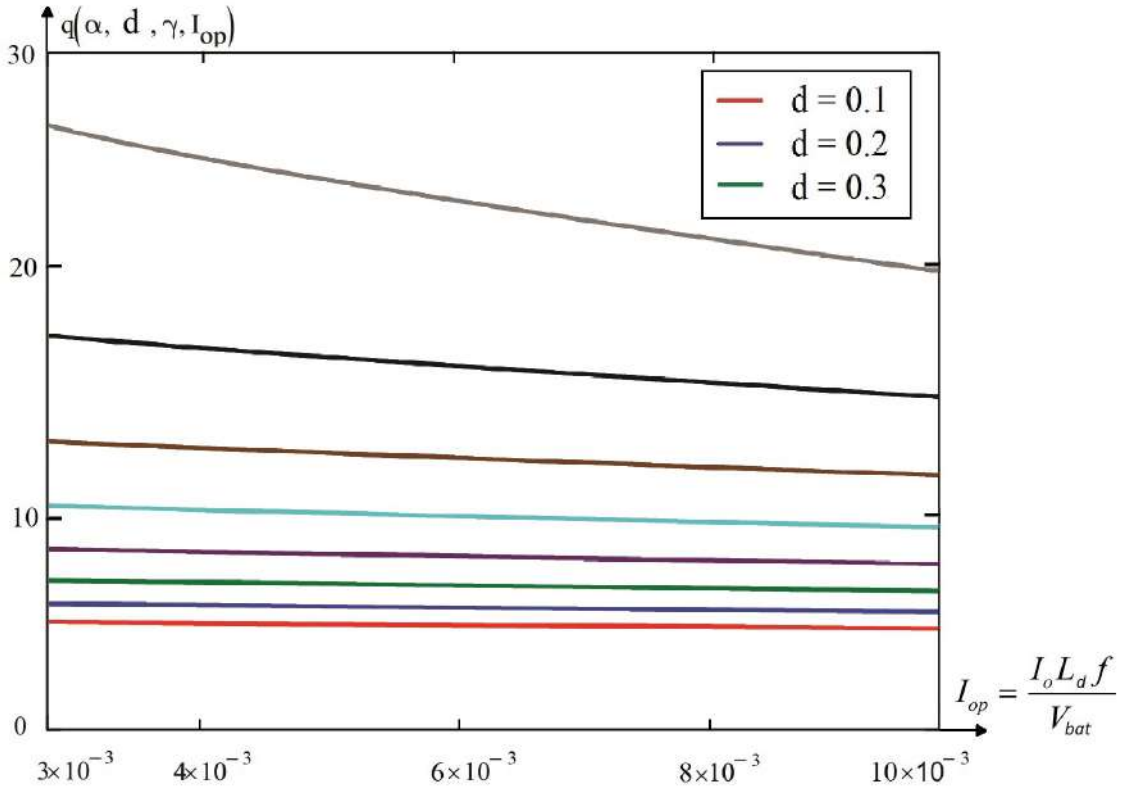
$$a = \frac{1}{\alpha\left(1 - d + I_{op}\left(\frac{1}{2\alpha - \frac{\sqrt{\alpha^2(1+d)^2 + 2{I_{op}}^2\gamma}}{2} + \frac{\alpha(d-3)}{2}} + \frac{1}{2\alpha}\right)\right)} \tag{131}$$

$$b = \frac{I_{op}}{4\alpha^2(d-1)\left(1 + \frac{\alpha(d-3) - \sqrt{\alpha^2(1+d)^2 + 2{I_{op}}^2\gamma}}{4\alpha}\right)} \tag{132}$$

$$c = \frac{1}{I_{op}\gamma}\left[1 - \frac{\alpha(3-d) - \sqrt{\alpha^2(1+d)^2 + 2{I_{op}}^2\gamma}}{2\alpha(d-1)}\right]^2 \tag{133}$$

By replacing the equations a, b and c in equation 130, it is possible to represent the static gain as a function of the parameterized current for different duty cycles, as illustrated in Figure 68.

Figure 68 – Static gain of the push-pull stage with a regenerative voltage clamper for duty cycle variation as a function of the parameterized current



Source: Own elaboration

It is possible to analyze that the static gain is linear for a duty cycle variation. So, the static gain decreases when the current increases. Also, the greater the duty cycle, the greater the static gain.

Furthermore, equation 127 is parameterized. So, equation 134 is found, which represents the ideal push-pull stage parameterized static gain considering the voltage clamper.

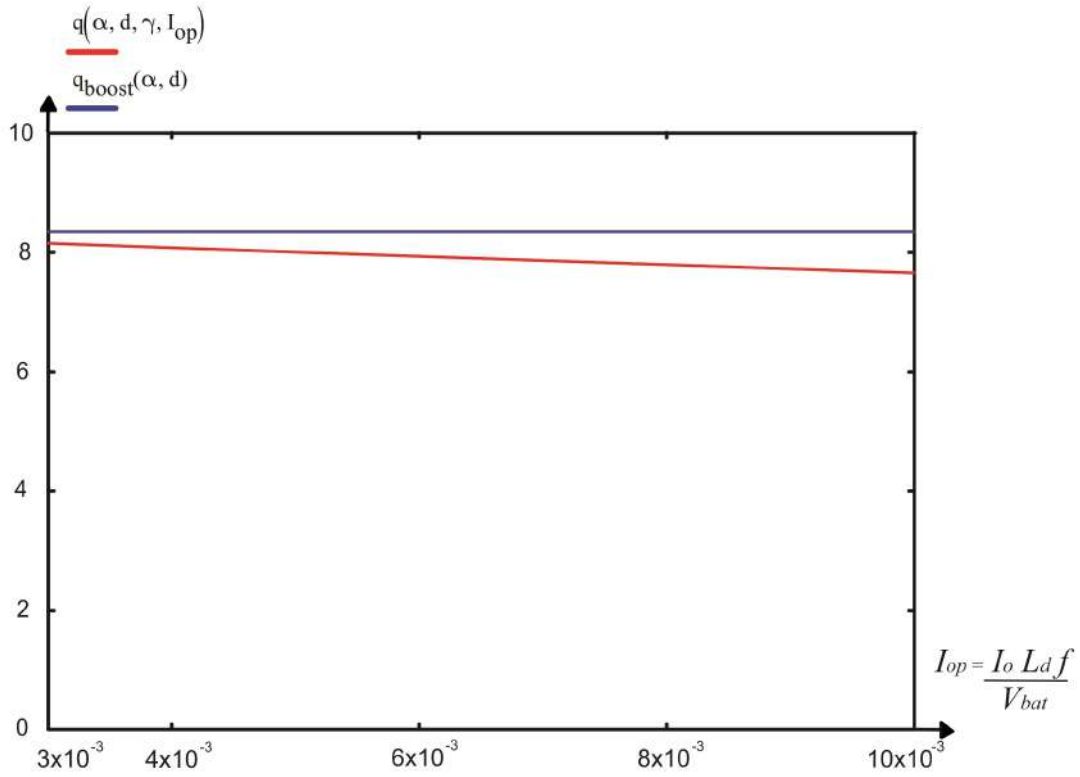
$$q_{ideal}(\alpha, d, \gamma, I_{op}) = \frac{1}{\alpha(1-d)} - \frac{1 - \frac{2}{(1-d)}}{\gamma I_{op}} \tag{134}$$

If the clampling resistance is not considered, γ is zero. So, it can be inferred from equation 134 that the static gain of the ideal push-pull stage is equal to the static gain of the classic boost converter considering the transformer turns ratio.

$$q_{boost}(\alpha, d) = \frac{1}{\alpha(1-d)} \tag{135}$$

Even though, the parameterized static gain of the boost converter is not changing for a parameterized current variation, the chart 69 illustrates this static gain with the push-pull stage static gain in order to prove its resemblance.

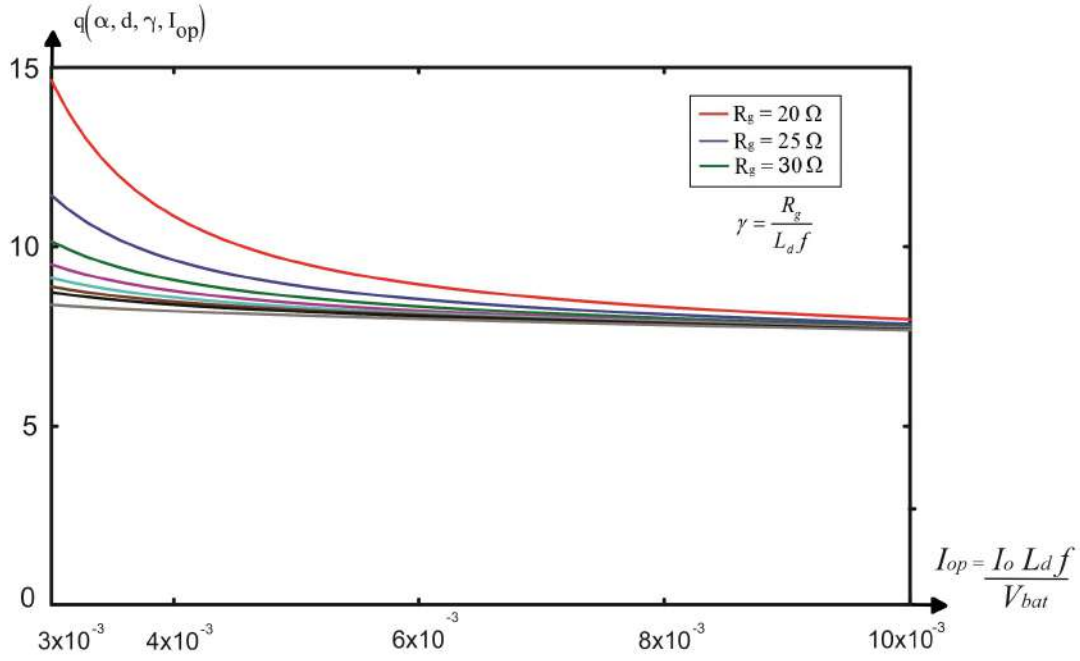
Figure 69 – Static gain of the push-pull stage with a regenerative voltage clamper and ideal boost converter as function of the parameterized current



Source: Own elaboration

Moreover, it is possible to analyze the different static gains for clamping resistance variation, keeping the same duty cycle. The chart is presented in Figure 70.

Figure 70 – Static gain of the push-pull stage with a regenerative voltage clamper for resistance variation as a function of the parameterized current



Source: Own elaboration

It can be noticed that by increasing the clamping resistance, the static gain decreases for a low parameterized current. However, for a high parameterized current the static gain does not change considerably, even for different clamping resistances.

In addition, the clamping voltage can be parameterized. Then, by replacing equations 128 and 129 in 111 and dividing by the battery voltage, the expression 136 becomes dimensionless.

$$V_{Gnorm}(\alpha, d, \gamma, I_{op}) = \frac{V_G}{V_{bat}} = \left[\frac{\alpha(3-d) + \sqrt{\alpha^2(1+d)^2 + 2{I_{op}}^2\gamma}}{2\alpha(1-d)}\right] \tag{136}$$

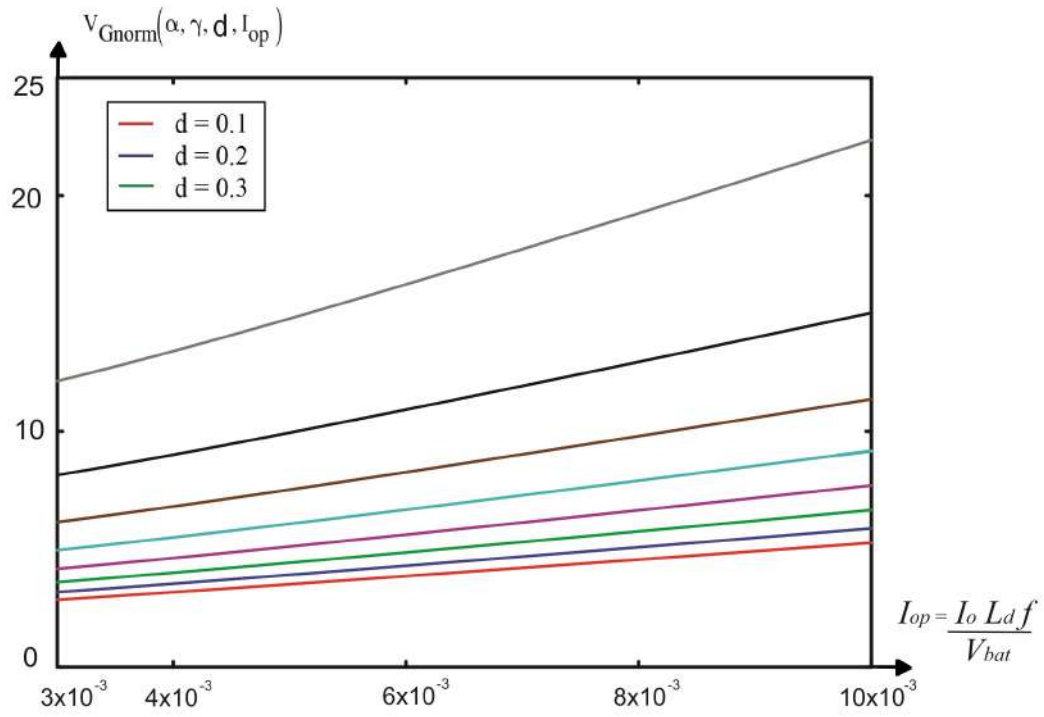
Furthermore, the parameterized clamping voltage for different duty cycles can be ploted as a function of the parameterized output current, as shown in Figure 71.

The greater the duty cycle and the current, the greater the clamping voltage.

Furthermore, as it was done for the static gain, a chart of the clamping voltage for different clamping resistances operating with a fix duty cycle can be ploted, as shown in Figure 72.

Then, the greater the clamping resistance, the greater the clamping voltage. Note that this chart considered a maximum clamping resistance of 100 Ω because a high resistance would change the graphic scales. So, it could be difficult to understand

Figure 71 – Clamping voltage for different duty cycles as a function of the parameterized current



Source: Own elaboration

the actual variation.

4.3.1.5 Voltage clamper circuit

The criteria of voltage ripple can be used to size the clamping capacitor, so it gives:

$$C_G = \frac{V_G - V_{bat}}{2 f R_g \Delta V_G} \tag{137}$$

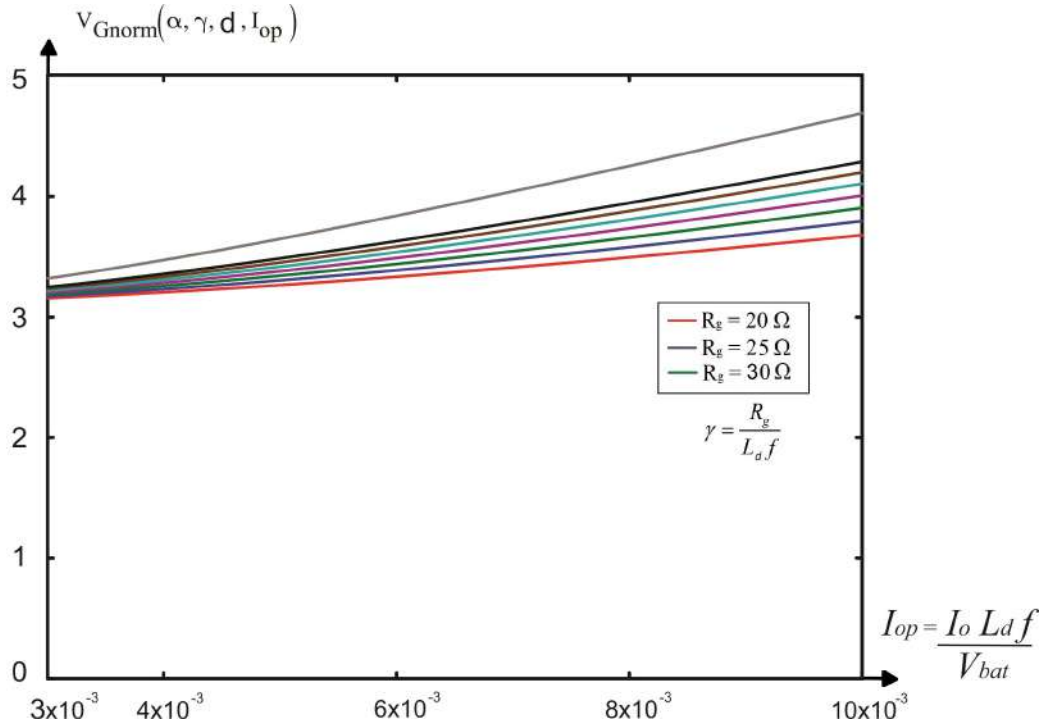
Which ΔV_G is defined by the converter designer.

Finally, the clamper sizing can be done by isolating the resistance (R_g) in the equation 111.

$$R_g = \frac{2\alpha(V_G - V_{bat})(d-1)(2V_{bat} - V_G + V_G d)}{{I_o}^2 L_d f} \tag{138}$$

Therefore, it is possible to calculate a clamping resistance needed to keep the design voltage across the Push-Pull Stage switches.

Figure 72 – Clamping voltage for different clamping resistances as a function of the parameterized current



Source: Own elaboration

Furthermore, the power dissipated in the clamping voltage circuit depends on its clamping resistance value, and it can be calculated through equation 139.

$$P_G := \frac{V_{bat}^2 \left[1 - \frac{\left[\alpha\cdot(d-3) - I_o\cdot\sqrt{\frac{\alpha^2\cdot(d+1)^2}{I_o^2} + \frac{2\cdot L_d\cdot R_g\cdot f}{V_{bat}^2}}\right]}{2\cdot\alpha\cdot(d-1)}\right]^2}{R_g} \tag{139}$$

Thus, the greater the clamping resistance, the smaller the power lost in the clamping circuit. So, increase the clamping resistance has an advantage.

4.3.2 Discontinuous Conduction Mode

4.3.2.1 Circuit operation

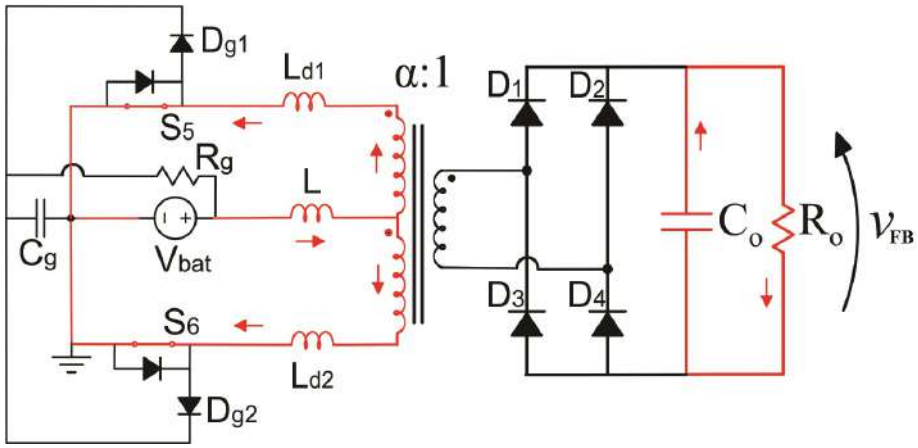
Although the converter should not operate in DCM, it is mandatory to study this operation in order to find a critical condition to operate in CCM. Therefore, the same methodology used in the CCM operation will be used.

Also, there are eight topological states, but half are symmetrical in one switching period. So, only four steps will be needed to understand the converter operation.

Time interval Δt_1 - The switch S_6 is conducting and the current in the inductor is null since the previous step. At t_0, the switch S_5 is gated on, then the inductor is

magnetized with a linear current. The first topological state is presented in Figure 73.

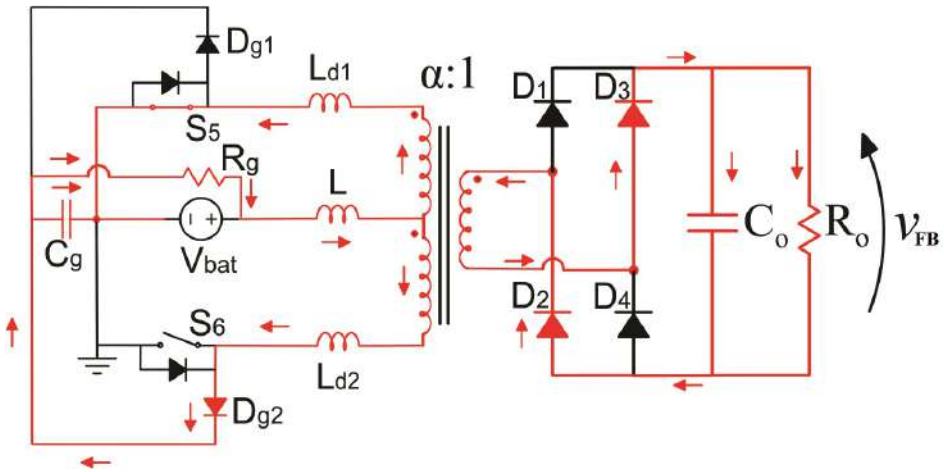
Figure 73 – First topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - DCM operation



Source: Own elaboration

Time interval Δt_2 - At t_1, the switch S_6 is turned off. Thus, the energy stored in the leakage inductance (L_{d2}) is transferred to the clamping capacitor through clamping diode D_{g2}. Hence, the energy stored in the inductor (L) is transferred to the load through the polarization of diodes D_2 and D_3. The second topological state is presented in Figure 74.

Figure 74 – Second topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - DCM operation

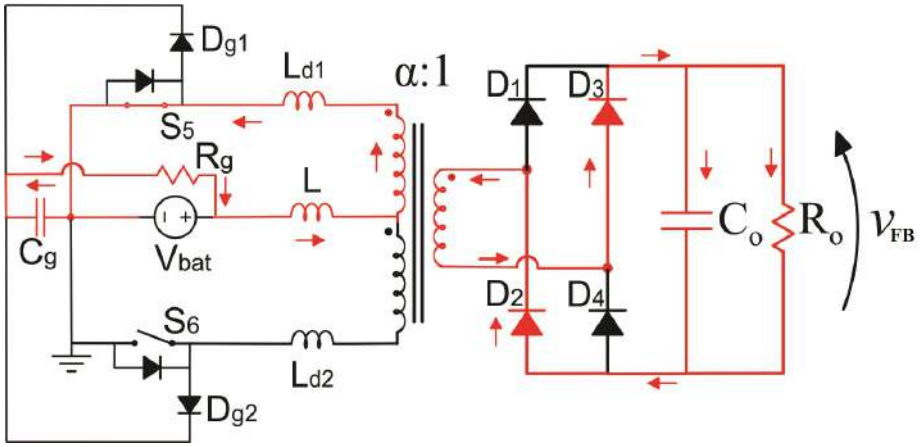


Source: Own elaboration

Time interval Δt_3 - When the energy stored in the leakage inductance becomes

zero, the clamping diode stops to conduct current. Therefore, the power stored in the clamping capacitor demagnetizes through the clamping resistance and goes to the load together with the inductor current. The third topological state is presented in Figure 75.

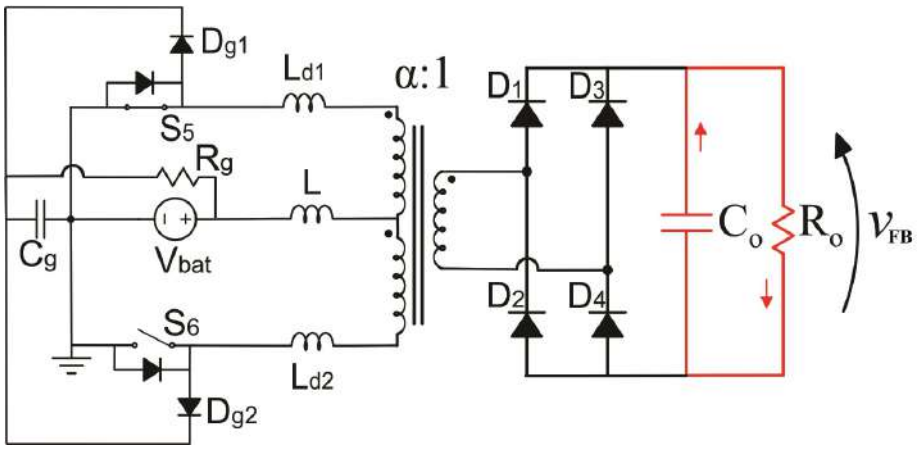
Figure 75 – Third topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - DCM operation



Source: Own elaboration

Time interval Δt_4 - At t_3, the inductor is completely demagnetized and then all the diodes stop to conduct. So, in this topological state only the output capacitor transfer power to the load. The fourth topological state is presented in Figure 76.

Figure 76 – Fourth topological state of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - DCM operation

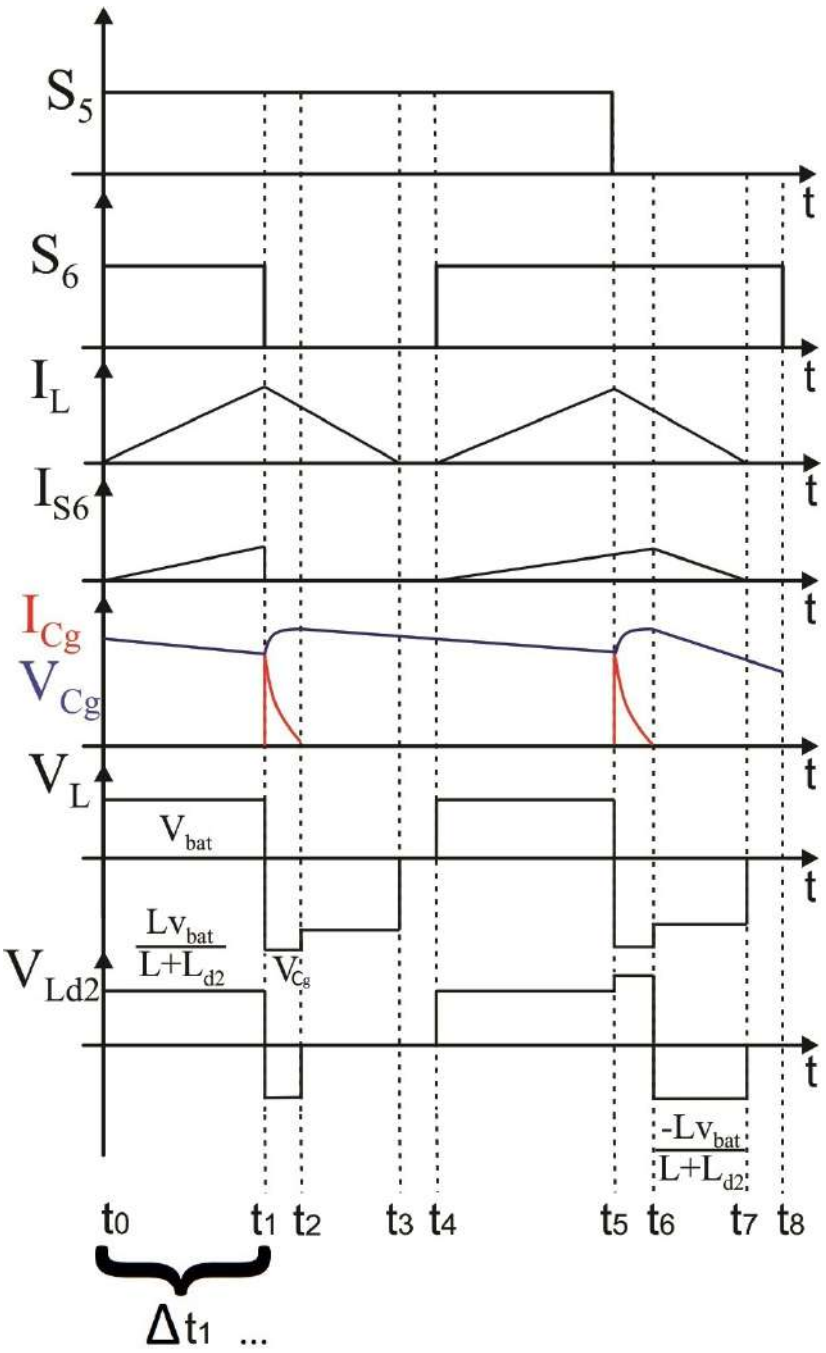


Source: Own elaboration

4.3.2.2 Waveforms

From the topological states studied above, it is achievable to find the converter mainly waveforms operating in the discontinuous conduction mode, and then do some mathematical analysis. The waveforms are presented in Figure 77.

Figure 77 – Main waveforms of the DC-DC current-fed push-pull converter with leakage inductance and partially regenerative voltage clamper - DCM operation



Source: Own elaboration

4.3.2.3 Output Characteristics

First of all, in order to find the critical CCM point, some expressions can be defined by analyzing Figure 77.

$$\Delta t_1 = \frac{dT_S}{2} \tag{140}$$

$$\Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 = \frac{T_S}{2} \tag{141}$$

In addition, the average current in the output diodes are:

$$I_o = 2I_{Dmd} \tag{142}$$

$$I_{Dmd} = \frac{\alpha I_{L\max}(\Delta t_2 + \Delta t_3)}{2T_S} \tag{143}$$

Note that in this first analysis the current of the clamping resistor is not considered, in order to understand the circuit operation and after that add some complexity.

The time intervals the store energy in the inductor is ΔT_1, so its current expression can be written as:

$$I_{L\max} = \frac{V_{bat}\Delta t_1}{L} \tag{144}$$

Then, by replacing 140 in 144 leads to:

$$I_{L\max} = \frac{V_{bat}dT_S}{2L} \tag{145}$$

At the time intervals ΔT_2 and ΔT_3, the inductor is transferring energy and then its current becomes zero in the end of the period, so the following expression can be written:

$$I_{L\max} - \frac{(\alpha V_{FB} - V_{bat})(\Delta t_2 + \Delta t_3)}{L} = 0 \tag{146}$$

If 145 be replaced in 146, it leads to:

$$\frac{V_{bat}dT_S}{2L} = \frac{(\alpha V_{FB} - V_{bat})(\Delta t_2 + \Delta t_3)}{L} \tag{147}$$

Isolating the term $(\Delta t_2 + \Delta t_3)$ in the equation 147 gives:

$$(\Delta t_2 + \Delta t_3) = \frac{V_{bat}dT_S}{2(\alpha V_{FB} - V_{bat})} \tag{148}$$

If 144 be replaced in 143, it leads to:

$$I_{Dmd} = \frac{\alpha V_{bat}\Delta t_1(\Delta t_2 + \Delta t_3)}{2Lf} \tag{149}$$

By substituting 149 in 142, gives:

$$I_o = \frac{\alpha V_{bat} \Delta t_1 (\Delta t_2 + \Delta t_3)}{Lf} \tag{150}$$

Finally, if 140 and 148 be replaced in 150, gives:

$$I_o = \frac{\alpha {V_{bat}}^2 d^2}{4Lf(\alpha V_{FB} - V_{bat})} \tag{151}$$

It is possible to realize that the voltage output depends on the load current, different from the CCM operation.

Therefore, in order to find the critical CCM operation point, the analysis consider that the inductor current becomes zero in a half cycle, so Δt_4 is zero.

$$\Delta t_4 = \frac{T_S}{2} - \Delta t_1 - (\Delta t_2 + \Delta t_3) \tag{152}$$

Thus, if 140 and 148 be replaced in 152, leads to:

$$\Delta t_4 = \frac{T_S}{2} - \frac{dT_S}{2} - \frac{V_{bat} d T_S}{2(\alpha V_{FB} - V_{bat})} \tag{153}$$

With some algebraic manipulations, the equation 154 is found.

$$\Delta t_4 = \frac{(1-d)\alpha V_{FB} - V_{bat}}{2f(\alpha V_{FB} - V_{bat})} \tag{154}$$

The average current in the inductor is:

$$I_{Lmd} = \frac{V_{bat} d T_S}{2L} \tag{155}$$

From the state that the energy is transferred to the load, it is possible to obtain:

$$I_{L\max} = \frac{(\alpha V_{FB} - V_{bat})(1-d)}{2fL} \tag{156}$$

Finally the critical inductance current can be defined by replacing the ideal static gain 63 in 155.

$$I_{Lcrit} = \frac{\alpha V_{FB} d(1-d)}{2fL} \tag{157}$$

The calculus of the output critical current should consider the influence of the clamping resistor current, so:

$$I_{RG} = \frac{f I_{L\max} \Delta t_2}{2} \tag{158}$$

The time interval that the clamping diode conducts is equals to:

$$\Delta t_2 = \frac{L_d}{\left(\frac{V_G}{2} - \alpha V_{FB}\right)} I_{Lmd} \tag{159}$$

Then, by changing 159 in 158 leads to:

$$I_{RG} = \frac{f I_{L\max} L_d I_{Lmd}}{(V_G - 2\alpha V_{FB})} \tag{160}$$

After that, it is mandatory to find the clamping voltage, so:

$$V_G - I_{RG} R_g - V_{bat} = 0 \tag{161}$$

Then, if 160 be replaced into 161, leads to:

$$V_G = \frac{(V_{bat} + 2\alpha V_{FB}) + \sqrt{(V_{bat} - 2\alpha V_{FB})^2 + \frac{L_d R_g \alpha V_{FB} V_{bat}^2 d^3}{4fL^2(\alpha V_{FB} - V_{bat})}}}{2} \tag{162}$$

Finally, the current in the clamping resistor can be found by substituting 162 in 161.

$$I_{RG} = \frac{(V_{bat} + 2\alpha V_{FB}) + \sqrt{(V_{FB} - 2\alpha V_{FB})^2 + \frac{L_d R_g \alpha V_{FB} V_{bat}^2 d^3}{4fL^2(\alpha V_{FB} - V_{bat})}} - 2V_{bat}}{2R_g} \tag{163}$$

Now, by replacing 154 and 148 in 149 gives:

$$I_{Dmd} = \frac{\alpha d^2 V_{bat}^2}{4fL(\alpha V_{FB} - V_{bat})} - 2\alpha I_{RG} \tag{164}$$

In addition, the static gain for DCM can also be found with equation 122. So, by substituting 155,162 and 163 in 122, it gives:

$$q_{dcm} = a + b + c \tag{165}$$

which:

$$a = \frac{\alpha V_{bat} V_{FB} d^2}{4LfI_o(\alpha V_{FB} - V_{bat})} \tag{166}$$

$$b = -\frac{\sqrt{(V_{bat} - 2\alpha V_{FB})^2 - \frac{L_d R_g \alpha V_{FB} V_{in}^2 d^3}{4L^2 f(V_{bat} - \alpha V_{FB})}} + 2\alpha V_{FB} - V_{bat}}{2R_g I_o} \tag{167}$$

$$c = -\frac{1}{I_o R_g V_{bat}} \left(\frac{\sqrt{(V_{bat} - 2\alpha V_{FB})^2 - \frac{L_d R_g \alpha V_{FB} V_{in}^2 d^3}{4L^2 f(V_{bat} - \alpha V_{FB})}} + 2\alpha V_{FB} - V_{bat}}{2} \right)^2 \tag{168}$$

It is possible to analyze through this equation that the static gain of the DCM operation depends on the load. Also, the equation 165 is complex because there are output voltage in both sides of the equation.

Furthermore, the study of the critical inductance and output current is necessary. So, the following equations shows how to operate the converter in CCM.

Then, if it is considered a constant output voltage, the critical CCM current can be found by substituting equation 164 in 142.

$$I_{ocrit} = \frac{\alpha d^2 V_{bat}^2}{4fL(\alpha V_{FB} - V_{bat})} - 2\alpha I_{RG} \tag{169}$$

Finally, if the equation 163 be replaced in 169, it leads to:

$$I_{ocrit} = a - b \tag{170}$$

Which a and b are defined as:

$$a = \frac{\alpha d^2 V_{bat}^2}{4fL(\alpha V_{FB} - V_{bat})} \tag{171}$$

$$b = \alpha \frac{2\alpha V_{FB} - V_{bat} + \sqrt{(V_{bat} - 2\alpha V_{FB})^2 + \frac{L_d R_g \alpha V_{FB} V_{bat}^2 d^3}{4fL^2(\alpha V_{FB} - V_{bat})}}}{R_g} \tag{172}$$

In addition, it is important to find the critical inductance to a CCM operation. A good approach for the average inductor current for this case is:

$$I_{Lavg} = \frac{I_o}{\alpha(1-d)} \tag{173}$$

Finally, if the equation 155 be replaced into 173, 174 is found, which represents the critical inductance for a CCM operation.

$$L_{crit} = \frac{\alpha V_{bat} d(1-d)}{2fI_o} \tag{174}$$

4.3.2.4 Parameterization

First of all, equation 165 is too complex to be parameterized. Therefore, the DCM static gain will be simplified to be parameterized. So, if the leakage inductance and clamping resistance are zero, the following DCM static gain is found:

$$q_{dcm} = \frac{V_{bat} d^2}{4fLI_o} + \frac{1}{\alpha} \tag{175}$$

Note that equation 175 is similar to the DCM boost converter static gain, as presented in (MARTINS; BARBI, 2006).

However, the static gain cannot be parameterized yet because it considers the push-pull inductance instead of the leakage inductance. Therefore, with the variables defined in table 2, the push-pull inductance can be substituted by the leakage inductance using the following approximation shown in equation 176.

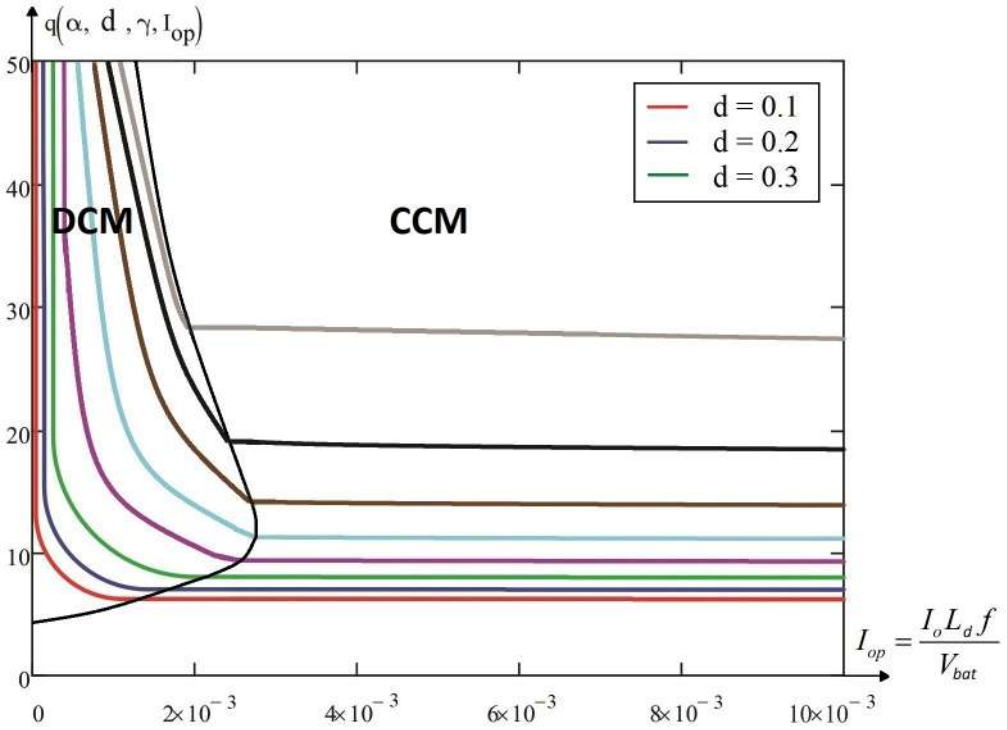
$$L = 40L_d \tag{176}$$

Then, this simplified static gain can be parameterized with the same parameters used in the CCM operation, as presented in equation 177.

$$q_{dcm}(\alpha, \gamma, d, I_{op}) = \frac{d^2}{160 I_{op}} + \frac{1}{\alpha} \tag{177}$$

Finally, the chart in Figure 78 represents the static gain parameterized for the DCM and CCM operation for different duty cycle as a function of the parameterized current.

Figure 78 – Static gain of the Push-Pull Stage with a partially regenerative voltage clamper for CCM and DCM operations



Source: Own elaboration

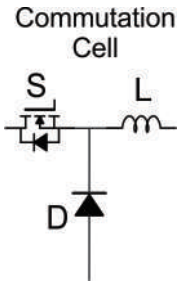
This chart was done by interpolation method using the software MathCad. The DCM static gains are plotted until the parameterized current reachs the critical current. Then, after that the CCM static gains are plotted to trace the DCM and CCM limits.

4.4 UNIDIRECTIONAL ISOLATED DC-DC CURRENT-FED PUSH-PULL CONVERTER WITH LEAKAGE INDUCTANCE AND ACTIVE VOLTAGE CLAMPER

There are some active voltage clampers that can be applied in the current-fed push-pull converter. However, to verify new possibilities of voltage clampers for the push-pull converter, this Dissertation Thesis proposes to modify the circuit of the regenerative voltage clamper by introducing a commutation cell on it. The commutation

cell, represented in Figure 79, can be used to create a static converter the performs like a snubber circuit.

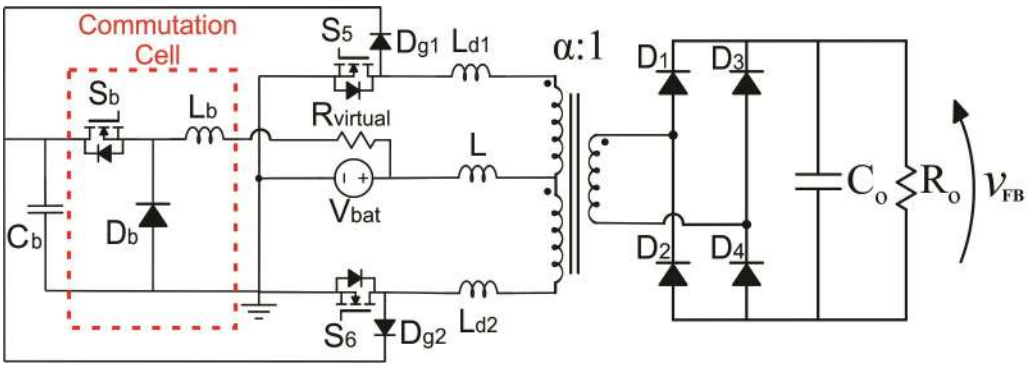
Figure 79 – Commutation Cell



Source: Own elaboration

Furthermore, it is possible to substitute the clamping resistance of the regenerative circuit for an inductor, and add a virtual resistance. Then, the circuit becomes a Current-fed Buck Converter, as shown in Figure 80.

Figure 80 – Unidirectional isolated DC-DC current-fed push-pull stage with leakage inductance and the buck converter



Source: Own elaboration

All the buck analysis can be applied to size this active snubber. Also, all the analysis made for the regenerative voltage clamper is validated for the unidirectional Isolated DC-DC Current-fed Push-Pull Converter with the Buck Converter operating as a voltage clamper. Thus, the output characteristics will not be necessary again, as they remain the same.

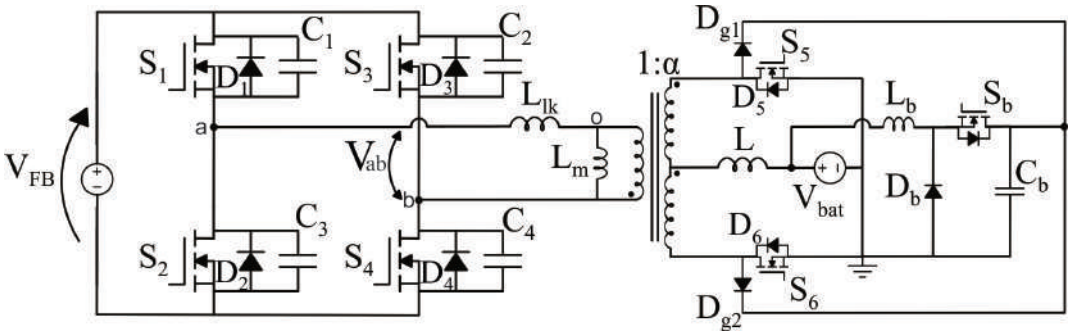
Besides, the circuit operation and waveforms of the Push-Pull stage applying the Buck Converter as a snubber are equal to its regenerative snubber version. Therefore, it will not be described again because the complete operation will be shown in the Isolated Bidirectional DC-DC Converter Based on the Integration of the Full-Bridge and the Current-Fed Push-Pull Converters.

5 STUDY OF THE ISOLATED BIDIRECTIONAL DC-DC CONVERTER

The DC-DC Full Bridge ZVS-PWM Stage studied in chapter 3 and the Current-Fed Push-Pull Stage studied in chapter 4 are connected to perform a Bidirectional Converter. In fact, the connection of both stages is equal to replace the diodes for switches on the unidirectional converters and apply a modulation technique for all MOSFETs. There must be an appropriate modulation to transfer power from one source to another, regardless the current's direction.

Then, the Isolated Bidirectional DC-DC Converter based on the integration of the DC-DC Full-Bridge ZVS-PWM and current-fed Push-Pull converters is presented in Figure 81.

Figure 81 – Isolated Bidirectional DC-DC Converter clamped with a buck converter



Source: Own elaboration

It can be noticed the buck converter acting as a voltage clamper. The Bidirectional Converter requires a voltage clamping circuit connected to switches S_5 and S_6 in order to limit the voltage that they must support, as studied in chapter 4, because in some operation steps the energy stored on the leakage inductance of the transformer and the anti-parallel diodes of the push-pull switches are discharged at the same switches, which increases dramatically its voltage.

To reduce losses in the clamping circuit, a transformer with a small leakage inductance is required so that it does not accumulate much energy, but that same inductance has a fundamental role in the soft commutation.

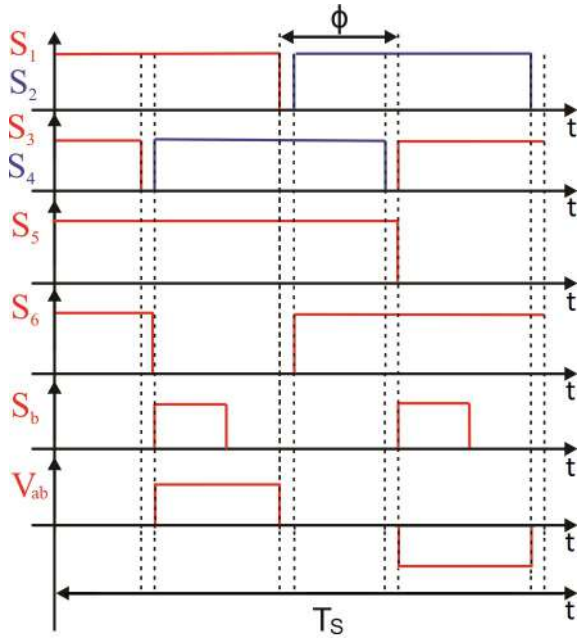
Furthermore, as the converter is bidirectional, it has two power flow directions, positive and negative. The positive direction refers to the power transfer from source V_{FB} to V_{bat} and the negative refers to the opposite power flow.

Besides, the output characteristics obtained for the unidirectional converters in the previous chapters remains the same for the bidirectional converter. Thus, this chapter will focus in the circuit operation, waveforms and stresses of the Isolated Bidirectional DC-DC Converter.

5.1 GATE SIGNALS

First of all, in order to understand the operation steps of the converter, it is necessary to visualize the gate signals of each switch. Thus, as can be seen in Figure 82, the signals of each leg are complementary and consequently the voltage V_{ab} and the power transferred to the battery is controlled by the lagging angle between the command signals of legs (Φ) in the Full-Bridge Stage.

Figure 82 – Gate signals of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

This is the same modulation used in the unidirectional converters, so all the analysis remain the same. Also, it is included a dead-time between the complementary switches of each leg to verify soft switching.

Moreover, the modulation of the Current-Fed Push-Pull Stage is performed, so switch S_5 is gated off at the time the voltage V_{ab} is negative and switch S_6 is turned off at the time the voltage V_{ab} is positive so there will be no short-circuit at the output with a voltage induced at the secondary side.

Also, all the switches are MOSFETs because of the frequency, current and voltage range that the circuit operates, but mainly because of the lower conduction loss in comparison with IGBT, since the converter operates in ZVS.

In addition, the calculation of the buck's duty cycle is represented in equation

178.

$$d_b = \frac{V_{bat}}{V_{Cb}} \tag{178}$$

Therefore, buck's operating frequency should be two times the bidirectional converter frequency in order to have a symmetrical operation. This higher frequency decreases the inductor size and volume.

5.2 CIRCUIT OPERATION

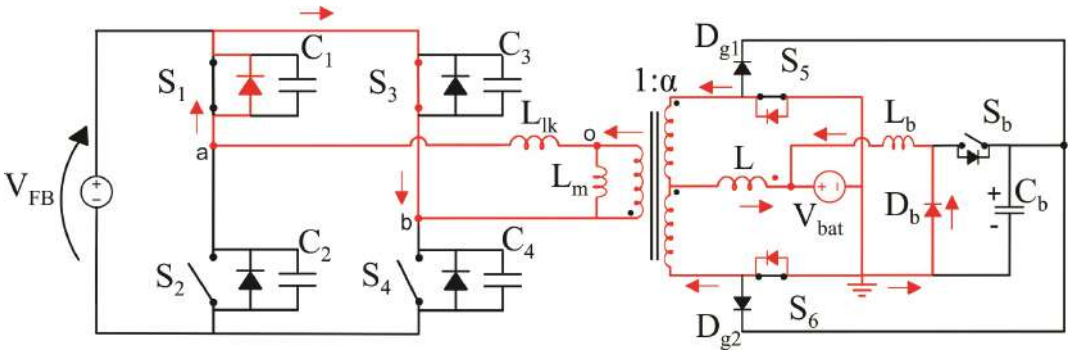
The analysis of the circuit presented in Figure 23 applying the modulation of Figure 82 will be divided for the positive and negative power flow, as mentioned previously.

5.2.1 Positive power flow

In this analysis, the topological states are symmetric for half commutation period. So, although there are fourteen topological states, only seven will be needed to understand the circuit's operation.

Time interval Δt_1 - At time t_0, the switches S_1, S_3, S_5 and S_6 are turned on, so the voltage across the transformer (V_{ab}) is zero. However, the current tends to flow through diode D_1 because it has a lower resistance than the MOSFET. In addition, the transformer secondary current continues to flow through switch S_6 and the current stored in the buck converter is discharged in the battery because of the previous step. The topological state that represent this time interval is shown in Figure 83.

Figure 83 – First topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter

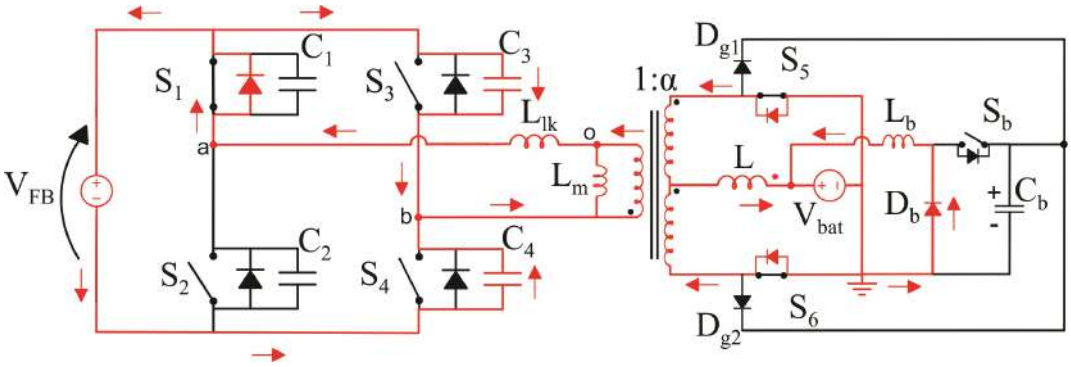


Source: Own elaboration

Time interval Δt_2 - This operation step represents the period which soft switching occurs. Therefore, when the switch S_3 is switched off and S_4 has not been switched on yet, the current in the primary flows through the capacitors C_3 and C_4, charging and discharging it, respectively. In addition, the secondary side is short-circuited, since the

voltage in the primary is zero. The topological state that represent this time interval is shown in Figure 84.

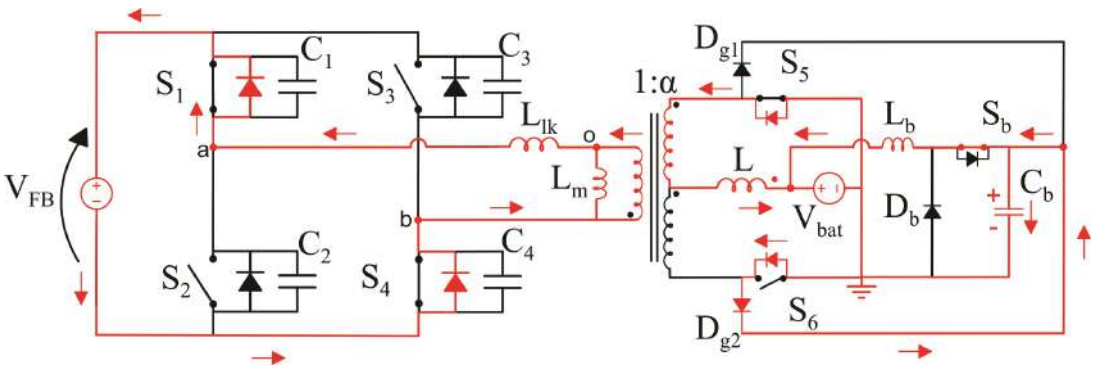
Figure 84 – Second topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Time interval Δt_3 - At time t_2, switch S_4 is gated on. Thus, as the current in the leakage inductance is increasing linearly and negative, the current flows through the diodes D_1 and D_4 until it reaches zero, when starts the next operation step. In addition, due to the previous steps, the anti-parallel diode D_6 of the switch S_6 has an energy stored, what it is called reverse recovery, and its current flows through the clamping circuit because the diode D_{g2} is forward biased. Furthermore, this energy charges the buck capacitor and inductor. Then, the equivalent circuit of the buck operation is a current source in parallel with buck's capacitor and the commutation cell. Also, the output of this equivalent circuit is the battery voltage.The topological state that represent this time interval is shown in Figure 85.

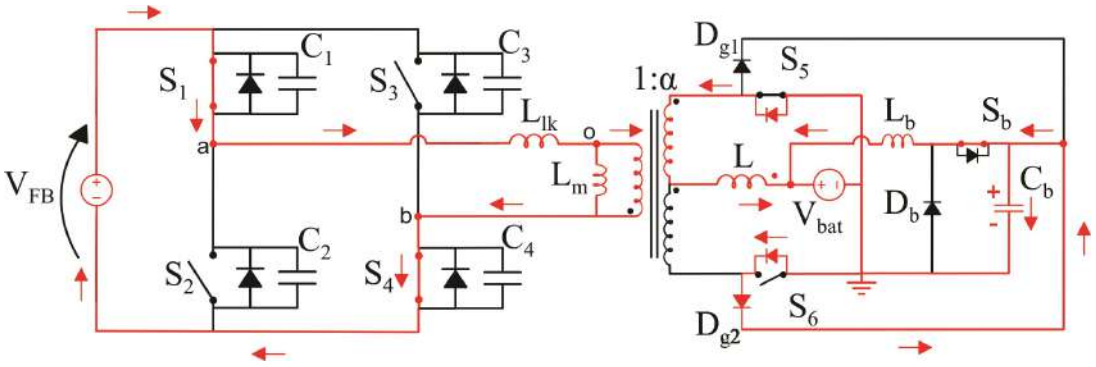
Figure 85 – Third topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Time interval Δt_4 - When the current in the leakage inductance is zero, it starts to grow linearly until it reaches the nominal value. In this step, the voltage at the transformer primary side is still zero. That step represents a loss of duty cycle, because the secondary is short-circuited. In addition, the current flows through the switches S_1 and S_4 because the current in the leakage inductance has changed direction. The topological state that represent this time interval is shown in Figure 86.

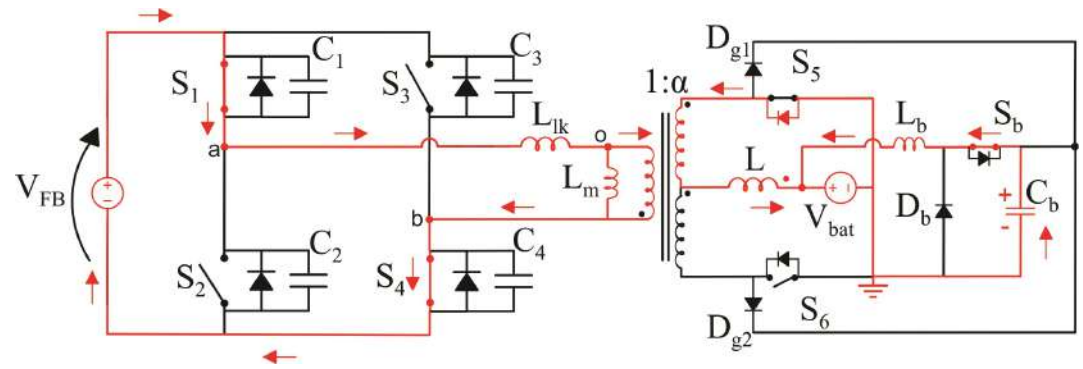
Figure 86 – Fourth topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Time interval Δt_5 - At time t_4, the current in the leakage inductance reaches its nominal value, so the voltage across the terminals of the primary of the transformer is not zero anymore, so the power is transferred through the switch S_5. As the energy from the reverse recovery ends and the buck switch is still turned on, the energy stored in the buck capacitor keep discharging into the battery through the inductor. The topological state that represent this time interval is shown in Figure 87.

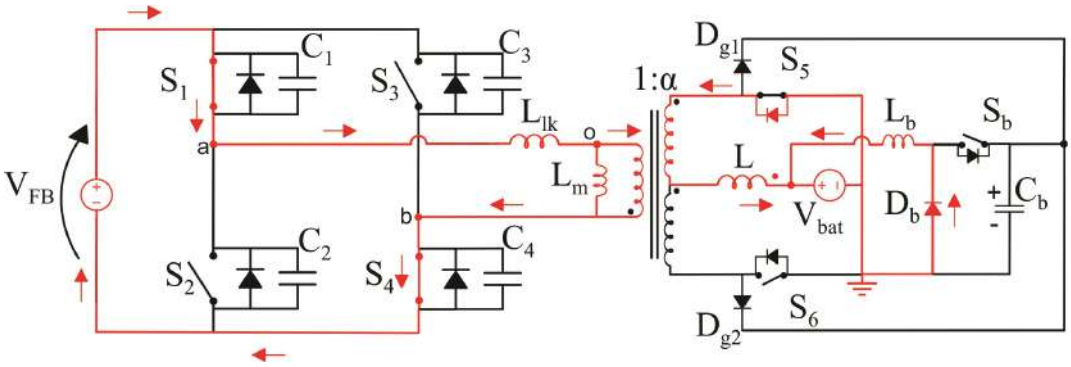
Figure 87 – Fifth topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Time interval Δt_6 - This time interval is similar to the previous one, the difference is that the buck converter is gated off, so only its inductor provides energy to the battery. The topological state that represent this time interval is shown in Figure 88.

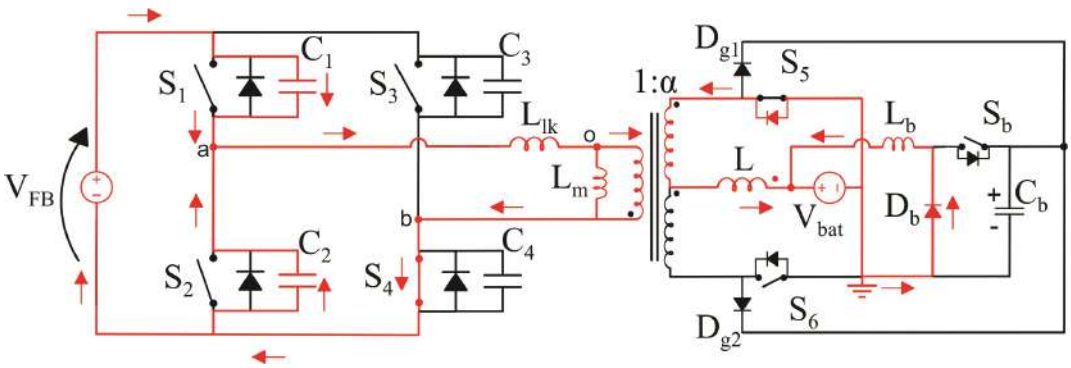
Figure 88 – Sixth topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Time interval Δt_7 - At t_6, there is a dead-time between switches S_1 and S_2. So, when S_1 turns off and S_2 has not been turned on yet, the voltage across the transformer primary side is zero, so the output short-circuited. In addition, the current stored in the leakage inductance flows through the capacitors C_1 and C_2, charging and discharging, respectively. Furthermore, to achieve soft commutation, the capacitors need to be charged and discharged in a period of time shorter than the dead-time imposed on the switches, as studied before. Also, as the buck switch is turned off, the buck inductor keep providing energy to the battery.The topological state that represent this time interval is shown in Figure 89.

Figure 89 – Seventh topological state for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter

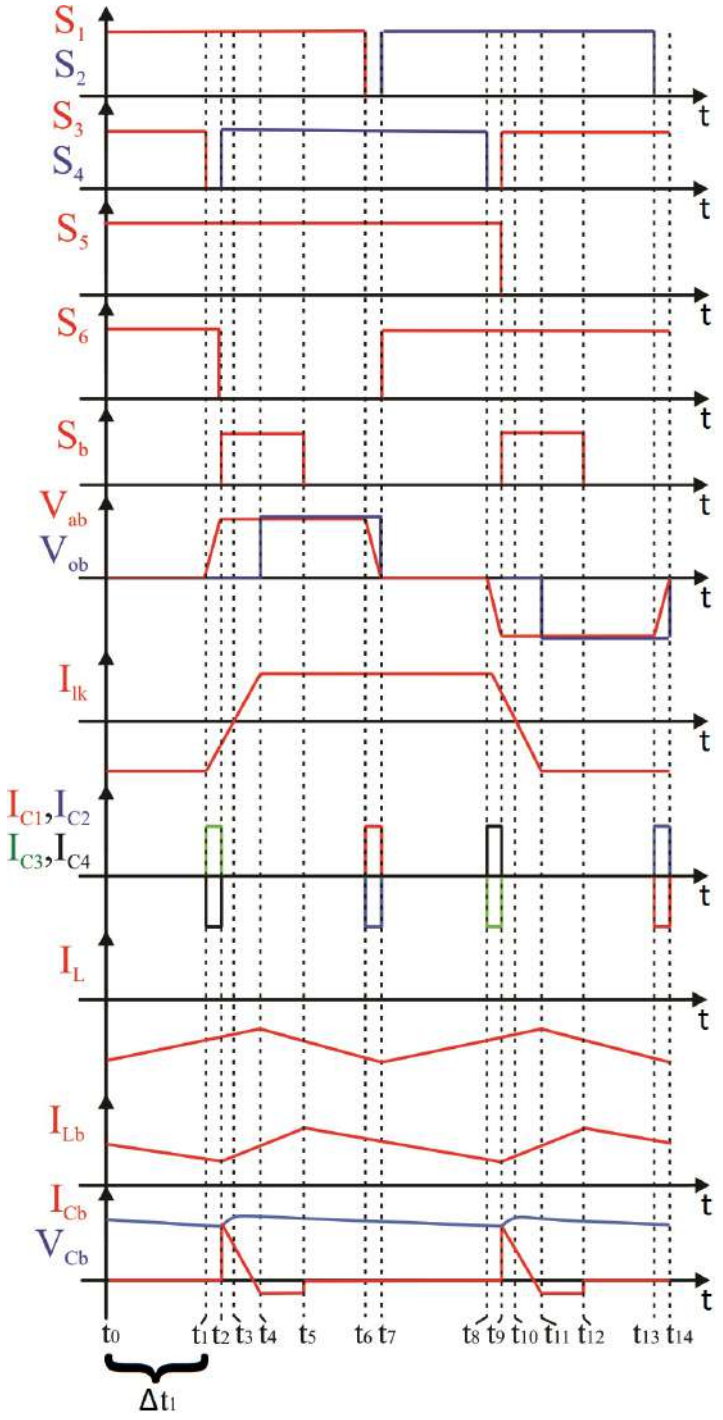


Source: Own elaboration

5.2.1.1 Waveforms

The time intervals and main waveforms of the converter operating with a positive power flow is presented in Figure 90, to clarify its operation.

Figure 90 – Waveforms for the positive operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Although the voltage stresses are not represented in Figure 90, their maximum

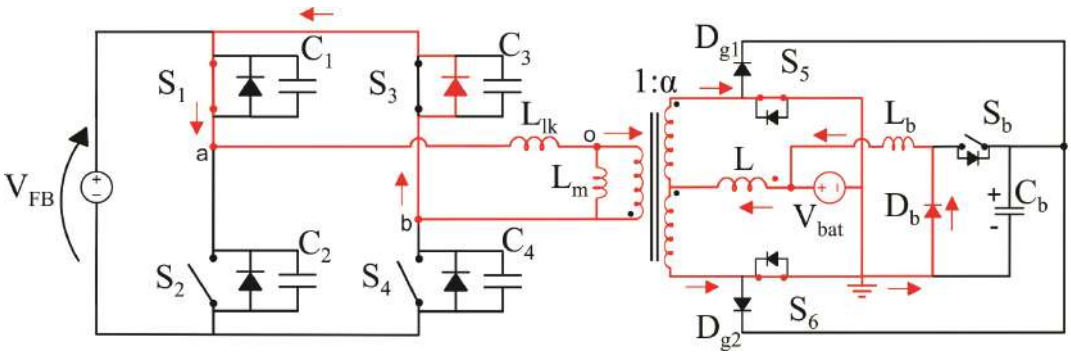
values will be presented separately further in this chapter.

5.2.2 Negative power flow

The converter with power flow has also fourteen topological states, but half of those are complementary. So, only seven time intervals will be needed to understand it.

Time interval Δt_1 - In the first stage of operation, the switches S_5 and S_6 are gated on. Thus, there is zero voltage across V_{ab}. As the switches S_1 and S_3 are turned on, a current stored in the leakage inductance due to the previous step circulates through those switches and in the push-pull side this current start to change its trajectory from switch S_6 to S_5 in a linear way because it is short-circuited. The topological state that represent this time interval is shown in Figure 91.

Figure 91 – First topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



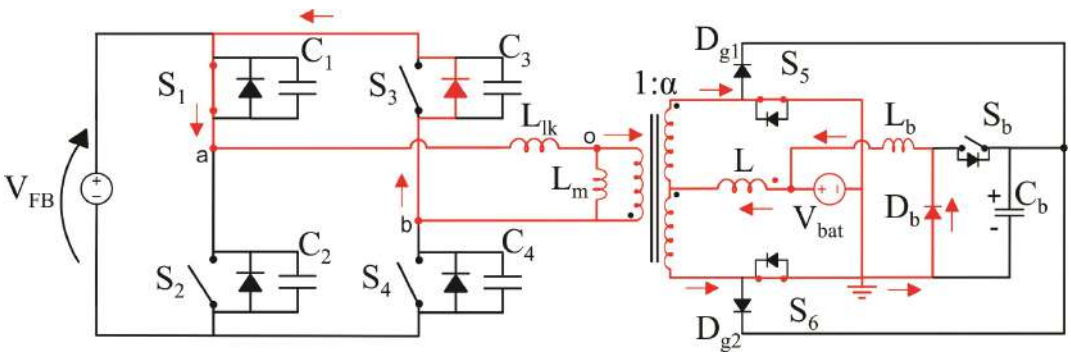
Source: Own elaboration

Time interval Δt_2 - At time t_2, switch S_3 is gated off while S_4 has not been triggered on yet. But, there is an intrinsic diode in anti-parallel with the switch S_3. Therefore, the current flows through this diode, keeping the operation step equals to the previous step. So, as the current does not flow through capacitors C_3 and C_4, in this power flow the full-bridge does not have soft commutation. The topological state that represent this time interval is shown in Figure 92.

Time interval Δt_3 - At time t_3, switch S_4 is turned on and S_6 is turned off. Thus, there is a positive voltage across V_{ab} and the current flows through the switches D_1 and D_4. The reverse recovery current of the diode D_6 and the leakage current of transformer is transferred to the buck capacitor and the battery through the polarization of diode D_{g2}. In addition, the current in the full-bridge switches has this direction because there is an energy stored in the leakage inductance that imposes this condition. The topological state that represent this time interval is shown in Figure 93.

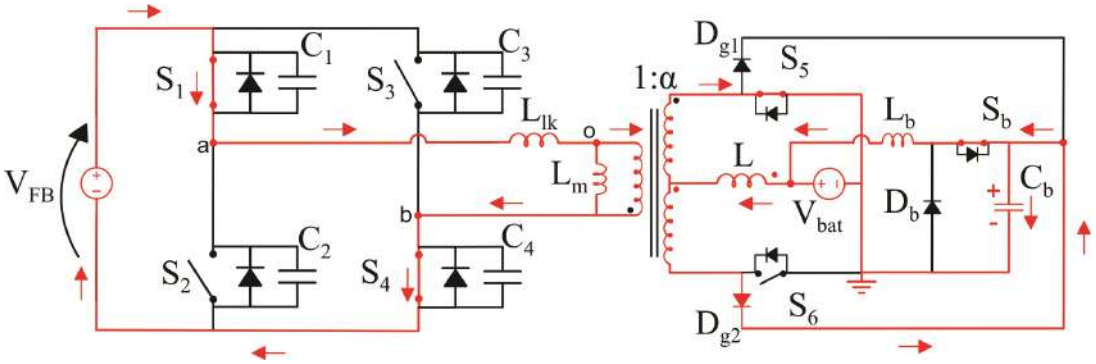
Time interval Δt_4 - In the fourth step of operation, the buck converter continues to transfer energy to the battery and all the power flows through the switch S_5. In this

Figure 92 – Second topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

Figure 93 – Third topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

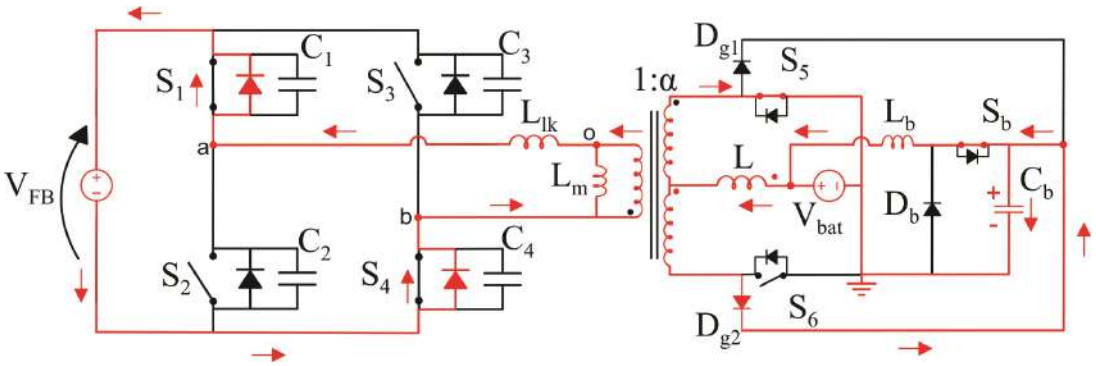
step the current that flows through the leakage inductor is negative, so it flows through the switches' anti-parallel diodes as it has changed its direction. The topological state that represent this time interval is shown in Figure 94.

Time interval Δt_5 - At time t_4, the current in the leakage inductor has been completely discharged, then the buck capacitor discharges in the battery keeping the voltage across the push-pull switches clamped. Meanwhile, the push-pull converter remains the same as the previous step. The topological state that represent this time interval is shown in Figure 95.

Time interval Δt_6 - This time interval is similar to the previous one, the only difference is that the buck converter is gated off, so its capacitor does not provide energy to the battery anymore. The topological state that represent this time interval is shown in Figure 96.

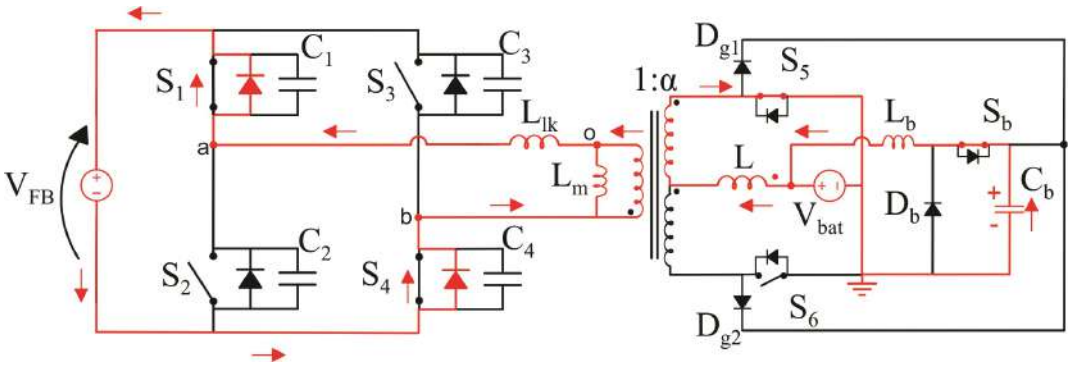
Time interval Δt_7 - At time t_6, switch S_1 turns off while S_2 has not been triggered on yet. In the full-bridge converter the current keeps flowing through D_1 and D_4. In the

Figure 94 – Fourth topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



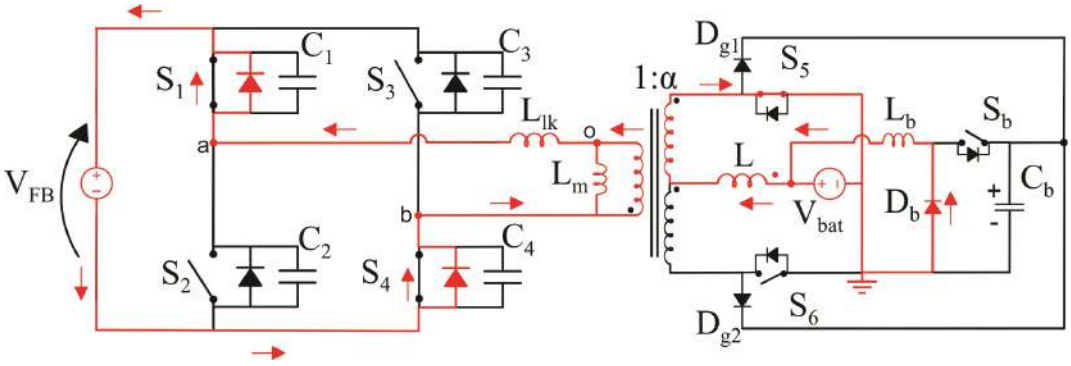
Source: Own elaboration

Figure 95 – Fifth topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

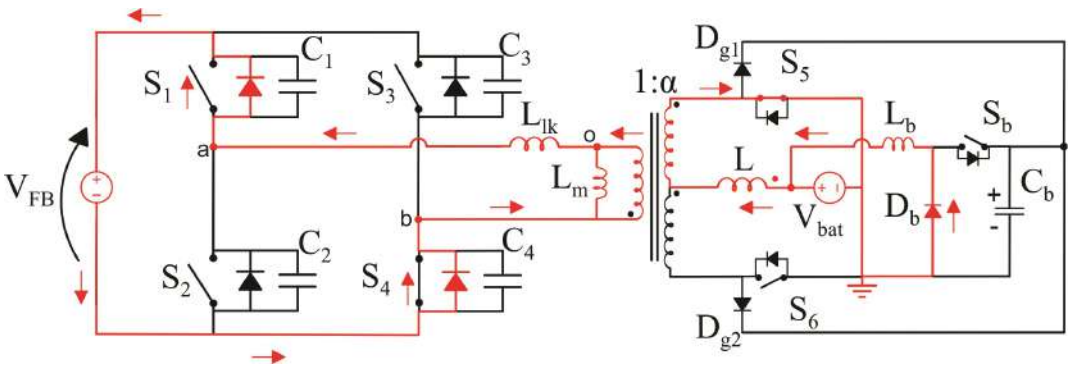
Figure 96 – Sixth topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

push-pull the currents on switches S_5 and the buck converter remains equals to the previous step. The topological state that represent this time interval is shown in Figure 97.

Figure 97 – Seventh topological state for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

5.2.2.1 Waveforms

The time intervals of the circuit operating with a negative direction is presented in Figure 98. This Figure also shows the main waveforms to clarify the converter's operation.

It is possible to analyze that the converter operating in the negative power flow does not present soft commutation. The diode in anti-parallel with the MOSFETs of the Full-Bridge side are direct polarized at the dead-time interval, which the capacitor of these MOSFETs should be charging.

Then, as the converter operates with hard switching at the Full-Bridge side, it is expected a lower efficiency for the converter operating in the negative power flow.

Although the voltage stresses are not represented in Figure 98, their maximum values will be presented separately further in this chapter.

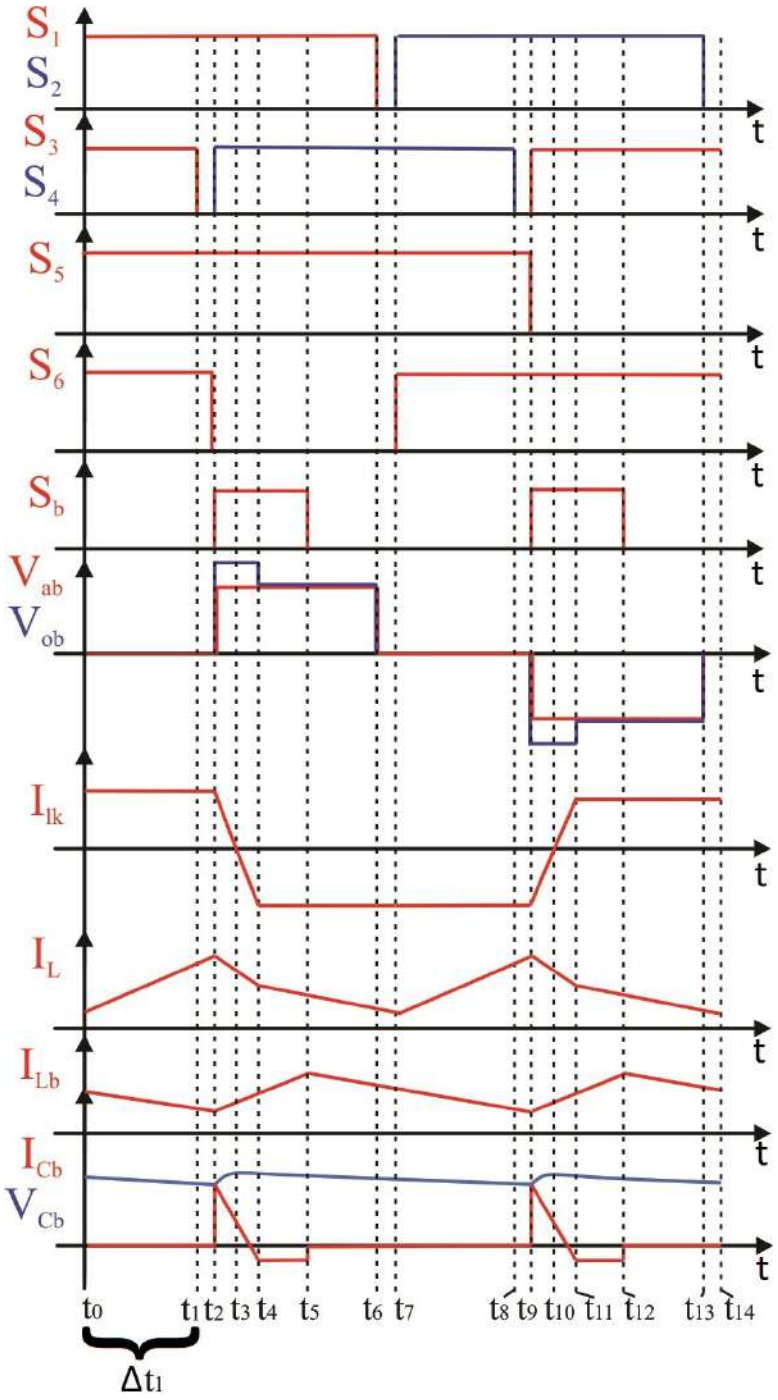
5.3 VOLTAGE STRESSES

Calculate the voltage stresses across the circuit's components is fundamental to size the prototype. Therefore, this section shows some equations that will be used in the next chapters.

First of all, the voltage across the switches on the Full-Bridge Stage is equal to the input voltage.

$$V_{SFB} = V_{FB} \tag{179}$$

Figure 98 – Waveforms for the negative operation of the Isolated Bidirectional DC-DC Converter and Buck Converter



Source: Own elaboration

The voltage across the switches on the Push-Pull Stage is equal to the voltage of the buck capacitor.

$$V_{SPP} = V_{Cb} \tag{180}$$

Also, the voltage across the switch and diode of the buck converter and the clamping diodes are equal to equation 180.

Furthermore, the maximum voltage across the primary and secondary side of the transformer can be calculated as shown in equations 181 and 182.

$$V_{TP} = \frac{V_{Cb}}{2\alpha} \tag{181}$$

$$V_{TS} = \frac{V_{Cb}}{2} \tag{182}$$

5.4 CURRENT STRESSES

The current stresses in the circuit's components are other important parameter to size the prototype, because it defines the thermal stresses of the components.

There are some average and RMS current values for each power flow direction. However, those values are equal since the waveforms are mirrored for both power flow. Therefore, only one equation will be established for each component.

First of all, the maximum current in the Full-Bridge Stage is defined in equation 183.

$$I_{lk} = \frac{\alpha P_{out}}{V_{bat}} \tag{183}$$

However, the converter's waveforms present more defined topological states, so they will be redefined as follows:

$$\Delta t_1 = (1 - D)\frac{T_s}{2} \tag{184}$$

While Δt_1 remains the same as calculated in chapter 3, Δt_2 and Δt_7 represents now the dead-time between the switches gate signals, as follows:

$$\Delta t_2 = \Delta t_7 = \Delta t_d \tag{185}$$

Also, Δt_3 and Δt_4 represent the time that Buck's capacitor is being charged.

$$\Delta t_3 = \Delta t_4 = (D - D_{ef})\,\frac{T_s}{2} - \Delta t_d \tag{186}$$

Furthermore, Δt_5 is found with equation 187.

$$\Delta t_5 = \frac{L_b I_{Lb}}{2V_{Cb}} \tag{187}$$

In addition, Δt_6 is represented by equations 188.

$$\Delta t_6 = D_{ef}\frac{T_s}{2} - \Delta t_5 \tag{188}$$

Finally, the time interval that leakage inductance demagnetize can be approximated as follows:

$$\Delta t_{lk} = \frac{I_{lk}L_{lk}}{V_{FB}} \tag{189}$$

With these time equations the current stresses of the bidirectional converter can be found. Therefore, the average current across the switches S_1 and S_2 located in the full-bridge converter can be calculated as follows:

$$\mathrm{I}_{S12\_avg} = \frac{1}{\mathrm{T_s}} \cdot \left(- \int_0^{\Delta \mathrm{t}_1} \mathrm{I_{lk}dt} + \int_0^{\Delta \mathrm{t}_5 + \Delta \mathrm{t}_6} \mathrm{I_{lk}dt} \right) \tag{190}$$

The average current across the switches S_3 and S_4 can be calculated as:

$$\mathrm{I}_{S34\_avg} = \frac{1}{\mathrm{T_s}} \cdot \left(\int_0^{\Delta \mathrm{t}_1} \mathrm{I_{lk}dt} + \int_0^{\Delta \mathrm{t}_5 + \Delta \mathrm{t}_6} \mathrm{I_{lk}dt} \right) \tag{191}$$

The RMS current across the switches of the full-bridge is calculated by applying the square root of the sum of the squared terms.

$$\mathrm{I_{S12\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}} \cdot \left[\int_0^{\Delta \mathrm{t}_1} \left(\mathrm{I_{lk}}\right)^2 \mathrm{dt} + \int_0^{\Delta \mathrm{t}_5 + \Delta \mathrm{t}_6} \left(\mathrm{I_{lk}}\right)^2 \mathrm{dt} \right]} \tag{192}$$

$$\mathrm{I_{S34\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}} \cdot \left[\int_0^{\Delta \mathrm{t}_1} \left(\mathrm{I_{lk}}\right)^2 \mathrm{dt} + \int_0^{\Delta \mathrm{t}_5 + \Delta \mathrm{t}_6} \left(\mathrm{I_{lk}}\right)^2 \mathrm{dt} \right]} \tag{193}$$

The average current in the push-pull switches is demonstrated in the equation 194.

$$I_{SPP\_avg} = \frac{I_{bat}}{2} \tag{194}$$

The RMS current in the push-pull switches is demonstrated in the equation 195.

$$I_{SPP\_rms} = I_{bat}(1-d) \tag{195}$$

The stresses in the buck components are based on the power that is transferred through this clamper and the time step that it operates. Although these variables were not defined yet, the current stresses will mention them as they will be defined further.

The average current across the buck switch is defined as:

$$\mathrm{I_{Sb-avg}} = \frac{1}{\mathrm{T_s}} \left[\int_0^{\mathrm{d_b T_s}} \left(\mathrm{I_{Lb}}\right) \mathrm{dt} \right] \tag{196}$$

In addition, the rms current in the same switch can be defined as:

$$\mathrm{I_{Sb\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}} \cdot \left[\int_0^{\mathrm{d_b T_s}} (\mathrm{I_{Lb}})^2 \, \mathrm{dt}\right.} \tag{197}$$

The average current across the buck diode is defined as:

$$\mathrm{I_{Db\_avg}} = \frac{1}{\mathrm{T_s}} \left[\int_0^{(1-\mathrm{d_b})\cdot \mathrm{T_s}} (\mathrm{I_{Lb}}) \, \mathrm{dt}\right] \tag{198}$$

In addition, the rms current in the same diode can be defined as:

$$\mathrm{I_{Db\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}} \cdot \left[\int_0^{(1-\mathrm{d_b})\cdot \mathrm{T_s}} (\mathrm{I_{Lb}})^2 \, \mathrm{dt}\right]} \tag{199}$$

Moreover, the current stresses in the clamping diode must be calculated. First, the maximum current have to be calculated. However, the time interval that the current goes from zero to its maximum value is not represented in the converter's waveform because it is not another topological state, so this interval will be defined as follows:

$$\Delta \mathrm{t_g} = \frac{2\alpha \mathrm{D_{ef}} I_{\mathrm{lk}} \mathrm{L_{lk}}}{\mathrm{V_{Cb}}} \tag{200}$$

With the time necessary to the current reaches its maximum value, it is possible to calculate the maximum current that flows through the clamping diode as:

$$\mathrm{I_{Dg}} = \frac{\mathrm{V_{Cb}} \Delta \mathrm{t_g}}{2\mathrm{L_{lk}} \alpha^2} \tag{201}$$

So, the average and RMS current on these components are shown in equations 202 and and 203, respectively.

$$\mathrm{I_{Dg\_avg}} = \frac{1}{\mathrm{T_s}} \cdot \int_0^{(\Delta \mathrm{t_3} + \Delta \mathrm{t_4})} \frac{\mathrm{I_{Dg}}}{2} \mathrm{dt} \tag{202}$$

$$\mathrm{I_{Dg\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}} \cdot \int_0^{\Delta \mathrm{t_3} + \Delta \mathrm{t_4}} \left(\frac{\mathrm{I_{Dg}}}{2}\right)^2 \mathrm{dt}} \tag{203}$$

The rms current across the buck's capacitor is calculated using the rms current across the clamping diodes.

$$I_{Cb\_rms} = 2 I_{Dg\_rms} \tag{204}$$

Moreover, it is necessary to calculate the average and rms current in the magnetic components to size it.

The push-pull inductor has the same rms current of the batteries, since they are in series.

$$I_{Lrms} = I_{bat} \tag{205}$$

The buck inductor has the current proportional to its power.

$$I_{Lbrms} = \frac{P_{buck}}{V_{bat}} \tag{206}$$

Finally, the rms current in the primary and secondary side of the transformer are illustrated in equations 207 and 208.

$$I_{TP\_rms} = I_{lk} \tag{207}$$

$$I_{TS\_rms} = I_{SPP\_rms} = I_{bat}(1-d) \tag{208}$$

Note that the maximum current in the inductors can be estimated by adding half of the designed ripple current to the equations above. For instance, the equation 209 illustrates the maximum current that flows through the push-pull inductor.

$$I_{L\max} = I_{Lrms} + \frac{\Delta I_L}{2} \tag{209}$$

Therefore, with the current stresses, the Isolated Bidirectional DC-DC Converter can be designed and applied in DC microgrid applications to convert the voltage from the DC bus to the battery and vice-versa.

Furthermore, It can be inferred that the proposed bidirectional converter has some advantages and disadvantages.

First of all, some advantages include the soft commutation in the Full-Bridge Stage and the small power loss in the Push-Pull Stage due to the application of the Buck Converter that regenerates energy back to the battery.

The main disadvantage is on the negative power flow, since the switches of the Full-Bridge Stage do not achieved soft commutation because its parallel capacitors does not charge and discharge during the dead-time interval. Certainly, there is more power lost when the bidirectional converter is operating in the negative power flow than in the positive power flow.

6 CONVERTER CONTROL

First of all, a converter that charges and discharges batteries must have its current controlled to keep the converter stabilized in an operation point. Therefore, it is necessary a closed-loop control system to the variable follow a reference.

Furthermore, the converter transfer function that relates the current variation for the converter's duty cycle variation is necessary to project the controller.

Therefore, to impose an operation point to the converter its frequency domain transfer function must be found through methods such as state space or small-signal AC model as presented in (ERICKSON; MAKSIMOVIC, 2007).

There are two main variables that should be controlled, the clamping capacitor voltage presented in the Appendix B and the current that charges or discharges the battery. Also, the voltage control of the batteries will not be presented.

So, this chapter presents the control method for the Push-Pull inductor current. The clamping capacitor voltage control mathematical analysis and transfer function are presented in the Appendix section, since the open-loop operation should be sufficient to maintain the clamped voltage under the Push-Pull Stage MOSFETs breakdown voltage found on datasheet.

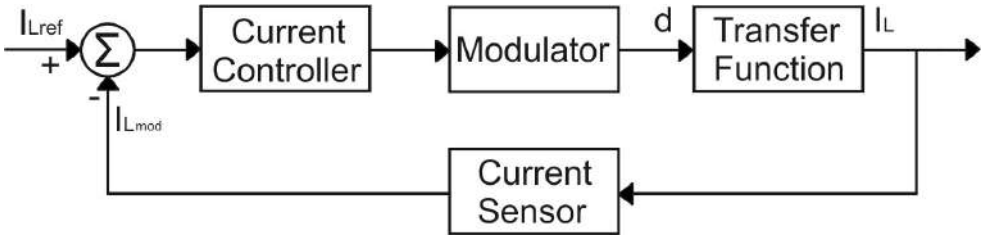
6.1 PUSH-PULL INDUCTOR CURRENT CONTROL

The push-pull inductor current is used to control the current that charges and discharges the batteries as well as the power flux direction. To study this closed-loop system, it is possible to disregard the clamping circuit influence as its currents is much smaller and it can be applied in the current reference's value.

Also, this methodology needs only one current sensor because the clamping circuit is already controlled by using a voltage sensor.

Since the closed-loop systems are uncoupled, the following block diagram presented in Figure 99 can describe the closed-loop for the push-pull inductor current control.

Figure 99 – Closed-loop control system of the push-pull inductor current

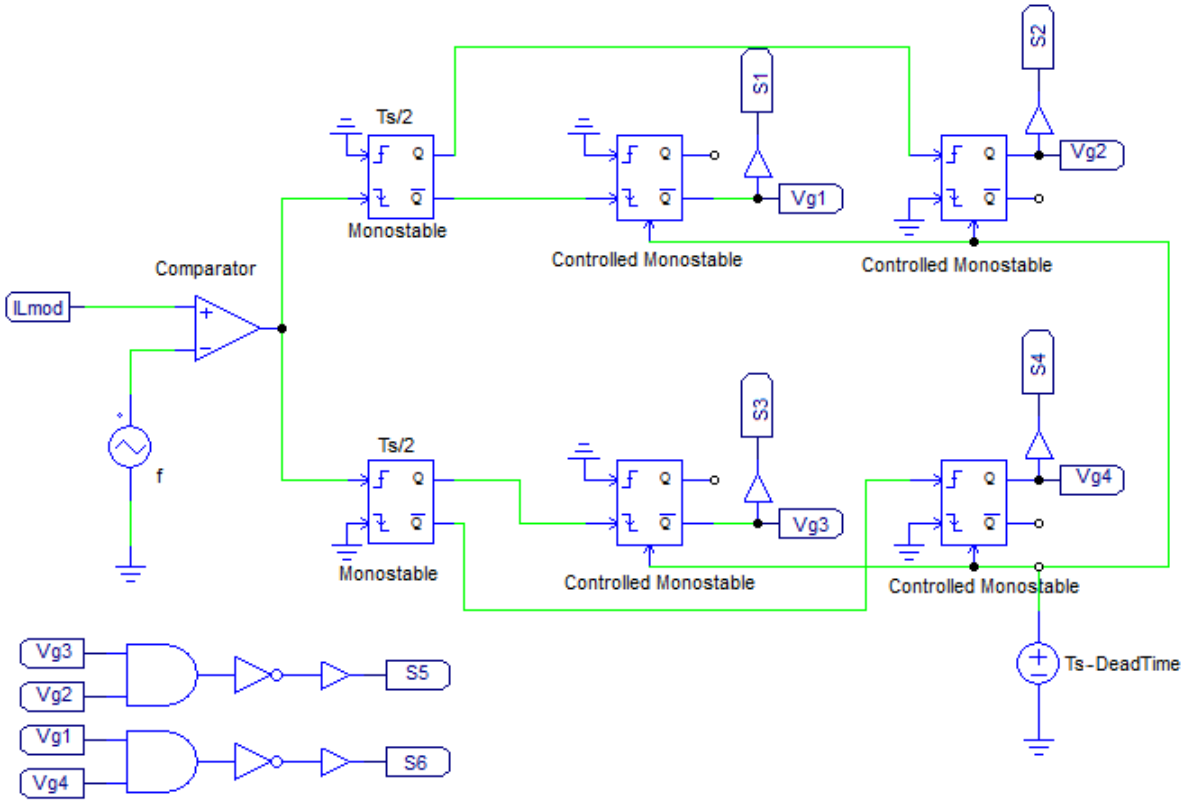


Source: Own elaboration

Which the current reference I_{Lref} should be equals to the design batteries current plus the clamping circuit current.

In addition, the output modulation signal resulted from the closed-loop control system is used to gate on the converter's MOSFETS, this signal is represented by I_{Lmod} in Figure 100.

Figure 100 – Gate signals strategy



Source: Own elaboration

The gate signals strategy is done by using some monostable circuits, comparator and logic AND gate. Furthermore, the buck's gate signal is implemented separately.

In addition, to obtain the model of the converter and find its transfer function, it is necessary to study the two topological states that changes the voltage across the inductor (L), which discharges the clamping circuit.

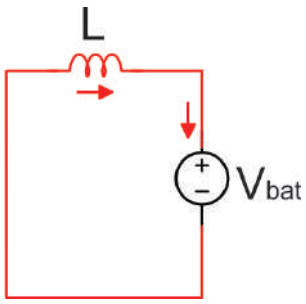
6.1.1 Circuit Operation

The Current-Fed Push-Pull Stage operating in steady state is analyzed below. Note, that this analysis consider some circuit simplifications. Therefore, it can be analyzed with only two topological states. Since the converter was already studied in previous chapter, the gate signals and detailed circuit operation will not be shown again.

Therefore, the Current-Fed Push-Pull Stage presents two different equivalent circuits for its topological states, as described below:

Time interval Δt_1 - At the first step, the voltage across the transformer (V_{ab} is null because both switches of the Push-Pull are turned on. Then, the equivalent circuit of Figure 101 represents the first topological state.

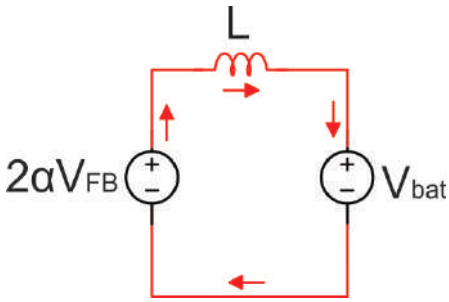
Figure 101 – First topological state of the Current-Fed Push-Pull Stage



Source: Own elaboration

Time interval Δt_2 - At the second step, the voltage in the transformer is not null, then the voltage reflected to the Push-Pull Stage becomes $2\alpha V_{FB}$, as shown in Figure 102.

Figure 102 – Second topological state of the Current-Fed Push-Pull Stage



Source: Own elaboration

6.1.2 Transfer Function

Each topological state has a different voltage across the inductor, as presented below:

$$V_{bat} = -V_L \tag{210}$$

$$2\alpha V_{FB} = V_L + V_{bat} \tag{211}$$

Thus, it is possible to calculate an expression for the voltage across the transformer disregarding the influence of the leakage inductance.

$$V_{ox} = \frac{0\,(t_1) + 2\alpha V_{FB}\left(\frac{T_S}{2} - t_1\right)}{\frac{T_S}{2}} \tag{212}$$

Then, by simplifying the equation:

$$V_{ox} = 2\alpha V_{FB}\left(1 - \frac{2t_1}{T_S}\right) \tag{213}$$

To consider the influence of the leakage inductance of the transformer, it is mandatory to add the time that the inductance current is transferred to the clamping circuit in the first period.

$$t_1 = t_d + t_{Llk} \tag{214}$$

Then, if 214 be replaced in 213 there is the voltage V_{ab} instead of V_{ox}.

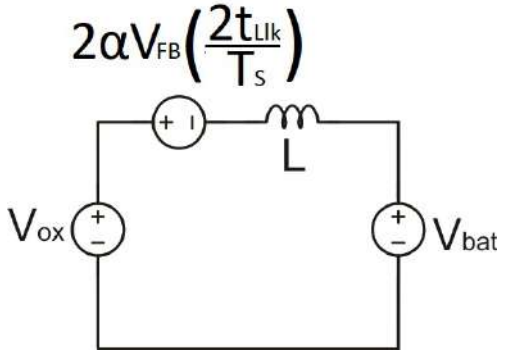
$$V_{ab} = 2\alpha V_{FB}\left(1 - \frac{2t_d}{T_S}\right) - 2\alpha V_{FB}\left(\frac{2t_{Llk}}{T_S}\right) \tag{215}$$

The first term of equation 215 is exactly V_{ox}, so the equation can be simplified.

$$V_{ab} = V_{ox} - 2\alpha V_{FB}\left(\frac{2t_{Llk}}{T_S}\right) \tag{216}$$

Then, an equivalent circuit that represents the converter can be found with equation 216, as shown in Figure 103.

Figure 103 – Current-Fed Push-Pull Stage equivalent circuit



Source: Own elaboration

A relation can be used to rewrite the voltage source as a resistance.

$$2\alpha V_{FB}\left(\frac{2t_{Llk}}{T_S}\right) = R_{Llk} I_L \tag{217}$$

Find the resistance R_{Llk} requires an expression for time interval t_{Llk}. This time interval represents the period that the leakage inductance current is transferred to the clamping capacitor. It is possible to calculate this time by using the formula of the voltage across the leakage inductance (L_d).

$$V_{Llk} = L_d \frac{dI_L}{dt} \tag{218}$$

The voltage across the leakage inductance referred to the Push-Pull Stagee is equals to the DC Bus voltage multiplied by the transform turns ratio (α).

$$2\alpha V_{FB} = L_d \frac{I_L}{t_{Llk}} \tag{219}$$

If time t_{Llk} from equation 219 be isolated, gives:

$$t_{Llk} = \frac{L_d I_L}{2\alpha V_{FB}} \tag{220}$$

Finally, the resistance R_{Llk} can be found by replacing equation 220 in 217.

$$R_{Llk} = 2L_d f \tag{221}$$

So, R_{Llk} is a resistance that consumes reactive power and depends on the leakage inductance and commutation frequency of the converter. Furthermore, it is also known that this power will actuality be transferred back to the battery through the clamping circuit.

The converter duty cycle can be written as:

$$1 - \frac{2t_d}{T_S} = d \tag{222}$$

Therefore, if equations 220 and 222 be replaced in 215, leads to:

$$V_{ab} = 2\alpha V_{FB} d - 2L_d f I_L \tag{223}$$

Finally, it is possible to find a new equivalent circuit model, as presented in Figure 104.

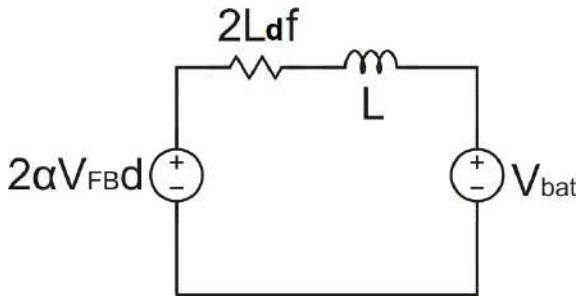
Applying the Kirchhoff Voltage Law, it is achievable to get the following expression:

$$2\alpha V_{FB} d = V_{bat} + 2L_d f I_L + L \frac{dI_L}{dt} \tag{224}$$

It is desirable to acquire a transfer function that relates the current (I_L) as a function of the duty cycle (d). As a result, a perturbation needs to be done in the desirable converter's variable around its operation point.

$$d = d + \tilde{\Delta} d \tag{225}$$

Figure 104 – New Current-Fed Push-Pull Stage equivalent circuit



Source: Own elaboration

$$I_L = I_L + \tilde{\Delta I_L} \tag{226}$$

Moreover, if the equations 225 and 226 be replaced in 224, it is found:

$$2\alpha V_{FB}(d + \tilde{\Delta} d) = V_{bat} + 2L_d f(I_L + \tilde{\Delta I_L}) + L\frac{d(I_L + \tilde{\Delta I_L})}{dt} \tag{227}$$

The DC terms can be disregard as the converter's static gain was already found.

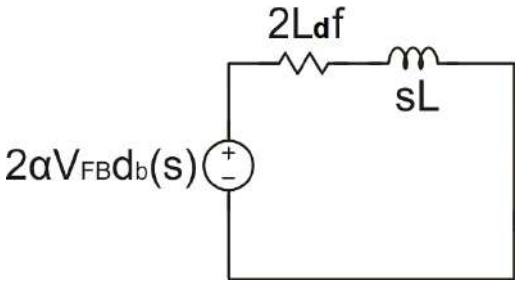
$$2\alpha V_{FB}\tilde{\Delta} d = 2L_d f\tilde{\Delta I_L} + L\frac{d\tilde{\Delta I_L}}{dt} \tag{228}$$

In addition, the Laplace Transform can be performed in the equation 228.

$$2\alpha V_{FB} d(s) = 2L_d f I_L(s) + sLI_L(s) \tag{229}$$

Finally, the equation 229 allows to write an equivalent circuit that represents the Small-Signal AC model, as shown in Figure 105.

Figure 105 – Small-signal AC model of the new Current-Fed Push-Pull Stage equivalent circuit



Source: Own elaboration

Furthermore, if some algebraic manipulations be done in equation 229, the transfer function that represents the inductor current variation as a function of the duty cycle variation is found, as presented in equation 230.

$$\frac{I_L(s)}{d(s)} = \frac{2\alpha V_{FB}}{sL + 2L_d f} \tag{230}$$

6.1.3 Transfer Function Validation

It is possible to validate the transfer function by applying the AC Sweep tool in the converter circuit and in the transfer function adopting a simulation software.

Therefore, the amplitude and phase of both theoretical transfer function and the switched model can be plotted in the same bode diagram.

In order to acquire the bode diagram, some variable must be defined as represented in table 3.

Table 3 – Specifications for the current transfer function validation of the Push-Pull Stage

Specification	**Value**
Rated power (P_{out})	2000 W
DC bus voltage (V_{FB})	400 V
Transformer turns ratio (α)	0.185
Push-Pull inductor (L)	43.2 μH
Leakage inductance referred to the Push-Pull Stage (L_d)	1.108 μH
Switching frequency (f)	40 kHz

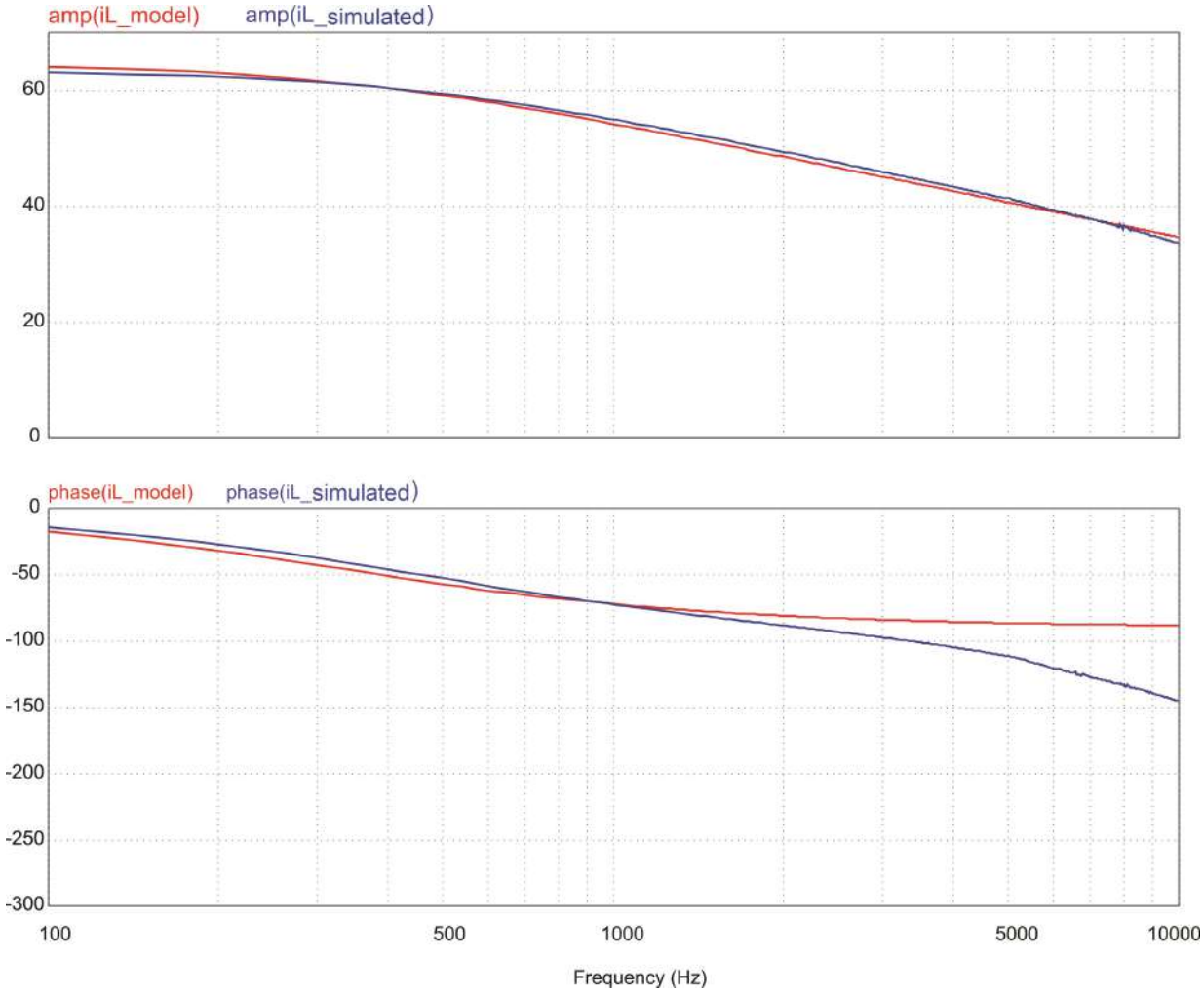
Source: Own elaboration

The switching frequency is 40 kHz. Thus, the transfer function should be validated in the region which the controller will be applied. Usually, the cut-off frequency of the controller is one decade smaller than the switching frequency. So, Figure 106 illustrates the bode diagram of both models until 10 kHz, though the controller must be project with a cutoff frequency smaller than 4 kHz.

Also, a current sensor in series with the Push-Pull inductor measures I_L. Furthermore, this measured current is compared with a desirable current reference. Therefore, Figure 107 represents the closed-loop control system with the PI that should be applied to modulate the converter. In addition, the PI controller project can be found in Appendix D.

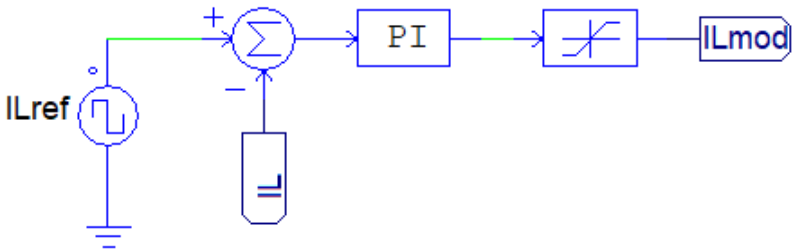
Thus, the current reference (I_{Lref}) can be calculated with equation 231. Note that the reference must vary its signal to prove that the converter is bidirectional. So, the reference will be a square wave with maximum and minimum represented in equation 231 which the frequency is 100 Hz. Note that this random frequency of the reference is

Figure 106 – Bode diagram of the model and simulated Current-Fed Push-Pull Stage transfer function



Source: Own elaboration

Figure 107 – Closed-Loop control system with a PI controller



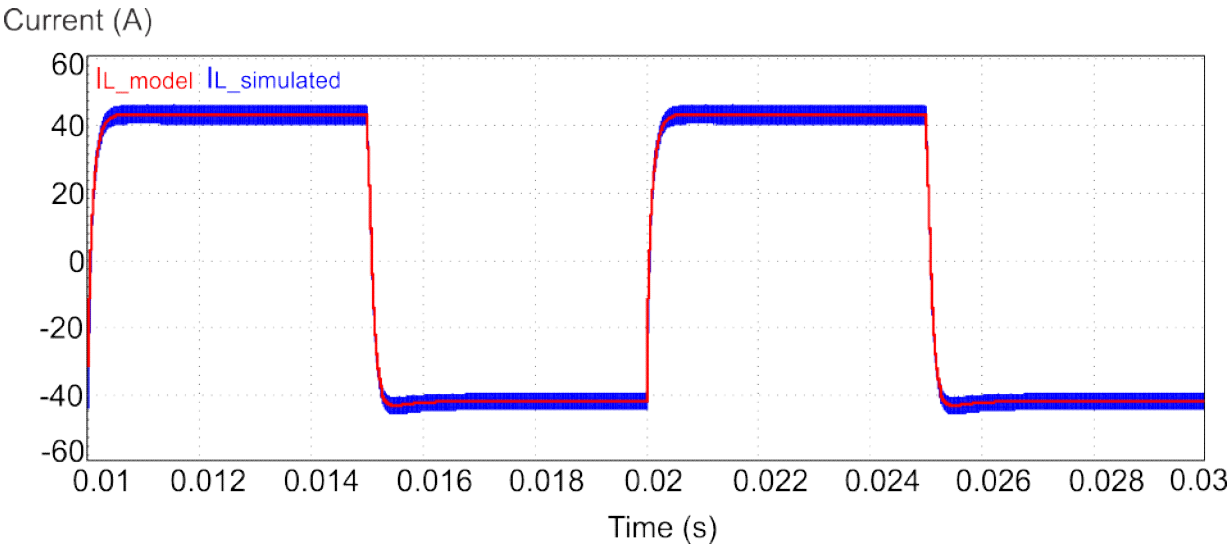
Source: Own elaboration

done to verify the transition between the converter's power flows.

$$I_{Lref} = \pm\frac{P_{out}}{V_{bat}} = \pm 41.667A \tag{231}$$

Therefore, with the signal I_{Lmod} obtained from Figure 107 applied in Figure 100, it is possible to obtain the controlled current of the Push-Pull inductor as a function of the time, represented in Figure 108. Furthermore, Figure 108 also presents the model of the current transfer function obtained in equation 230, which is plotted by applying the same signal (I_{Lmod}) in the transfer function.

Figure 108 – Controlled current in the Push-Pull inductor



Source: Own elaboration

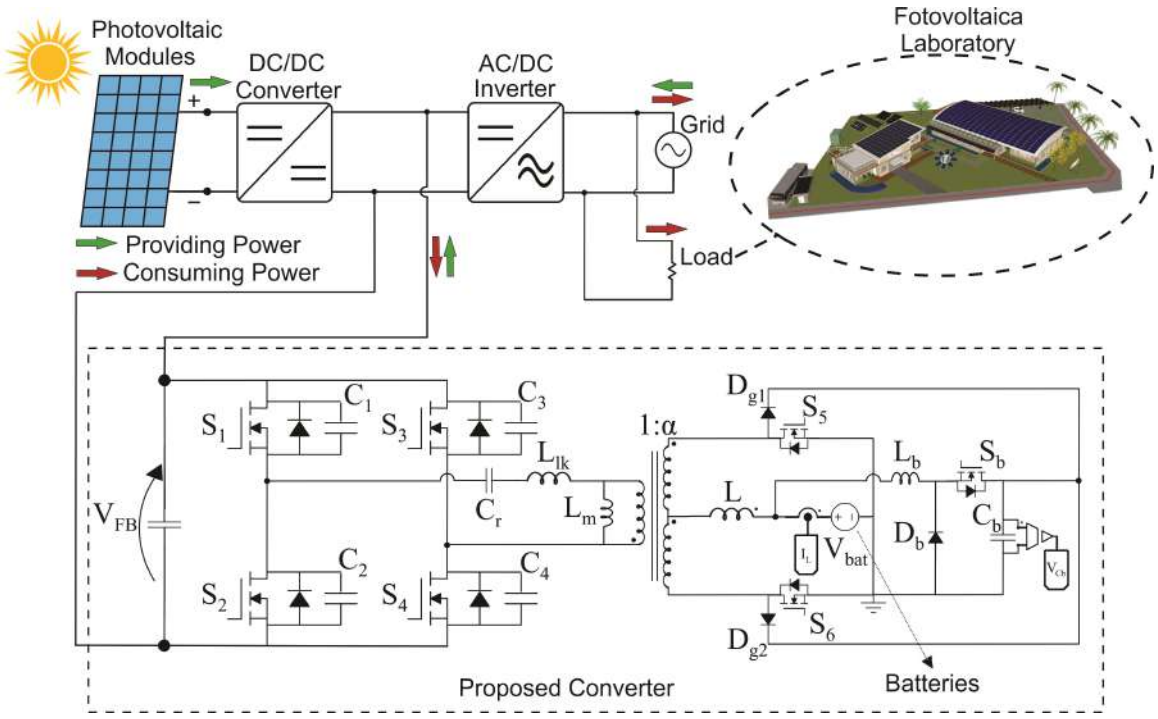
Then, the controlled current presented the smooth transition between both converter's power flows, which attest the bidirectional operation.

7 PROJECT AND SIZING OF THE PROPOSED CONVERTER

The DC microgrid needs an efficient, reliable and controllable converter to connect a battery bank on it. Also, the converter must isolate the high voltage bus from the low voltage supply to customers, which provides safety to users. So, the converter proposed in this research fits the necessity as it has a bidirectional and isolated power flow with a controllable current that charges and discharges the batteries.

Thus, the Isolated Bidirectional Converter based on the assimilation of the DC-DC Full-Bridge ZVS-PWM and Current-Fed Push-Pull Converters, clamped with the Buck Converter is used to connect the DC bus from a DC microgrid and Lithium-ion batteries as represented in Figure 109.

Figure 109 – Proposed converter applied in the DC microgrid



Source: Own elaboration

Therefore, this chapter will focus on the project and sizing of the proposed converter, so the practical results can authenticate the theories.

The converter will be developed with the specifications shown in table 4.

As presented in earlier chapters, the converter has the Full-Bridge and Current-Fed Push-Pull Stages and a Buck Converter integrated. So, the sizing will be done separately for each stage. In addition, the entire circuit evaluation is available at the Appendix A that contains a MathCad spreadsheet, this sheet presents a the step-by-step design calculation of all the circuits components for both the Power Stage and Signal

Table 4 – Specifications of the proposed converter

Specification	**Value**
Rated power (P_{out})	2000 W
DC bus voltage (V_{FB})	400 V
Lithium-ion batteries voltage (V_{bat})	48 V
Switching frequency (f)	40 kHz
Buck's switching frequency (f_b)	80 kHz
Minimum power to achieve ZVS (P_{min})	800 W
Buck voltage (V_{Cb})	220 V
Prototype Dimension	26.5 cm x 30 cm

Source: Own elaboration

Conditioning Stage. Thus, this chapter will only explain some design characteristics and show some results of the author's circuit design.

7.1 DC-DC FULL-BRIDGE ZVS-PWM STAGE

7.1.1 Leakage inductance

As studied in chapter 3, the leakage inductance of the transformer performs a lost in the effective duty cycle of the Full-bridge Stage. Thus, the inductance can be calculated by stipulating a duty cycle loss.

$$\Delta D = 0.05 \tag{232}$$

For instance, considering the Full-bridge stage duty cycle (D) equals to 0.7, the effective duty cycle is presented in equation 233.

$$D_{ef} = D - \Delta D = 0.65 \tag{233}$$

Therefore, the transformer turns ratio can be calculated as shown in equation 234.

$$\alpha = \frac{V_{bat}}{V_{FB} D_{ef}} = 0.185 \tag{234}$$

The current in the leakage inductance of the Full-Bridge Stage can be calculated as shown in equation 235.

$$I_{lk} = \frac{\alpha P_{out}}{V_{bat}} = 7.692A \tag{235}$$

Furthermore, the leakage inductance is calculated using equation 236.

$$L_{lk} = \frac{V_{FB} \Delta D}{4 I_{lk} f} = 16.25\mu H \tag{236}$$

7.1.2 Series capacitor

The capacitor in series with the leakage inductance is necessary to filter the DC level resulted from the time of commutation of the Full-bridge and Push-Pull MOSFET's inequality. A DC current circulating through the transformer can saturate its core and damage the switches.

This capacitor is not presented in previous chapters since it does not changes the converter's topological states. However, the converter does not operate without this passive element to filter the DC level

The calculus of this capacitor is shown in (BARBI, 2007). The equation 237 is calculated based on the voltage drop through the capacitor. The smaller the capacitance, the greater its voltage drop and the output voltage. In addition, the voltage drop across the series capacitor (ΔV_{Cr}) is designed with 10 V.

$$C_r = \frac{I_{lk}}{2\alpha f \Delta V_{Cr} V_{FB}} = 9.65\mu F \tag{237}$$

7.1.3 Soft Commutation

To achieve soft commutation, a parallel capacitor with the MOSFETs must be calculated and also the dead-time between the gate signals in each leg.

The minimum capacitance value forthis conditions can be calculated with equation 238.

$$C_{min} = \left(\frac{I_{lkmin}}{V_{FB}}\right)^2 \cdot \frac{L_{lk}}{2} = 0.48nF \tag{238}$$

Note that equation 238 considers the minimum current in the leakage inductance to achieve ZVS.

Therefore, a commercial capacitance of 0.47 nF can be used. However, this capacitance cannot be called the commutation capacitance yet because it does not consider the MOSFET intrinsic capacitance, which is approximately 0.14 nF according to the component's datasheet. Therefore, with the sum of both capacitances, the commutation capacitance (C_c) is found.

Then, with the new capacitance value, the dead-time calculation is presented in equation 239.

$$\Delta t_d = \left(\frac{\pi}{2} - cos^{-1}\left(\frac{V_{FB}^2 D_{ef}}{P_{min}} \cdot \sqrt{\frac{2C_c}{L_{lk}}}\right)\right) \cdot \left(\sqrt{2L_{lk}C_c}\right) = 221ns \tag{239}$$

Finally, the dead-time must be greater than Δt_d for this circuit's condition to achieve soft switching.

7.2 CURRENT-FED PUSH-PULL STAGE

7.2.1 Push-pull inductor

First of all, the current in the push-pull inductor can be calculated as shown in equation 240.

$$I_L = \frac{P_{out}}{V_{bat}} = 41.667A \tag{240}$$

The inductor can be calculated using the current ripple criteria. Then, by selecting a ten percent current ripple ($\Delta I_L = 4.667A$), the inductance can be sized using equation 241.

$$L = \frac{V_{bat}d}{2f\Delta I_L} = 43.2\mu H \tag{241}$$

7.3 BUCK CONVERTER

The buck converter that will be used as a clamping circuit to limit the voltage across MOSFET's S_5 and S_6 should be sized according to the power transferred. There are many ways to size this auxiliary converter, so the main challenge of this section is to specify the power recovered by the buck converter.

First of all, a clamping voltage is specified as represented in equation 242.

$$V_{Cb} = 220V \tag{242}$$

Then, the maximum voltage across the secondary side of the transformer is half of the clamping voltage.

$$V_{os} = \frac{V_{Cb}}{2} = 110V \tag{243}$$

The duty cycle of the Buck Converter can be calculated using expression 244.

$$d_b = \frac{V_{bat}}{V_{Cb}} = 0.218 \tag{244}$$

The time that the clamping diodes are forward biased can be calculated using expression 245. This equation was obtained with the current and voltage across the leakage inductance. So, the equation can be calculated as:

$$\Delta t_g = \frac{I_{lk}L_{lk}}{2V_{FB}} = 156ns \tag{245}$$

With the time necessary to the current reaches its maximum value, it is possible to calculate the maximum current that flows through the clamping diode, similar to equation 201. So, the equation can be redefined and calculated as:

$$I_{Dg} = \frac{V_{Cb}\Delta t_g}{2L_{lk}\alpha^2} = 31A \tag{246}$$

The time that buck's input capacitor is being charged can be calculated with expression 247.

$$\Delta t_{lk} = \frac{I_{lk}L_{lk}}{V_{FB}} = 0.313\mu s \tag{247}$$

With the voltage across buck's input capacitor fixed in 220 V and the current presenting a triangular waveform with the base equals to Δt_buck and the peak equals to I_{Dg}, the approximated power that buck converter will transfer can be calculated as:

$$P_{buck} = f_b \int_0^{\Delta t_{lk}} I_{Dg}V_{Cb}dt = 170W \tag{248}$$

The equation 248 representing the triangular area is not divided by two because there are two clamping diodes that charge buck's capacitor.

Moreover, the buck converter will be designed to transfer up to 200 W only to investigate its operation because the lower the power that this converter transfer, the greater will be its efficiency. Also, low power transfer reduces the size and volume of the auxiliary converter.

So, the average current through buck's inductor is calculated in equation 249.

$$I_{Lb} = \frac{P_{buck}}{V_{bat}} = 4.167A \tag{249}$$

Then, by specifying a ripple current equals to 25% ($\Delta I_{Lb} = 0.25$) and the buck's frequency two times greates than the push-pull frequency, the buck inductor can be calculated as shown in equation 250.

$$L_b = \frac{V_{bat}(V_{Cb} - V_{bat})}{f_b V_{Cb}\Delta I_{Lb}} = 0.45mH \tag{250}$$

Finally, the buck's capacitor can be sized with a defined ripple voltage and checked with the RMS current criteria. The equation 251 represents the input buck capacitance for one percent of voltage ripple.

$$C_b = \frac{I_{Cbrms}d_b}{f\Delta V_{Cb}} = 4.96\mu F \tag{251}$$

Therefore a commercial polypropylene capacitor which withstands high peak current has to be found with a proper RMS current. Normally the manufactures provide the maximum RMS current for each capacitance value in the datasheets, so this criteria can be observed too.

In addition, this evaluation can be found in Appendix A. So, four commercial polypropylene with $0.47\mu F$ are used in parallel at the prototype in order to keep the voltage input stability.

7.4 VOLTAGE STRESSES

The voltage stresses across each active and passive component in the proposed converter are shown in table 5. Which, the calculated values were obtained with equations from chapter 5.

Table 5 – Voltage stresses across the components

Component	**Maximum value**
Full-Bridge Stage MOSFET (V_{SFB})	400 V
Push-Pull Stage MOSFET (V_{SPP})	220 V
Buck MOSFET (V_{Sb})	220 V
Clamping Diode (V_{Dg})	220 V
Buck Diode (V_{Db})	220 V
Transformer primary side (V_{TP})	598.83 V
Transformer secondary side (V_{TS})	110 V

Source: Own elaboration

It is necessary to know the voltage stresses to choose the proper components to apply in the prototype, they have to support a voltage greater than it is shown in table 5.

7.5 CURRENT STRESSES

The current stresses across each active and passive components in the proposed converter are shown in table 6. These results were obtained through equations presented in chapter 5.

7.6 MAGNETIC COMPONENTS

The method used to calculate the transformer and inductor is demonstrated in (BARBI, 2007), which the ferrite core, the current density, winding configuration, air gap and losses are sized by using the Faraday‘s and Ampere‘s Laws.

Note the losses and then the thermal stresses will be estimated next.

7.6.1 Push-Pull inductor

The inductance of the push-pull inductor was calculated with the ripple current technique, shown in equation 241. Therefore, the specifications shown in table 7 will be used to size the inductor.

Which:

Table 6 – Current stresses in the components

Component	Average value	RMS value
Full-Bridge Stage MOSFET 1 and 2	1.35 A	5.3 A
Full-Bridge Stage MOSFET 3 and 4	3.65 A	5.3 A
Push-Pull Stage MOSFET	20.833 A	29.167 A
Buck MOSFET	0.9 A	1.95 A
Clamping Diode	0.49 A	2.75 A
Buck Diode	3.26 A	3.69 A
Transformer primary side	0 A	7.7 A
Transformer secondary side	20.833 A	29.167 A
Push-Pull inductor	41.67 A	41.67 A
Buck inductor	4.167 A	4.167 A

Source: Own elaboration

Table 7 – Specifications of the push-pull inductor

Specification	Value
L	43.2 μH
ΔI_L	4.167 A
B_{max}	0.3 T
J_{max}	450 $\frac{A}{cm^2}$
K_w	0.7

Source: Own elaboration

- B_{max} is the peak flux density swing;
- J_{max} is the maximum allowed current density;
- K_w is the winding factor.

7.6.1.1 Ferrite core

To calculate the ferrite core, the method is based on the Core Area Product, which is obtained by multiplying the core magnetic cross-section area (A_e) by the window area (A_w) available for the winding, as illustrated in Figure 110.

The core area product and its result are represented in 252

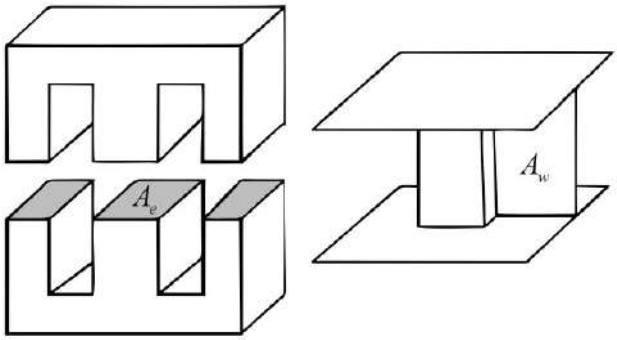
$$A_e A_w = \frac{L I_{L\max} I_{Lrms}}{B_{\max} J_{\max} K_w} = 7.937 cm^4 \tag{252}$$

Then, based on the equation 252, the ferrite core NEE-65/33/39 was used to design the push-pull inductor. Furthermore, its specifications are illustrated in table 8.

Which:

- V_{core} is the ferrite core volume;
- l_{turn} is the magnetic path length.

Figure 110 – Core and bobbin representation



Source: Adapted from (BARBI, 2007)

Table 8 – Specifications of the ferrite core NEE-65/33/39

Specification	**Value**
A_e	7.98 cm^2
A_w	11.31 cm^2
V_{core}	117.3 cm^3
l_{turn}	14.7 cm

Source: Own elaboration

7.6.1.2 Number of turns

The number of turns is calculated with equation 253.

$$N_{LPP} = \frac{LI_{L\max}}{B_{\max}A_e} = 8 \tag{253}$$

7.6.1.3 Air gap

The air gap is calculated with equation 254.

$$l_{airgapPP} = \frac{{N_{LPP}}^2 \mu_o A_e}{L} = 0.188cm \tag{254}$$

Which μ_o is the air permeability and it is equals to $4.\pi.10^{-7}\frac{H}{m}$.

7.6.1.4 Current density

The conductors are calculated according to maximum current density and skin effect. In order to achieve the current density requirement, the copper area must be greater than the result of equation 255.

$$S_{copperPP} = \frac{I_{Lrms}}{J_{\max}} = 0.093cm^2 \tag{255}$$

In addition, to avoid the skin effect, the diameter of the copper must be smaller than the value presented in equation 256.

$$R_{\max} = \frac{15}{\sqrt{f}} = 0.075cm \tag{256}$$

Then, the selected AWG 28 has 0.032 cm of diameter, the copper are (S_{cu}) is 0.000810 cm^2 and the insulated area (S_{AWG}) is 0.001083 cm^2.

Thus, the number of conductors in parallel to meet these criteria is calculated as follows:

$$n_{cond}=\frac{S_{copperPP}}{S_{cu}} = 115 \tag{257}$$

To achieve this number of conductors, four Litz wires will be used. Furthermore, this material has thirty AWG 28 wires in parallel. Therefore, the Litz wire presents another insulated area that should be approximated for the fulfillment calculation.

7.6.1.5 Fulfillment performance

To check if it is possible to build the inductor or not, a k factor is calculated as presented in 258. The factor must be smaller than 1 to fit the bobbin area.

$$k = \frac{N_{LPP}S_{AWG}n_{cond}}{K_w A_w} = 0.823 \tag{258}$$

7.6.2 Buck inductor

The inductance of the buck inductor was calculated with the ripple current technique, shown in equation 250. Therefore, the specifications shown in table 9 will be used to size the inductor.

Table 9 – Specifications of the buck inductor

Specification	Value
L_b	0.45 H
ΔI_{Lb}	1.042 A
B_{max}	0.3 T
J_{max}	450 $\frac{A}{cm^2}$
K_w	0.7

Source: Own elaboration

Note that this ripple current represents 25% of the buck RMS current.

7.6.2.1 Ferrite core

The core area product and its result are represented in 259

$$A_e A_w = \frac{L I_{Lbmax} I_{Lbrms}}{B_{\max} J_{\max} K_w} = 0.837 cm^4 \tag{259}$$

Based on the equation 259, the ferrite core MMT140EE5525 was used to design the buck inductor. Furthermore, its specifications are illustrated in table 10.

Table 10 – Specifications of the ferrite core MMT140EE5525

Specification	**Value**
A_e	4.22 cm^2
A_w	3.756 cm^2
V_{core}	28.84 cm^3
l_{turn}	12 cm

Source: Own elaboration

7.6.2.2 Number of turns

The number of turns is calculated with equation 260.

$$N_{Lb} = \frac{L_b I_{Lbmax}}{B_{\max} A_e} = 15 \tag{260}$$

7.6.2.3 Air gap

The air gap is calculated with equation 261.

$$l_{airgapPP} = \frac{{N_{Lb}}^2 \mu_o A_e}{L} = 0.276 cm \tag{261}$$

7.6.2.4 Current density

The copper area must be greater than the result of equation 262.

$$S_{copperBuck} = \frac{I_{Lbrms}}{J_{\max}} = 0.00926 cm^2 \tag{262}$$

Also, the diameter of the copper must be smaller than the value presented in equation 256.

Then, the selected AWG 24 has 0.051 cm of diameter, the copper are (S_{cu}) is 0.002047 cm^2 and the insulated area (S_{AWG}) is 0.002586 cm^2.

Thus, the number of conductors in parallel to meet these criteria is calculated as follows:

$$n_{cond} = \frac{S_{copperBuck}}{S_{cu}} = 5 \tag{263}$$

Again, to achieve this number of conductors, a Litz wire will be used. Furthermore, this material has ten AWG 24 wires in parallel. Therefore, the Litz wire presents another insulated area that should be approximated for the fulfillment calculation.

7.6.2.5 Fulfillment performance

The factor must be smaller than 1 to fit the bobbin area.

$$k = \frac{n_{cond} N_{Lb} S_{AWG}}{K_w A_w} = 0.884 \tag{264}$$

7.6.3 External inductor

First of all, the inductance of the transformer was measured with 5 μH using an Impedance Analyzer E4990A of the company KEYSIGHT. Therefore, this value was subtracted from the equation 236 and then the external inductor was designed with the same principles above. In summary, the result was a ferrite core MTT140EE4220 with two turns of an Litz wire AWG 24.

7.6.4 Transformer

Some specifications shown in table 11 will be used to size the transformer.

Table 11 – Specifications of the transformer

Specification	Value
α	0.185
P_{out}	2000 W
B_{max}	0.3 T
J_{max}	450 $\frac{A}{cm^2}$
K_w	0.7
K_p	0.5

Source: Own elaboration

Which K_p is the primary utilization factor.

7.6.4.1 Ferrite core

The core area product and its result are represented in 265

$$A_e A_w = \frac{P_{out}}{K_w K_p B_{\max} J_{\max} f} = 10.582 cm^4 \tag{265}$$

Then, based on the equation 265, the ferrite core NEE-65/33/39 was used to design the transformer. Furthermore, since it is the same core used in the push-pull inductor, its specifications are illustrated in table 8.

7.6.4.2 Number of turns

The number of turns in the primary side is calculated with equation 266.

$$N_{TP} = \frac{V_{PC}}{4B_{\max}A_e f} = 16 \tag{266}$$

The number of turns in the secondary side is calculated with equation 267.

$$N_{TS} = \frac{N_{TP}}{\alpha} = 3 \tag{267}$$

7.6.4.3 Current density

The copper will be calculated as presented in the inductors. There a winding section for each side of the transformer, since the current is different.

$$S_{TP} = \frac{I_{TP_rms}}{J_{\max}} = 0.017cm^2 \tag{268}$$

$$S_{TS} = \frac{I_{TS_rms}}{J_{\max}} = 0.065cm^2 \tag{269}$$

The wire AWG 28 was selected again, so the number of conductors in parallel is calculated as follows:

$$n_{TP}=\frac{S_{TP}}{S_{cu}} = 22 \tag{270}$$

$$n_{TS}=\frac{S_{TS}}{S_{cu}} = 81 \tag{271}$$

To achieve this number of conductors, three Litz wires will be used. This wire contains thirty AWG 28 in parallel.

7.6.4.4 Fulfillment performance

To check if it is possible to build the transformer, the k factor is calculated considering both sides of the transformer, as presented in 272.

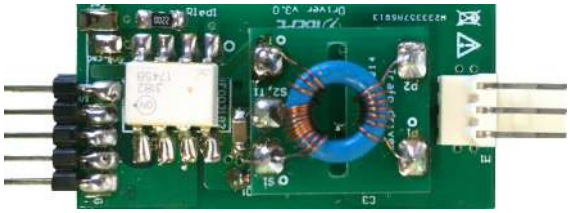
$$k = \frac{n_{TP}N_{TP}S_{AWG}}{K_w A_w} + \frac{n_{TS}N_{TS}S_{AWG}}{K_w A_w} = 0.75 \tag{272}$$

7.7 GATE DRIVERS

The gate drivers used in this Master Thesis were developed by the engineers of the Brazilian Institute of Power Electronics and Renewable Energy (IBEPE), presented in Figure 111. They accept the low-power PWM output of the TMS320F28069 and produces a high-current drive input for the gate terminal of the MOSFET. The principles

and operation of the gate drivers will not be covered, since it is not the goal of this research.

Figure 111 – Gate Driver from IBEPE



Source: Own elaboration

7.8 PROTOTYPE

After sizing the converter and its components, some Printed Circuit Board (PCB) are developed to connect all the designed circuits. Beyond the power stage studied until now, some sub-circuits have to be constructed to debug the prototype such as the circuits to connect and read the input of voltage and current sensors, the signal conditioning to convert the signals to the DSP ADC input limits, the desired voltage source input of these components and some buffer amplifier to prevent the Pulse Width Modulation (PWM) signal source from being affected by any current source that may cause a signal noise.

Although the sub-circuits are important to design and debug the prototype, these are mainly done with basic electronic solutions implementing operational amplifiers, voltage regulators and Sallen-Key filter. So, their operation will be presented in the Appendix A.

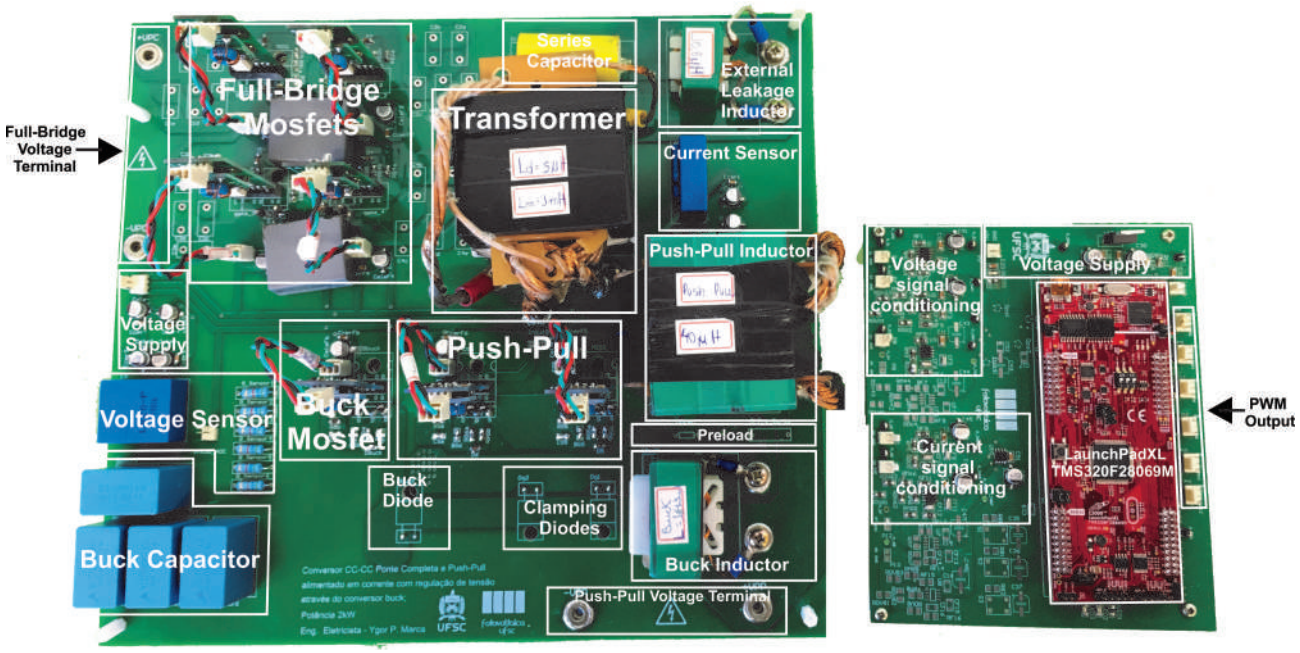
In summary, the prototype presents two main PCBs, the power stage PCB and the signal conditioning PCB, as presented in Figure 112. The power stage has the converters, gate drivers, voltage and current source, and the signal conditioning PCB has the DSP, buffer circuit, operational amplifier circuits, Sallen-Key filters and voltage regulation. Then, both the PCBs are connected through armored cables preventing Electromagnetic interference (EMI).

7.9 POWER LOSS

An important study in a prototype design is the power losses, because it provides results for the thermal constraints and optimization of the converter's efficiency.

There are some major source of loss in a power electronics prototype and in this project they can be divided in the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) loss, diode loss, core loss and copper loss.

Figure 112 – Prototype detailed



Source: Own elaboration

7.9.1 MOSFET Loss

The MOSFET presents switching and conducting losses, represented by equations 273 and 274 respectively. Although the Full-Bridge ones do not have switching losses since it they operate in soft switching, the others do, so it is calculated.

$$P_{mswitching} = \frac{I_{max} V_{max} (t_r + t_f)}{2T_s} \tag{273}$$

$$P_{mconducting} = \frac{T_{on} R_{ds} I_{rms}^2}{T_s} \tag{274}$$

These values can be found in the components' datasheet:

- t_r is the rise time;
- t_f is the fall time;
- R_{ds} is the on resistance.

7.9.2 Diode Loss

The diode also presents switching and conducting losses, represented by equations 275 and 276 respectively. However, most diodes have a fast recovery time, which

decreases its switching loss.

$$P_{dswitching} = \frac{V_{max} I_{rms} t_{rr} f}{2} \tag{275}$$

$$P_{dconducting} = V_{TO} I_{med} + R_F I_{rms}^2 \tag{276}$$

These values can be found in the components' datasheet:

- t_{rr} is the reverse recovery time;
- V_{TO} is the diode threshold voltage;
- R_F is the on resistance.

Note that the diode resistance can be calculated through the forward drop voltage versus forward current graphic.

7.9.3 Core Loss

The losses in the ferrite core are caused by hysteresis and Eddy Current Loss, so they are determined by the following expression:

$$P_{core} = \Delta B^{2.4} (K_h f + K_f f^2) V_{core} \tag{277}$$

Which:

- ΔB is the magnetic flux density excursion;
- K_h is the hysteresis loss coefficient;
- K_f is the eddy current loss coefficient.

Moreover, it is possible to calculate ΔB as follows:

$$\Delta B = \frac{L I_{max}}{N A_e} \tag{278}$$

7.9.4 Copper Loss

The copper losses are due to the Joule and Skin effect. Although the skin effect can be decreased by selecting a proper copper diameter according to the switching frequency, the Joule effect cannot be diminished. The equation 279 represents the core loss.

$$P_{copper} = \frac{\rho_{copper} I_{rms}^2 l_{turn} N}{n_{cond}} \tag{279}$$

Which:

- ρ_{copper} is the copper electrical resistivity;
- N is the number of turns.

7.9.5 Total losses

Finally, the total losses in the prototype calculated with the equations presented in this section are represented in table 12.

Table 12 – Power losses of the prototype

Specification	Value
Full-Bridge Stage MOSFET	20.3 W
Push-Pull Stage MOSFET	22.9 W
Buck MOSFET	1.36 W
Clamping Diode	1.55 W
Buck Diode	3.01 W
Transformer	5.164 W
Push-Pull Stage inductor	4.02 W
Buck inductor	3.93 W
External inductor	0.55 W
Total	63 W

Source: Own elaboration

Besides the thermal stresses calculation, the total losses are important to optimize the converter's components and also compare the estimated power losses with the real converter's efficiency.

7.10 THERMAL STRESSES

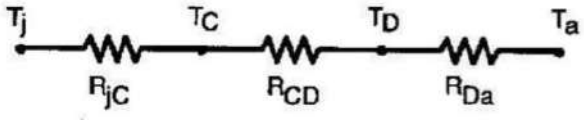
The calculation of thermal stresses is very important to design the converter, since that an overheat would damage its components. The aim is to make sure the semiconductor junction temperature remains below the greatest value allowed by the manufacturer. Besides, the degradation of a semiconductor results in chemical reactions on a nuclear scale that collapse the component structure. Thus, the lower the working temperature at the junction, the lower the failure rate.

To calculate the thermal stresses the Figure 113 will represent the thermal circuit relating the temperature with some resistors.

Which:

- T_j is the junction temperature;
- T_C is the encapsulation temperature;
- T_D is the heat sink temperature, considered 100$^{\circ}C$;

Figure 113 – Prototype detailed



Source: (BARBI, 2007)

- R_{jc} is the thermal resistance of the junction-capsule;
- R_{CD} is the thermal resistance between the semiconductor and heat sink;
- R_{Da} is the ambient heat sink resistance;
- T_a is the room temperature, considered 50$°C$.

Therefore, the step-by-step calculation will be presented in Appendix A. In summary, a room temperature is adopted, then the necessity of a heat sink is checked by calculating the total resistance of each component and comparing with its datasheet value. If the calculated resistance is smaller than the datasheet resistance, then a heat sink must be sized to keep the component operating below the maximum junction temperature.

Therefore, the maximum thermal resistance of the heat sink for each component can be calculated using the power loss of each component ($P_comploss$), as follows:

$$R_{Dacomp} = \frac{T_j - T_a}{P_{comploss}} - R_{jc} - R_{CD} \tag{280}$$

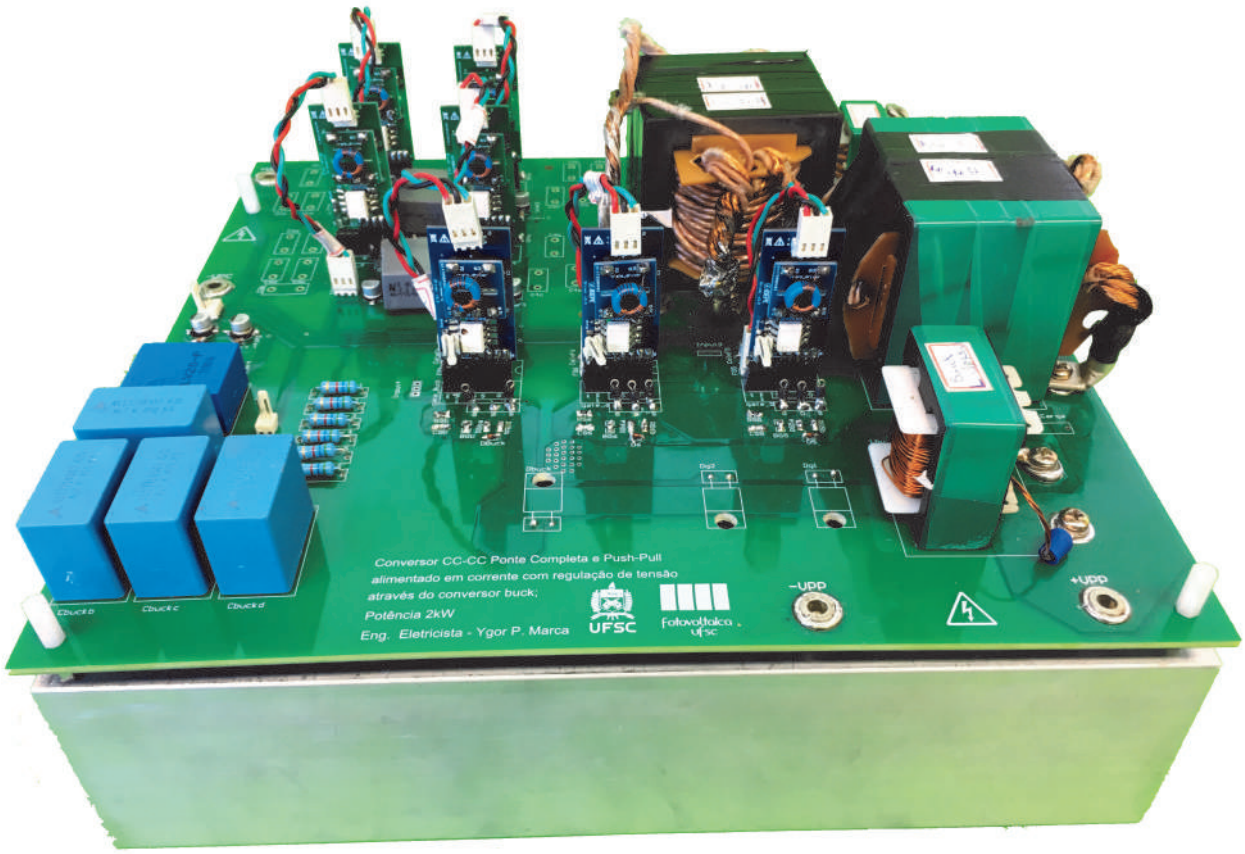
While equation 280 is used to check the maximum resistance for each component, equation 281 calculates the heat sink resistance by applying a correction factor (F_C) for the room temperature used, a safety factor (F_S) and the total power losses (P_{Tloss}).

$$R_{Da} = F_C \frac{T_j - T_a}{F_S P_{Tloss}} = 0.667 \frac{°C}{W} \tag{281}$$

The safety factor is applied in the formula in order to oversize the heat sink as using a high ambient temperature. In addition, some coolers can be applied so the cool forced wind decreases its temperature.

So, the model HS 21575 was used to connected the semiconductors as represented in Figure 114. The heat sink model has a resistance equals to 0.353 $\frac{\Delta^{o}C}{W}$, which is smaller than the resistance found in equation 281 to secure a low temperature operation.

Figure 114 – Final prototype connected to the heat sink



Source: Own elaboration

Furthermore, it is necessary to calculate each semiconductor junction-capsule thermal resistance using equation 280 and check if the junction temperature is bellow the recommended by the manufacturer, which will be presented next.

In addition, the thermal stresses in the magnetic elements must be calculated to verify if the core will not overheat and be damaged, otherwise it has to be substituted. The equation 282 gives the temperature rise in these components:

$$\Delta T = 23(P_{core} + P_{copper})(A_e A_w)^{-0.37} \tag{282}$$

So, the components' temperature rise considering the heat sink are presented in table 13.

In conclusion, the design of a proper heat sink ensures a low temperature rise in the active components. So, the thermal stresses should not be a problem in the prototype operation.

Table 13 – Temperature rising of the converter's components

Component	**Temperature rise**
Full-Bridge Stage MOSFET	88.6 $\Delta°C$
Push-Pull Stage MOSFET	88.1 $\Delta°C$
Buck MOSFET	83.9 $\Delta°C$
Clamping Diode	86.7 $\Delta°C$
Buck Diode	95.4 $\Delta°C$
Transformer	20.23 $\Delta°C$
Push-Pull Stage indutctor	17.5 $\Delta°C$
Buck inductor	32.5 $\Delta°C$
External inductor	6.5 $\Delta°C$

Source: Own elaboration

8 EXPERIMENTAL RESULTS

This chapter presents the experimental results of the proposed converter that will be used to prove its efficiency and the bidirectional power flow. The equipment and set up necessary to debug the project and do the tests will be explained through the chapter.

It is necessary a different set up for each power flow, so in the positive power flow the voltage source is connected in V_{FB} and a resistive load is connected in V_{bat}, also for the negative power flow the opposite connection is correct.

Therefore, the connections change for each set up. However, in a microgrid both sides would be bidirectional power sources, the Lithium-ion batteries and DC bus. Then, in a real application the set up would be equal for both power flows.

It is noticed the importance of having only one modulation technique for both power flows, since it offers a better and faster transition between the power flow directions. Also, with a fast transition the converter becomes controllable to keep the DC bus voltage constant. Some bidirectional converters presented in the literature with two different modulations for each power flow may not work in real applications.

Thus, to generate the gate signals and process the control, a DSP from Texas Instruments (LAUNCHXL-F25069M) was used. The modulation technique presented in previous chapter is shown in Figures 115 and 116. It was not possible to acquire all of the gate signals in a single picture since the model MDO3024 from Tektronix used has four channels.

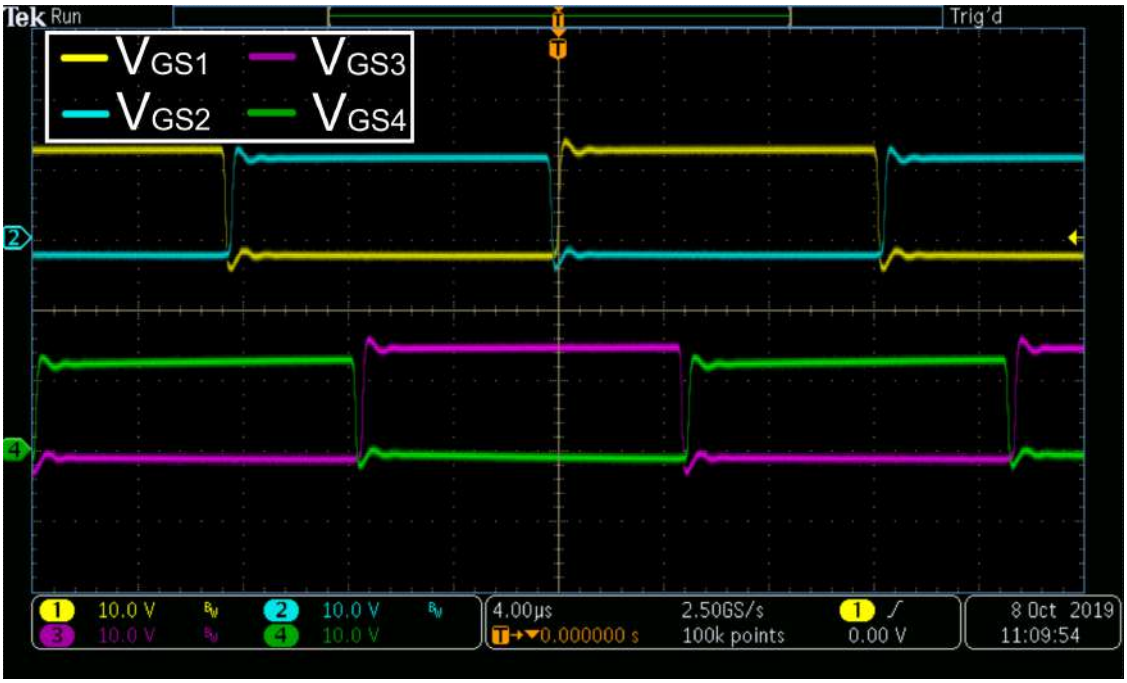
The time division in the Figures above illustrate a switching period of 25 μs that represents the switching frequency of 40 kHz. In addition, it can be noticed the designed dead-time on the gate signals in the Full-bridge MOSFETs and the phase shift between the Full-bridge's legs that represents the duty cycle.

It is very important to notice the synchronization between the gate signals of the Full-bridge Stage and Push-Pull Stage, since any delay could cause a current peak in the leakage inductance that would damage the components. So, MOSFET S_5 must be gated on when S_1 is gated on and gated off when S_3 is gated on, also MOSFET S_6 must be gated on when S_2 is gated on and gated off when S_4 is gated on as illustrated in Figure 82. Furthermore, this current peaks will be illustrated in the positive power flow results.

8.1 POSITIVE POWER FLOW

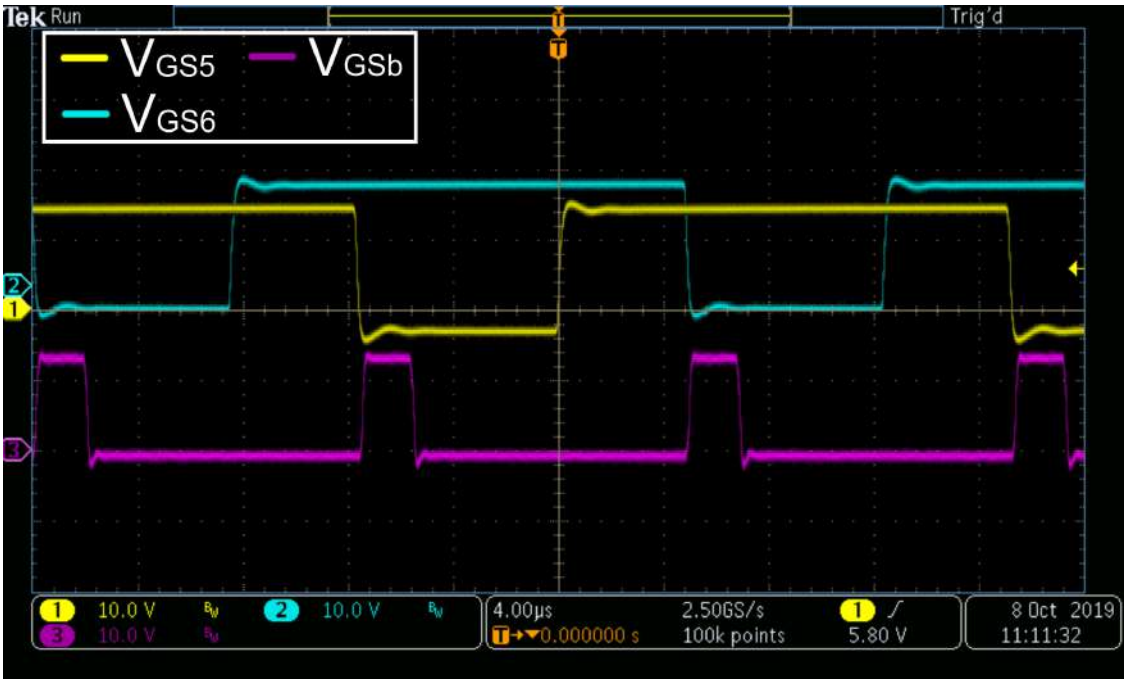
In the positive power flow set up a power supply was connected across the 120 μF polypropylene capacitors of the Full-bridge terminals that represents the DC bus and a resistive load was connected in the Push-Pull terminal that represents the batteries. Note that for this application, the batteries would be charging.

Figure 115 – Gate signals of the DC-DC Full-Bridge ZVS-PWM Stage MOSFETs



Source: Own elaboration

Figure 116 – Gate signals of the Current-Fed Push-Pull Stage and Buck MOSFETs



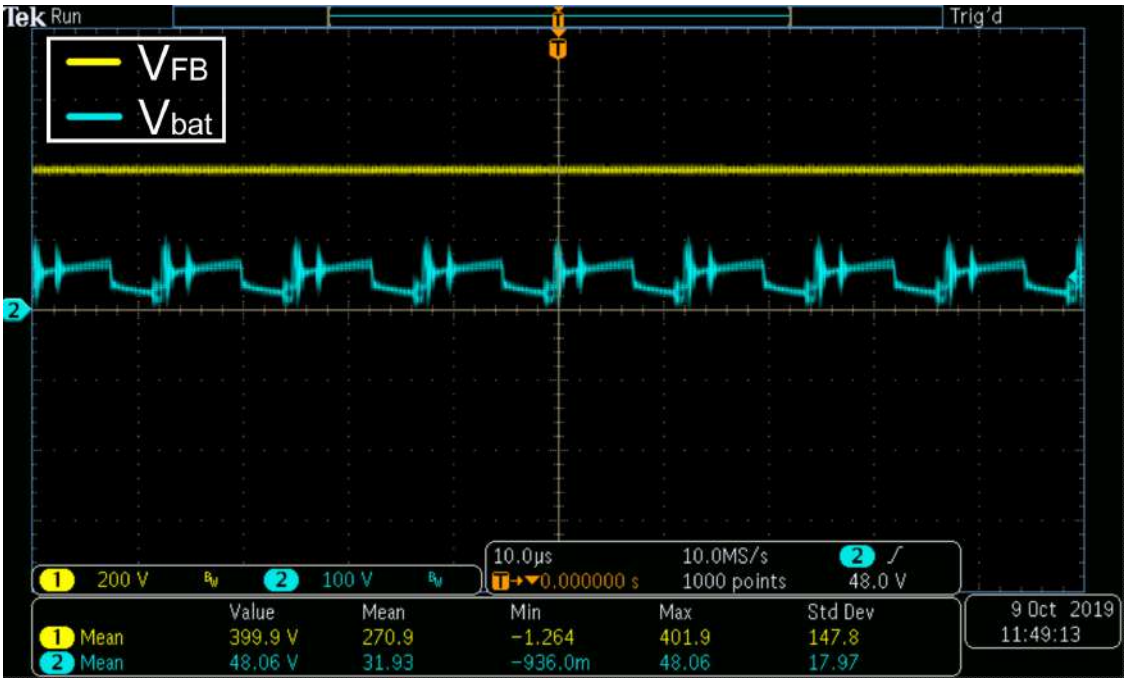
Source: Own elaboration

The resistive load can be calculated through equation 283.

$$R_{bat} = \frac{V_{bat}^2}{P_{out}} = 1.152\Omega \tag{283}$$

This low resistance that dissipates 2000 W was obtained through the parallel connection of some electric household heater. Therefore, for the designed converter, when the power source supply full load or 2000 W, the input and output voltages are acquired as represented in Figure 117.

Figure 117 – DC bus and battery voltages for the positive power flow



Source: Own elaboration

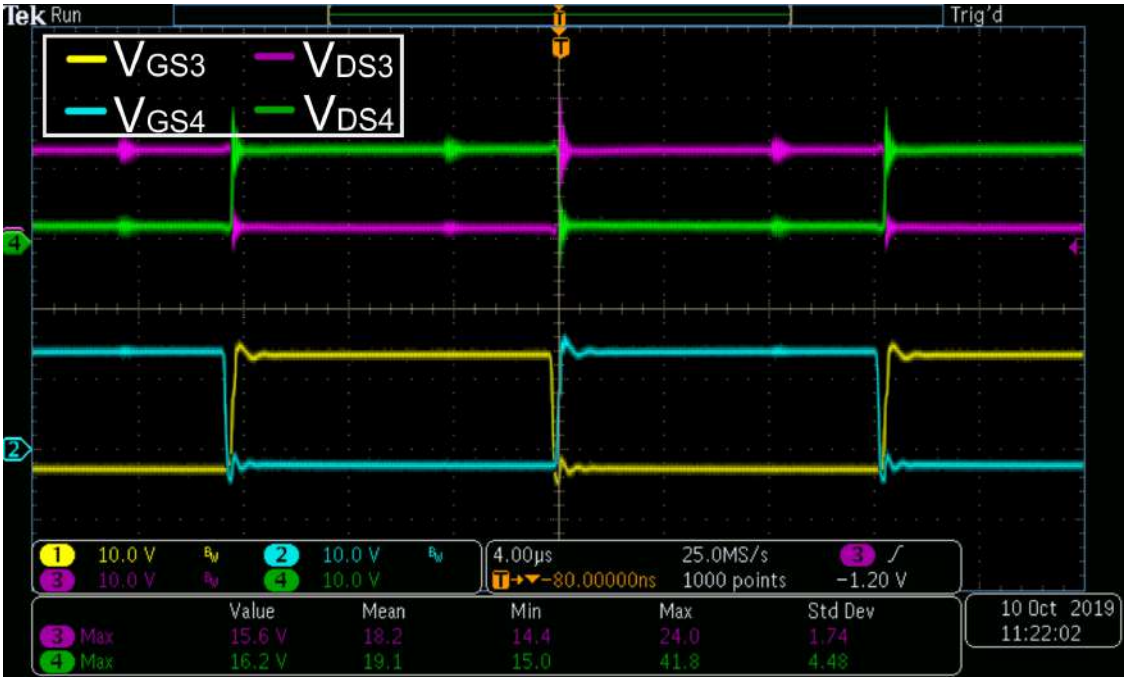
Then, the input DC bus voltage (V_{FB}) was 400 V and the Lithium-ion battery bank (V_{bat}) was 48 V as expected.

An important result to analyze is the soft commutation of the MOSFETs in the Full-Bridge Stage. In Figure 118 are shown the gate signals and drain-source breakdown voltage of the MOSFETs in the critical leg (S_3 and S_4).

Therefore, to analyze the Zero Voltage Switching it is necessary to decrease the time interval observed in the oscilloscope to 200 nanoseconds. In addition, as the ZVS is achieved only for a minimum load current, the analysis will be demonstrated by increasing the input power supply. Then, Figure 119 shows that for a low output current the converter is still operating with hard commutation, since the voltage across S_4 does not reach zero until the dead-time ends.

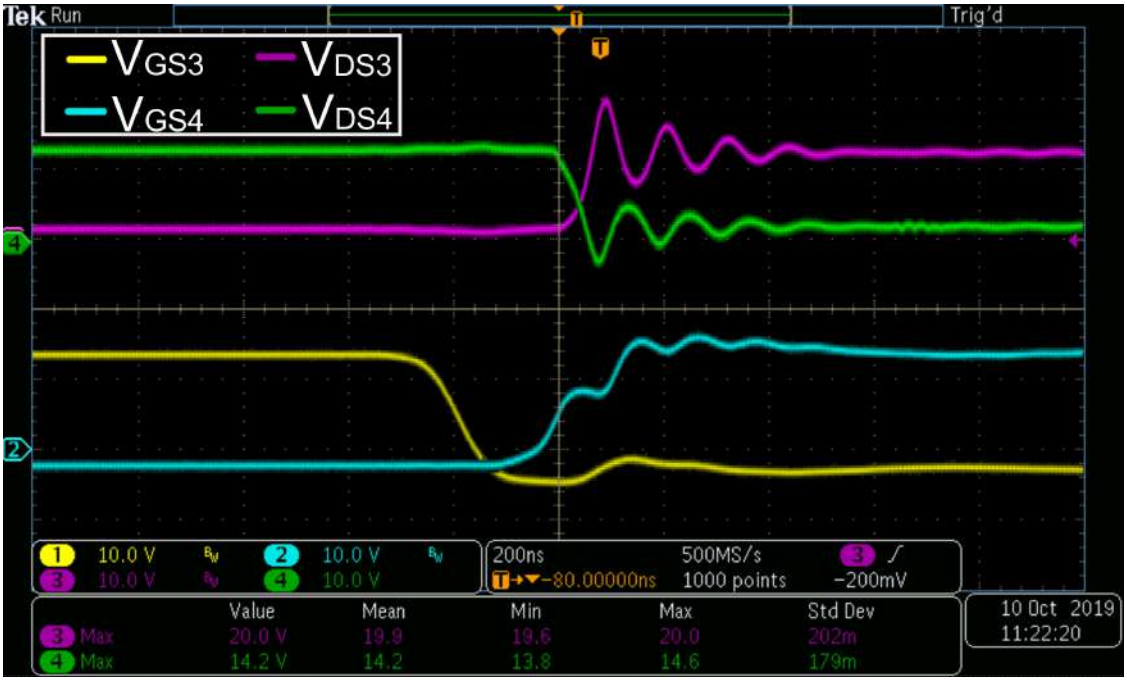
Furthermore, it is notable the voltage ringing caused by the hard switching and understand the importance of the soft commutation. So, when the load current approaches the minimum value necessary to achieve ZVS, the breakdown voltage across S_4 during the dead-time is almost zero and the voltage ringing is mitigated as represented in Figure 120.

Figure 118 – Gate signals and breakdown voltage of the Full-bridge MOSFET's lagging leg for the positive power flow



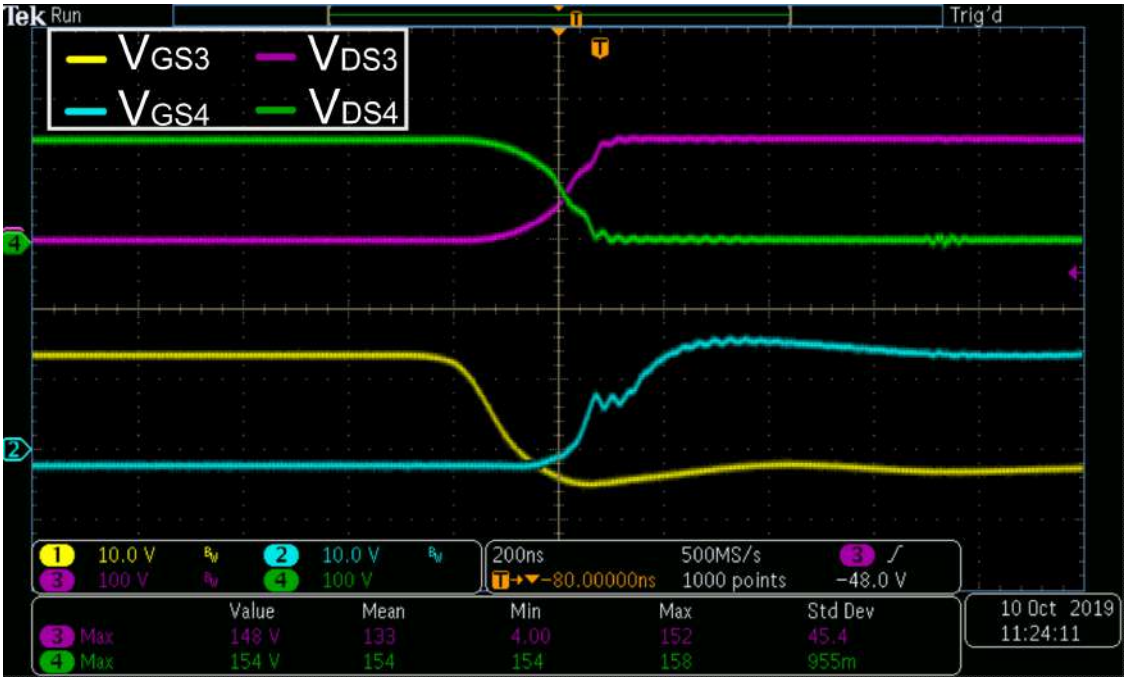
Source: Own elaboration

Figure 119 – Hard switching for the positive power flow



Source: Own elaboration

Figure 120 – Hard switching with almost the minimum load current to achieve ZVS for the positive power flow



Source: Own elaboration

So, Figure 120 presents a breakdown voltage of 150 V in the Full-bridge MOSFETs. After this point, the load current is greater than the minimum current to achieve ZVS as it was designed to be with 40% of the nominal output power (800 W). Thus, Figure 121 illustrates the soft commutation of the Full-bridge's critical leg and also the maximum breakdown voltage for nominal power of 400 V.

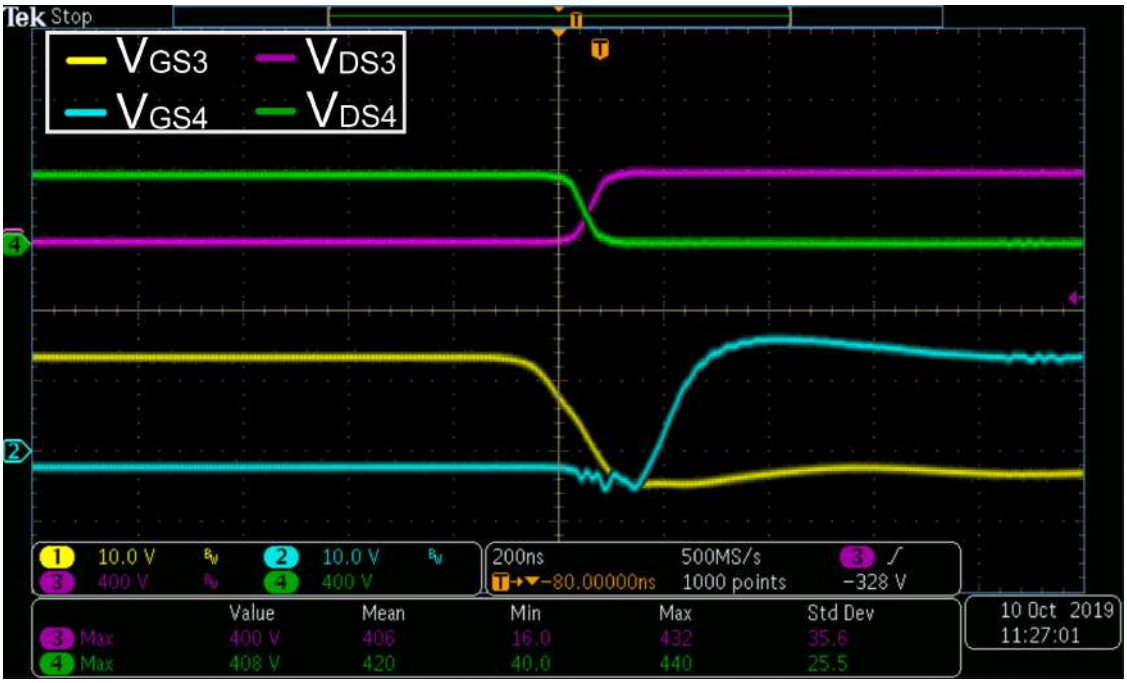
It is notable the decrease of the voltage ringing when the converter is operating with Soft Commutation as the peak voltage that appears in Figure 118 is totally gone in Figure 121.

In addition, it is important to analyze the buck converter's operation as an active voltage clamper. The operation of the converter was designed with a voltage input of 220 V on its capacitor and , so the Push-Pull MOSFETs are clamped with the same voltage. However, as the buck and Push-Pull MOSFETs used have a breakdown voltage of 600 V, the analysis of the voltage clamping operation will be presented for values near the maximum a minimum clamping voltage.

Note that this analysis is possible only for the positive power flow since the buck's power flow comes only from the diode reverse recovery current. A voltage clamper lower than the designed 220 V in the negative set up would increase the buck's current that could damage the circuit.

In an open-loop operation, by varying the buck's duty cycle it is possible to vary

Figure 121 – Soft switching for the positive power flow



Source: Own elaboration

the breakdown voltage across the MOSFETs. So, Figure 122 shows the MOSFETs breakdown voltages of the Push-Pull Stage and the voltage in buck's capacitor with a low voltage and Figure 123 illustrates the same waveforms with a high voltage. So, it is possible to claim that the greater is the buck's duty cycle, the smaller is the capacitor voltage and vice-versa.

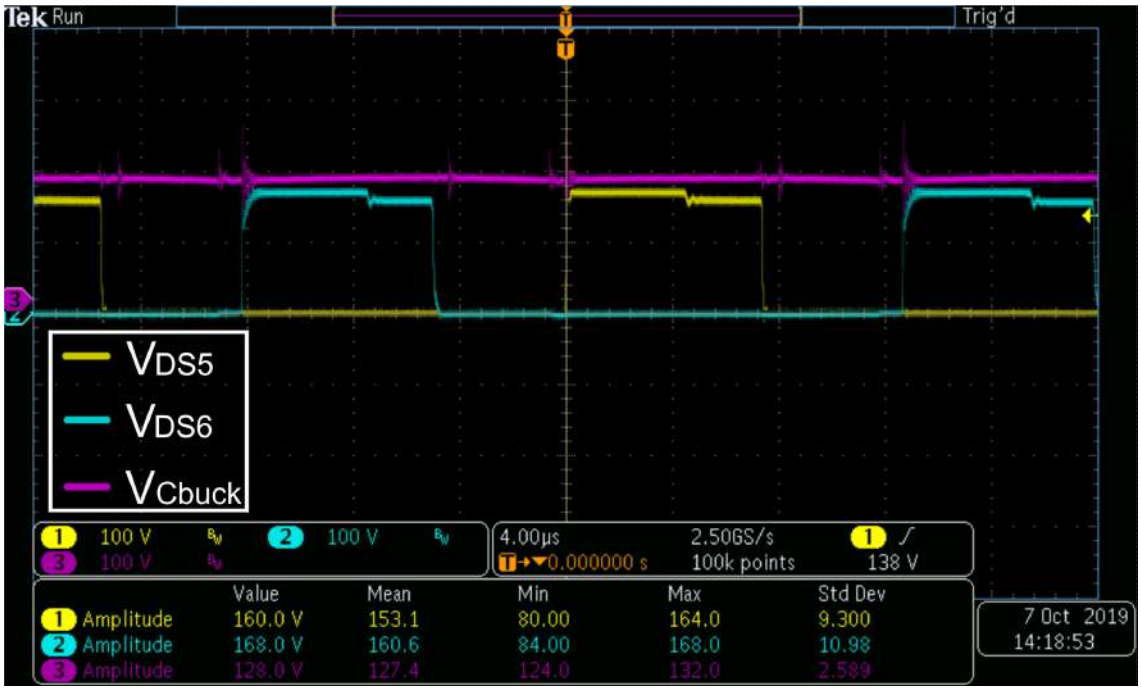
So, the minimum clamping voltage should be near the ideal MOSFET's breakdown voltage of the Push-Pull Stage, as represented in Figure 122.

Also, the maximum clamping voltage must be smaller than the maximum breakdown voltage of the acquired Push-Pull MOSFET, as represented in Figure 123.

In an ideal operation, the buck converter would not be used in the positive power flow operation. However, in practical experience the reverse recovery current of the diodes in anti-parallel with the Push-Pull MOSFETs are significant for high power applications and could cause a destructive voltage peak in the same MOSFET, if there is not a snubber circuit.

Furthermore, the buck's converter presented itself as a great solution for operate as an active snubber. So, with the results obtained for a open-loop operation that imposes an input voltage with a designed duty cycle, the operation with a closed-loop control of the input voltage is not necessary since the converter is already stable and it would increase the DSP processing. Also, the buck's duty cycle can be calculated by adopting a clamping voltage and applying in equation 178.

Figure 122 – Low clamping voltage for the positive power flow



Source: Own elaboration

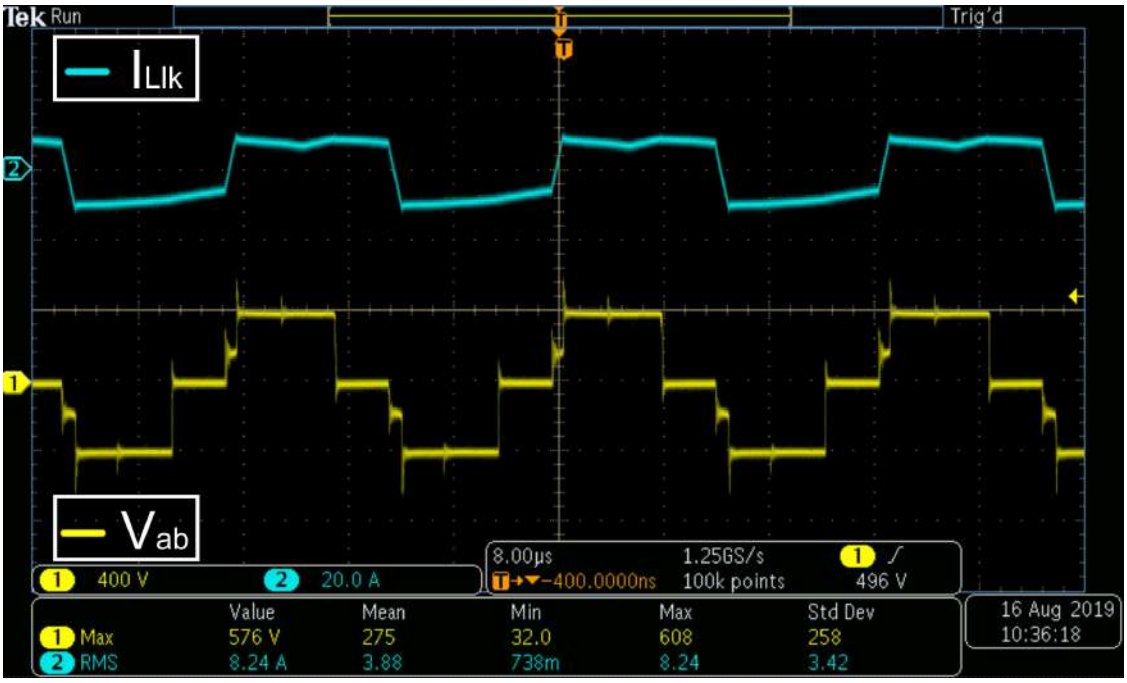
Figure 123 – High clamping voltage for the positive power flow

Source: Own elaboration

In fact, in practical experience the buck's converter duty cycle should gate on its MOSFET when a Push-Pull MOSFET is gated off or some near that because this is the period when the buck's capacitor is charged. Therefore, the attempt to control the input voltage failed with a PI controller as the transfer function presents a pole in the origin and the Push-Pull operation was affected.

Moreover, it is very important to analyze the behavior of the current and voltage across the primary side of transformer and compare it with the theory presented about the Full-BRidge Stage, since the current in the leakage inductance is very important to achieve ZVS. So, Figure 124 illustrates the voltage and current in the transformer which are similar to what was presented in the theory, without a noticeable influence of the clamped circuit in the primary side voltage.

Figure 124 – Transformer's primary side voltage and leakage inductance current for the positive power flow



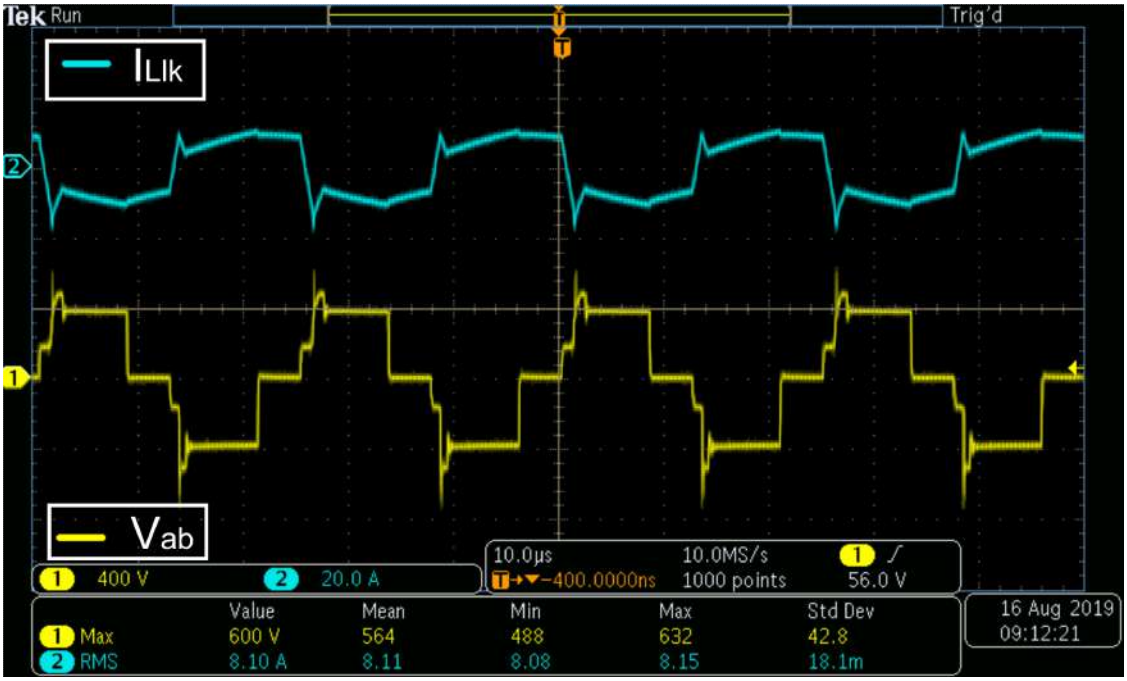
Source: Own elaboration

As can be seen from Figure 124 the leakage inductance current plunged in a certain period, this phenomenon is due to the delay between the gate signals from the Full-bridge and Push-Pull Stages since the hardware circuit used to gate drive these MOSFETs have different values of bead inductor and gate resistance.

Thus, a small difference does not harm the circuit's operation, as it is clear in Figure 124. However, when this delay is great some non-expected topological state could damage the circuit and the main cause of a considerable delay is the software used to generate the gate signals.

So, by applying some delay in the Push-Pull Stage gate signals this phenomenon is better explained, as it is represented in Figure 125.

Figure 125 – Transformer's primary side voltage and leakage inductance current with a gate signal delay between the power stages for the positive power flow



Source: Own elaboration

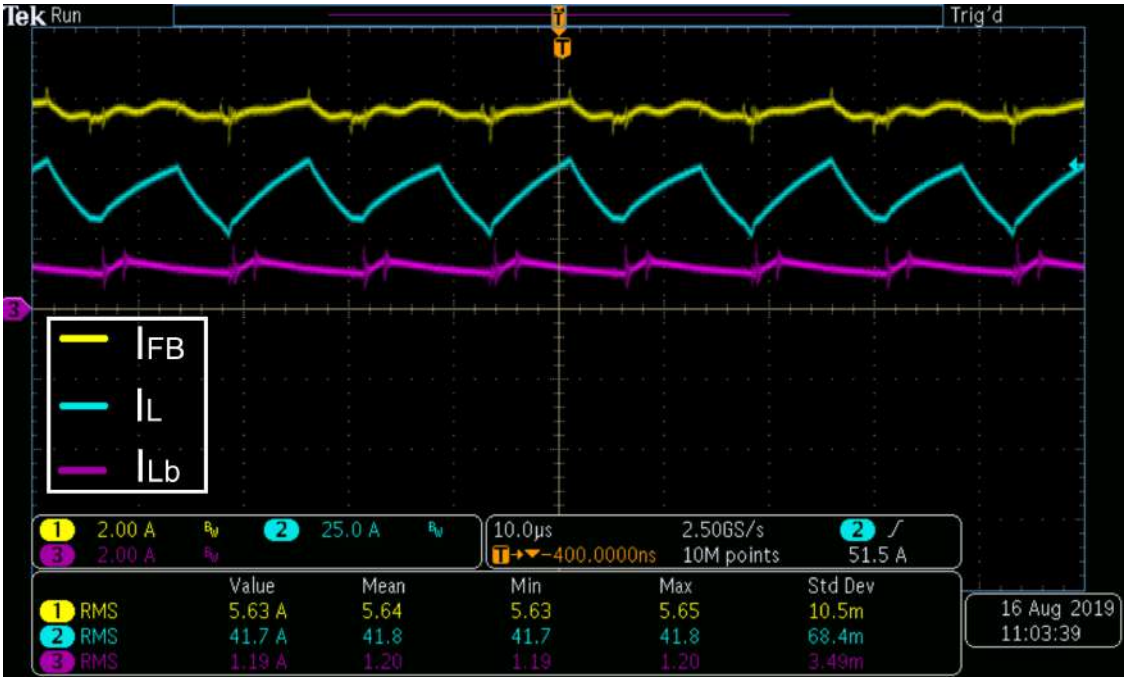
Therefore, it is clear that by gating on the MOSFETs of the Full-Bridge Stage S_1 and S_3 before gating on the MOSFETs of the Push-Pull Stage S_5 and S_6, respectively, there are still a voltage across the transformer and so the leakage inductance current keeps increasing until the end of the delay. Note that this phenomenon also happens for the negative side, so it has to be avoided by generating synchronized gate signals.

Finally, the current of two power stages and the buck converter are presented in Figure 126.

It can be observed that the current in the buck converter is great for a low clamping voltage, since the diodes in anti-parallel with the Push-Pull MOSFETs have a high reverse recovery current. So, in the negative set up this phenomenon has to be considered, so that the buck converter is not overloaded. Actually, this can be easily obtained by applying a clamping voltage of 300 V instead of the 220 V designed.

Also, it can be seen in graph the current of the Full-bridge and Push-Pull which represents the input and output current, respectively. Although the current waveforms are as expected in theory, their RMS values will not be considered to an efficiency analysis since the oscilloscope does not offer an acceptable measurement precision.

Figure 126 – Current in the Full-bridge Stage, Push-Pull Stage and Buck converter for the positive power flow



Source: Own elaboration

8.2 NEGATIVE POWER FLOW

In the negative power flow set up a power supply was connected in the Push-Pull terminal that represents the batteries and a resistive load was connected in the 120 μF polypropylene capacitors of the Full-bridge terminals that represents the DC bus. Note that for this application, the batteries are being discharged.

The resistive load can be calculated through equation 284.

$$R_{FB} = \frac{V_{FB}^2}{P_{out}} = 80\Omega \tag{284}$$

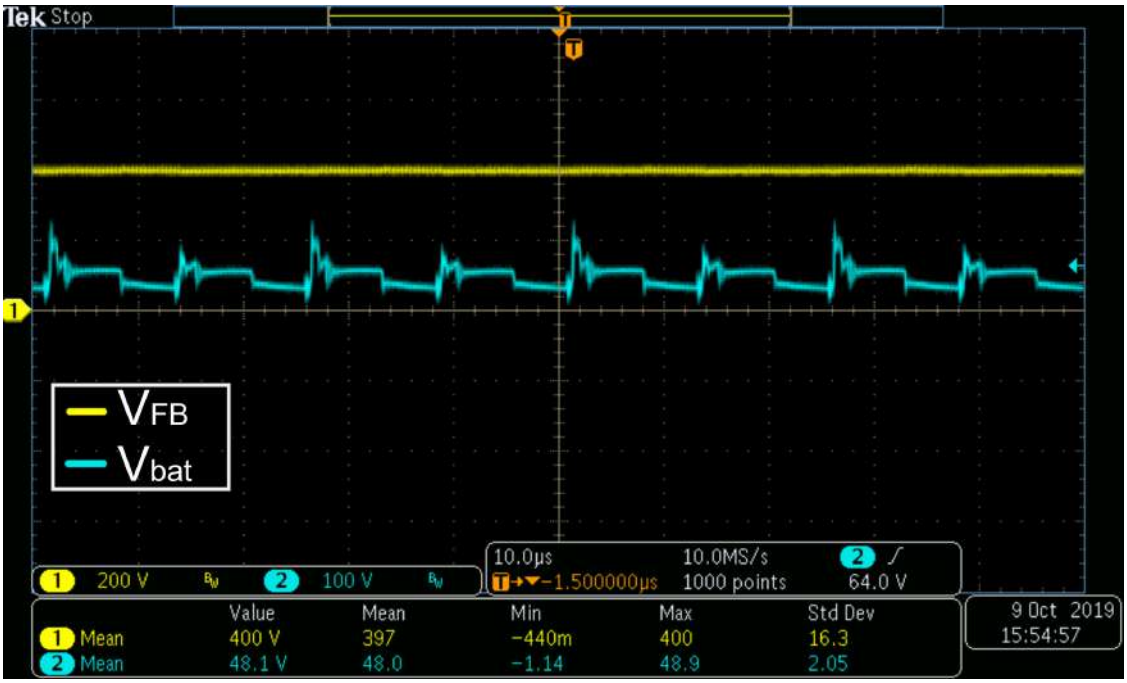
This resistance that dissipates 2000 W was obtained through the series connection of the same electric household heater used in the positive power flow. Thus, for the designed converter, when the converter is operation with full load or 2000 W, the input and output voltages are acquired as represented in Figure 127.

Again, the input DC bus voltage (V_{FB}) was 400 V and the Lithium-ion battery bank (V_{bat}) was 48 V as expected.

An important result to analyze is the commutation of the Full-bridge MOSFETs. Therefore, it is shown in Figure 128 the gate signals and drain-source breakdown voltage of the MOSFETs in the critical leg (S_3 and S_4).

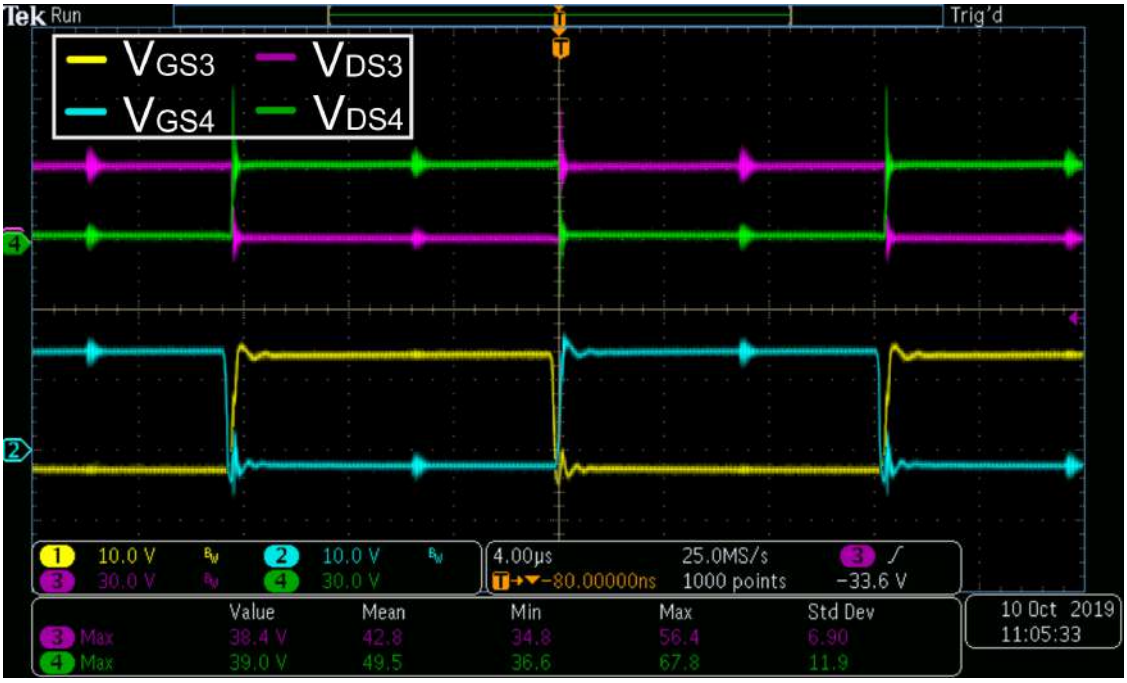
However, to analyze the commutation it is necessary to decrease the time interval

Figure 127 – DC bus and Battery voltage for the negative power flow



Source: Own elaboration

Figure 128 – Gate signals and breakdown voltage of the Full-bridge MOSFET's lagging leg for the negative power flow

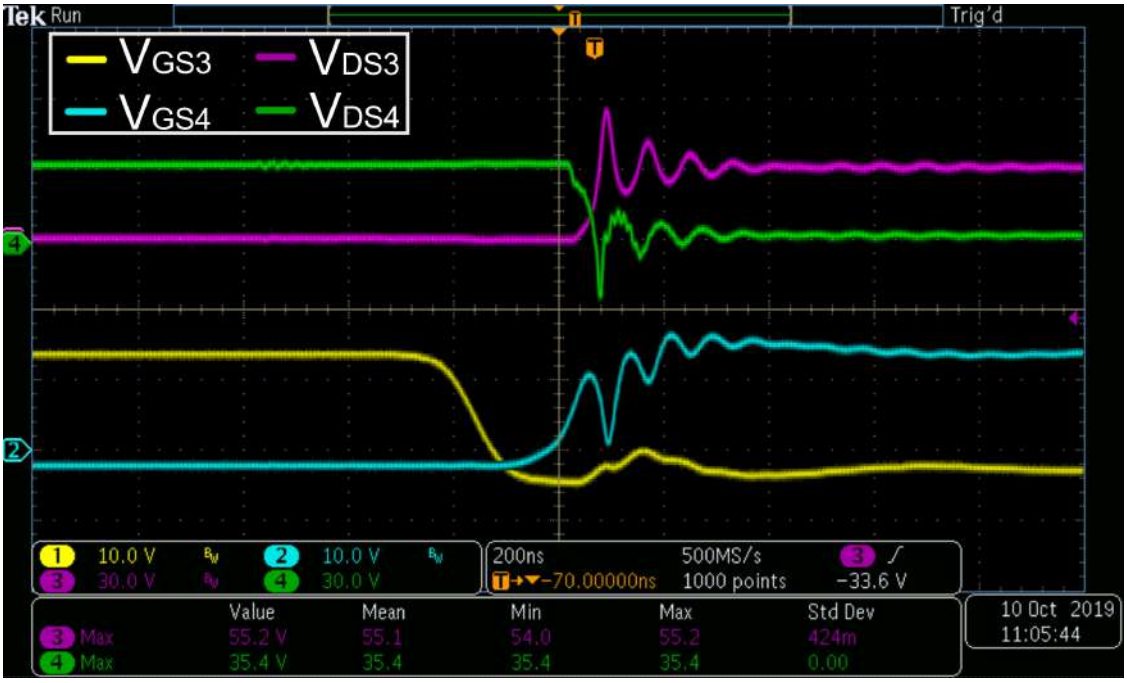


Source: Own elaboration

observed in the oscilloscope to 200 nanoseconds. As it was studied in the topological states of the negative power flow, the Full-bridge cStage does not operates with ZVS in any period, even with maximum load current, because the commutation capacitors do not charge and discharge during the dead-time interval between the MOSFET's gate signals.

Therefore, to do the analysis for the negative power flow, some Figures will be presented by increasing the input power supply to verify the converter's commutation. Then, Figure 129 shows that for a low output current the converter is operating with hard commutation, since the voltage across S_4 does not reach zero before the end of the dead-time interval.

Figure 129 – Hard switching for a low input current and the negative power flow



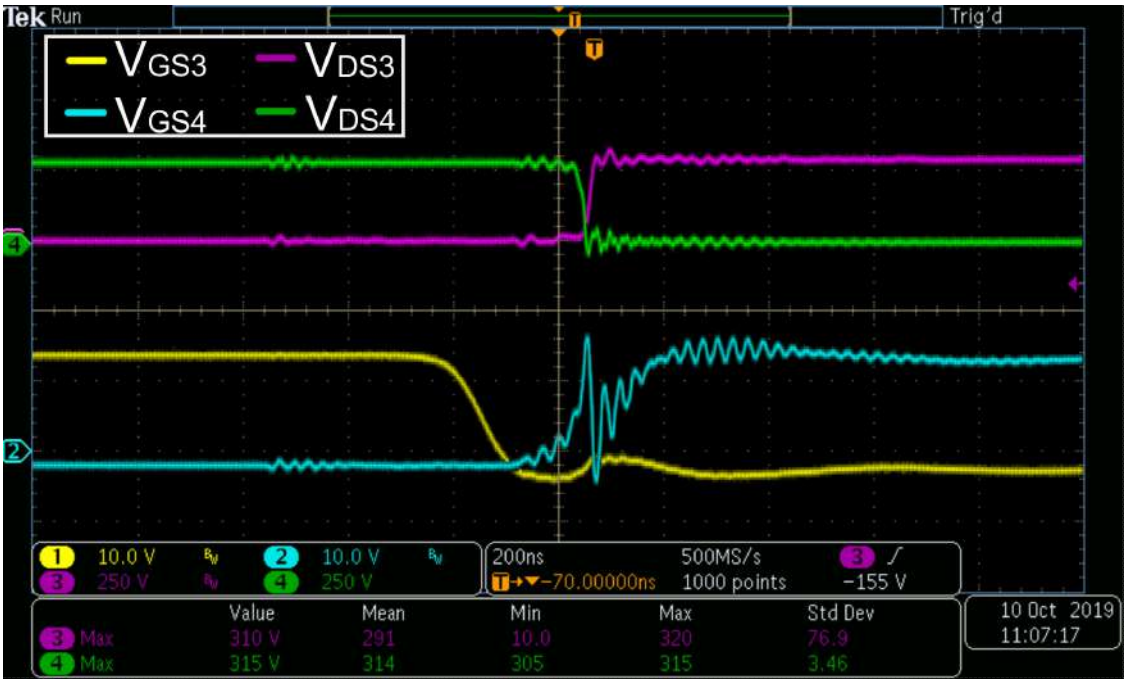
Source: Own elaboration

It can be inferred from Figure 129 that the commutation starts after the dead-time, so it is a hard switching. Also, this kind of commutation generates voltage ringing in both gate-source and drain-source signals.

However, for a low input current some phenomenons are not stabilized yet, such as the intrinsic capacitance of the MOSFET that changes according to the drain-source voltage increase. So, these voltage ringing should be checked again for a higher power application, as represented in Figure 130.

The supplied graph in Figure 130 denotes a sharply decline compared with the voltage ringing expressed in Figure 129 for the breakdown voltage across the MOSFETs, but the gate signals are still being affected by the switching noise.

Figure 130 – Hard switching for a medium input current and the negative power flow



Source: Own elaboration

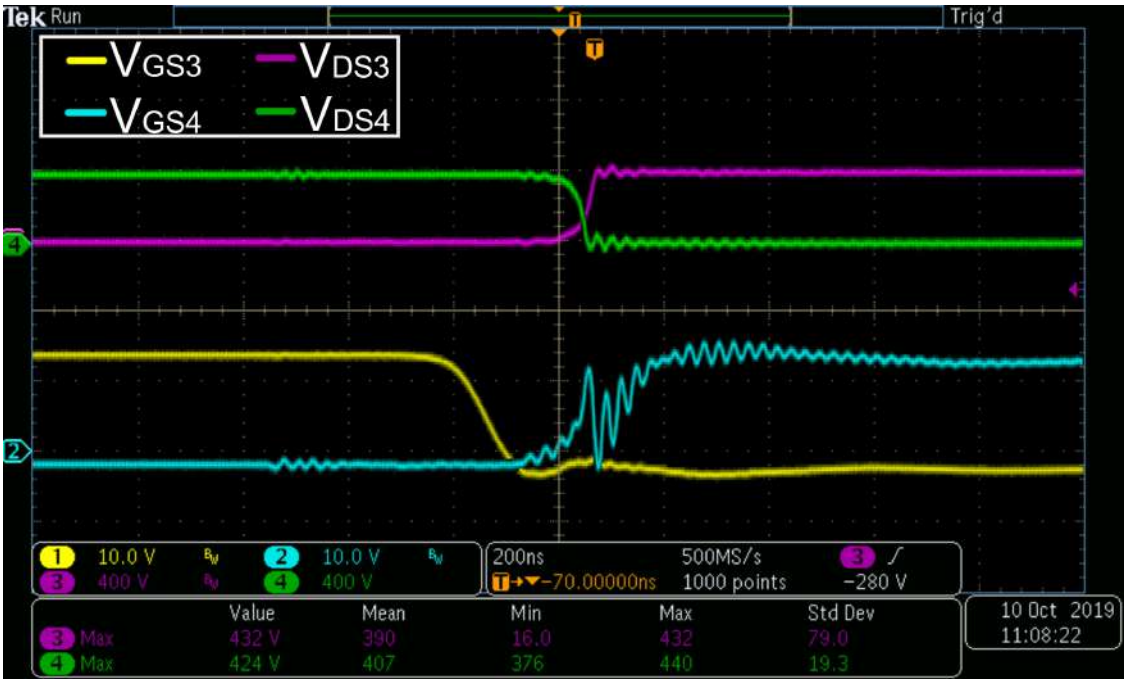
Although this noise did not harm the circuit's operation, some voltage spike could gated on or off a MOSFET in an inadequate time period if the spike last too long, which was not the case. Also, these voltage ringing can be due to the cable's inductance interference in the voltage measurement, since the negative spike in V_{GS4} would be sufficient to gated off V_{DS4} and it did not, so the voltage ringing is heightened by the cable's inductance.

Furthermore, as explained before, the voltage ringing should decline for a high power operation, since the converter was designed to a full load operation and the voltage ringing in the circuit presents a fast dynamic for light load. The given Figure 131 outlines a low voltage ringing in both gate-source and drain-source voltage for a full load operation.

The provided Figure 131 presents a breakdown voltage of 400 V and a hard switching since the commutation occurs after the dead-time ends.

In addition, it is important to analyze the buck's operation as an active voltage clamper for the negative power flow. The operation of the converter was tested with a voltage input of 300 V on its capacitor, so the Push-Pull MOSFETs are clamped with the same voltage. The higher the clamping voltage, the greater the efficiency of the converter. Then, as the buck and Push-Pull MOSFETs acquired have a breakdown voltage of 600 V, the analysis of the voltage clamper operation will be presented with 300 V instead of the designed 220 V.

Figure 131 – Hard switching for a maximum input current and the negative power flow



Source: Own elaboration

Furthermore, as explained for the positive power flow, an open-loop operation is sufficient to keep the clamping voltage stable, since the tests done with light and full load kept reliable. So, Figure 132 shows the Push-Pull MOSFETs breakdown voltages and the voltage in buck's capacitor with 300 V.

Moreover, it is very important to analyze the behavior of the current and voltage across the primary side of transformer and compare it with theory. Therefore, Figure 133 shows the voltage and current in the transformer which are similar to what was predicted by theory, with a considerable influence of the clamped circuit in the primary side voltage, because now the energy regenerated by buck's converter comes from the leakage inductance that is much higher than a diode reverse recovery energy.

The given Figure 133 presents also a different waveform shape of the leakage inductance current, which is explained by a delay between gate signals of both Full-bridge and Push-Pull MOSFETs.

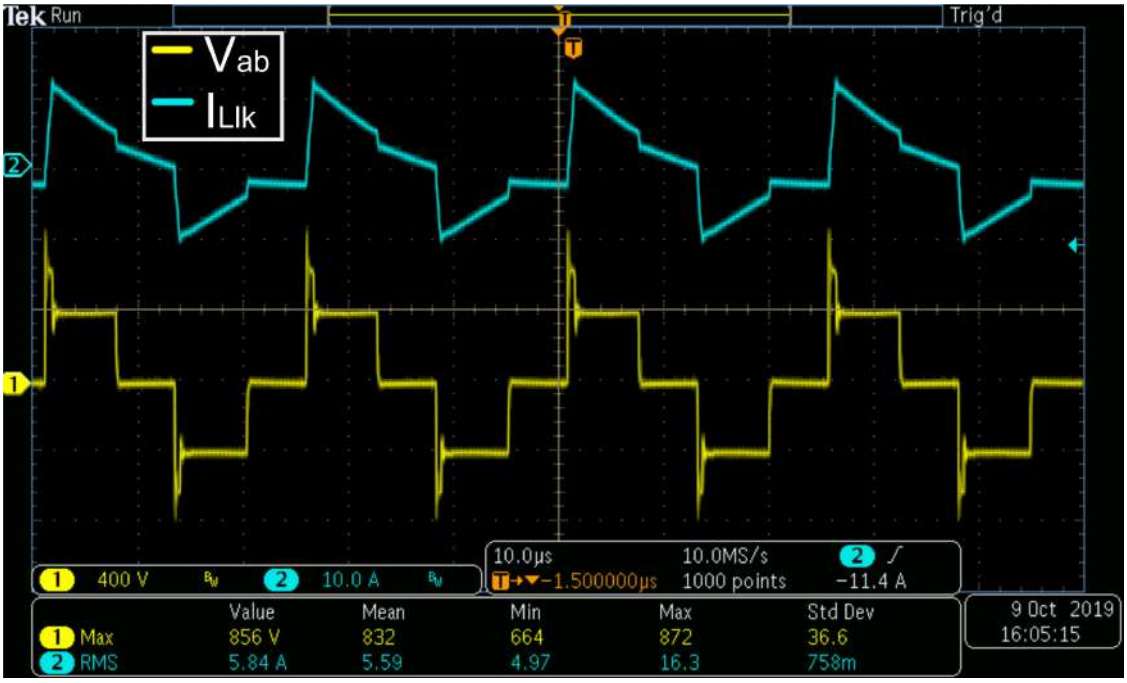
So, as explained for the positive power flow, a current peak may occur in the negative power flow if a Push-Pull MOSFET is gated off before the Full-bridge MOSFET is gated on. For instance, S_6 is turned off before S_4 is turned on.

The inappropriate gate signal's delay is due to the different MOSFETs used in the Full-Bridge and Push-Pull power stages. Thus, a satisfactory solution is apply a delay in the DSP software to compensate the hardware delay. Therefore, it is possible to turn off S_6 before turn on S_4, which causes the leakage current to decrease instead

Figure 132 – Clamping voltage for the negative power flow

Source: Own elaboration

Figure 133 – Transformer's primary side voltage and leakage inductance current for the negative power flow

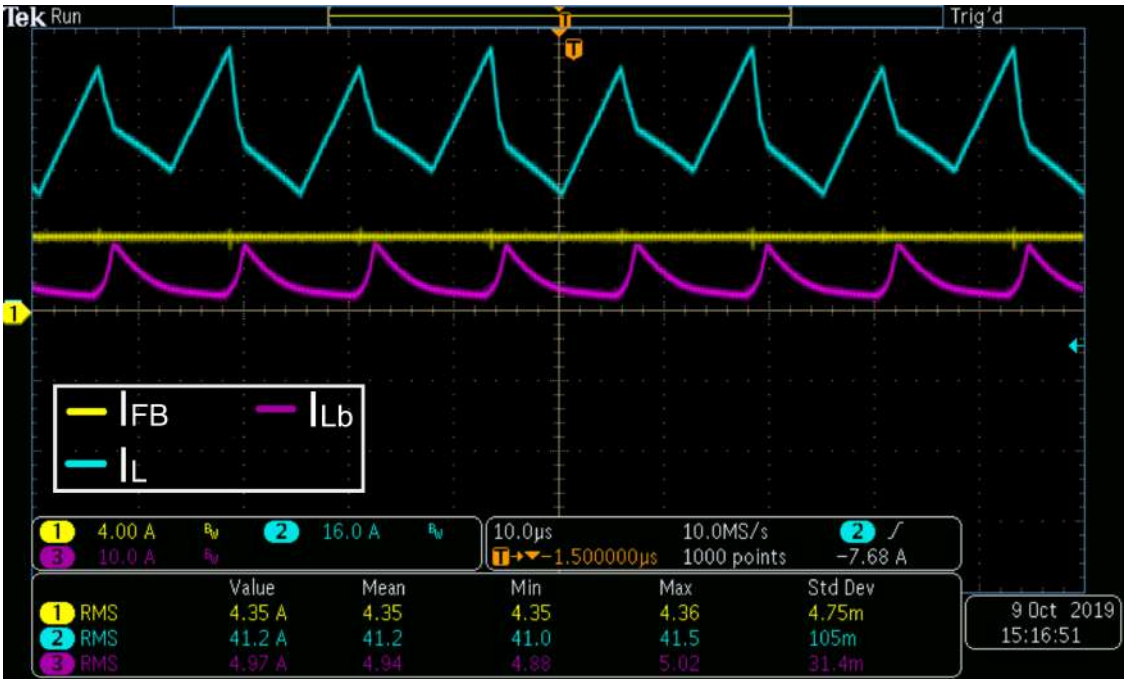


Source: Own elaboration

of increase. In other words, the current declined in Figure 133 is different from what theory predicted because of the mentioned delay.

Finally, the current of the two power stages and the Buck converter are presented in Figure 134.

Figure 134 – Current in the Full-bridge Stage, Push-Pull Stage and Buck converter for the negative power flow



Source: Own elaboration

It can be observed in Figure 134 that the current in the buck converter is great for a 300 V of clamping voltage, since the diodes in anti-parallel with the Push-Pull MOSFETs have a high reverse recovery current and the energy stored in the leakage inductor referred to the secondary side of the transformer demagnetize over the circuit, as explained in the Push-Pull theory.

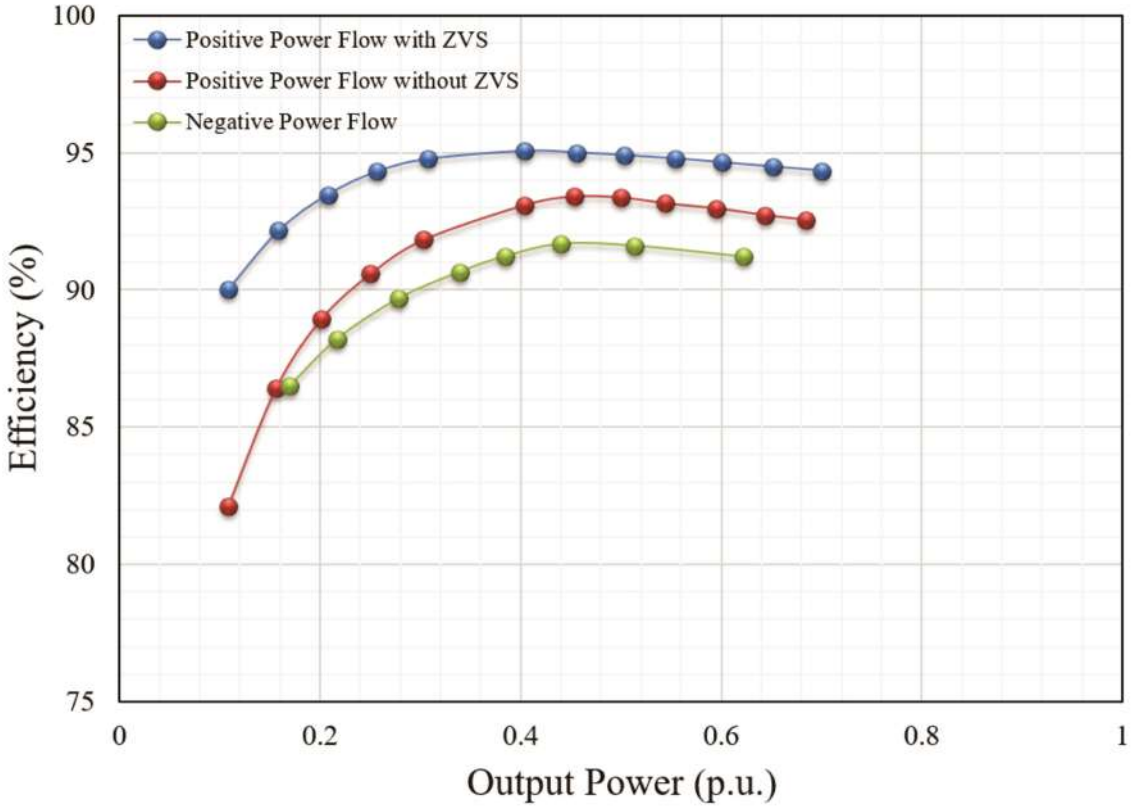
Finally, it can be seen in graph the current of the Full-bridge and Push-Pull Stages which represent the output and input current, respectively. It can be noticed a different waveform shape of Push-Pull inductor's current as presented in the theory, since a higher energy amount is regenerated back to the circuit, which distorts the waveform.

8.3 EFFICIENCY

Finally, one of the most important characteristic of a converter is the efficiency, so the last set up must connect a power analyzer equipment to confirm its performance for both positive and negative power flow.

So, a Power Analyzer model PA400 from Tektronix was connected in both input and output of the converter for both power flows. In fact, for the positive power flow two different set ups considered hard and soft commutation of Full-bridge's MOSFET. In addition, the equipment has a current limit of 30 A, which limited the power to 70% of its nominal value. Finally, Figure 135 describes the converter's efficiency as a function of the processed power.

Figure 135 – Converter's efficiency



Source: Own elaboration

The given illustration of Figure 135 delineates three performance curves, which have the maximum value of 95.1% for the positive power flow when it operates with ZVS and 91.8% for the negative power flow.

Therefore, it is evident the high efficiency of the proposed converter when compared with the maximum efficiency found in the State of the Art for similar converter topologies, which the maximum efficency of the positive power flow was 88% and the negative power flow was 80%.

In addition, it is notable the positive operation with an efficiency higher than 90% for all load test conditions when it has soft switching and the operation without soft commutation that decreases the converter's performance in at least 2%. Then, the efficiency results prove the soft switching efficacy and explain one reason that

contributes to reduce the efficiency for the negative power flow.

Furthermore, all the efficiency tests were done for an open-loop operation, since the batteries were not used in the converter's tests.

9 CONCLUSION

The dissertation thesis studied the application of a DC microgrid that can manage and distribute energy among several power sources and loads, with safe and stable operation. First of all, the existent market technologies in this field were exploited to understand the microgrid control needs and power distribution. Therefore, it was verified in this research the necessity of design an Isolated DC-DC Bidirectional Converter to connect the Lithium-ion battery bank with the microgrid DC bus. So, as the master thesis was done in the power electronics field, the bidirectional converter topology and its modulation technique were proposed and studied.

Therefore, the theoretical investigation about the DC-DC Full-Bridge ZVS-PWM and Current-Fed Push-Pull stages were presented in order to understand some concepts necessary to perform the Bidirectional Converter. So, as the bidirectional converter preserves the characteristics of both power stages, the sizing was accomplished preserving the same analysis.

In conclusion, the Isolated Bidirectional DC-DC Converter Based on the Integration of the Full-Bridge and the Current-Fed Push-Pull Converters clamped with a Buck converter was designed and tested with 2000 Watts. It presented an overall efficiency of 95.1% for the positive power flow and 91.8% for the negative power flow. So, this converter could be applied in DC microgrid applications to charge and discharge the Lithium-ion battery bank with the microgrid DC bus, since the experimental results confirmed the theoretical topological states, waveforms and deduced equations.

An unique modulation technique used for both power flow directions proved effective in practical experience, which confirms the bidirectionality of the converter and a voltage regulation through its static gain. Also, it is was observed the importance of implementing synchronized gate signals for both the Full-Bridge and Push-Pull Stage MOSFETs, since the signals delay would cause undesirable topological states and current stresses in the converter operation.

Furthermore, the soft commutation demonstrated its importance in the converter's efficiency, noise and voltage ringing by comparing it with hard switching. The Zero Voltage Switching is observed in the converter's positive power flow direction when the processed power reaches the minimum power projected to achieve ZVS.

Additionally, the Buck Converter resulted in a stable active voltage clamp that regenerates energy back to the main circuit, even for an open-loop operation which do not controls its input voltage. In fact, an open-loop system favored the practical experience, since the transfer function calculated is not simple to compensate. Actually, with the Buck's application proved, some others converter could be applied for the same goal.

Besides the converter's analysis, the proposed DC microgrid can to solve the

renewable energy problems such as intermittency and offer a safe connection of Lithium-ion batteries to stabilize the system. So, for future microgrid applications, this study can be used as a reference to understand the microgrid power flow and the control solutions necessary to perform the system.

9.1 FUTURE STUDIES

To conclude, some final proposals of future works are listed:

- Design other converter to be used as a voltage clamp and compare its efficiency with the Buck Converter;
- Study, project and implement an effective voltage clamp controller;
- Study and apply soft commutation for the negative power flow to optimize the converter's efficiency on this power flow direction;
- Study the leakage inductance interference in the converter's efficiency;
- Verify the influence of the magnetizing inductance in the converter's operation;
- Study the effect of the gate signals delay between both converter stages.

REFERENCES

ALAM, Farooq et al. Robust droop control design for a hybrid AC/DC microgrid. **2016 UKACC 11th International Conference on Control**, IEEE, p. 1–6, 2016.

ALMAZROUEI, Sumayya; HAMID, Abdul-Kadir; SHAMSUZZAMAN, Mohammad. Predictive energy management in large-scale grid connected PV-batteries system. **2018 5th International Conference on Renewable Energy: Generation and Applications (ICREGA)**, IEEE, p. 315–318, 2018.

AMARAL, Ricardo Cézar do et al. **Impacto técnico e econômico da energia solar fotovoltaica em prédios públicos através de geração distribuída**. [S.l.: s.n.], 2016.

BARBI, Ivo. **Eletrônica de potência: Projeto de fontes chaveadas**. [S.l.]: Ediçao do autor, 2007.

BARBI, Ivo; PÖTTKER, Fabiana. **Soft Commutation Isolated DC-DC Converters**. [S.l.]: Springer, 2019.

BOSCH. [S.l.: s.n.], 2014. BPT-S 5 Hybrid Battery-storage solar inverter system.

BRASIL, MME. Balanço Energético Nacional. **MME, Empresa de Pesquisa Energética (EPE), Brasília, DF.**, 2018.

BRITO, Sérgio de Salvo. [S.l.]: Tutorial de Energia Solar - Princípios e Aplicações, 2006. Available in: http://www.cresesb.cepel.br/index.php.

BUDH, Dhananjay D; VIRULKAR, Vasudeo B. Smoothing control for BESS based hybrid renewable energy system. **2014 IEEE Students' Conference on Electrical, Electronics and Computer Science**, IEEE, p. 1–4, 2014.

CHEN, Guipeng et al. An optimized modulation method tor full-bridge/push-pull bi-directional DC-DC converter with wide-range ZVS and reduced spike voltage. **IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society**, IEEE, p. 1247–1253, 2014.

CHOI, Eun Sik; LEE, Yun Jae. **Method of controlling charging and discharging of battery energy storage device and the battery energy storage device for the same**. [S.l.]: US Patent n. 9,634,510, Apr. 2017.

CHUNG, Yong Ho; KANG, Byung Kwan; PARK, Ah Ryeon. **Battery energy storage system**. [S.l.]: US Patent n. App. 10/003,199, 2018.

CUBAS, Javier; PINDADO, Santiago; DE MANUEL, Carlos. Explicit expressions for solar panel equivalent circuit parameters based on analytical formulation and the

Lambert W-function. **Energies**, Multidisciplinary Digital Publishing Institute, v. 7, n. 7, p. 4098–4115, 2014.

CUTRIGHT, Richard Hayes et al. **Delivery of multiple grid services with energy storage system**. [S.l.]: US Patent n. 9,991,716, June 2018.

DADIALLA, Kamalprit; HARDAS, RS. Development of prototype model of DC-DC bi-directional converter. **2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)**, IEEE, p. 1620–1623, 2017.

DANESHPAJOOH, Hamid; BAKHSHAI, Alireza; JAIN, Praveen. Modified dual active bridge bidirectional DC-DC converter with optimal efficiency. **2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)**, IEEE, p. 1348–1354, 2012.

E-GEAR. [S.l.]: E-Gear, LLC, 2015. Battery energy storage system.

ELECTRIC, Tabuchi. [S.l.]: Tabuchi Electric Company of America, Limited, 2018. Eco Intelligent Battery System.

ERICKSON, Robert W; MAKSIMOVIC, Dragan. **Fundamentals of power electronics**. [S.l.]: Springer Science & Business Media, 2007.

GIRARD, Antoine; PAPPAS, George J. Approximate hierarchies of linear control systems. **2007 46th IEEE Conference on Decision and Control**, IEEE, p. 3727–3732, 2007.

GUAN, Yajuan et al. Frequency stability of hierarchically controlled hybrid photovoltaic-battery-hydropower microgrids. **IEEE Transactions on Industry Applications**, IEEE, v. 51, n. 6, p. 4729–4742, 2015.

GUERRERO, Josep M; HANG, Lijun; UCEDA ANTOLÍN, Javier. Control of distributed uninterruptible power supply systems. **IEEE Transactions on Industrial Electronics**, IEEE, v. 55, n. 8, p. 2845–2859, 2008.

GUI, Han-Dong et al. An optimized efficiency-based control strategy for islanded paralleled PV micro-converters. **2015 IEEE Applied Power Electronics Conference and Exposition (APEC)**, IEEE, p. 229–234, 2015.

HAN, Byung-Moon. Battery SoC-based DC output voltage control of BESS in stand-alone DC microgrid. **2016 IEEE Region 10 Conference (TENCON)**, IEEE, p. 1445–1449, 2016.

HE, F et al. Control of parallel grid-connected photovoltaic inverters with common DC bus. **2nd IET Renewable Power Generation Conference (RPG 2013)**, p. 1–4, 2013.

HOLVECK, Mark; KOCHEROV, Yevgeniy. **Control systems for microgrid power inverter and methods thereof**. [S.l.]: US Patent n. 9,964,978, May 2018.

INCORPORATED, Texas Instruments. [S.l.]: Bidirectional DC-DC Converter Design Guide, 2015. TI Designs: TIDA-BIDIR-400-12 Bidirectional DC-DC Converter.

INGETEAM. [S.l.]: Ingeteam Ltda, 2016. Solar energy solutions - INGECON SUN STORAGE 1Play.

JAIN, Manu; DANIELE, Matteo; JAIN, Praveen K. A bidirectional DC-DC converter topology for low power application. **IEEE Transactions on power electronics**, IEEE, v. 15, n. 4, p. 595–606, 2000.

JIAN, Chen; YUTIAN, Liu; GUANNAN, Bao. Optimal operating strategy for distribution networks with pv and bess considering flexible energy storage. **2016 IEEE Power and Energy Society General Meeting (PESGM)**, IEEE, p. 1–5, 2016.

KARSTENSEN, Peter Iwer Hoedt; MANEZ, Kevin Tomas; ZHANG, Zhe. Control of a three-port DC-DC converter for grid connected PV-battery applications. **2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG)**, IEEE, p. 1–4, 2018.

KAWAKAMI, Noriko et al. Development of a 500-kW modular multilevel cascade converter for battery energy storage systems. **IEEE Transactions on Industry Applications**, IEEE, v. 50, n. 6, p. 3902–3910, 2014.

KHAWAJA, Yara et al. Optimal cost-based model for sizing grid-connected PV and battery energy system. **2017 IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT)**, IEEE, p. 1–6, 2017.

KUMAR, Shailendra; SINGH, Bhim. Harmonics detection based control of solar-BESS microgrid with grid synchronization. **2017 7th International Conference on Power Systems (ICPS)**, IEEE, p. 684–690, 2017.

KWANG-SEOB KIM, Byung-Ki Kwon; HYUN, Dong-Seok. Development of 500[kWh] Lithium-Ion Battery Energy Storage System with 2[MVA] Power Conditioning System for Utility Interconnection. **International Conference on Renewable Energies and Power Quality**, p. 672–676, 2012.

KYOCERA. [S.l.]: Kyocera Fineceramics GmbH, 2015. Battery Storage System 4.8/7.2.

LIMA, Glauber de Freitas. **A modified flyback converter applied in a capacitive power tranfer for electric vehicle battery charger**. [S.l.: s.n.], 2019.

LUO, F et al. A generalized droop-control scheme for decentralized control of inverter-interfaced microgrids. **2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)**, IEEE, p. 1320–1323, 2013.

MARTINS, Denizar Cruz; BARBI, Ivo. **Eletrônica de Potência: conversores cc-cc básicos não isolados**. [S.l.]: Edição dos Autores, 2006.

MASSIGNAN, Julio AD; MACHADO, Ricardo Q; BOSCO, João. Fluxo de Potência e Fluxo de Potência Ótimo e suas Aplicações em Microredes. **Comunicação Técnica USP - EESC - EEC**, 2016.

MOUSSAOUI, Z et al. An overview of the control scheme for distributed power systems. **Southcon/96 Conference Record**, IEEE, p. 584–591, 1996.

OLALLA, Carlos et al. Architectures and control of submodule integrated DC–DC converters for photovoltaic applications. **IEEE Transactions on Power Electronics**, IEEE, v. 28, n. 6, p. 2980–2997, 2013.

PANASONIC. [S.l.]: Panasonic India Pvt. Ltd, 2017. Storage battery system using Lithium-ion batteries.

PENG, Fang Z et al. A new ZVS bidirectional DC-DC converter for fuel cell and battery application. **IEEE Transactions on power electronics**, IEEE, v. 19, n. 1, p. 54–65, 2004.

PERAÇA, Mauro Tavares et al. **Conversores CC-CC elevadores para aplicação em equipamentos de refrigeração**. [S.l.: s.n.], 2002.

PINHO, Joâo Tavares; GALDINO, Marco Antonio. Manual de engenharia para sistemas fotovoltaicos. **Rio de Janeiro**, v. 1, p. 47–499, 2014.

RODRÍGUEZ, José et al. Predictive current control of a voltage source inverter. **2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)**, IEEE, v. 3, p. 2192–2196, 2004.

SHUVRA, Mahfuz A; CHOWDHURY, Badrul H. Autonomous control of smart inverters in grid connected and islanded mode. **2017 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)**, IEEE, p. 1–5, 2017.

SILVA, Faruk JN. **Estudo de um Conversor Push-Pull Alimentado em Corrente com Grampeamento Ativo–**. [S.l.: s.n.], 1998.

SINGH, Navdeep; GOSWAMI, Arvind. Study of P-V and I-V Characteristics of Solar Cell in MATLAB/Simulink. **International Journal of Pure and Applied Mathematics**, ISSN 1314-3395 online version, v. 118, n. 24, 2018.

SMA. [S.l.]: SMA Solar Technology AG, 2016. Sunny Boy Storage 2.5.

SUAREZ SOLANO, Diego Leandro et al. **Sistema de supervisão e controle de geração solar fotovoltaica para aplicação em microrredes inteligentes**. [S.l.: s.n.], 2015.

SUBRAMANYAM, P Venkata; VYJAYANTHI, C. Integration of PV and battery system to the grid with power quality improvement features using bidirectional AC-DC converter. **2016 International Conference on Electrical Power and Energy Systems (ICEPES)**, IEEE, p. 127–132, 2016.

SUCH, Matthew Clayton; MASADA, Glenn Y. BESS control on an microgrid with significant wind generation. **2017 IEEE Power & Energy Society General Meeting**, IEEE, p. 1–5, 2017.

SUZAN, EREN et al. **DC-bus controller for an inverter**. [S.l.]: US Patent n. 9,948,108, Apr. 2018.

THOMAS, Stephan; STIENEKER, Marco; DE DONCKER, Rik W. Development of a modular high-power converter system for battery energy storage systems. **EPE Journal**, Taylor & Francis, v. 23, n. 1, p. 34–40, 2013.

TOPAN, Paris Ali et al. State of charge (SoC) and state of health (SoH) estimation on lithium polymer battery via kalman filter. **2016 2nd International Conference on Science and Technology-Computer (ICST)**, IEEE, p. 93–96, 2016.

TRINABESS. [S.l.]: Trina Solar Limited, 2018. Solar Battery energy solutions - T Series (N6052T).

UPASANI, Mayuri; PATIL, Sangita. Grid connected solar photovoltaic system with battery storage for energy management. **2018 2nd International Conference on Inventive Systems and Control (ICISC)**, IEEE, p. 438–443, 2018.

WANG, B; ZARGHAMI, M; VAZIRI, M. Energy management and peak-shaving in grid-connected photovoltaic systems integrated with battery storage. **2016 North American Power Symposium (NAPS)**, IEEE, p. 1–5, 2016.

XIA, Tian et al. Modeling and simulation of battery energy storage system (BESS) used in power system. **2015 5th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)**, IEEE, p. 2120–2125, 2015.

XU, Xiaokang et al. Application of new generic models for PV and battery storage in system planning studies. **2017 IEEE Power & Energy Society General Meeting**, IEEE, p. 1–5, 2017.

YU, Ji et al. Bidirectional droop control of interlinking converter in AC/DC hybrid micro-grid. **2016 3rd International Conference on Information Science and Control Engineering (ICISCE)**, IEEE, p. 879–883, 2016.

ZHU, L. A Novel Soft-Commutating Isolated Boost Full-Bridge ZVS-PWM DC-DC Converter for Bidirectional High Power Applications. **IEEE Transactions on Power Electronics**, IEEE, v. 21, n. 2, p. 422–429, 2006.

APPENDIX A – CONVERTER SIZING

Federal University of Santa Catarina
Technological Center
Post-graduation Program in Electrical Engineering

UNIVERSIDADE FEDERAL DE SANTA CATARINA

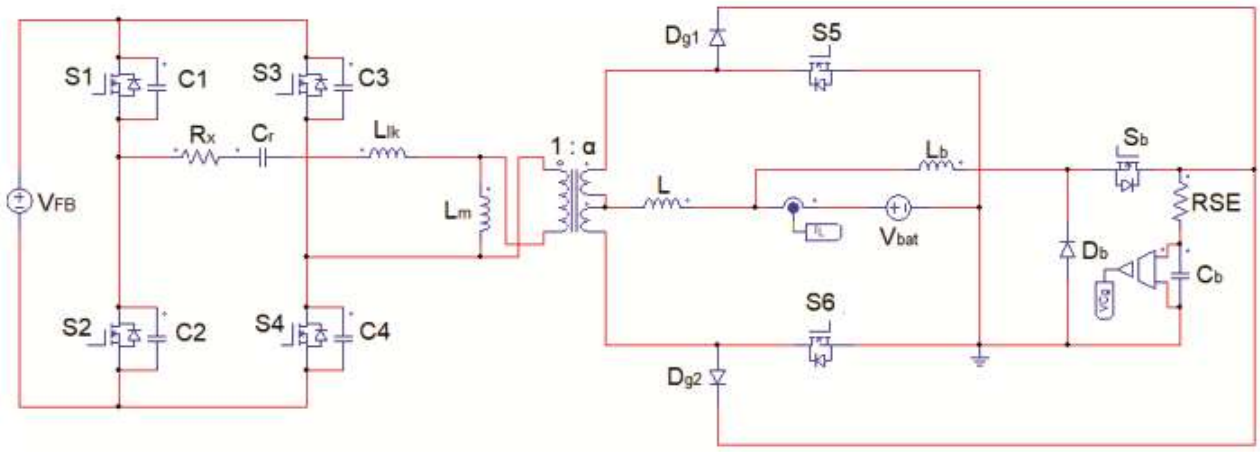
fotovoltaicaufsc

Master's student: Ygor Pereira Marca
Professor Advisor: Prof. Ivo Barbi, PhD.

Isolated Bidirectional DC-DC Converter

This MathCad sheet shows the sizing of the proposed converter and calculates the stresses on all circuit elements, the choice of components, the thermal stresses and the design of the magnetic elements. The project will be elaborated considering the rated power of 2kW

Electrical Circuit:



Specifications:

$P_{out} := 2000W$	Rated Power
$V_{FB} := 400V$	DC bus voltage
$V_{bat} := 48V$	Battery voltage
$f := 40 \cdot 10^{3} Hz$	Switching Frequency
$f_b := 80kHz$	Buck's switching Frequency
$P_{o\_min} := 800W$	Mininum power to achieve ZVS
$V_{Cb} := 220V$	Buck voltage

Full-Bridge ZVS-PWM Stage

$D := 0.7$ Full-Bridge Stage duty cycle operation point

$\omega_s := 2 \cdot \pi \cdot f = 2.513 \times 10^5 \frac{1}{s}$ Angular frequency

$T_s := \frac{1}{f} = 2.5 \times 10^{-5} s$ Switching time

$I_L := \frac{P_{out}}{V_{bat}} = 41.667 A$ Barrety Current

Leakage Inductance

$\Delta D := 0.05$ Loss of Duty Cycle

$D_{ef} := D - \Delta D = 0.65$ Effective Duty Cycle

$V_{op} := V_{FB} \cdot D_{ef} = 260 V$ Voltage across the Full-Bridge side of the transformer

$\alpha := \frac{V_{bat}}{V_{FB} \cdot D_{ef}} = 0.185$ Transformer turns ratio

$V_{os} := \alpha \cdot V_{FB} = 73.846 V$ Voltage across the Push-Pull side of the transformer

$I_{lk} := I_L \cdot \alpha = 7.692 A$ Leakage inductance current

$L_{lk} := \frac{(\Delta D \cdot V_{FB})}{4 \cdot I_{lk} \cdot f} = 16.25 \cdot \mu H$ Leakage inductance

$R_x := \alpha^2 \cdot L_{lk} \cdot f = 0.022 \Omega$ Leakage series resistance

$\Delta D_{conf} := 4 \cdot f \cdot L_{lk} \cdot \frac{\alpha \cdot I_L}{V_{FB}} = 0.05$ Confirmation of duty cycle loss

Series capacitor

$C_{s1} := \frac{4 \cdot (\alpha)^2}{\pi^2 \cdot f^2 \cdot L_{lk}} = 0.531 \cdot \mu F$ First criterion

$\Delta V_C := 0.025$ Capacitor Ripple voltage

$C_{s2} := \frac{I_{lk}}{2 \cdot f \cdot \Delta V_C \cdot V_{FB}} = 9.615 \cdot \mu F$ Second criterion

The second model will be used since it gives a bigger capacitance value

Minimum power operation

$I_{lk\_min} := \frac{P_{o\_min}}{V_{op}} = 3.077\,A$ Minimum leakage current to achieve ZVS

$\Delta D_{min} := \frac{4 \cdot I_{lk\_min} \cdot L_{lk} \cdot f}{V_{FB}} = 0.02$ Duty cycle loss for minimum ZVS operation

$D_{min} := D_{ef} + \Delta D_{min} = 0.67$ Effective duty cycle for minimum ZVS operation

Lagging leg commutaion and dead-time

$C_{min} := \left(\frac{I_{lk\_min}}{V_{FB}}\right)^2 \cdot \frac{L_{lk}}{2} = 4.808 \times 10^{-10}\,F$ Minimum ZVS capacitance

$C_{max} := \left(\frac{I_{lk}}{V_{FB}}\right)^2 \cdot \frac{L_{lk}}{2} = 3.005 \times 10^{-9}\,F$ Maximum ZVS capacitance

$C_{external} := 0.47 \cdot 10^{-9}\,F$ External Capacitor in parallel

$C_{MOSFET} := 0.14\,F\,10^{-9}$ MOSFET capacitance

$C_c := C_{external} + C_{MOSFET} = 6.1 \times 10^{-10}\,F$

$Z := \sqrt{\frac{L_{lk}}{2 \cdot C_c}} = 115.411\,\Omega$ Resonant Impedance

$I_{lk\_min2} := \frac{V_{FB}}{Z} = 3.466\,A$ Minimum leakage current to achieve ZVS for the new commutation capacitor value

$I_{lk} \cdot Z = 887.776\,V$

$I_{lk\_min2} \cdot Z = 400\,V$ To ensure soft commutation

$I_{lk} \cdot Z > V_{FB}$

$\Delta := \operatorname{acos}\left(\frac{V_{FB}}{Z \cdot I_{lk\_min2}}\right) = 0$ The lagging leg soft commutation limit imples that Angle Δ is zero

$t_\Delta := \frac{\Delta}{2 \cdot \pi} \cdot \sqrt{2 \cdot L_{lk} \cdot C_c} = 0$ Commutation time

$t_{d\_min} := \left(\frac{\pi}{2} - \Delta\right) \cdot \left(\sqrt{2 \cdot L_{lk} \cdot C_c}\right) = 221.17\,s \cdot 10^{-9}$ Minimum dead-band

$t_d := 230 \cdot 10^{-9}\,s$ Adopted dead-time

$T_x := \frac{T_s}{2} - t_d = 1.227 \times 10^{-5}\,s$ Switching period of each leg with dead-band

Transformer magnetizing inductance

$\Delta I_{Lm} := \frac{I_{lk}}{10} = 0.769\,A$ Magnetizing current

$\Delta t_{Lm} := D_{ef} \cdot T_x = 7.976 \times 10^{-6}\,s$ Magnetizing inductance time

$L_m := \frac{V_{FB} \cdot \Delta t_{Lm}}{\Delta I_{Lm}} = 4.147 \times 10^{-3}\,H$ Magnetizing inductance

$I_{lk\_ef} := \sqrt{\left(\frac{\Delta I_{Lm}}{2}\right)^2 + I_{lk}^{\,2}} = 7.702\,A$ Effective leakage inductance current

Full-Bridge ZVS-PWM Stage

Current-fed Push-Pull Stage

$I_L = 41.667\,A$ Battery current

$I_{FB} := \frac{P_{out}}{V_{FB}} = 5\,A$ DC bus current

$d := 1 - D = 0.3$ Push-Pull Stage duty cyle

$L_d := 2 \cdot \alpha^2 \cdot L_{lk} = 1.108 \times 10^{-6}\,H$ Leakage inductance referred to the Push-Pull side

Push-Pull Inductor

$I_L = 41.667\,A$ Push-Pull inductor current

$\Delta I_L := 0.1 \cdot I_L = 4.167\,A$ Inductor ripple current

$L := \frac{V_{bat} \cdot d}{2 \cdot f \cdot \Delta I_L} = 43.2 \cdot \mu H$ Push-Pull inductance

Current-fed Push-Pull Stage

Rated Power test

Load evaluation

Current-Fed Push-Pull Stage

$R_{batnom} := \frac{V_{bat}^2}{P_{out}} = 1.152\,\Omega$ Load to evaluate the battery charge

Full-Bridge ZVS-PWM Stage

$R_{FBnom} := \frac{V_{FB}^2}{P_{out}} = 80\,\Omega$ Load to evaluate the battery discharge

Rated Power test

Buck Converter as a clamping voltage circuit

Buck design

$V_{os} = 73.846\,V$ Voltage across the transformer in the push-pull stage

$V_{Cb} > 2 \cdot V_{os}$ Theoretical voltage limit

$V_{Cb} = 220\,V$ Specified buck voltage

$d_{buck} := \frac{V_{bat}}{V_{Cb}} = 0.218$ Buck's duty cycle

$\Delta t_{lk} := \frac{I_{lk} \cdot L_{lk}}{V_{FB}} = 0.313 \cdot \mu s$ Time interval that leakage inductance demagnetize

$\Delta t_g := \frac{I_{lk} \cdot L_{lk}}{2 \cdot V_{FB}} = 156.25\,s \cdot 10^{-9}$ Time interval that clamping diodes conduct

$I_{Dg} := \frac{V_{Cb} \cdot (\Delta t_g)}{2 \cdot L_{lk} \cdot \alpha^2} = 31.033\,A$ Maximum clamping diodes current

$P_b := \int_0^{\Delta t_{lk}} \left[(I_{Dg}) \cdot V_{Cb} \right] dt \cdot f_b = 170.681\,W$ Rated power of Buck converter

$P_{bn} := 200W$ New rated power of Buck converter

$I_b := \frac{P_b}{V_{bat}} = 4.167\,A$ Buck's inductor current

$\Delta I_{Lb} := 0.25 I_b = 1.042\,A$ Buck's inductor ripple current

$$L_b := \frac{V_{bat}\cdot(V_{Cb} - V_{bat})}{V_{Cb}\cdot f_b \cdot \Delta I_{Lb}} = 0.45\cdot 10^{-3}\,H$$ Buck's inductor value

Buck Converter as a clamping voltage circuit

Time intervals

Time intervals' calculation

$$\Delta t_1 := (1 - D)\cdot\frac{T_s}{2} = 3.75 \times 10^{-6}\,s$$

$$\Delta t_2 := t_d = 2.3 \times 10^{-7}\,s$$

$$\Delta t_3 := (D - D_{ef})\cdot\frac{T_s}{2} - \Delta t_2 = 3.95 \times 10^{-7}\,s$$

$$\Delta t_4 := \Delta t_3 = 3.95 \times 10^{-7}\,s$$

$$\Delta t_5 := \frac{L_b\cdot I_b}{2V_{Cb}} = 4.264 \times 10^{-6}\,s$$

$$\Delta t_6 := D_{ef}\cdot\frac{T_s}{2} - \Delta t_5 = 3.861 \times 10^{-6}\,s$$

$$\Delta t_7 := \Delta t_2 = 2.3 \times 10^{-7}\,s$$

Time intervals

Current Stresses

Average currents

$$I_{S12\_avg} := \frac{1}{T_s}\cdot\left(-\int_0^{\Delta t_1} I_{lk}\,dt + \int_0^{\Delta t_5+\Delta t_6} I_{lk}\,dt\right) = 1.346\,A$$ MOSFET 1 and 2 average currents

$$I_{S34\_avg} := \frac{1}{T_s}\cdot\left(\int_0^{\Delta t_1} I_{lk}\,dt + \int_0^{\Delta t_5+\Delta t_6} I_{lk}\,dt\right) = 3.654\,A$$ MOSFET 3 and 4 average currents

$I_{TP\_avg} := I_{lk} = 7.692\,A$ Average current in the Full-Bridge side of the transformer

$I_{TS\_avg} := I_L\cdot(1 - d) = 29.167\,A$ Average current in the Push-Pull side of the transformer

$$I_{S56\_avg} := \frac{I_L}{2} = 20.833\,A$$ MOSFET 5 and 6 average currents

$$I_{Dg\_avg} := \frac{1}{T_s}\cdot\int_0^{\Delta t_3+\Delta t_4}\frac{I_{Dg}}{2}\,dt = 0.49\,A$$ Clampling diode average current

$$I_{Sb\_avg} := \frac{1}{T_s}\cdot\left[\int_0^{d_{buck}\cdot T_s}(I_b)\,dt\right] = 0.909\,A$$ Buck MOSFET average current

$$I_{Db\_avg} := \frac{1}{T_s}\cdot\left[\int_0^{(1-d_{buck})\cdot T_s}(I_b)\,dt\right] = 3.258\,A$$ Buck diode average current

RMS currents

$$I_{S12\_rms} := \sqrt{\frac{1}{T_s}\cdot\left[\int_0^{\Delta t_1}(I_{lk})^2\,dt + \int_0^{\Delta t_5+\Delta t_6}(I_{lk})^2\,dt\right]} = 5.302\,A$$ MOSFET 1 and 2 RMS currents

$$I_{S34\_rms} := \sqrt{\frac{1}{T_s}\cdot\left[\int_0^{\Delta t_1}(I_{lk})^2\,dt + \int_0^{\Delta t_5+\Delta t_6}(I_{lk})^2\,dt\right]} = 5.302\,A$$ MOSFET 3 and 4 RMS currents

$$I_{TP\_rms} := I_{lk} = 7.692\,A$$ RMS current in the Full-Bridge side of the transformer

$$I_{TS\_rms} := I_L\cdot(1-d) = 29.167\,A$$ RMS current in the Push-Pull side of the transformer

$$I_{Lrms} := I_L = 41.667\,A$$ RMS current in the Push-Pull inductor

$$I_{S56\_rms} := I_L\cdot(1-d) = 29.167\,A$$ MOSFET 5 and 6 RMS currents

$$I_{Dg\_rms} := \sqrt{\frac{1}{T_s}\cdot\int_0^{\Delta t_3+\Delta t_4}\left(\frac{I_{Dg}}{2}\right)^2 dt} = 2.758\,A$$ Clampling diode RMS current

$$I_{Sb\_rms} := \sqrt{\frac{1}{T_s}\cdot\left[\int_0^{d_{buck}\,T_s}(I_b)^2\,dt\right]} = 1.946\,A$$ Buck MOSFET RMS current

$$I_{Cb\_rms} := \sqrt{(2I_{Dg\_rms})^2} = 5.517\,A$$ Buck capacitor RMS current

$$I_{Db\_rms} := \sqrt{\frac{1}{T_s}\cdot\left[\int_0^{(1-d_{buck})\cdot T_s}(I_b)^2\,dt\right]} = 3.684\,A$$ Buck diode RMS current

$I_{Lb\_rms} := I_b = 4.167\,A$ Buck inductor RMS current

Peak Current

$I_{S12\_max} := I_{lk} = 7.692\,A$ Maximum current in the MOSFET 1 and 2

$I_{S34\_max} := I_{lk} = 7.692\,A$ Maximum current in the MOSFET 3 and 4

$I_{S56\_max} := I_L = 41.667\,A$ Maximum current in the MOSFET 5 and 6

$I_{Sb\_max} := I_b = 4.167\,A$ Maximum current in the Buck MOSFET

$I_{Db\_max} := I_b = 4.167\,A$ Maximum current in the Buck diode

$I_{Dg} = 31.033\,A$ Maximum current in the clamping diodes

Current Stresses

Voltage stresses

Maximum voltage

$V_S := V_{FB} = 400\,V$ MOSFET S1, S2, S3 and S4 maximum voltage

$V_{TP} := \frac{V_{Cb}}{2 \cdot \alpha} = 595.833\,V$ Maximum voltage across the Full-Bridge side of the transformer

$V_{TS} := \frac{V_{Cb}}{2} = 110\,V$ Maximum voltage across the Push-Pull side of the transformer

$V_{S56} := 2 \cdot \alpha V_{FB} = 147.692\,V$ Theoretical MOSFET S5 and S6 maximum voltage

$V_{S56} := V_{Cb} = 220\,V$ MOSFET S5 and S6 maximum voltage

$V_{Dg} := V_{Cb} = 220\,V$ Clamping diode voltage

$V_{Sb} := V_{Cb} = 220\,V$ Buck MOSFET voltage

$V_{Db} := V_{Cb} = 220\,V$ Buck diode voltage

Voltage stresses

Input Buck Capacitor

Capacitor Design

$\Delta V_{Cb} := 0.01 \cdot V_{Cb} = 2.2\,V$ 10% voltage ripple

$$C_{buck} := \frac{I_{Cb\_rms} \cdot d_{buck}}{f \cdot \Delta V_{Cb}} = 13.677 \cdot \mu F$$ Voltage ripple criterion

Datasheet - https://en.tdk.eu/inf/20/20/db/fc_2009/MKP_B32674_678.pdf

B32674 - Datasheet Specifications:

$RSE := 8.4 \cdot 10^{-3} \cdot \Omega$

$P_{CBuck} := RSE \cdot I_{Cb\_rms}^{2} = 0.256\,W$

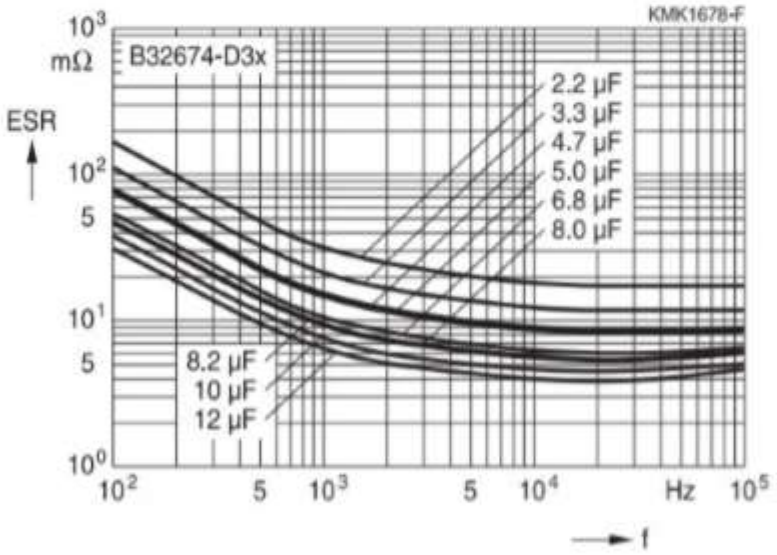
$I_{RMSmax} := 8.5A$

$V_{Cmax} := 300V$

$C_{buck} := 4.7\mu F$

$C_{buck} := 4 \cdot 4.7\mu F = 18.8 \cdot \mu F$ Four capacitors in parallel

300 V DC



$$\Delta V_{C1} := \frac{I_{Cb\_rms} \cdot d_{buck}}{f \cdot C_{buck}} = 1.601\,V$$ New voltage ripple

Input Buck Capacitor

Magnetic Components

Transformer

Especifications

$J_{max} := 450 \frac{A}{cm^2}$ Current density

$\Delta B_{max} := 0.3T$ Maximum magnetic flux density

$T_a := 40$ Ambient temperature

$K_u := 0.7$ Transformer window utilization factor

$K_p := 0.5$ Utilization factor

$P_{out} = 2 \times 10^3 W$ Power processed by the transformer

$f = 4 \times 10^4 \frac{1}{s}$ Switching frequencyo

$\alpha = 0.185$ Transformer turns ratio

$\mu o := 4 \cdot \pi \cdot 10^{-7} \frac{H}{m}$ Magnetic permeability in air

$B := 0.15T$ Magnetic flux density

Core choice

$$AeAw := \frac{P_{out}}{K_u \cdot K_p \cdot J_{max} \cdot \Delta B_{max} \cdot f} = 10.582 \cdot cm^4$$

MAGMATTEC

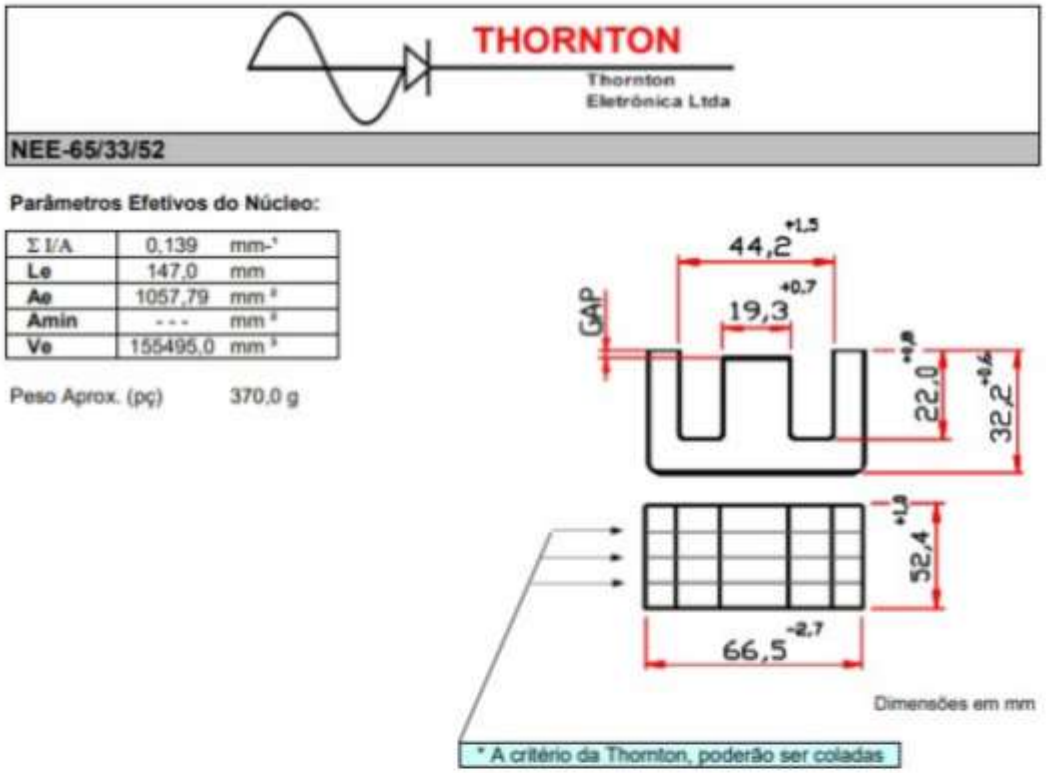
Núcleos de Ferrite

Material – 139 e 140

Tabela 3 – Núcleos E

CÓDIGO PRODUTO	PRODUTO	AL [nH/esp²]	A	B	C	D	E	F	Le [cm]	Ae [cm²]	Aw [cm²]	As [cm²]	V [cm³]	Peso [g]
1.01.0087	MMT140EE2005K	1480	20	13	10	6,3	5,2	5,3	4,3	0,31	0,479	13,11	0,827	3,25
1.01.0580	MMT140EE2006	1490	20	14	10	7,3	5,6	5,6	4,6	0,32	0,512	14	0,88	3,48
1.01.0110	MMT139EE2507	1900	25	18	13	8,7	7,5	7,5	5,75	0,525	0,870	21,68	1,748	7,5
1.01.0088	MMT140EE3007	2080	30	20	15	9,7	7,2	7,3	6,7	0,6	1,193	28,97	2,458	10,5
1.01.0089	MMT140EE4012	4490	41	29	16	11	12	12	7,9	1,53	1,704	48,20	6,164	29,5
1.01.0090	MMT140EE4220	6350	42	30	21	15	12	20	9,7	2,4	2,560	72,83	12,69	54
1.01.0113	MMT139EE5525	7950	55	38	28	19	17	25	12	4,22	3,756	120,07	28,84	129
1.01.0091	MMT140EE6527	8870	67	44	33	22	20	27	14,7	5,32	5,372	164,49	44,5	192

* Outras dimensões estão disponíveis sob consulta.



Selected Core E-65/33/52 from Thorton

$A_e := 10.57cm^2$

$A_w := 11.31cm^2$

$A_e \cdot A_w = 119.547 \cdot cm^4$

$V_{core} := 117.3cm^3$

$l_e := 14.7cm$

Number of turns

$$N_P := \frac{V_{FB}}{4 \cdot A_e \cdot B \cdot f} = 15.768$$

$N_P := \text{ceil}(N_P) = 16$ Number of turns in primary side of transformer

$N_S := \alpha \cdot N_P = 2.954$

$N_S := \text{ceil}(N_S) = 3$ Number of turns in secondary side of transformer

Currents in transformer windings

$$S_{prim} := \frac{I_{TP\_rms}}{J_{max}} = 0.017 \cdot cm^2$$ Primary winding section

$$S_{sec} := \frac{I_{TS\_rms}}{J_{max}} = 0.065 \cdot cm^2$$ Secondary winding section

Pelicular Effect

$$\Delta := \frac{7.5cm}{\sqrt{\frac{f}{Hz}}} = 0.038 \cdot cm$$

$$R_{max} := 2 \cdot \Delta = 0.075 \cdot cm$$

Tabela 3

AWG	Diâmetro Cobre (cm)	Área Cobre (cm^2)	Diâmetro Isolamento (cm)	Área Isolamento (cm^2)	OHMS/CM 20 °C	OHMS/CM 100 °C	AMP. para 450A/cm^2
10	0,259	0,052620	0,273	0,058572	0,000033	0,000044	23,679
11	0,231	0,041729	0,244	0,046738	0,000041	0,000055	18,778
12	0,205	0,033092	0,218	0,037309	0,000052	0,000070	14,892
13	0,183	0,026243	0,195	0,029793	0,000066	0,000080	11,809
14	0,163	0,020811	0,174	0,023800	0,000083	0,000111	9,365
15	0,145	0,016504	0,156	0,019021	0,000104	0,000140	7,427
16	0,129	0,013088	0,139	0,015207	0,000132	0,000176	5,890
17	0,115	0,010379	0,124	0,012164	0,000166	0,000222	4,671
18	0,102	0,008231	0,111	0,009735	0,000209	0,000280	3,704
19	0,091	0,006527	0,100	0,007794	0,000264	0,000353	2,937
20	0,081	0,005176	0,089	0,006244	0,000333	0,000445	2,329
21	0,072	0,004105	0,080	0,005004	0,000420	0,000561	1,847
22	0,064	0,003255	0,071	0,004013	0,000530	0,000708	1,465
23	0,057	0,002582	0,064	0,003221	0,000668	0,000892	1,162
24	0,051	0,002047	0,057	0,002586	0,000842	0,001125	0,921
25	0,045	0,001624	0,051	0,002078	0,001062	0,001419	0,731
26	0,040	0,001287	0,046	0,001671	0,001339	0,001789	0,579
27	0,036	0,001021	0,041	0,001344	0,001689	0,002256	0,459
28	0,032	0,000810	0,037	0,001083	0,002129	0,002845	0,364
29	0,029	0,000642	0,033	0,000872	0,002685	0,003587	0,289
30	0,025	0,000509	0,030	0,000704	0,003386	0,004523	0,229
31	0,023	0,000404	0,027	0,000568	0,004269	0,005704	0,182
32	0,020	0,000320	0,024	0,000459	0,005384	0,007192	0,144
33	0,018	0,000254	0,022	0,000371	0,006789	0,009070	0,114
34	0,016	0,000201	0,020	0,000300	0,008560	0,011437	0,091
35	0,014	0,000160	0,018	0,000243	0,010795	0,014422	0,072
36	0,013	0,000127	0,016	0,000197	0,013612	0,018186	0,057
37	0,011	0,000100	0,014	0,000160	0,017165	0,022932	0,045
38	0,010	0,000080	0,013	0,000130	0,021644	0,028917	0,036
39	0,009	0,000063	0,012	0,000106	0,027293	0,036464	0,028
40	0,008	0,000050	0,010	0,000086	0,034417	0,045981	0,023
41	0,007	0,000040	0,009	0,000070	0,043399	0,057982	0,018

AWG used - 28

$A_{cu\_nu} := 0.000810cm^2$

Number of conductors in parallel

$n_{pri} := ceil\left(\frac{S_{prim}}{A_{cu\_nu}}\right) = 22$ Primary side of transformer

$n_{sec} := ceil\left(\frac{S_{sec}}{A_{cu\_nu}}\right) = 81$ Secondary side of transformer

Since the transformer needs a lot of wires in parallel, some Litz wire that contains 30 AWG 28 wires in parallel will be used.

$A_{cu\_iso} := 0.007083cm^2$ New section of Fio Litz

Window Usage Factor

$A_{pri} := \frac{N_P \cdot A_{cu\_iso} \cdot n_{pri}}{0.7} = 3.562 \cdot cm^2$ Area setted by primary winding

$A_{sec} := \frac{2 \cdot N_S \cdot A_{cu\_iso} \cdot n_{sec}}{0.7} = 4.918 \cdot cm^2$ Area setted by secondary winding

$K_1 := \frac{A_{pri}}{A_w} = 0.315$

$K_2 := \frac{A_{sec}}{A_w} = 0.435$

$K_1 + K_2 = 0.75$ Since the value is smaller than 1, the project is compatible

Core loss

$K_h := 4 \cdot 10^{-5} s$

$K_f := 4 \cdot 10^{-10} s^2$

$P_{coreTrans} := \left(\frac{B}{T}\right)^{2.4} \cdot \left(K_h \cdot f + K_f \cdot f^2\right) \cdot V_{core} \cdot \frac{W}{cm^3} = 2.768\,W$

Copper loss

$\rho := 1.72 \times 10^{-6} \cdot \Omega \cdot cm$ AWG 24 resistivity at 100 ° C

$$P_{cu\_pri} := \frac{N_P \cdot l_e \cdot \rho}{S_{prim}} \cdot I_{TP\_rms}^2 = 1.4\,W$$

$$P_{cu\_sec} := \frac{N_S \cdot l_e \cdot \rho}{S_{sec}} \cdot I_{TS\_rms}^2 = 0.996\,W$$

$$P_{cu} := P_{cu\_pri} + P_{cu\_sec} = 2.396\,W$$

Total losses

$$P_{total\_transformer} := P_{coreTrans} + P_{cu} = 5.164\,W$$

Calculation of temperature rise

$$R_{th} := 23 \cdot \left(\frac{A_e \cdot A_w}{cm^4} \right)^{-0.37} \cdot \frac{C}{W} = 3.918 \frac{A \cdot s^4}{m^2 \cdot kg}$$

$$\Delta T_n := R_{th} \cdot P_{total\_transformer} = 20.231\,C$$

So, 20 ºC degrees of temperature rise is acceptable as the core has a maximum temperature of 100 degrees.

Push-Pull inductor

Specifications

$L = 4.32 \times 10^{-5}\,H$ Inductance of Push-Pull

$\Delta I_L = 4.167\,A$ Inductor ripple current

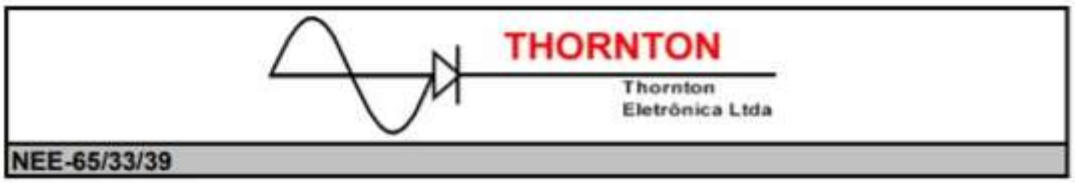
$B_{max} := 0.3T$ Maximum magnetic flux density

$J_{max} := 450 \frac{A}{cm^2}$ Current density

$K_w := 0.7$ Transformer window utilization factor

Core choice

$$AeAw_L := \frac{L \cdot I_L \cdot I_{Lrms}}{B_{max} \cdot J_{max} \cdot K_w} = 7.937 \cdot cm^4$$

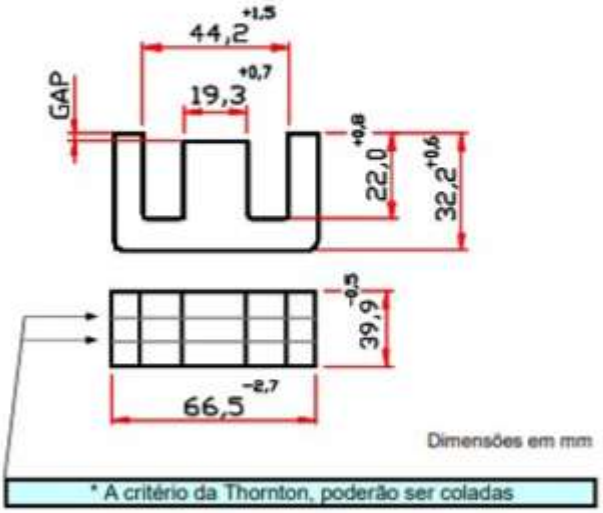


NEE-65/33/39

Parâmetros Efetivos do Núcleo:

Σ l/A	0,18	mm-¹
Le	147,0	mm
Ae	798,0	mm ²
Amin	- - -	mm ²
Ve	117300,0	mm ³

Peso Aprox. (pç) 291,2 g



Selected Core E-65/33/39

$A_e := 7.98cm^2$

$A_W := 11.31cm^2$

$A_e \cdot A_W = 90.254 \cdot cm^4$

$V_{core} := 117.3cm^3$

$l_e := 14.7cm$

Number of turns

$$N_L := ceil\left(\frac{L \cdot I_L}{B_{max} \cdot A_e}\right) = 8$$

$$B_{max} := \frac{L \cdot I_L}{N_L \cdot A_e} = 0.282\,T$$

Air gap calculation

$$\mu_o := 4 \cdot \pi \cdot 10^{-7} \frac{H}{m}$$

$$l_{airgap} := \frac{N_L^{\,2} \cdot \mu_o \cdot A_e}{L} = 0.149 \cdot cm$$

Pelicular effect

$$\Delta := \frac{7.5\text{cm}}{\sqrt{\frac{f}{\text{Hz}}}} = 0.038\cdot\text{cm}$$

$$R_{max} := 2\cdot\Delta = 0.075\cdot\text{cm}$$

AWG used - 28

$$A_{cu\_nu} := 0.000810\text{cm}^2$$

$$A_{cu\_iso} = 7.083 \times 10^{-7}\,\text{m}^2$$ For Litz wire

$$S_{cu} := \frac{I_{Lrms}}{J_{max}} = 0.093\cdot\text{cm}^2$$

Number of conductors in parallel

$$n_{cond} := \text{ceil}\left(\frac{S_{cu}}{A_{cu\_nu}}\right) = 115$$

So, four Litz wire of AWG 28 will be used in parallel

Copper loss

$$\rho_{fio} := \frac{0.000708\cdot\Omega}{\text{cm}}$$

$$l_{fio} := N_L\cdot l_e = 1.176\,\text{m}$$

$$R_{cu} := \frac{\rho_{fio}\cdot l_e\cdot N_L}{n_{cond}} = 7.24 \times 10^{-4}\,\Omega$$

$$P_{cu\_L} := R_{cu}\cdot I_{Lrms}^2 = 1.257\,\text{W}$$

Core loss

$$\Delta B := 0.15\text{T}$$

$$P_{core\_L} := \left(\frac{\Delta B}{\text{T}}\right)^{2.4}\cdot\left(K_h\cdot f + K_f\cdot f^2\right)\cdot V_{core}\cdot\frac{\text{W}}{\text{cm}^3} = 2.768\,\text{W}$$

Calculation of temperature rise

$$Rt_{core\_L} := 23 \cdot \left(A_e \cdot A_w \cdot \frac{1}{cm^4} \right)^{-0.37} \cdot \frac{C}{W} = 4.347 \frac{A \cdot s}{K} \cdot \frac{K}{W}$$

$$\Delta T := \left(P_{cu\_L} + P_{core\_L} \right) \cdot Rt_{core\_L} = 17.497\,C$$

So, 17.5 ºC degrees of temperature rise is acceptable as the core has a maximum temperature of 100 degrees.

Window Usage Factor

$$A_{w\_min} := \frac{N_L \cdot A_{cu\_iso} \cdot n_{cond}}{K_w} = 9.309 \cdot cm^2$$

$$Exec := \frac{A_{w\_min}}{A_w} = 0.823$$

Total losses

$$P_{InductorPushPull} := P_{cu\_L} + P_{core\_L} = 4.025\,W$$

Buck inductor

Specifications

$L_b = 4.503 \times 10^{-4}\,H$ Buck inductance

$I_{Lb\_rms} = 4.167\,A$ RMS current

$\Delta I_{Lb} = 1.042\,A$ Inductor ripple current

$B_{max} := 0.3T$ Maximum magnetic flux density

$J_{max} := 450 \frac{A}{cm^2}$ Current density

$K_w := 0.7$ Transformer window utilization factor

Core choice

$$AeAw_L := \frac{L_b \cdot I_b \cdot I_{Lb\_rms}}{B_{max} \cdot J_{max} \cdot K_w} = 0.827 \cdot cm^4$$

Selected Core E-55/25 from Magmattec

$A_e := 4.22cm^2$

$A_w := 3.756cm^2$

$A_e \cdot A_W = 15.85 \cdot cm^4$

$V_{core} := 28.84cm^3$

$l_e := 12cm$

Number of turns

$$N_{Lbuck} := ceil\left(\frac{L_b \cdot I_b}{B_{max} \cdot A_e}\right) = 15$$

$$B_{max} := \frac{L_b \cdot I_b}{N_{Lbuck} \cdot A_e} = 0.296\,T$$

Air gap calculation

$$\mu_o := 4 \cdot \pi \cdot 10^{-7} \frac{H}{m}$$

$$l_{airgap} := \frac{N_{Lbuck}^2 \cdot \mu_o \cdot A_e}{L} = 0.276 \cdot cm$$

Pelicular Effect

$$\Delta := \frac{7.5cm}{\sqrt{\frac{f_b}{Hz}}} = 0.027 \cdot cm$$

$$R_{max} := 2 \cdot \Delta = 0.053 \cdot cm$$

AWG used - 24

$A_{cu\_nu} := 0.002047cm^2$

$$S_{cobre} := \frac{I_{Lb\_rms}}{J_{max}} = 9.259 \times 10^{-3} \cdot cm^2$$

$$n_{cond} := ceil\left(\frac{S_{cobre}}{A_{cu\_nu}}\right) = 5$$

$S_{fioiso} := 0.002586cm^2$

$A_{cu\_iso} := 0.031cm^2$ Litz wire AWG 24 with 10 wires in parallel

Copper loss

$$\rho_{fio} := \frac{0.000708 \cdot \Omega}{cm}$$

$$l_e = 12 \cdot cm$$

$$l_{fio} := N_{Lbuck} \cdot l_e = 1.8\,m$$

$$R_{cu} := \frac{\rho_{fio} \cdot l_{fio}}{n_{cond}} = 0.025\,\Omega$$

$$P_{cu\_Lb} := R_{cu} \cdot I_{Lb\_rms}^{2} = 0.443\,W$$

Core loss

$$\Delta B := \frac{L_b \cdot I_b}{N_{Lbuck} \cdot A_e} = 0.296\,T$$

$$P_{core\_Lb} := \left(\frac{\Delta B}{T}\right)^{2.4} \cdot \left(K_h \cdot f + K_f \cdot f^2\right) \cdot V_{core} \cdot \frac{W}{cm^3} = 3.49\,W$$

Calculation of temperature rise

$$Rt_{core\_Lb} := 23 \cdot \left(A_e \cdot A_w \cdot \frac{1}{cm^4}\right)^{-0.37} \cdot \frac{K}{W} = 8.274 \cdot \frac{K}{W}$$

$$\Delta T := \left(P_{cu\_Lb} + P_{core\_Lb}\right) \cdot Rt_{core\_Lb} = 32.538\,K$$

Window Usage Factor

$$A_{w\_min} := \frac{N_{Lbuck} \cdot A_{cu\_iso} \cdot n_{cond}}{K_w} = 3.321 \cdot cm^2$$

$$Exec := \frac{A_{w\_min}}{A_w} = 0.884$$

Total losses

$$P_{InductorBuck} := P_{cu\_Lb} + P_{core\_Lb} = 3.933\,W$$

External inductor

Specifications

$L_{lk} = 1.625 \times 10^{-5}\,H$ Total leakage inductance

Since the transformer presented a leakage indutance of 5 µH, the new value of the external leakage inductance can be recalculated as follows:

$L_{lk} := 1.625 \times 10^{-5}\,H - 5\mu H$ External inductance

$B_{max} := 0.3T$ Maximum magnetic flux density

$J_{max} := 450\,\frac{A}{cm^2}$ Current density

$K_w := 0.7$ Transformer window utilization factor

Core choice

$$AeAw_{Lk} := \frac{L_{lk} \cdot I_{TP\_rms} \cdot I_{TP\_avg}}{B_{max} \cdot J_{max} \cdot K_w} = 0.07 \cdot cm^4$$

Selected Core E-42/20 from Magmattec

$A_e := 2.4cm^2$

$A_w := 2.56cm^2$

$A_e \cdot A_w = 6.144 \cdot cm^4$

$V_{core} := 12.69cm^3$

$l_e := 9.7cm$

Number of conductors in parallel

$$N_{Ldisp} := ceil\left(\frac{L_{lk} \cdot I_{lk}}{B_{max} \cdot A_e}\right) = 2$$

$$B_{max} := \frac{L_{lk} \cdot I_{lk}}{N_{Ldisp} \cdot A_e} = 0.18\,T$$

Air gap calculation

$\mu_o := 4 \cdot \pi \cdot 10^{-7}\,\frac{H}{m}$

$$l_{airgap} := \frac{N_{Ldisp}^{\ 2} \cdot \mu_o \cdot A_e}{L} = 0.028 \cdot mm$$

Pelicular effect

$$\Delta := \frac{7.5\,cm}{\sqrt{\frac{f}{Hz}}} = 0.038\cdot cm$$

$$R_{max} := 2\cdot\Delta = 0.075\cdot cm$$

AWG used - 24

$$A_{cu\_nu} := 0.002047\,cm^2$$

$$S_{cobre} := \frac{I_{TP\_rms}}{J_{max}} = 0.017\cdot cm^2$$

$$n_{cond} := ceil\left(\frac{S_{cobre}}{A_{cu\_nu}}\right) = 9$$

$A_{cu\_iso} = 3.1 \times 10^{-6}\,m^2$ Litz wire AWG 24 with 10 wires in parallel

Copper loss

$$\rho_{fio} := \frac{0.000708\cdot\Omega}{cm}$$

$l_e = 9.7\cdot cm$

$$l_{fio} := N_{Ldisp}\cdot l_e = 0.194\,m$$

$$R_{cu} := \frac{\rho_{fio}\cdot l_{fio}}{n_{cond}} = 1.526\times 10^{-3}\,\Omega$$

$$P_{cu\_Lr} := R_{cu}\cdot I_{TP\_rms}^2 = 0.09\,W$$

Core loss

$$\Delta B := \frac{L_{lk}\cdot I_{TP\_rms}}{N_{Ldisp}\cdot A_e} = 0.18\,T$$

$$P_{core\_Lr} := \left(\frac{\Delta B}{T}\right)^{2.4}\cdot\left(K_h\cdot f + K_f\cdot f^2\right)\cdot V_{core}\cdot\frac{W}{cm^3} = 0.466\,W$$

Calculation of temperature rise

$$Rt_{core\_Lr} := 23 \cdot \left(A_e \cdot A_w \cdot \frac{1}{cm^4} \right)^{-0.37} \cdot \frac{C}{W} = 11.749 \frac{A \cdot s}{K} \cdot \frac{K}{W}$$

$$\Delta T := \left(P_{cu\_Lr} + P_{core\_Lr} \right) \cdot Rt_{core\_Lr} = 6.532\,C$$

Window Usage Factor

$$A_{w\_min} := \frac{N_{Ldisp} \cdot A_{cu\_iso} \cdot n_{cond}}{K_w} = 0.797 \cdot cm^2$$

$$Exec := \frac{A_{w\_min}}{A_w} = 0.311$$

Total losses

$$P_{InductorDisp} := P_{cu\_Lr} + P_{core\_Lr} = 0.556\,W$$

Magnetic Components

Signal Conditioning

Signal Conditioning

Sallen-key Filter

Capacitors (Defines the filter bandwidth):

$C_1 := 10nF$

$C_2 := 10nF$

Resistors (Set filter stabilization speed):

$R_1 := 1k\Omega \quad R_2 := 1k\Omega$

Filter cutoff frequency:

$$f_c := \frac{1}{2\pi\sqrt{R_1 \cdot R_1 \cdot C_1 \cdot C_2}} = 15.915 \cdot kHz$$

$$Q := \frac{\sqrt{R_1 \cdot R_1 \cdot C_1 \cdot C_2}}{C_1 \cdot \left(R_1 + R_2 \right)} = 0.5$$

$j := \sqrt{-1}$

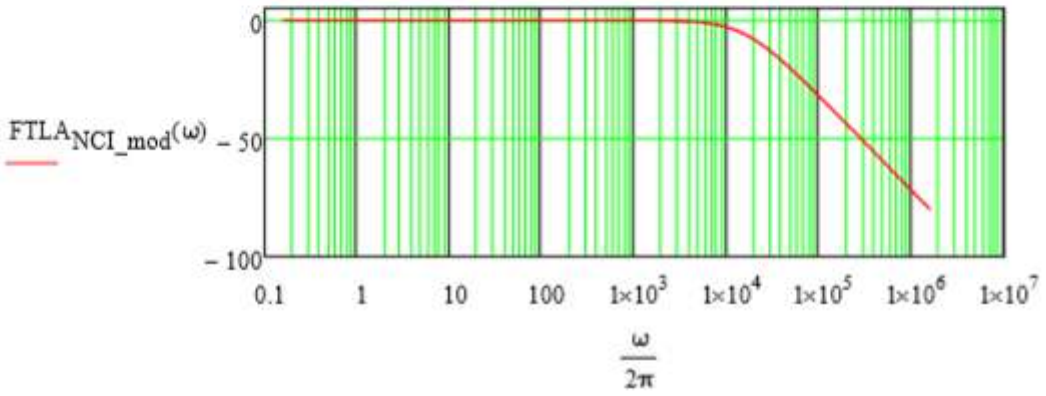
$$G(\omega) := \frac{(2\cdot\pi\cdot f_c)^2}{(j\cdot\omega)^2 + j\cdot\omega\cdot\frac{(2\cdot\pi\cdot f_c)}{Q} + (2\cdot\pi\cdot f_c)^2}$$

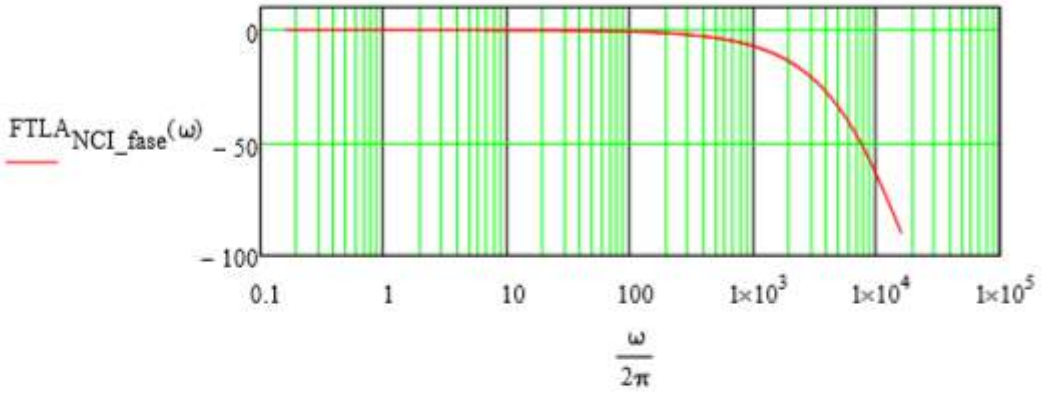
Uncompensated open loop transfer function:

$$FTLA_{NCI}(\omega) := G(\omega)$$

$$FTLA_{NCI\_mod}(\omega) := 20\cdot\log(|FTLA_{NCI}(\omega)|)$$

$$FTLA_{NCI\_fase}(\omega) := \frac{180}{\pi}\arg(FTLA_{NCI}(\omega))$$





Push Pull Inductor Current buffer

$$I_{nominal} := 42A$$

$$I_{sensor1} := \frac{I_{nominal}}{2100} = 0.02\,A$$

$$R_{buffer1} := 100\Omega$$

$$V_{out\_cond1} := I_{sensor1}\cdot R_{buffer1} = 2\,V$$

Buck input voltage buffer

$V_{Cb} = 220\,V$

$R_{serie\_buck} := 6 \cdot 5.6 \cdot 10^{3}\,\Omega$

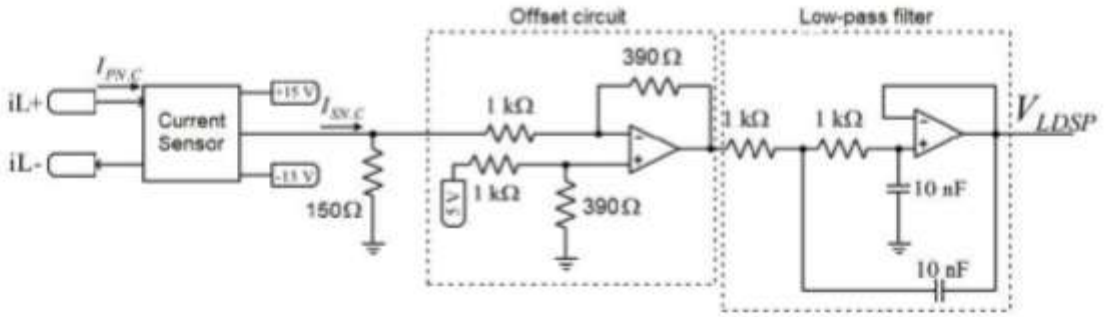
$I_{SensorBuckIn} := \frac{V_{Cb}}{R_{serie\_buck}} = 6.548 \times 10^{-3}\,A$

$I_{SensorBuckOut} := 2.5 \cdot I_{SensorBuckIn} = 0.016\,A$

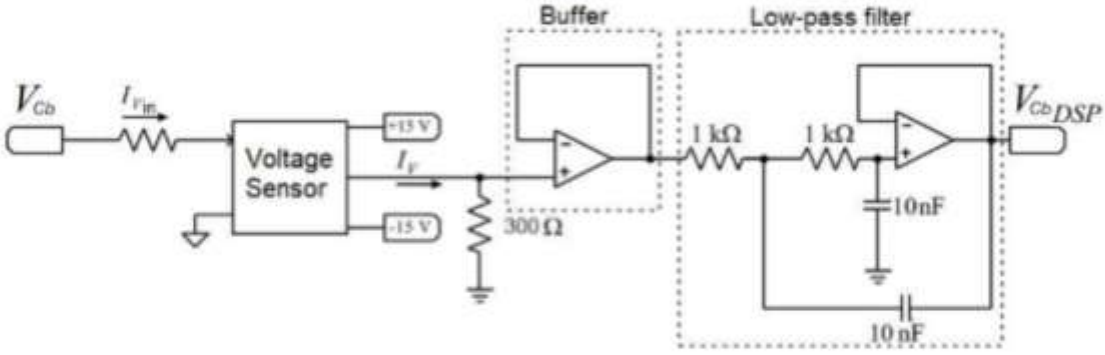
$R_{buffer3} := 180\,\Omega$

$V_{out\_cond3} := I_{SensorBuckOut} \cdot R_{buffer3} = 2.946\,V$

Push-Pull Inductor current signal conditioning



Buck input capacitor voltage signal conditioning



The signal conditioning gain must be applied in the DSP program in order to adjust the references

Signal Conditioning

Components list

Components choice

MOSFET

S1, S2, S3 and S4 - ZVS-PWM Full-Bridge Stage

Part Number:FCP13N60NFS-ND Manufacturer FCP13N60N

Datasheet:https://www.onsemi.com/pub/Collateral/FCPF13N60NT-D.pdf

Specifications

$V_{gs} := -30 + 30V$

$V_S := 600V$

$E := 400V$

$t_f := 9.8 \times 10^{-9} s$

$t_r := 10.6 \cdot 10^{-9} s$

This time values depends on the gate drive circuit used. A high gate resistnce or bead filter increase this time.

$T_s = 2.5 \times 10^{-5} s$

$T_1 := D \cdot T_s = 1.75 \times 10^{-5} s$

$R_{ds} := 0.258\Omega$

$C_{oss} := 145 \times 10^{-12} F$

$C_{rss} := 5 \times 10^{-12} F$

$$Ploss\_S1 := \frac{T_1 \cdot R_{ds} \cdot I_{S12\_rms}^{2}}{T_s} = 5.076\,W$$

Since there is soft switching, switching loss will not be considered

$$Ploss\_S3 := \frac{T_1 \cdot R_{ds} \cdot I_{S34\_rms}^{2}}{T_s} = 5.076\,W$$

$C_{ds} := C_{oss} - C_{rss} = 0.14\,F \cdot 10^{-9}$

MOSFET intrinsic capacitnce

Sb - Buck Converter

For the buck converter, it was used the same MOSFET of the Full-Bridge stage, since buying a larger number of MOSFET makes it cheaper.

Part Number:FCP13N60NFS-ND Manufacturer FCP13N60N

Datasheet:https://www.onsemi.com/pub/Collateral/FCPF13N60NT-D.pdf

Specifications

$V_{gs} := -30 + 30V$

$V_S := 600V$

$E := 400V$

$t_f := 9.8 \times 10^{-9}\,s$

$t_r := 10.6 \cdot 10^{-9}\,s$

$T_s = 2.5 \times 10^{-5}\,s$

$T_1 := D \cdot T_s = 1.75 \times 10^{-5}\,s$

$R_{ds} := 0.258\Omega$

$C_{oss} := 145 \times 10^{-12}\,F$

$C_{rss} := 5 \times 10^{-12}\,F$

$$Ploss_{Switching\_Sbuck} := \frac{I_{Sb\_max} \cdot E \cdot (t_r + t_f) \cdot f}{2} = 0.68\,W$$

$$Ploss\_conduction\_Sbuck := \frac{T_1 \cdot R_{ds} \cdot I_{Sb\_rms}^{2}}{T_s} = 0.684\,W$$

$$Ploss\_Sbuck := Ploss_{Switching\_Sbuck} + Ploss\_conduction\_Sbuck = 1.364\,W$$

$C_{ds} := C_{oss} - C_{rss} = 0.14\,F \cdot 10^{-9}$

S5 and S6 - Curren-Fed Push-Pull Stage

Part Number: Digikey IXFP72N30X3-ND Manufacturer IXFP72N30X3

Datasheet:https://www.littelfuse.com/~/media/electronics/datasheets/discrete_mosfets/littelfuse_discrete_mosfets_n-channel_ultra_junction_ixf_72n30x3_datasheet.pdf.pdf

$V_{gs} := -20 + 20V$

$V_S := 300V$

$E := 220V$

$t_f := 11 \times 10^{-9}\,s$

$t_r := 25 \cdot 10^{-9}\,s$

$T_s = 2.5 \times 10^{-5}\,s$

$T_1 := d \cdot T_s = 7.5 \times 10^{-6}\,s$

$R_{ds} := 19 \cdot 10^{-3}\Omega$

$C_{oss} := 800 \times 10^{-12}\,F$

$C_{rss} := 2 \times 10^{-12}\,F$

$$Ploss_{switching\_S5} := \frac{I_{S56\_max} \cdot E \cdot (t_r + t_f) \cdot f}{2} = 6.6\,W$$

$$Ploss\_conduction\_S5 := \frac{T_1 \cdot R_{ds} \cdot I_{S56\_rms}^{2}}{T_s} = 4.849\,W$$

$$Ploss\_S5 := Ploss_{switching\_S5} + Ploss\_conduction\_S5 = 11.449\,W$$

$$C_{ds} := C_{oss} - C_{rss} = 0.798\,F \cdot 10^{-9}$$

Diodes

Dg1 and Dg2 - Clamping diodes

Part Number: 497-7612-5-ND Manufacturer STTH8R04DI

Datasheet:
https://www.st.com/content/ccc/resource/technical/document/datasheet/37/69/21/51/3e/64/44/8a/CD00156055.pdf/files/CD00156055.pdf/jcr:content/translations/en.CD00156055.pdf

$$\Delta V_F := 2V - 1.8V = 0.2\,V$$

$$\Delta I_F := 60A - 45A = 15\,A$$

$$R_F := \frac{\Delta V_F}{\Delta I_F} = 0.013\,\Omega$$

$$V_{TO} := 0.64V$$

$$Q_C := 29.3 \cdot 10^{-9}$$

$$d_{if\_dt} := \frac{100}{10^{-6}}$$

$$t_{rr\_Dg1} := s \cdot \sqrt{\frac{Q_C \cdot 3}{d_{if\_dt}}} = 2.965 \times 10^{-8}\,s$$

$$P_{Dg1\_cond} := V_{TO} \cdot I_{Dg\_avg} + R_F \cdot I_{Dg\_rms}^{2} = 0.351\,W$$

$$P_{Dg1\_swit} := \frac{1}{2} \cdot V_{Dg} \cdot I_{Dg\_rms} \cdot f \cdot t_{rr\_Dg1} = 0.314\,W$$

$$P_{total\_D1} := P_{Dg1\_cond} + P_{Dg1\_swit} = 0.665\,W$$

Dbuck - Buck converter diode

$$I_F := 15A$$

Part Number: DPG15I400PM-ND Fabricante DPG15I400PM

Datasheet: http://ixapps.ixys.com/DataSheet/DPG15I400PM.pdf

$\Delta V_F := 2V - 1.5V = 0.5\,V$

$\Delta I_F := 60A - 20A = 40\,A$

$R_F := \frac{\Delta V_F}{\Delta I_F} = 0.013\,\Omega$

$V_{TO} := 0.7V$

$Q_C := 80 \cdot 10^{-9}$

$d_{if\_dt} := \frac{200}{10^{-6}}$

$t_{rr\_Db1} := s \cdot \sqrt{\frac{Q_C \cdot 3}{d_{if\_dt}}} = 3.464 \times 10^{-8}\,s$

$P_{Db\_cond} := V_{TO} \cdot I_{Db\_avg} + R_F \cdot I_{Db\_rms}^{2} = 2.45\,W$

$P_{Db\_swit} := \frac{1}{2} \cdot V_{Db} \cdot I_{Db\_rms} \cdot f \cdot t_{rr\_Db1} = 0.562\,W$

$P_{total\_Db} := P_{Db\_cond} + P_{Db\_swit} = 3.012\,W$

Soft switching Capacitor

$I_{Csoft\_ef\_sim} := 0.1A$

$C_{Csoft\_ex} := 0.47 \cdot 10^{-9} F$

$C_c = 6.1 \times 10^{-10} F$ Total soft switching capacitance

$I_{RMSCmax} := 0.6A$

$V_{Cmax} := 630V$

Part Number: Digikey BFC237510911-ND Fabricante DPP6 D1K-F

Full-Bridge leg capacitor

Datasheet: http://www.cde.com/resources/catalogs/DPP.pdf

Furthermore, two polypropylene capacitors with 2.2 µF found in the laboratory were conected in palallel with each Full-Bridge leg to attenuate the inductance reaction on switching. Note that this capacitor must support at least 400 Volts.

▲ Components list

▼ Converter Efficiency

Power loss

$P_{MOSFET} := 2 \cdot (Ploss\_S1 + Ploss\_S3 + Ploss\_S5) + Ploss\_Sbuck = 44.566\,W$

$P_{Diodes} := 2 \cdot P_{total\_D1} + P_{total\_Db} + P_{CBuck} = 4.537\,W$

$P_{TotalInductors} := P_{InductorPushPull} + P_{InductorBuck} + P_{InductorDisp} = 8.513\,W$

$P_{total\_transformer} = 5.164\,W$

$P_{Total\_Actives\_Elements} := P_{MOSFET} + P_{Diodes} = 49.103\,W$

$P_{Total} := P_{Total\_Actives\_Elements} + P_{TotalInductors} + P_{total\_transformer} = 62.78\,W$

$$\eta := \frac{(P_{out} - P_{Total}) \cdot 100}{P_{out}} = 96.861$$

Converter Efficiency

Thermal Stresses

Thermal Stresses Calculation

The thermal calculation of the components is done to verify the necessity of a sink, to prevent the switches and diodes from operate at high temperatures. This calculation is necessary to avoid damage in the components and increase the MTBF (Mean time between failure) of the converter. For this project, only one heatsink will be designed to connect all semiconductors. At the end, the junction temperature of each component will be checked.

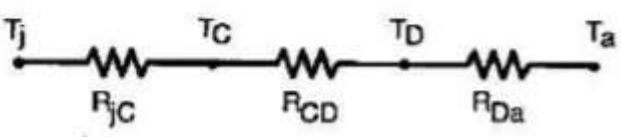
$T_a := 60\,\Delta°C$ Room temperature

$R_{cd\_mica} := 0.2\,\frac{\Delta°C}{W}$ Mica thermal resistance

$P_{Total\_Actives\_Elements} = 49.103\,W$

$$\%P_{TotalAtivos} := \frac{P_{Total\_Actives\_Elements}}{P_{out}} = 2.455 \cdot \%$$

Temperature dissipation resembles an electrical circuit and can be simplified as follows:



Which:

Tj is the junction temperature;
Tc is the encapsulation temperature;

Td is the heat sink temperature, considered 100 ºC;
Rjc is the thermal resistance of the junction-capsule;
Rcd is the thermal resistance between the semiconductor and heat sink;
Rda is the ambient heat sink resistance;
Ta is the room temperature, considered 50 ºC.

$T_J := 150 \cdot \Delta°C$ Maximum junction temperature — This value actually changes for each MOSFET and diode

$T_d := 100 \Delta°C$ Sink temperature projected

$\Delta T_{d\_a} := T_d - T_a = 40 \cdot \Delta°C$

So, the temperature rising in the components are calculated below:

MOSFET 1 and 2

$R_{jc\_12} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{d\_12} := T_J - \left(R_{jc\_12} + R_{cd\_mica}\right) Ploss\_S1 = 143.553 \cdot \Delta°C$ Sink Temperature

MOSFET 3 and 4

$R_{jc\_34} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{d\_34} := T_J - \left(R_{jc\_34} + R_{cd\_mica}\right) Ploss\_S3 = 143.553 \cdot \Delta°C$ Sink Temperature

MOSFET 5 and 6

$R_{jc\_56} := 0.32 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{d\_56} := T_J - \left(R_{jc\_56} + R_{cd\_mica}\right) Ploss\_S5 = 144.047 \cdot \Delta°C$ Sink Temperature

MOSFET Buck

$R_{jc\_buck} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{d\_buck} := T_J - \left(R_{jc\_buck} + R_{cd\_mica}\right) Ploss\_Sbuck = 148.268 \cdot \Delta°C$ Sink Temperature

Clamping diode

$R_{jc\_Dgramp} := 5.5 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{d\_Dgramp} := T_J - \left(R_{jc\_Dgramp} + R_{cd\_mica}\right) \cdot P_{total\_D1} = 146.209 \cdot \Delta°C$ Sink Temperature

Buck diode

$R_{jc\_Dbuck} := 4.2\,\frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_Dbuck} := T_J - \left(R_{jc\_Dbuck} + R_{cd\_mica}\right)\cdot P_{total\_Db} = 136.749\cdot\Delta°C$ Sink Temperature

Therefore, a heatsink will be projected to keep the semiconductors temperature below 100 ºC.

Heatsink sizing

$$R_{ja\_total} := \frac{T_J - T_a}{P_{Total\_Actives\_Elements}} = 1.833\cdot\frac{\Delta°C}{W}$$

If the total resistance value is smaller than any component Rja value found in the manufacturer datasheet, than the semiconductor need a heatsink to operante under the designed juntcion temperature.

$$R_{ja\_S12} := \frac{T_J - T_a}{Ploss\_S1} = 17.73\cdot\frac{\Delta°C}{W}$$

Therefore, the MOSFET FCP13N60NFS-ND used in the ZVS-PWM Full-Bridge stage and buck converter has the following junction to ambient thermal resistance:

$R_{ja\_S12} := 62.5\,\frac{\Delta°C}{W}$

So, a heatsink will be calculated in order to keep the temperature rising below the maximum temperature found in the manufacturer datasheet.

$CC := 0.62$ Length correction to 300mm

$FS := 1.2$ Safety factor

$FC := 1.257$ Correction factor that depends on the temperature difference of the case to the environment. At 60ºC, the factor is 1.257

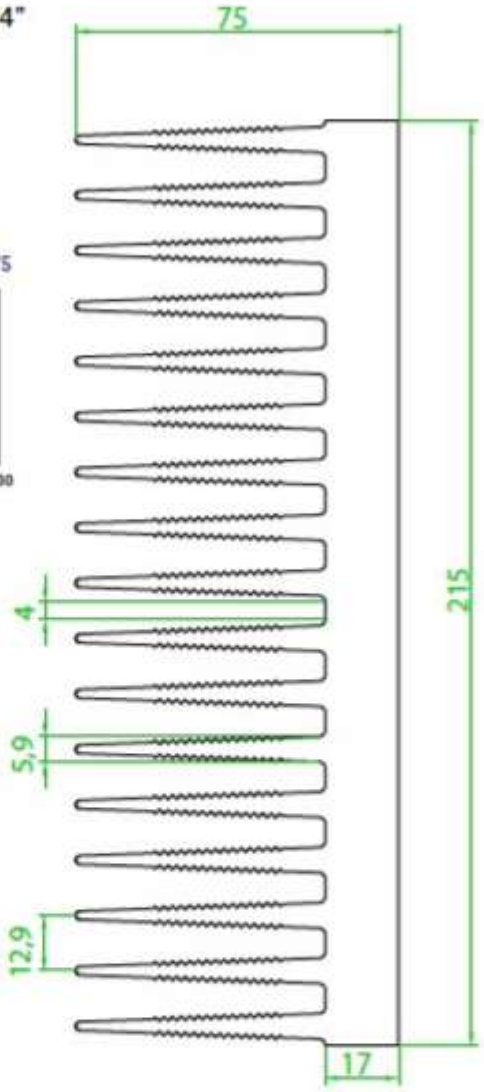
$$R_{da} := FC\cdot\frac{T_d - T_a}{FS\,P_{Total}} = 0.667\cdot\frac{\Delta°C}{W}$$ Maximum sink resistance

$R_{da\_sink} := 0.57\,\frac{\Delta°C}{W}$ Sinck resistance used

Código: HS 21575

106

Perímetro: 2965 mm
Resistência Térmica: 0,56 °C / W / 4"
Peso Linear: 21 kg/m
Capacidade Térmica: 921 J/kg K



$R_{da\_new} := R_{da\_sink} \cdot CC = 0.353 \cdot \frac{\Delta°C}{W}$ Thermal resistance for model HS 26574 considering 265mm x 300mm

The resulting Rda value is smaller than the maximum Rda, so it is expected that this heatsink will be able to dissipate all the power generated by the switches.

$T_{d\_new} := T_a + R_{da\_new} \cdot P_{Total} = 82.186 \cdot \Delta°C$ Sink temperature based on sink adopted.

MOSFET 1 and 2

$R_{jc\_12} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_12} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_12}\right) \cdot Ploss\_S1 = 88.633 \cdot \Delta°C$ Junction temperature

MOSFET 3 and 4

$R_{jc\_34} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_34} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_34}\right) \cdot Ploss\_S3 = 88.633 \cdot \Delta°C$ Junction temperature

MOSFET 5 and 6

$R_{jc\_56} := 0.32 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_56} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_56}\right) \cdot Ploss\_S5 = 88.14 \cdot \Delta°C$ Junction temperature

MOSFET Buck

$R_{jc\_buck} := 1.07 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_buck} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_buck}\right) \cdot Ploss\_Sbuck = 83.919 \cdot \Delta°C$

Clamping diode

$R_{jc\_Dgramp} := 5.5 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_Dgramp} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_Dgramp}\right) \cdot P_{total\_D1} = 85.978 \cdot \Delta°C$

Buck diode

$R_{jc\_Dbuck} := 4.2 \frac{\Delta°C}{W}$ Junction-capsule resistance

$T_{j\_Dbuck} := T_{d\_new} + \left(R_{cd\_mica} + R_{jc\_Dbuck}\right) \cdot P_{total\_Db} = 95.437\,\Delta°C$

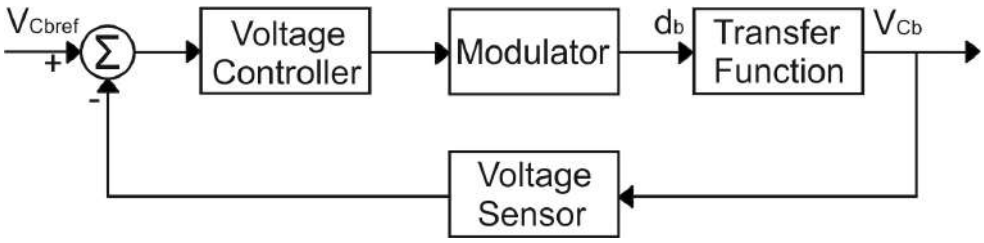
Since the temperature rising is below the components' datasheet constraints, the converter MTBF should increase.

Thermal Stresses

APPENDIX B – CLAMPING CAPACITOR VOLTAGE CONTROL

The block diagram presented in figure 136 illustrates a closed-loop system that compares a reference voltage with the voltage measured across the clamping capacitor. Also, the block diagram presents a PI controller to compensate the system, the modulator, the converter transfer function and the voltage sensor gain.

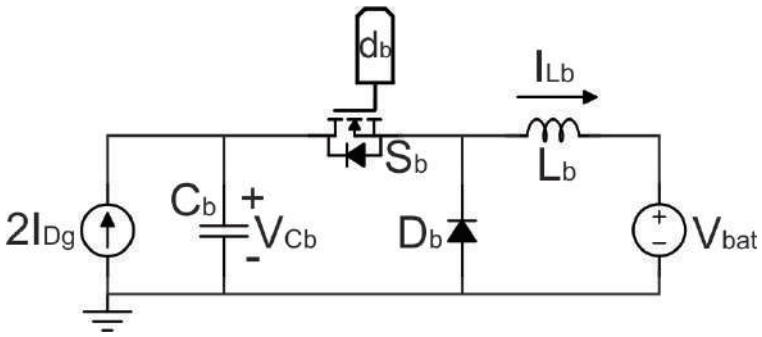
Figure 136 – Closed-loop control system of the clamping capacitor voltage



Source: Own elaboration

Thus, the clamping converter shown in figure 137 has the same characteristics of a buck converter, but its input voltage must be controlled instead of the output.

Figure 137 – Equivalent clamping converter



Source: Own elaboration

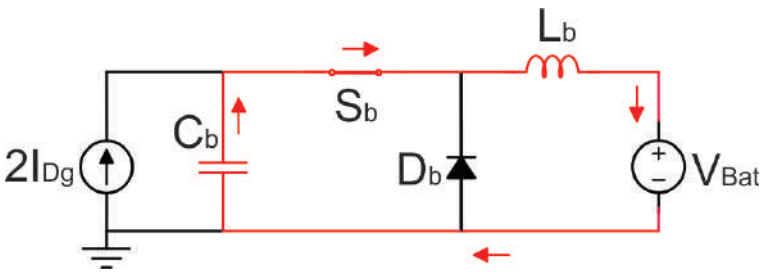
Furthermore, as the input voltage must be controlled in order to maintain a regulated voltage across the push-pull switches (S_5 and S_6), a transfer function of the clamping capacitor voltage (V_{Cb}) in relation to the converter's duty cycle (d_b) must be established.

B.0.1 Circuit Operation

First of all, the clamping converter presents two topological states, one that occurs when the switch S_b is turned on and other when it is turned off, as described below. Also, because of its simplicity, the gate signal will not be presented in this chapter.

Time interval Δt_1 - In the first topological state, the switch S_b is gated on and the diode D_b is reverse polarized. So, the energy stored in the clamping capacitor C_b is transferred to the battery. The first topological state is presented in figure 138.

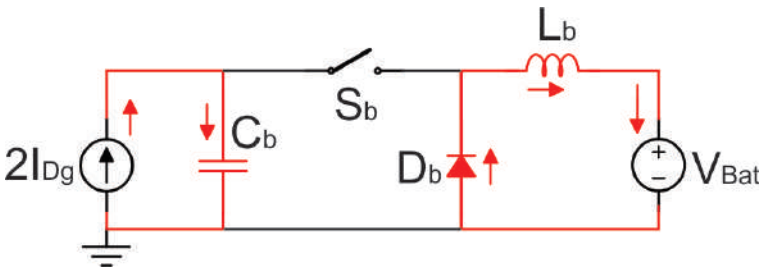
Figure 138 – First topological state of the clamping converter



Source: Own elaboration

Time interval Δt_2 - In the second topological state, the switch S_b is gated off and then the diode is directly polarized. So, at this stage the inductor (L_b) transfer energy to the battery and the clam capacitor is ready to store energy from the clamping diodes (D_{g2} and D_{g1}). The second topological state is presented in figure 139.

Figure 139 – Second topological state of the clamping converter



Source: Own elaboration

B.0.2 Transfer Function

The duty cycle (D_b) represents the period of time that the switch (S_b) is conducting. Then, the current and voltage across the switch and diode can be calculated.

$$I_{Db} = (1 - d_b)I_{Lb} \tag{285}$$

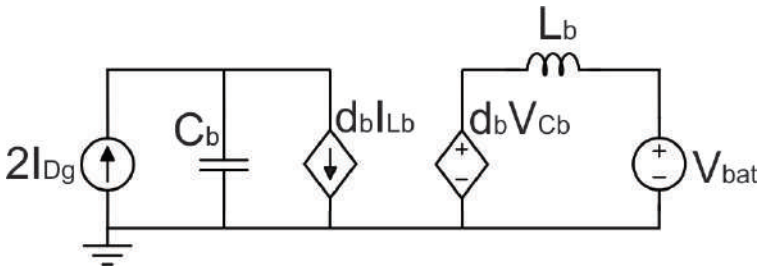
$$I_{Sb} = d_b I_{Lb} \tag{286}$$

$$V_{Db} = d_b V_{Cb} \tag{287}$$

$$V_{Sb} = (1 - d_b)V_{Cb} \tag{288}$$

Therefore, with the average values above, it is possible to design an average circuit model that represents the converter instead of the switched model. This model, presented in figure 140, has a virtual clamping resistance as described in a previous chapter.

Figure 140 – Average circuit model of the clamping converter



Source: Own elaboration

From the circuit above, the differential equations of the inductor voltage (V_{Lb}) and capacitor voltage (I_{Cb}) can be found.

$$L_b \frac{dI_{Lb}}{dt} = d_b V_{Cb} - R_V d_b I_{Lb} - V_{bat} \tag{289}$$

$$C_b \frac{dV_{Cb}}{dt} = 2I_{Dg} - d_b I_{Lb} \tag{290}$$

Which I_{Dg} represents the clamping diode current that charges the clamping capacitor.

Then, a small-signal modelling is realized by applying a perturbation near the operation point.

$$I_{Lb} = I_{Lb} + \Delta I_{Lb} \tag{291}$$

$$V_{Cb} = V_{Cb} + \Delta V_{Cb} \tag{292}$$

$$d_b = d_b + \Delta d_b \tag{293}$$

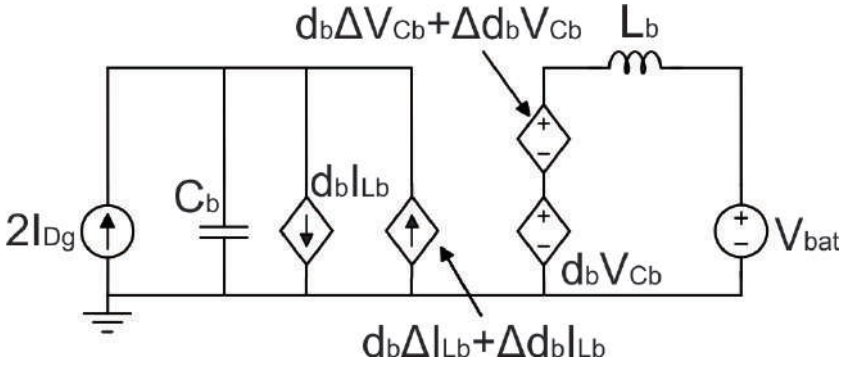
By replacing 291, 292 and 293 in 289 and 290, it gives:

$$L_b(\frac{di_{Lb}}{dt} + \frac{d\Delta I_{Lb}}{dt}) = (d_b + \Delta d_b)(V_{Cb} + \Delta V_{Cb}) - R_V(d_b \Delta I_{Lb} - \Delta d_b I_{Lb}) - V_{bat} \tag{294}$$

$$C_b\frac{dV_{Cb}}{dt} + C_b\frac{d\Delta V_{Cb}}{dt} = 2I_{Dg} - (d_bI_{Lb} + \Delta d_bI_{Lb} + d_b\Delta I_{Lb} + \Delta d_b\Delta I_{Lb}) \tag{295}$$

Then, the average and small-signal AC model can be developed, as represented in figure 141.

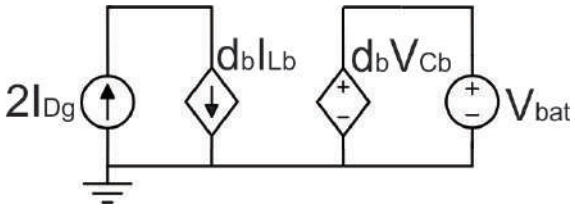
Figure 141 – Average and small-signal AC model of the clamping converter



Source: Own elaboration

Both models can be divided, the DC circuit, presented in figure 142, represents the steady and linearized variables in the operation point.

Figure 142 – DC circuit the clamping converter



Source: Own elaboration

Furthermore, this circuit can be used to find the converter static gain.

$$\frac{2I_{Dg}}{I_{Lb}} = d_b \tag{296}$$

$$\frac{V_{bat}}{V_{Cb}} = d_b \tag{297}$$

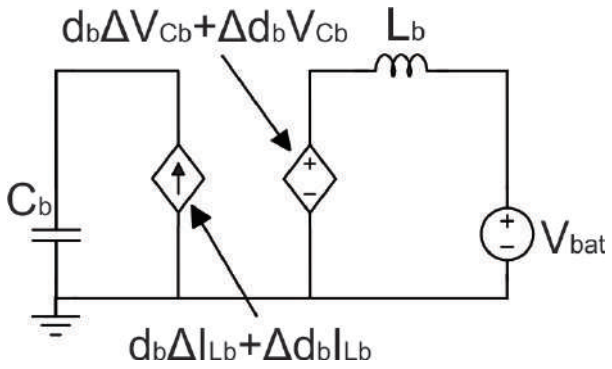
By eliminating the DC and second-order terms of equations 294 ans 295, the small-signal AC model is found.

$$\frac{d\Delta I_{Lb}}{dt} = \frac{d_b\Delta V_{Cb} + \Delta d_bV_{Cb} - R_Vd_b\Delta I_{Lb} - R_V\Delta d_bI_{Lb}}{L_b} \tag{298}$$

$$\frac{d\Delta V_{Cb}}{dt} = \frac{-\Delta d_b I_{Lb} - d_b \Delta I_{Lb}}{C_b} \tag{299}$$

The small-signal AC model, presented in figure 143, represents the variables that varies around the operation point.

Figure 143 – Small-signal AC model of the clamping converter



Source: Own elaboration

With some algebraic manipulations it is possible to find the relation of the clamping voltage variation for a duty cycle variation, by deriving equation 300.

$$\frac{d^2\Delta V_{Cb}}{dt^2} = -\frac{1}{C_b}\left(\frac{I_{Lb} d\Delta d_b}{dt} + \frac{d_b d\Delta I_{Lb}}{dt}\right) \tag{300}$$

Then, if 298 be replaced in 300 it leads to:

$$\frac{d^2\Delta V_{Cb}}{dt^2} + \frac{{d_b}^2\Delta V_{Cb}}{L_b C_b} + \frac{d_b \Delta d_b V_{Cb}}{L_b C_b} + \frac{d_b R_V}{L_b}\frac{d\Delta V_{Cb}}{dt} = -\frac{1}{C_b}\frac{I_{Lb} d\Delta d_b}{dt} \tag{301}$$

Furthermore, by replacing 299 in 301 leads to:

$$\frac{d^2\Delta V_{Cb}}{dt^2} + \frac{{d_b}^2\Delta V_{Cb}}{L_b C_b} + \frac{d_b \Delta d_b V_{Cb}}{L_b C_b} + \frac{d_b R_V}{L_b}\frac{d\Delta V_{Cb}}{dt} = -\frac{1}{C_b}\frac{I_{Lb} d\Delta d_b}{dt} \tag{302}$$

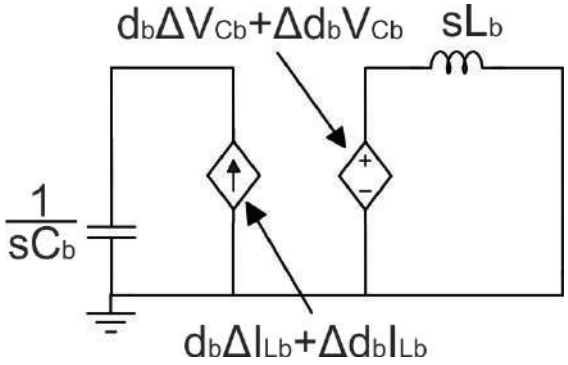
Also, by applying the Laplace transformer in 302, it gives a frequency domain response.

$$s^2\Delta V_{Cb}(s) + \frac{{d_b}^2\Delta V_{Cb}(s)}{L_b C_b} + \frac{d_b R_V \Delta V_{Cb}(s)}{L_b} = -\frac{d_b V_{Cb}\Delta d_b(s)}{L_b C_b} - \frac{s I_{Lb}\Delta d_b(s)}{C_b} \tag{303}$$

Then, the clamping voltage and duty cycle variation can be isolated in the equation 303.

$$\Delta V_{Cb}(s)\left(s^2 + \frac{d_b R_V}{L_b} + \frac{{d_b}^2}{L_b C_b}\right) = \Delta d_b(s)\left(-\frac{d_b V_{Cb}}{L_b C_b} - \frac{s I_{Lb}}{C_b}\right) \tag{304}$$

Figure 144 – Small-signal AC model of the clamping converter with the Laplace transform



Source: Own elaboration

So, the equation 304 can be written as a new equivalent circuit applying the Laplace Transform, as shown in figure 144.

Finally, the transfer function that represents the clamping voltage variation as a function of the duty cycle variation is presented in equation 305.

$$\frac{\Delta V_{Cb}(s)}{\Delta d_b(s)} = \frac{-\left(\frac{sI_{Lb}}{C_b} + \frac{d_b V_{Cb}}{L_b C_b}\right)}{\left(s^2 + \frac{sd_b R_V}{L_b} + \frac{{d_b}^2}{L_b C_b}\right)} \tag{305}$$

Note that the transfer function presents the average inductor current and clamping voltage, so they can be imposed by the designer. Also, the virtual resistance act as a first order damping factor.

B.0.3 Transfer Function Validation

It is possible to validate the transfer function by applying the AC Sweep tool in the converter circuit and in the transfer function adopting a simulation software.

Therefore, the amplitude and phase of both theoretical transfer function and the switched model can be plotted in the same bode diagram.

In order to acquire the bode diagram, some variable must be defined as represented in table 14.

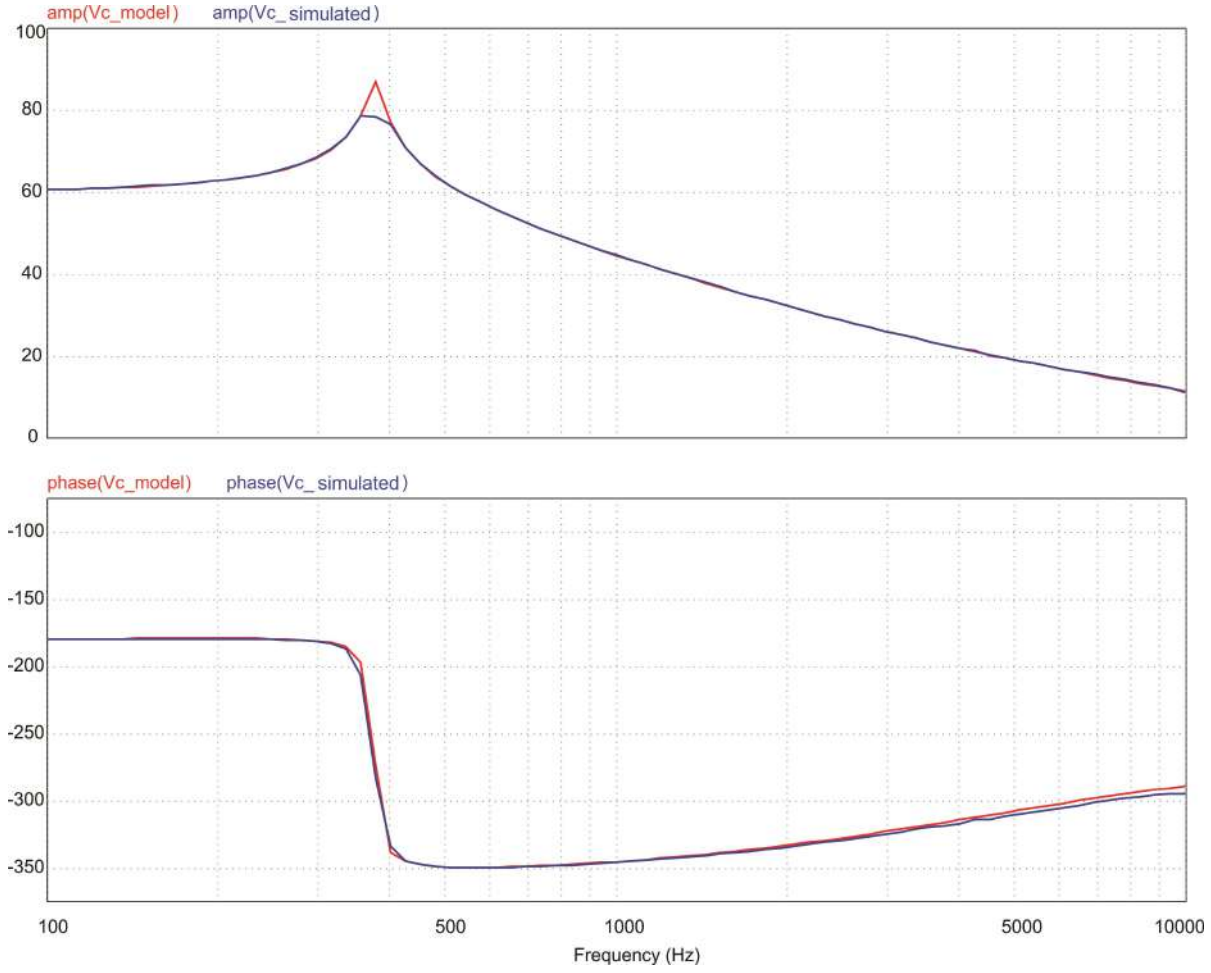
The transfer function should be validated in the region which the controller will be applied. Usually, the cut-off frequency of the controller is one decade smaller than the switching frequency. So, figure 145 illustrates the bode diagram of both models until 10 kHz.

Table 14 – Specifications for the transfer function validation of the Buck Converter voltage input

Specification	**Value**
Buck inductor current (I_{Lb})	4.167 A
Buck capacitor voltage (V_{Cb})	220 V
Buck inductor (L_b)	450 μH
Buck capacitor (C_b)	18.8 μF
Buck duty cycle (d_b)	0.218
Buck series resistance (R_V)	0.2 Ω

Source: Own elaboration

Figure 145 – Bode diagram of the model and simulated clamping voltage transfer function



Source: Own elaboration

APPENDIX C – VOLTAGE PI CONTROLLER

Clamping voltage control

Converter specifications:

$R_s := 0.2\Omega$

$j := \sqrt{-1}$ Imaginarium number

$I_{buck} := 4.167A$ Buck inductor's current

$C_{buck} := 18.8\mu F$ Buck capacitance

$L_{buck} := 0.45mH$ Buck inductance

$d_{buck} := 0.218$ Buck's duty cycle

$V_{Cbuck} := 220V$ Buck's capacitor voltage

$k_{vo} := \frac{1}{V}$ Sensor gain

$$G_v(\omega) := \frac{-\left[\frac{(j\cdot\omega)\cdot(I_{buck})}{C_{buck}} + \frac{d_{buck}\cdot V_{Cbuck}}{L_{buck}\cdot C_{buck}}\right]}{(j\cdot\omega)^2 + (j\cdot\omega)\cdot\frac{R_s\cdot d_{buck}}{L_{buck}} + \frac{d_{buck}^2}{L_{buck}\cdot C_{buck}}}$$

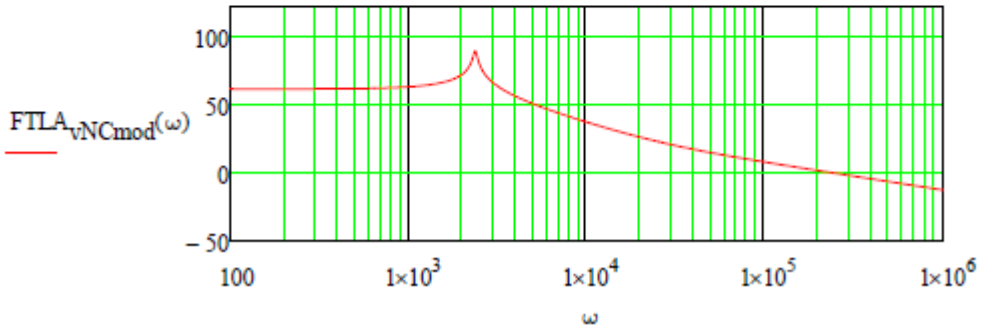
Transfer function of Vcbuck/d

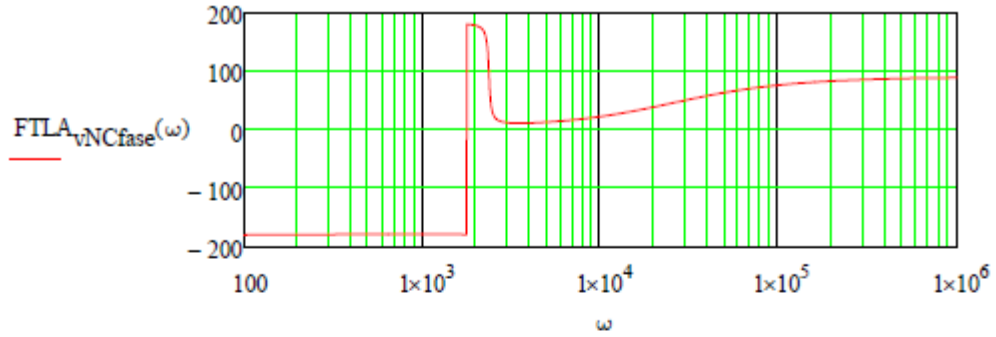
Closed-loop Control System:

$FTLA_{vNC}(\omega) := G_v(\omega)\cdot k_{vo}$

$FTLA_{vNCmod}(\omega) := 20\cdot\log\left(\left|FTLA_{vNC}(\omega)\right|\right)$

$FTLA_{vNCfase}(\omega) := \frac{180}{\pi}\cdot\arg\left(FTLA_{vNC}(\omega)\right)$





Due to the low gain at low frequencies and the phase invesion to 90°, it is necessary to implement a PT compensator with the following criteria:

$\omega_c := 2\cdot\pi\cdot 1000\text{Hz} = 6.283 \times 10^3 \frac{1}{s}$ Crossover frequency

$M_f := 120\cdot\frac{\pi}{180} = 2.094$ Phase frequency

$$\omega_z := \frac{\omega_c}{\tan\left(M_f - \frac{\pi}{2} - \arg\left(FTLA_{vNC}(\omega_c)\right)\right)} = 2.318 \times 10^4 \frac{1}{s}$$

$t := \frac{1}{\omega_z} = 43.146\cdot\mu s$ PI time constant

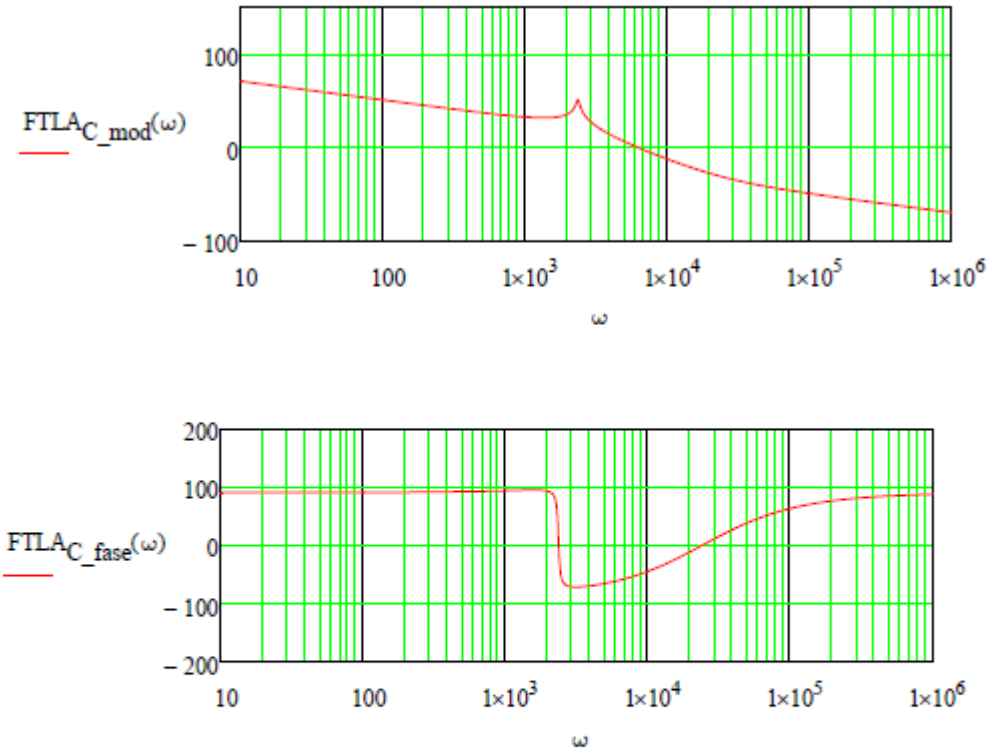
$$k_c := \frac{\omega_c}{\sqrt{\omega_z^2 + \omega_c^2}\cdot\left|FTLA_{vNC}(\omega_c)\right|} = 1.518 \times 10^{-3}$$ PI gain constant

$$C(\omega) := \frac{k_c\cdot(j\cdot\omega + \omega_z)}{j\cdot\omega}$$

$FTLA_C(\omega) := FTLA_{vNC}(\omega)\cdot C(\omega)$

$FTLA_{C\_mod}(\omega) := 20\cdot\log\left(\left|FTLA_C(\omega)\right|\right)$

$$FTLA_{C\_fase}(\omega) := \frac{180}{\pi}\cdot\arg\left(FTLA_C(\omega)\right)$$



With the module and phase graphs, it can be observed the low frequency gain that the compensator provides to the transfer function. The phase inversion was not solved, so the converter can be unstable for some phase. Therefore, a PI would work for simulation results in a correnct phase point, but a more complex compensator needs to be applied for a experimental application.

APPENDIX D – CURRENT PI CONTROLLER

Push-Pull Current Control

Converter specifications:

$j := \sqrt{-1}$ Imaginarium number

$V_{trip} := 1V$ Triangular gain

$k_{pwm} := \frac{1}{V_{trip}} = 1\frac{1}{V}$ PWM gain

$k_i := 1\frac{V}{A}$ Sensor gain

$V_{PC} := 400V$ Full-bridge voltage input

$L_{lk} := 16.25\mu H$ Leakage inductance

$\alpha := 0.185$ Transformer turns ratio

$L_d := 2\alpha^2 \cdot L_{lk} = 1.112 \times 10^{-6} H$ Leakage inductance reffered to the Push-Pull side

$L := 4.32 \times 10^{-5} H$ Push-Pull inductance

$f_s := 40kHz$ Commutation frequency

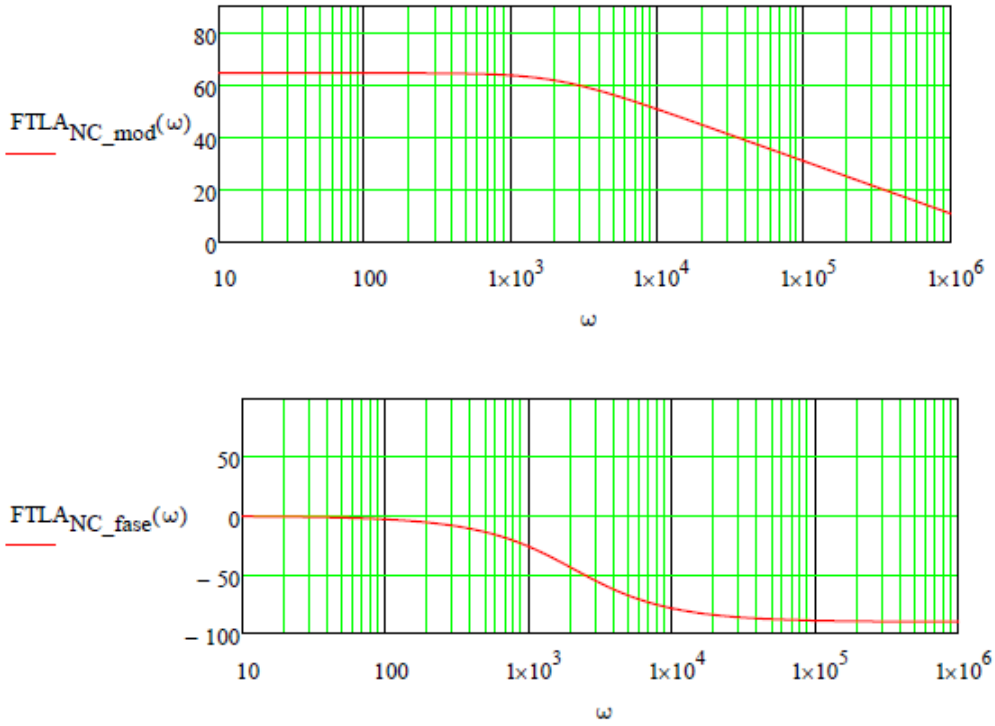
$$G_i(\omega) := \frac{2 \cdot \alpha V_{PC}}{(j \cdot \omega)L + 2 \cdot L_d \cdot f_s}$$ Transfer funciton of iL/d

Closed-loop Control System:

$$FTLA_{NC}(\omega) := k_i \cdot k_{pwm} \cdot G_i(\omega)$$

$$FTLA_{NC\_mod}(\omega) := 20 \cdot \log\left(\left|FTLA_{NC}(\omega)\right|\right)$$

$$FTLA_{NC\_fase}(\omega) := \frac{180}{\pi} \cdot \arg\left(FTLA_{NC}(\omega)\right)$$



Due to the low gain at low frequencies, it is necessary to implement a PI compensator with the following criteria:

$\omega_c := 2\cdot\pi\cdot 1000\text{Hz} = 6.283\times 10^3\,\frac{1}{s}$ Crossover frequency

$M_f := 90\cdot\frac{\pi}{180} = 1.571$ Phase frequency

$$\omega_z := \frac{\omega_c}{\tan\left(M_f - \frac{\pi}{2} - \arg\left(FTLA_{NC}(\omega_c)\right)\right)} = 2.06\times 10^3\,\frac{1}{s}$$

$t := \frac{1}{\omega_z} = 485.475\cdot\mu s$ PI time constant

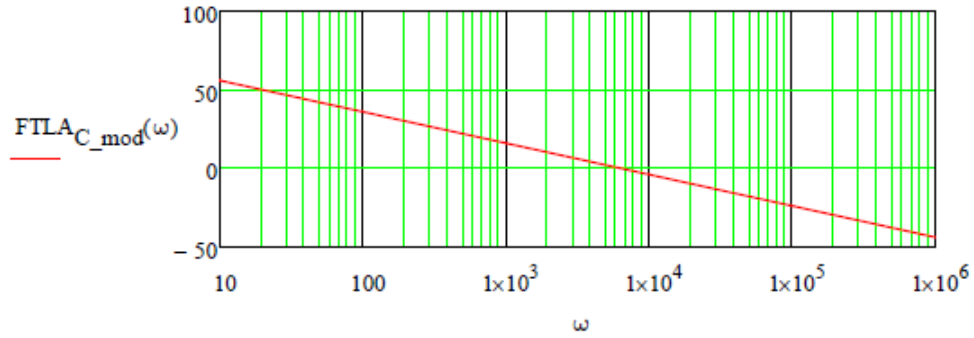
$$k_c := \frac{\omega_c}{\sqrt{\omega_z^{\,2} + \omega_c^{\,2}}\cdot\left|FTLA_{NC}(\omega_c)\right|} = 1.834\times 10^{-3}$$ PI gain constant

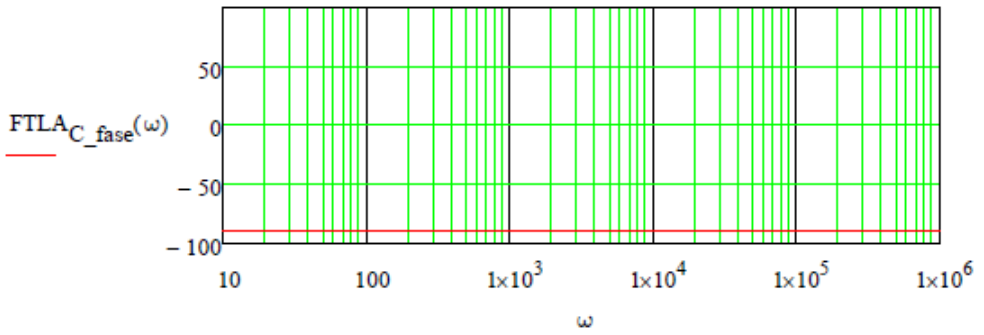
$$C(\omega) := \frac{k_c\cdot(j\cdot\omega + \omega_z)}{j\cdot\omega}$$

$$FTLA_{C}(\omega) := FTLA_{NC}(\omega)\cdot C(\omega)$$

$$FTLA_{C\_mod}(\omega) := 20\cdot\log\left(\left|FTLA_{C}(\omega)\right|\right)$$

$$FTLA_{C\_fase}(\omega) := \frac{180}{\pi}\cdot\arg\left(FTLA_{C}(\omega)\right)$$





With the module and phase graphs you can see the low frequency gain that the compensator provides to the transfer function.

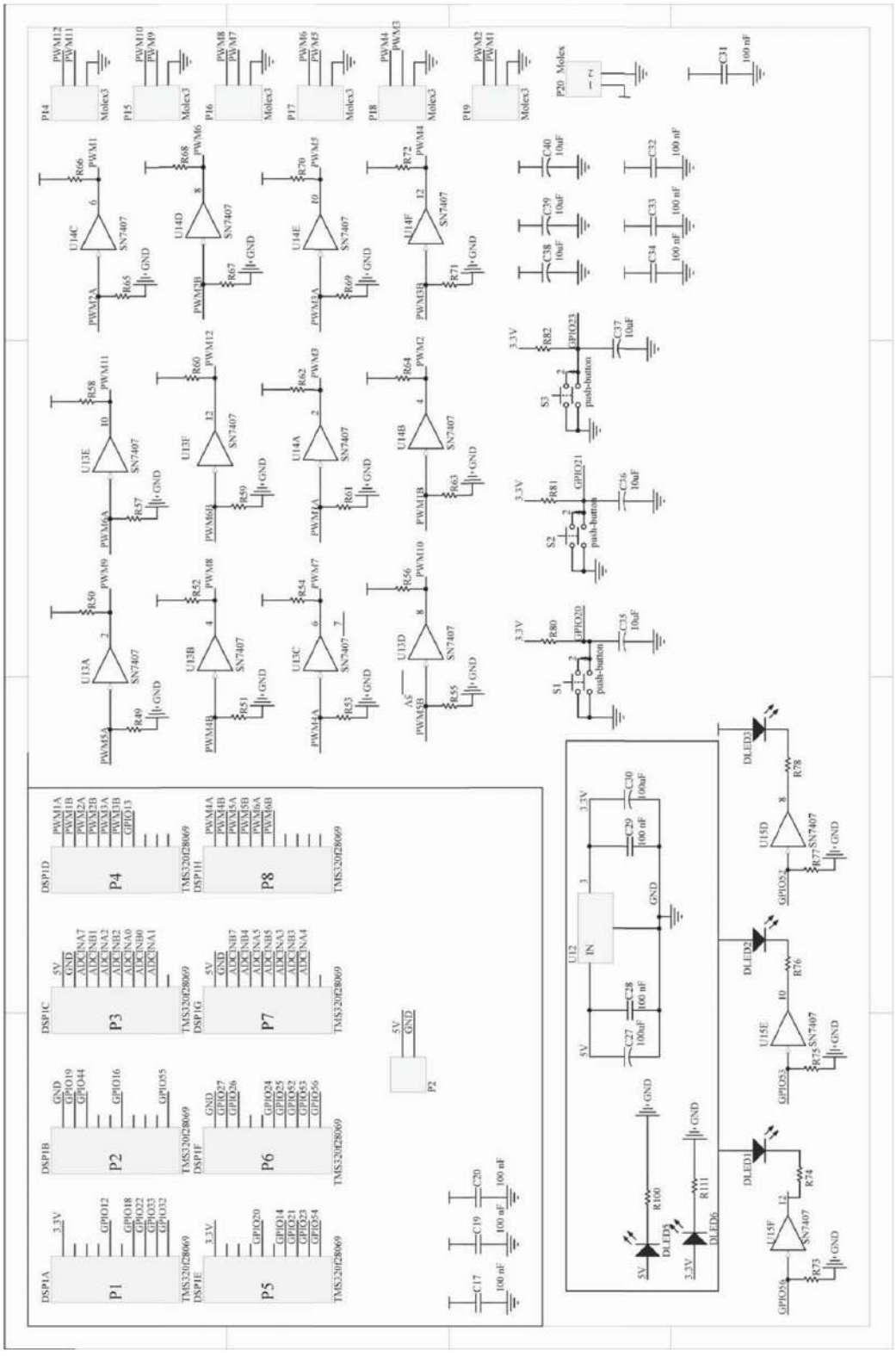
APPENDIX E – DSP CODE

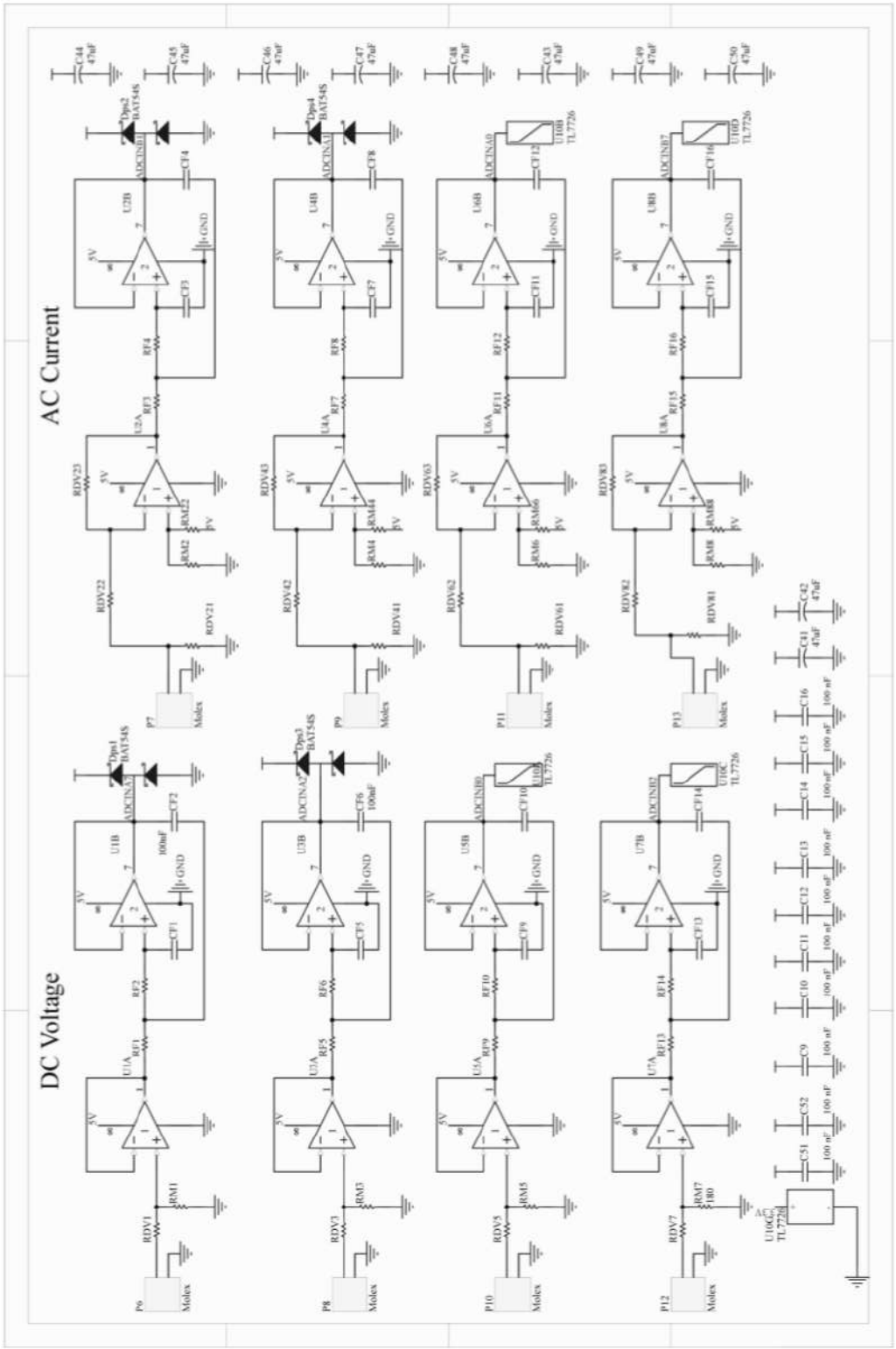
```
/*  ------------------------ Fotovoltaica Laboratory ---------------------------------
 *                     Federal University of Santa Catarina
 *
 *                                Ygor Pereira Marca
 *  ------------------------------------------------------------------------------------
*/

#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File
#include <math.h>               // Mathematical library
// Global variables used in this example:
Uint16 LoopCount;

//Defines
#define F_PWM 40000 //Setting a 40kHz switching frequency


int T_PWM, tm=220, DB;  //Declare int variables
double d, dbuck;  //Declare double variables

void configGPIO(void);   //GPIO set up
void configPWM(void);   //PWM set up

main()
{

    // Initiate the CPU

       InitGpio();              // Configure GPIO
       InitSysCtrl();           //Configure System Control
       InitPieCtrl();           //Configure Pie Control
       InitPieVectTable();      //Configure PieVect Table

        configPWM(); //Configure PWM

        while(1){};
}

void configPWM(void){

    T_PWM = 22500000/F_PWM; //Defining the time period
    tm = 200; //Dead-time
    DB = tm*0.045;

    d = 0.3; //Duty Cycle
    dbuck = 1-0.2; //Buck's Duty Cycle

//Full-Bridge Converter

//Gate Signals of S1 and S2
EPwm1Regs.TBPRD =  (2*T_PWM)-1; // Period = 1600 TBCLK counts
EPwm1Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Symmetrical mode
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Master module
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // sync flow-through
```

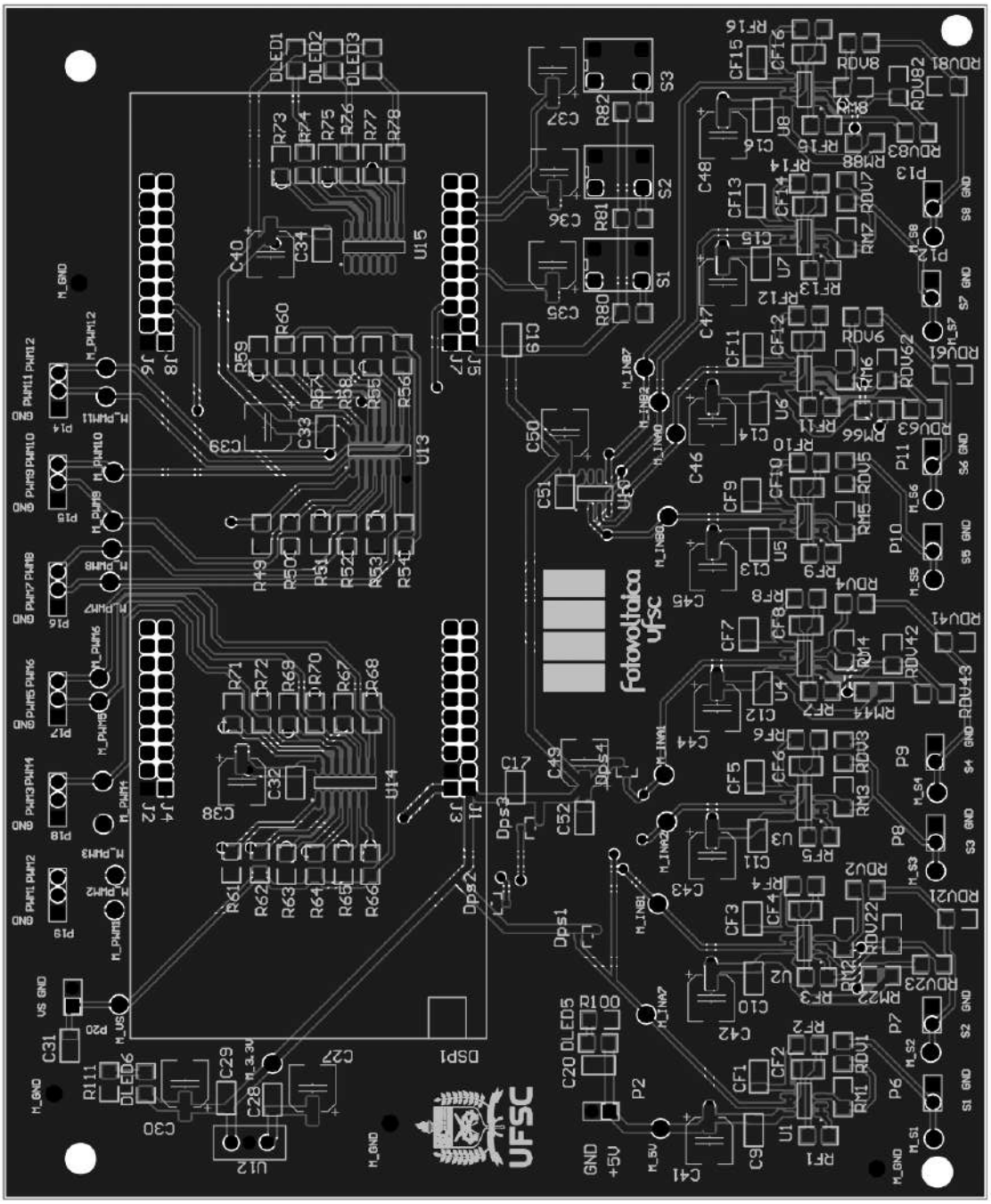
```
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM2A
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm1Regs.DBFED = DB; // FED = 50 TBCLKs
EPwm1Regs.DBRED = DB; // RED = 50 TBCLKs
EPwm1Regs.CMPA.half.CMPA = T_PWM; // adjust duty for output EPWM2A

//Gate Signals of S3 and S4
EPwm3Regs.TBPRD =  (2*T_PWM)-1; // Period = 1600 TBCLK counts
EPwm3Regs.TBPHS.half.TBPHS = T PWM*(1-d); // Set Phase register to zero
EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Symmetrical mode
EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Master module
EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm3Regs.CMPCTL.bit.LOADBMODE = CC CTR ZERO; // load on CTR=Zero
EPwm3Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM2A
EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm3Regs.DBCTL.bit.OUT MODE = DB FULL ENABLE; // enable Dead-band module
EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm3Regs.DBFED = DB; // FED = 50 TBCLKs
EPwm3Regs.DBRED = DB; // RED = 50 TBCLKs
EPwm3Regs.CMPA.half.CMPA = T_PWM; // adjust duty for output EPWM2A


//Push-Pull Converter

//Gate Signals of S6
EPwm2Regs.TBPRD = (T_PWM*2)-1; // Period = 1600 TBCLK counts
EPwm2Regs.CMPA.half.CMPA = T PWM*(1+d)-DB+2;//T PWM*(1+d)+DB/2-1;
EPwm2Regs.TBPHS.half.TBPHS = T_PWM-DB+2; // Set Phase register to zero
EPwm2Regs.TBCTR = 0;
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Symmetrical mode
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Master module
EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC SHADOW;
EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm2Regs.AQCTLA.bit.ZRO = AQ SET; // set actions for EPWM2A
EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;


//Gate Signals of S5
EPwm5Regs.TBPRD = (T_PWM*2)-1; // Period = 1600 TBCLK counts
EPwm5Regs.CMPA.half.CMPA = T_PWM*(1+d)-3;//T_PWM*(1+d)+DB/2-2;
EPwm5Regs.TBPHS.half.TBPHS = (T_PWM*2)-DB+3; // Set Phase register to zero
```

```
EPwm5Regs.TBCTR = 0;
EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Symmetrical mode
EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Master module
EPwm5Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm5Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm5Regs.CMPCTL.bit.LOADBMODE = CC CTR ZERO; // load on CTR=Zero
EPwm5Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM2A
EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;

//Buck Converter

EPwm6Regs.TBPRD = T PWM*0.5; // Period = 1600 TBCLK counts
EPwm6Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Master module
EPwm6Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm6Regs.CMPCTL.bit.LOADAMODE = CC CTR ZERO; // load on CTR=Zero
EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm6Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
EPwm6Regs.AQCTLA.bit.CAD = AQ CLEAR;
EPwm6Regs.CMPA.half.CMPA = dbuck*T_PWM*0.5; // adjust duty for output EPWM2A



// Initialize PWM module
InitEPwm();         // Initialize PWM
InitEPwm1Gpio();    // Default setting for PWM module 1
InitEPwm2Gpio();    // Default setting for PWM module 3
InitEPwm3Gpio();    // Default setting for PWM module 1
InitEPwm4Gpio();    // Default setting for PWM module 1
InitEPwm5Gpio();    // Default setting for PWM module 1
InitEPwm6Gpio();    // Default setting for PWM module 1

EPwm1Regs.TBCTR = 0; //Set phase to zero
EPwm2Regs.TBCTR = 0; //Set phase to zero
EPwm5Regs.TBCTR = 0; //Set phase to zero
}
```

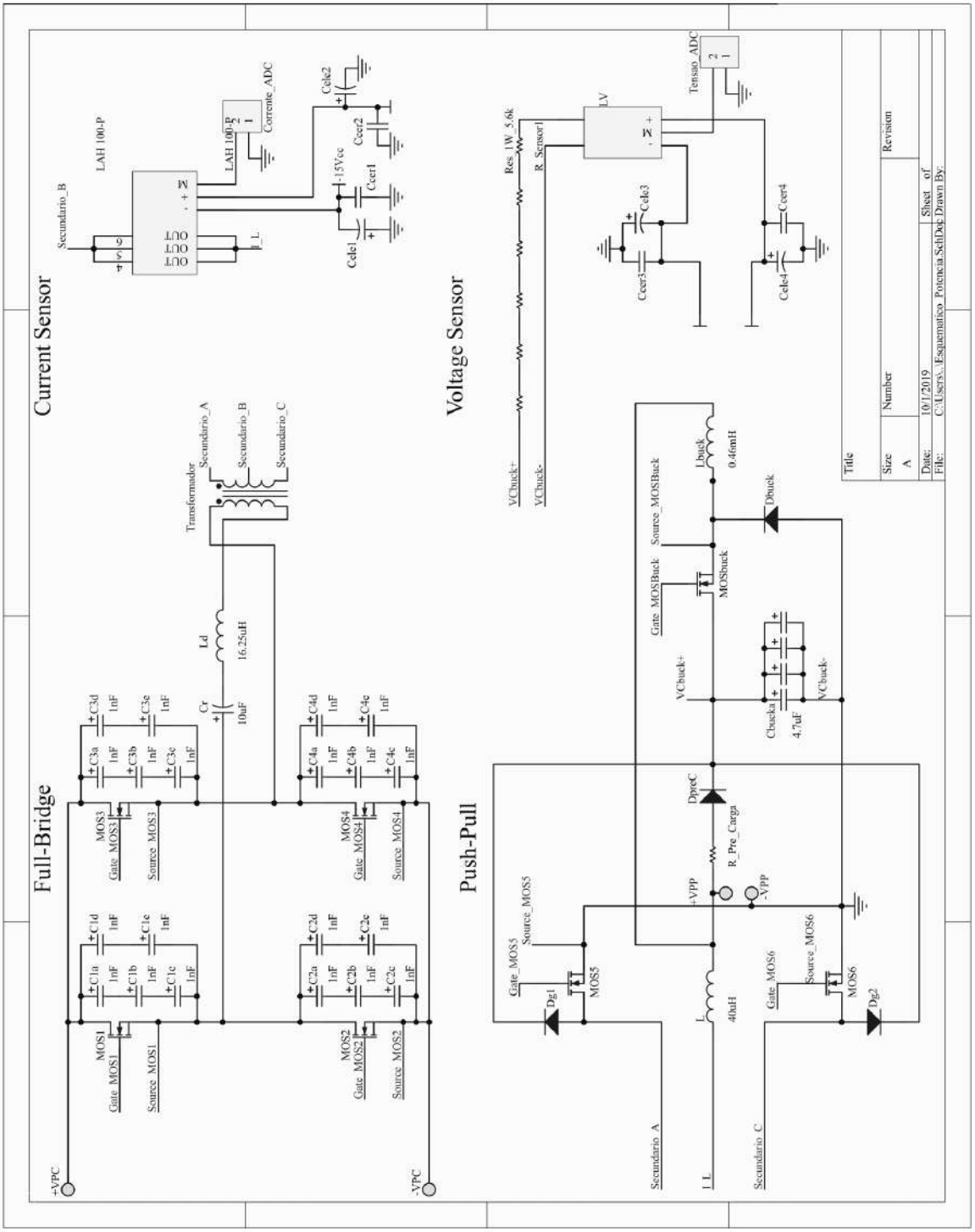
APPENDIX F – SIGNAL CONDITIONING PCB

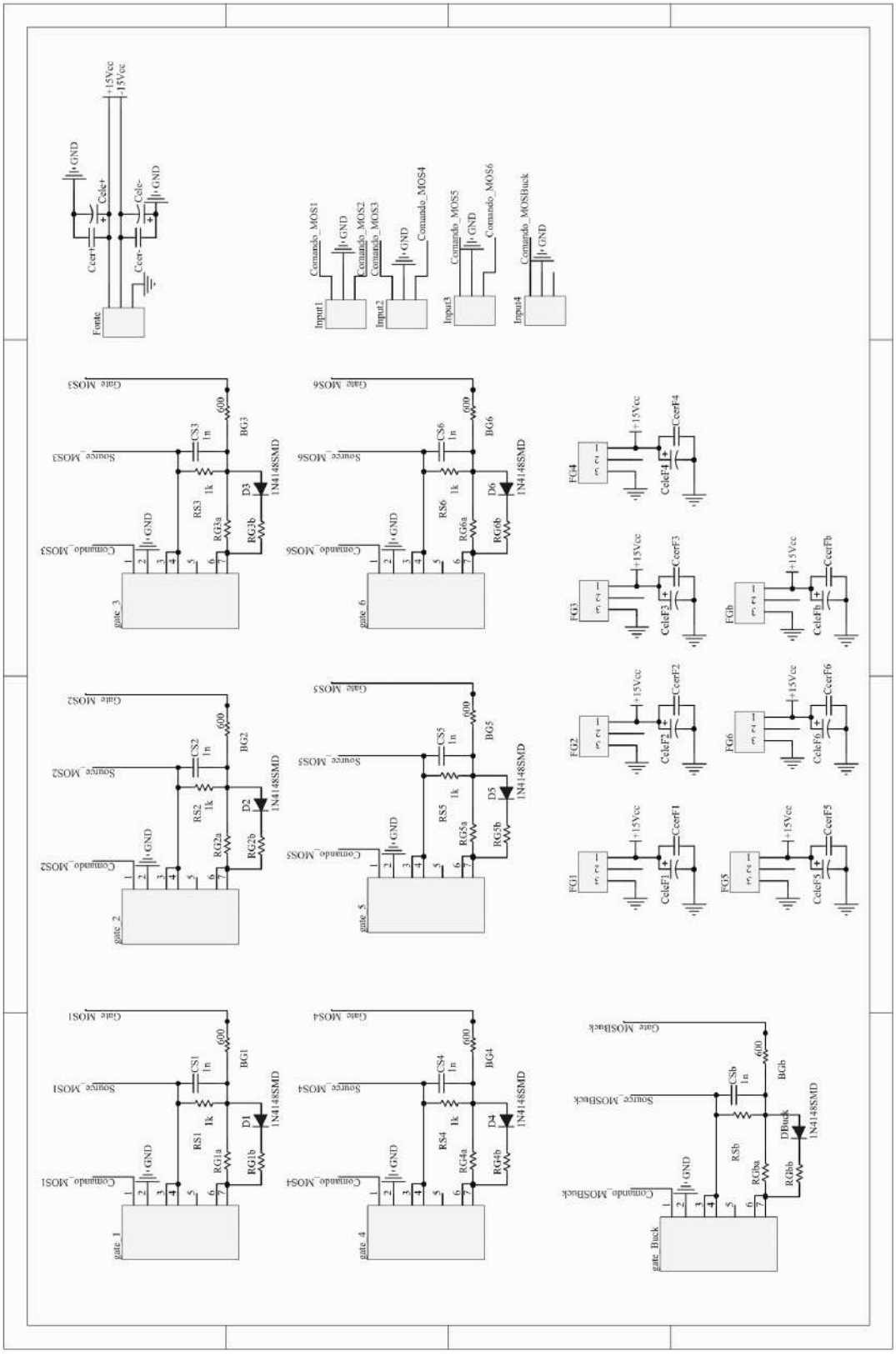


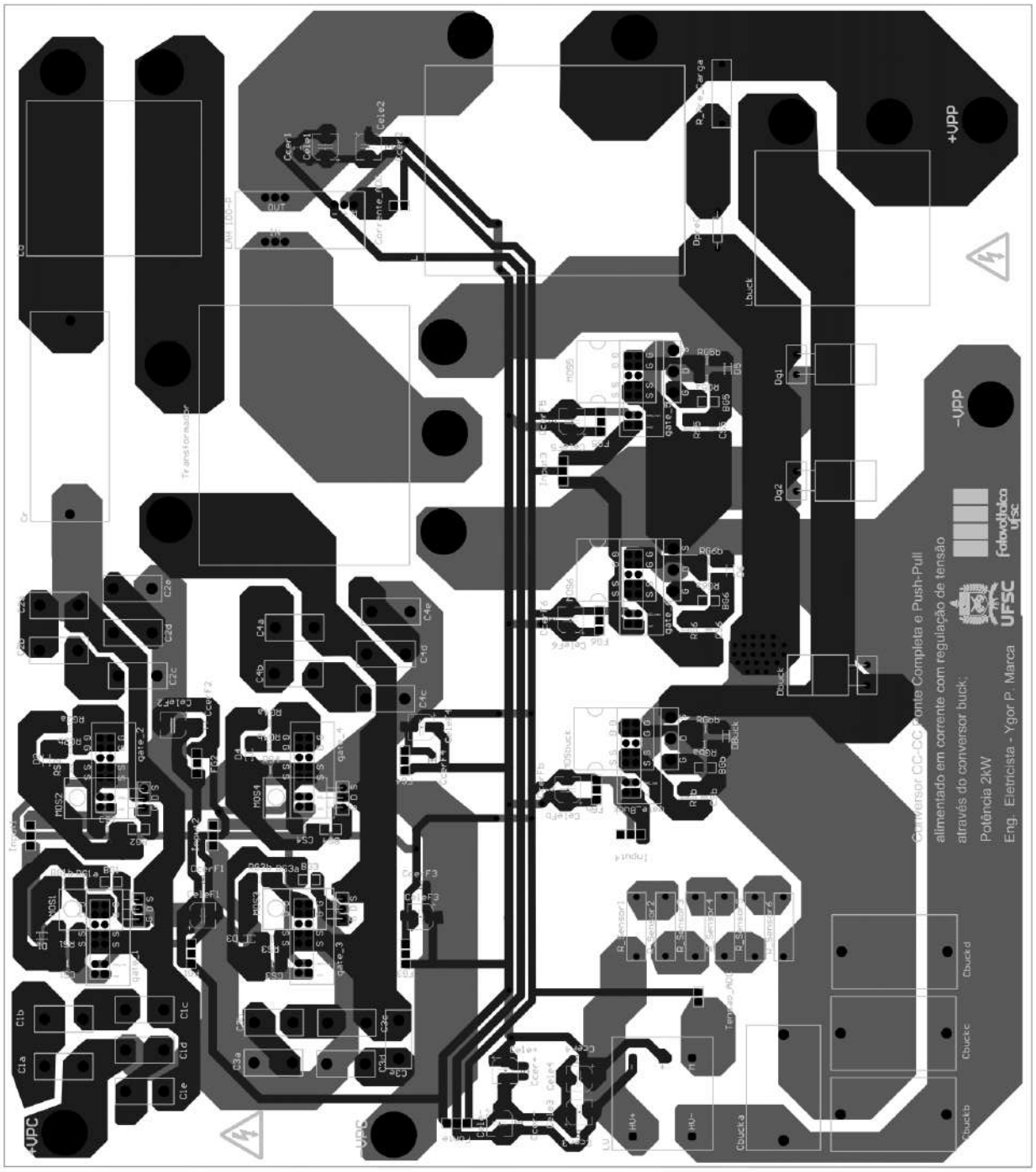

AC Current
DC Voltage
Molex
TL7726
BAT54S
100nF
100 nF
47nF
5V
0V
GND


fotovoltaica
ufsc
UFSC
DSP1
M_GND
+5V
GND

APPENDIX G – POWER STAGE PCB




+15Vcc
-15Vcc
GND
Cele+
Cele-
Ccer+
Ccer-
Fonte
Comando_MOS1
Comando_MOS2
Comando_MOS3
Comando_MOS4
Comando_MOS5
Comando_MOS6
Comando_MOSBuck
Input1
Input2
Input3
Input4
Gate_MOS3
Source_MOS3
Comando_MOS3
gate_3
CS3
RS3
RG3a
RG3b
BG3
D3
1N4148SMD
Gate_MOS6
Source_MOS6
Comando_MOS6
gate_6
CS6
RS6
RG6a
RG6b
BG6
D6
Gate_MOS2
Source_MOS2
Comando_MOS2
gate_2
CS2
RS2
RG2a
RG2b
BG2
D2
Gate_MOS5
Source_MOS5
Comando_MOS5
gate_5
CS5
RS5
RG5a
RG5b
BG5
D5
Gate_MOS1
Source_MOS1
Comando_MOS1
gate_1
CS1
RS1
RG1a
RG1b
BG1
D1
Gate_MOS4
Source_MOS4
Comando_MOS4
gate_4
CS4
RS4
RG4a
RG4b
BG4
D4
Gate_MOSBuck
Source_MOSBuck
Comando_MOSBuck
gate_Buck
CSb
RSb
RGba
RGbb
BGb
DBuck
1k
1n
600
FG4
CcerF4
CeleF4
FG3
CcerF3
CeleF3
FGb
CcerFb
CeleFb
FG2
CcerF2
CeleF2
FG6
CcerF6
CeleF6
FG1
CcerF1
CeleF1
FG5
CcerF5
CeleF5


+VPP
-VPP
Conversor CC-CC Fonte Completa e Push-Pull
alimentado em corrente com regulação de tensão
através do conversor buck.
Potência 2kW
Eng. Eletricista - Ygor P. Marca
UFSC
fotovoltaica
ufsc

APPENDIX H – LIST OF MATERIAL

LIST OF MATERIAL					
COMPONENT	BRAND	AMOUNT	VALUE ($)	TOTAL VALUE ($)	PART NUMBER
MOSFET N-CH 600V 13A TO220	ON Semiconductor	16	4.1930	67.09	FCP13N60N
MOSFET N-CH 600V 76A TO247	ROHM Semiconductor	4	10.2300	40.92	R6076ENZ1C9-ND
CAPACITOR FILM 4.7UF 10% 450VDC RADIAL	EPCOS (TDK)	10	3.0260	30.26	B32674D4475K000
CAPACITOR FILM 10UF 5% 250VDC AXIAL	KEMET	2	5.7000	11.40	C4GADUC5100AA1J
CAPACITOR FILM 1000PF 10% 630VDC RAD	DPP6D1K-F	40	0.5850	23.40	DPP6D1K-F
DIODE GEN PURP 400V 8A TO220AC	STMicroelectronics	8	1.6700	13.36	STTH8R04DI
DIODE GEN PURP 400V 15A TO220FP	IXYS	4	1.5400	6.16	DPG15I400PM
SENSOR CURRENT HALL LAH 100-P	LEM	2	23.6500	47.30	LAH 100-P
TRANSDUCR VOLTAG CLOSE LOOP 10MA	LEM	1	45.5400	45.54	LV 20-P
TL7726	Texas Instruments	8	2.2240	17.79	TL7726QDR
LM3940	Texas Instruments	3	1.8200	5.46	LM3940IT-3.3/NOPB
SN7407	Texas Instruments	8	0.7540	6.032	SN7407DR
LM 358	STMicroelectronics	8	0.3590	2.872	497-1591-1-ND
RESISTOR 0805 680Ω	Stackpole Elect. Inc.	20	0.0270	0.54	RMCF0805FT680RCT-ND
RESISTOR 0805 3.3kΩ	Stackpole Electronics	20	0.1520	3.04	RHM3.3KAHCT-ND
RESISTOR 0805 2.7kΩ	Rohn semicondutor	20	0.0560	1.12	1276-5295-1-ND
RESISTOR 0805 5,6Ω	Samsung E-M	20	0.3650	7.30	P15996CT-ND
RESISTOR 1206 220Ω	Panasonic E-C	20	0.0730	1.46	541-4190-1-ND
RES 300 OHM 1% 1/4W 1206	Stackpole Elect. Inc.	20	0.0360	0.72	RMCF1206FT300R
RES 60.4 OHM 1% 1/4W 1206	Stackpole Elect. Inc.	20	0.0360	0.72	RMCF1206FT60R4
RES 120 OHM 1% 1/4W 1206	Stackpole Elect. Inc.	20	0.0360	0.72	RMCF1206FT120R
RES 1K OHM 1% 1/4W SMD 1206	Stackpole Elect. Inc.	20	0.0360	0.72	RMCF1206FT1K00
CAP ALUM 47UF 20% 25V SMD	KEMET	50	0.1629	8.15	EDK476M025A9GAA
CAP CER 10000PF 250V X7R 0805	KEMET	30	0.3360	10.08	C0805V103KBRAC7800
CAP CER 0.033UF 50V 0805	KEMET	50	0.4060	20.30	C0805C333J5RACTU
CAP CER 0.1UF 250V X7T 0805	TDK Corporation	50	0.2620	13.10	C2012X7T2E104M125AE
CAP CER 150PF 450V 0805	TDK Corporation	30	0.1750	5.25	C2012C0G2W151J060AE

LIST OF MATERIAL					
COMPONENT	**BRAND**	**AMOUNT**	**VALUE ($)**	**TOTAL VALUE ($)**	**PART NUMBER**
CAP CER 0.1UF 25V X7R 1206	KEMET	50	0.2325	11.63	C1206F104K3RACTU
CAP CER 0.22UF 100V X7R 1206	KEMET	20	0.7550	15.10	C1206C476M9PACTU
CAP CER 5600PF 50V NP0 1206	KEMET	20	0.6900	13.80	C1206C562J5GAC7800
CAP CER 4700PF 100V NP0 1206	KEMET	20	0.5920	11.84	C1206C472J1GAC7800
CAP CER 10000PF 50V C0G/NP0 1206	KEMET	20	0.9800	19.60	C1206C103J5GACTU
LED RED CLEAR 1206 SMD R/A	QT Brightek (QTB)	25	0.2420	6.05	QBLP615-R
THERM PAD 16.51MMX12.7MM	TDB Corporation	14	0.5240	7.336	4171G-ND
FAN AXIAL 80X38MM 100-240VAC	Mechatronics Fan Group	3	23.5900	70.77	LPH80A99-BTHR
RES SMD 0 OHM JUMPER 1/8W 0805	Panasonic Elect. Comp.	25	0.0440	1.1	ERJ-6GEY0R00V
RES SMD 0 OHM JUMPER 1/4W 1206	Panasonic Elect. Comp.	25	0.0520	1.3	ERJ-8GEY0R00V
AC/DC CONVERTER 5V +/-15V 66W RT-65C	MEAN WELL USA Inc.	1	25.2100	25.21	RT-65C
IC OSC SGL TIMER 500KHZ 8-SOIC	Maxim Integrated	12	2.5850	31.02	ICM7555ISA+TCT-ND
OPTOISO 5KV 1CH	ON Semiconductor	12	2.3870	28.644	FOD3182SDV
MOSFET N/P-CH 30V 7.3/5.3A 8SOIC	Vishay	12	0.7960	9.552	SQ4532AEY-T1_GE3
FERRITE BEAD 600 OHM 0805 1LN	TDK Corporation	16	0.1040	1.664	MPZ2012S601ATD25
FERRITE BEAD 330 OHM 0805 1LN	Wurth Electronics Inc.	16	0.2000	3.2	742792037
FERRITE BEAD 1.5 KOHM 0805 1LN	Wurth Electronics Inc.	16	0.2200	3.52	742792097
FERRITE BEAD 1 KOHM 0805 1LN	TDK Corporation	16	0.1040	1.664	MPZ2012S102ATD25
DIODE GEN PURP 100V 200MA LL34	Fairchild SemiC.	16	0.0860	1.376	FDLL4148CT-ND
FERRITE CORE TOROID 610NH N49	TDK Corporation	12	0.3120	3.744	495-76561-ND
TVS DIODE 18V 29.2V DO214AA	Littelfuse Inc.	16	0.3144	5.0304	SMBJ18CALFCT-ND
PICCOLO C2000 LAUNCHXL-F28069M	Texas Instruments	1	27.0500	27.05	LAUNCHXL-F28069M
DIODE GEN PURP 400V 700MA AXIAL	Sanken	3	0.5200	1.56	AG01V1CT-ND
RES 10.0K OHM 1/2W 1% AXIAL	Vishay Dale	3	0.5800	1.74	CMF10.0KHFTR-ND
TOTAL	$694.29				