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MODULATION AND SYNCHRONIZATION ALGORITHMS FOR FPGA DRIVEN INDIRECT MATRIX CONVERTERS

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Esta Dissertação de Mestrado foi julgada aprovada para a obtenção do Título de “Mestre em Engenharia Elétrica”, e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica.

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And we know that all things work together for good to them that love God, to them who are the called according to his purpose.

Romans 8:28

Resumo

Uma visão compartilhada por especialistas é de que no futuro, comunidades residenciais e comerciais serão autossuficientes com respeito à produção de energia elétrica, incluindo unidades de microgeração às fontes de geração de energia elétrica. A interface entre as partes mecânicas e elétricas normalmente é realizada através de geradores elétricos, que por sua vez podem possuir frequência variável enquanto buscam melhor eficiência do processo. Neste contexto, a inserção destas fontes de energia necessita de um estágio de processamento de energia entre gerador e rede elétrica, buscando adequar níveis de amplitude e frequência das grandezas de corrente alternada (CA). Este trabalho busca estudar um conversor estático capaz de processar as grandezas entre dois sistemas CA distintos sem um estágio CC intermediário. As vantagens destas topologias são o rendimento elevado do processo, bem como redução de peso e volume do conversor estático, mantendo a capacidade de drenar e injetar correntes com formato sinusoidal para ambos estágios CA. Esta dissertação propõe um estudo da operação destes conversores estáticos, bem como uma caracterização estática e dinâmica. Um estudo de algoritmos necessários para realizar esta interface, bem como uma revisão de como projetar e implementar estes algoritmos também é apresentada. Também são apresentados resultados experimentais obtidos através de um protótipo, verificando o funcionamento do conversor.

Palavras-chave: Conversores Matriciais, Estratégias de Modulação, FPGA, Sincronismo.

Resumo Expandido

Introdução

Desde os tempos remotos, a humanidade utiliza as fontes de energia acessíveis para facilitar a execução de tarefas frequentes. No período atual, a eletrecidade é um recurso indispensável para a sociedade moderna, garantindo o funcionamento de dispositios criados, e consequentemente proporcionando uma melhor qualidade de vida. Ainda é possível correlacionar o desenvolvimento socioeconômico de determinada sociedade e os índices de geração e utilização de energia, visto que sociedades mais desenvolvidas possuem maior demanda por recursos energéticos.

Não obstante, o processo de geração de energia possui grande impacto ambiental, principalmente devido às fontes de energia utilizadas. Em um primeiro momento, a sociedade começou a utilizar combustíveis naturais, como petróleo, carvão e gás natural, como fontes de energia. No entanto, a utilização de tais materiais causam grandes impacto negativos. Então, foi dado início a uma busca por fontes de energia alternativas e renováveis, visando recuzir o uso de combustíveis naturais. No presente, energias hidrocinética, eólica e solar se salientam dentre as fontes de energia alternativa, visto que sua inserção na matriz energética ocorre de forma mais atrativa.

A utilização de energias renováveis que dependem de geradores elétricos (hidrocinética, solar) necessitam de uma etapa de processamento de energia entre gerador e a rede elétrica, visando adequar níveis de tensão e frequência. Geralmente, geradores elétricos são dispositivos trifásicos, e a frequência das variáveis elétrica é diretamente relacionada à velocidade di gerador. No entanto, a velocidade rotórica, bem como níveis de tensão e corrente dos geradores elétricos são variáveis, justificando a necessidade desse estágio de processamento. Esse estágio pode ser realizado por conversores estáticos de potência, objeto de estudo da eletrônica de potência. Neste senso, existem várias alternativas para adaptar os níveis de tensão e frequência, como conversores CA-CC-CA, CA-CC-CC-CA ou CA-CA. Para operações de microgeração, os níveis de tensão e corrente são muito menores que em aplicações de alta potência, possibilitando a utilização de diferentes topologias para o processamento de energia.

Motivação

A literatura descreve diversas topologias que efetuam a compatibilidade entre sistemas AC distintos. Dentre elas, os conversores diretos de frequência (ou conversores CA-CA) efetuam o processamento sem uma etapa CC intermediária. Tais dispositivos possuem alta densidade de potência, robustez e confiabilidade. No entanto, esses conversores possuem alta complexidade, e são altamente dependentes das tecnologias dos semicondutores utilizados. Ressalta-se ainda que tais conversores são comumente utilizados em aplicações aeroespaciais, principalmentes no segmento de MEAs (More Electric Aircrafts), onde a tensão gerada pelas turbinas das embarcações variam normalmente entre $300 - 800$ Hz. Tais convesores são o objeto de estudo principal deste trabalho.

Os conversores matriciais são conversores estáticos de potência compostos por um arranjo de interruptores controlados que conectam diretamente entradas e saídas. É interessante notar que não existem restrições de frequência para as variáveis elétricas. Além disso, tais dispositivos são desprovidos de elementos armazenadores de energia, como indutores e capacitores, por não possuírem um estágio CC intermediário.

Dentre as topologias de conversores matriciais, destacam-se os conversores matriciais diretos (CMCs) e indiretos (IMCs), os quais compõem duas distintas áreas de estudo. Um dos maiores desafios é comandar os interruptores de forma que o fluxo de potência entre entrada e saída seja mantido, estabelecendo sincrinismo entre entrada–conversor e conversor–saída, objetos de estudo dessa dissertação.

Metodologia

A presente dissertação é dividada em cinco capítulos, cada um explorando um conceito diferente relacionado à operação do conversor matricial e a forma como pode ser estabelecido o sincronimsmo entre conversor e rede elétrica. Ainda são explorados resultados experimentais utilizando um protótipo.

Primeiramente, é realizado um breve estudo de topologias que podem ser utilizadas para realizar a interface entre dois sistemas CA, conforme discutido anteriormente.

O Capítulo 2 apresenta uma modelagem matemática para o conversor, utilizando modelos contínuos e discretos para representar a dinâmica do conversor matricial indireto. Ainda pe realizada uma análise estática do conversor, verificando a forma como ocorre o fluxo de potência entre entrada e saída.

Logo após, o Capítulo 3 discute diversas estratégias de modulação, demonstrando o funcionamento do conversor utilizando as estratégias mais adequadas para a aplicação desejada. As estratégias de modulação demonstradas são ainda mais exploradas no Apêndice C.

O Capítulo 4 apresenta alguns algoritmos necessários para a implementação das estratégias de modulação apresentadas no capítulo anterior, bem como métodos para estabelecer o sincronismo do conversor. Diagramas de blocos e/ou implementações utilizando FPGAs são apresentadas para elucidar a operação do conversor matricial indireto.

Finalmente, o Capítulo 5 apresenta resultados experimentais dos algoritmos propostos, bem como resultados da operação de um protótipo do conversor matricial indireto.

Três apêndices são apresentados no fim do trabalho para elucidar alguns dos conceitos utilizados no decorrer da dissertação. O Apêndice A apresenta um método para discretizar modelos contínuos utilizando espaço de estados. O Apêndice B apresenta alguns conceitos, definições e convenções, como as transformações de Clarke e Park, bem como ocmponentes de sequência. Por fim, o Apêndice C apresenta uma nálise matemática dos esquemas de modulação apresentados no Capítulo 3.

Resultados e Discussão

Os resultados experimentais do conversor são demonstrados utilizando uma implementação baseada em um FPGA. Foram implementadas estratégias de sincronismo entre entrada–conversor e conversor–saída, bem como uma estratégia de modulação apresentada durante o trabalho, visando minimizar a utilização de recursos do FPGA, bem como minimizar ruídos internos ao sistema gerados por eventuais erros numéricos e de quantização. Verificou-se que a implementação funciona de maneira adequada para a operação do conversor com potência de saída igual a aproximadamente 500 W.

Considerações Finais

O desenvolvimento de novas tecnologias de semicondutores e a busca por métodos mais eficientes de efetuar a conversão de energia entre dois sistemas CA distintos resultam em tecnologias mais complexas, como o conversor discutido no decorrer deste trabalho. As maiores vantagens da utilização do conversor estudado o maior rendimento, vida útil extendida e reduzido volume e peso. No entanto, o número de dispositivos semicondutores utilizados, bem como a complexidade dos circuitos auxiliares e a demanda por medidas de proteção contra faltas e falhas dificula a utilização do conversor estudado. Portanto, faz-se necessário o estudo do conversor apresentado, justificando assim o trabalho apresentado.

Palavras-chave: Conversores Matriciais, Estratégias de Modulação, FPGA, Sincronismo.

Abstract

A vision shared by many experts is that future communities? residential and commercial developments will be self-sufficient with respect to energy production, including micro-generation units in electricity generation power sources. The interface between mechanical parts and electric quantities is often implemented through electrical generators which employ variable electrical frequency while aiming to increase the process efficiency. In this context, the insertion of such power sources requires an energy processing stage between generator and electrical grid, which adapts amplitude and frequency levels for alternating current (AC) quantities. This work aims to study a static power converter able to process directly the AC electric quantities between two distinct AC systems without an intermediary DC stage. The main advantages of such topologies are the increased efficiency of the energy conversion and reduction of weight and volume of the power converter, while maintaining the ability to drain and inject sinusoidal currents for both AC systems. This thesis proposes a study of how to operate these power converters, as well as static and dynamic characterization of such converters. A study on some of the algorithms necessary to perform the interface between both AC systems, as well as a review on how to design and implement these algorithms and experimental results obtained through a prototype are also presented, verifying the power converter operation.

Keywords: Matrix Converters, Modulation Strategies, FPGA, Synchronism.

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LIST OF ABBREVIATIONS

DC	Direct Current
AC	Alternate Current
MEA	More Electric Aircraft
CMC	Conventional Matrix Converter
IMC	Indirect Matrix Converter
SMC	Sparse Matrix Converter
VSMC	Very Sparse Matrix Converter
BBC	Back-to-Back
THD	Total Harmonic Distortion
wTHD	Weighted Total Harmonic Distortion
FPGA	Field Programmable Gate Array
DSP	Digital Signal Processor
MOSFET	Metal Oxide Semiconductor Field Effect
IGBT	Insulated Gate Bipolar Transistor
FCS-MPC	Finite-Control-Set Model Predictive Control
VSI	Voltage Source Inverter
CSI	Current Source Inverter
SVM	Space Vector Modulation
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
HVSVM	High Voltage Space Vector Modulation
LVSVM	Low Voltage Space Vector Modulation
TLSVM	Three-Level Space Vector Modulation
HVZCS	High-Voltage Zero Current Switching
LVZCS	Low-Voltage Zero Current Switching
HVZVS	High-Voltage Zero Voltage Switching
LVZVS	Low-Voltage Zero Voltage Switching
TLZCS	Three-Level Zero Current Switching
TLZVS	Three-Level Zero Voltage Switching
CSVM	Conventional Space Vector Modulation
ISVM	Improved Space Vector Modulation

NZSVM	Non-Zero Space Vector Modulation
RPSVM	Reactive Power Space Vector Modulation
CORDIC	Coordinate Rotation Digital Computer
PLL	Phase-Locked Loop
FLL	Frequency-Locked Loop
SRF-PLL	Synchronous Reference Frame Phase Locked Loop
VCO	Voltage Controlled Oscillator
LF	Line Filter
LMS	Least Mean Squares
CLMS	Complex Least Mean Squares
ACLMS	Augmented Complex Least Mean Squares
SLE	Strictly Linear Estimator
WLE	Widely Linear Estimator
PWM	Pulse-Width Modulator
HRPWM	High Resolution Pulse-Width Modulator
FSM	Finite-State Machine
CLK	Clock of a Digital System
SiC	Silicon Carbide

LIST OF SYMBOLS

R_x^{pk}	Peak Value of a generic variable R of the x stage
$\vec{v}_x$	Three-phase vector of the x stage
ω_x	Angular frequency of the x stage
m	Modulation index
$\mathbb{I}_{n\text{x}n}$	n-order identity matrix
$\mathbb{O}_{m\text{x}n}$	mxn matrix filled with zeros
$[\mathbb{T}_M]$	Matrix converter switching matrix
φ_x	Angle of a sinusoidal variable pertaining to x
θ_x	Estimated angle
X_{16}	Number in Hexadecimal base
X_2	Number in Binary base
j	$\sqrt{-1}$
$\Re\{\bullet\}$	Real part of a complex valued number
$\Im\{\bullet\}$	Imaginary part of a complex valued number
$\{\bullet\}^T$	Transpose Operator
$\{\bullet\}^H$	Hermitian Operator

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1 INTRODUCTION

1.1 CONTEXTUALIZATION

Since ancient times, humanity uses energy sources available to facilitate the execution of frequent tasks. In the current period of time, electricity is an indispensable resource to the modern society which guarantees the functionality of created devices, leading to a better quality of life. It is possible to correlate the socioeconomic development of a certain society and electricity generation and utilization indexes, whereas more developed nations possesses a higher energy demand.

Nonetheless, the energy generation process has a great environmental impact, in most part due to the employed energy inputs. In a first moment, society started using natural fuels, like petroleum, coal and natural gases, as energy inputs. However, the utilization of such materials causes heavy negative environmental impacts. A search for alternative and renewable energy sources was started, while aiming to reduce the use of natural fuels. Presently, hydrokinetic, eolic and solar energy stand out among such energy alternatives, as their energetic matrix insertion happen to be more attractive.

The utilization of renewable energy sources which depend on electric generators (hydrokinetic, solar) needs an energy processing stage between generator and electric grid, aiming to adequate voltage and frequency levels. Generally, electric generators are three-phase devices, and the frequency of electrical quantities are directly related to the rotor velocity of the generator. However, the rotor velocity, as well as current and voltage levels of a generator are variables, which justifies the need for a processing stage.

There is a need for devices which accomplish this energy processing stage. Such processing can be performed by static power converter, object of study of power electronics. Such devices aim to maximize the process efficiency [3, 4]. In this sense, there are many alternatives which adapt voltage and frequency levels, such as AC-DC-AC, AC-DC-DC-AC or AC-AC power converters. For micro-generation operation, the voltage and current levels are much lower than in high-power applications, as many different topologies can be used to process power from the generator.

In the literature, there are many static power converters topologies which accomplish the compatibility between distinct AC systems. Amongst them are the DC-AC-DC, which possesses an intermediary direct current level, which helps decoupling the converter input and output. Currently, this is the most used topology for grid-tied applications. Another alternative is the AC-DC-DC-AC converters, which possesses two different direct current stages, and are used when there is a high voltage level differences between both AC stages, obtaining a higher efficiency, as a DC-AC-DC converter would operate in an undesirable point of operation.

Finally, the AC-AC converters do not posses an intermediary DC stage. These devices have a high power density, robustness and reliability. However, such converters have a high complexity and are heavily dependent on employed semiconductor technology. Usually, the matrix converter is employed in the More Electric Aircraft (MEA) industry segment to process the power generated from aircraft turbines, which usually generate voltages with variable frequency in a range of 300 – 800 Hz. These converters are the main objects of study of this work.

1.2 MOTIVATION

The Matrix Converter is a static power converter composed mainly a controlled switch arrangement which directly connects three-phase sources and loads [5, 6]. On of the important points to be noted is that there are no frequency restriction for voltage and current electrical quantities, such as input and output voltages and currents [5]. Also, such converters do not possess an intermediary DC stage, disregarding the utilization of energy storing devices, such as capacitors and inductors.

Among the matrix converter topologies, the direct (or conventional) matrix converter (CMC) [7] and the indirect matrix converter (IMC) [6, 1] structures compose two different branches of study. The CMC traditionally possesses nine four-quadrant switches, usually resulting in a number of eighteen switches and diodes for the switch realization.

The IMC topology has many different implementations, the traditional IMC [6, 1], the Sparse Matrix Converter [6], the Very Sparse Matrix Converter (VSMC) [8] and the Ultra Sparse Matrix Converter (USMC) [9]. The IMC has the same number of switches of the CMC, while the VSMC uses a different switch realization which reduces the number of switches and the SMC and USMC possesses a simpler implementation, substituting some switches for diodes while sacrificing the possibility of operating with a bidirectional power flux.

One of the greatest challenges of the topology is the way to command the switches and the control of the structure power flow, as well as the synchronism of the converter, which are the object of study of this work.

1.3 OBJECTIVES

The objective of this work are described in the following topics:

- Present a mathematical analysis of the Indirect Matrix Converter;
- Describe and compare different modulation techniques for the IMC;
- Study and present algorithms useful for the operation of the IMC for grid-tied applications;
- Implement algorithms in an FPGA useful for the correct operation of the Matrix Converter;
- Validate through experimental results a SMC using the algorithms presented in this work.

1.4 LITERATURE REVIEW

According to [4], the most desired characteristics of a static power converter interfacing AC voltages and currents (AC-DC-AC, AC-DC-DC-AC, AC-AC) are:

- Low-cost and compact power circuit;
- Sintetization of the output voltage with arbitrary voltage and frequency;
- Input and output currents with a sinusoidal format, i.e., with a low harmonic distortion;
- Operation with a high power factor for any load condition;
- Bidirectional power flux and regeneration capabilities.

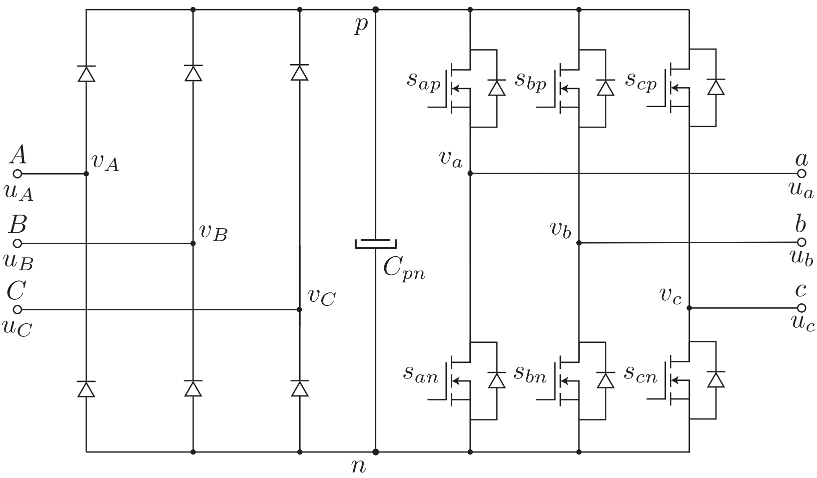


Figure 1.1 – Unidirectional power converter with a diode bridge rectifier, widely used in the industry for variable frequency motor drives.

Considering the ideal characteristics presented previously, the matrix converter is highly attractive due to the efficiency maximization, as well as weight and volume reduction [4, 10].

A unidirectional power converter configuration illustrated in Figure 1.1 has great acceptability in the industry for motor drives, as it presents low cost and high robustness. However, the structure needs a large energy storage device, which has a large volume and weight and has a smaller life cycle if compared to the other components and degrades the converter efficiency. Another problem is related to the degradation of the energy quality, as presented in [11, 12, 13], as the structure has a lower power factor if compared to the other reviewed

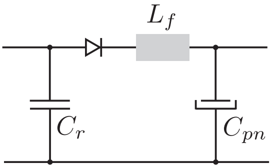


Figure 1.2 – Unidirectional power converter passive power factor correction structure, widely used in low power motor drive applications.

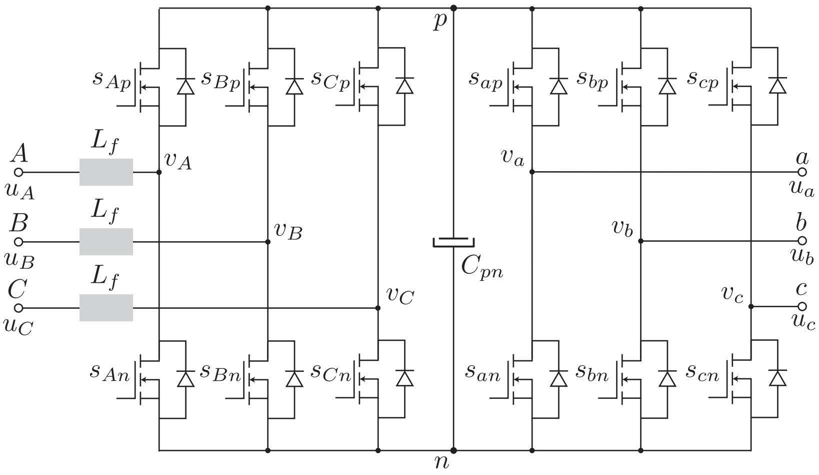


Figure 1.3 – Bidirectional Voltage Link Back-to-Back Converter (VL-BBC).

structures.

There are some passive ways to increase the power factor, such as using multi-pulse diode rectifiers or introducing structures such as the one illustrated in Figure 1.2, which is used in low power applications and hinders the converter efficiency. However, such converters do not present sinusoidal currents for both AC systems, and should not be used for grid-tied applications. Also, the use of this type of topology in applications which demands reversible power flow, such as lifts, power trains and wind power converter systems is not feasible.

An alternative to the previously presented topology is the Back-to Back connection (BBC) [14]. In this case, two identical power converters are connected through a DC-link created by a large energy storage device, as shown in Figure 1.3. This structure has a bidirectional power flux and has a high power factor. A drawback is that the problems with large energy storage devices still persists, and the structure has a higher volume, weight and cost if compared to the previous structure. This structure is widely used in grid-tied applications.

The main characteristic of matrix converters is the absence of a energy storage device, i.e., the absence of a DC-link between input and output, as it directly connects input and output. The origin of the matrix converter concept can be dated from the end of the 1960s to

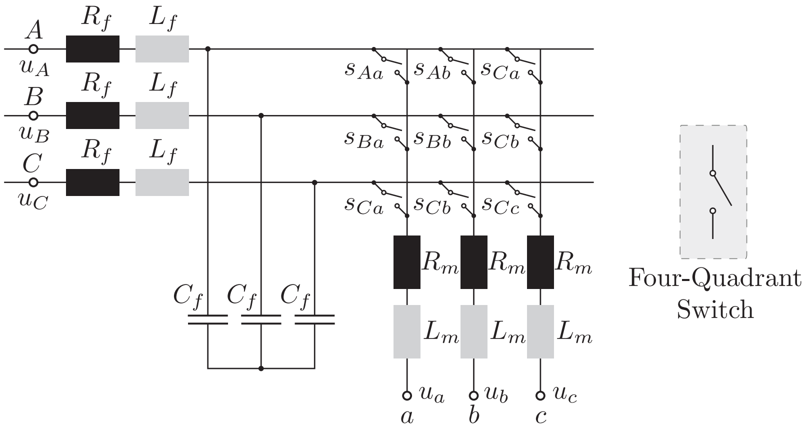


Figure 1.4 – Conventional (or Direct) Matrix Converter topology employing four-quadrant switches.

the beginning of the 1970s formulating the CMC topology. One of the earliest materials on matrix converters can be found in [15]. However, the technology at the time limited the operation of the converter. The converter name is due to the Switching Matrix which describes the output as a function of the input and the switching matrix, as seen in Chapter 2.

The CMC topology, illustrated by Figure 1.4, is composed by nine four-quadrant switches with possible implementations illustrated in Figure 1.5. A complete analysis of the conventional matrix converter with different switch realizations is presented in [16].

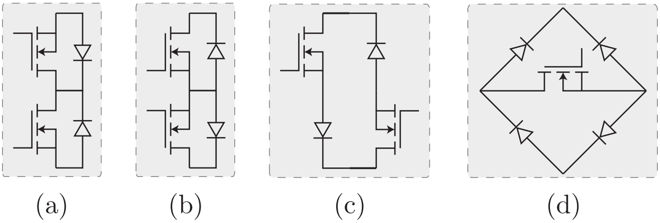


Figure 1.5 – Four ways of implementing a four-quadrant switch, with (b) presenting an advantage in the gate-driver construction.

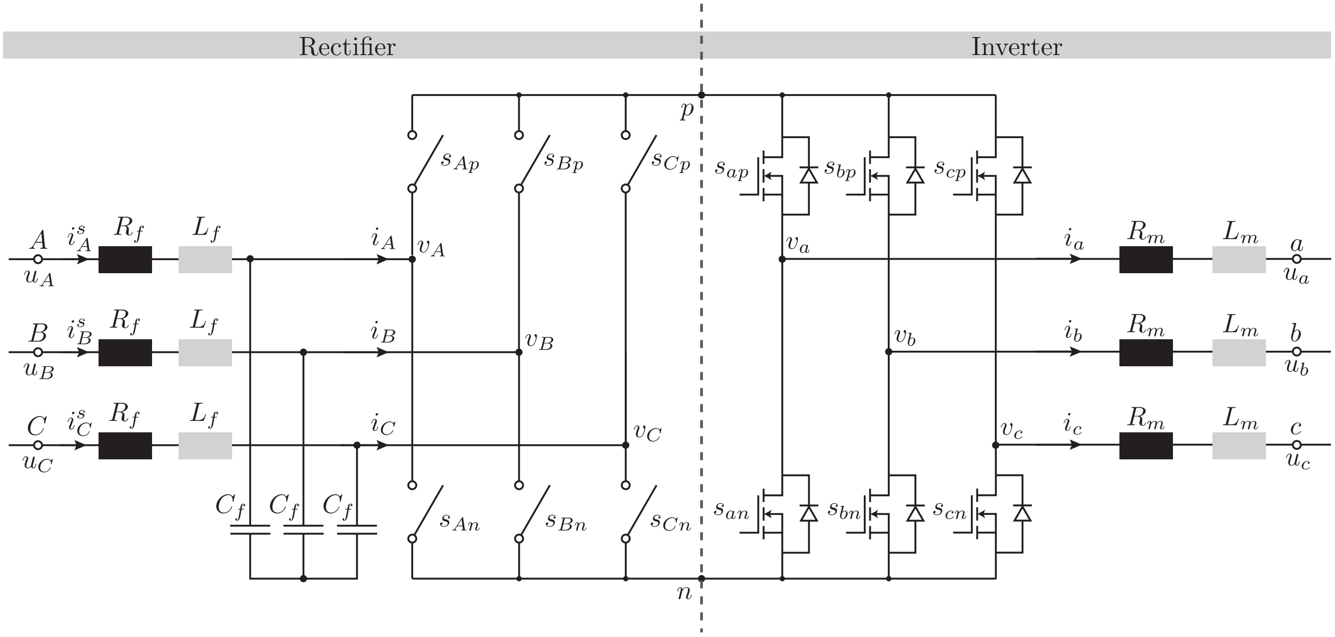

Rectifier
Inverter
A
u_A
i_A^s
R_f
L_f
B
u_B
i_B^s
C
u_C
i_C^s
C_f
C_f
C_f
i_A
i_B
i_C
v_A
v_B
v_C
s_{Ap}
s_{Bp}
s_{Cp}
s_{An}
s_{Bn}
s_{Cn}
p
n
s_{ap}
s_{bp}
s_{cp}
s_{an}
s_{bn}
s_{cn}
v_a
v_b
v_c
i_a
i_b
i_c
R_m
L_m
a
u_a
b
u_b
c
u_c

Figure 1.6 – Indirect Matrix Converter (IMC) topology, composed by six four-quadrant switches and six two-quadrant switches.

A carrier-based modulation for the CMC was first introduced by Venturini in [17], which posses sinusoidal inputs and outputs and has a limited gain of 0.5. An optimized carrier-based modulation which injects the 3^{rd} harmonic might elevate the gain to 0.866 [7, 18], although harder to implement. The space vector modulation for the CMC has approximately the same gain as the 3^{rd} harmonic injection, but functions for different types of loads while possessing a lower THD [1].

An issue inherent to the topology is the need to perform multi-step commutation to avoid inter-phase short-circuits. This elevates the complexity of the implementation, since an auxiliary hardware is needed to avoid such problems.

An alternative to the previously presented topology is the Indirect Matrix Converter (IMC), as is illustrated in Figure 1.6. An inherent characteristic of the IMC is the decoupling between rectifier and inverter stage, which enables different modulation strategies with reduced switching losses.

The IMC topology allows the insertion of a Delta switch in the inverter stage, which reduces conduction losses and further elevating the converter efficiency, reaching efficiency values over 98% according to [1].

1.5 METHODOLOGY AND ORGANIZATIONAL STRUCTURE

The present work is divided into five chapters, each approaching a different concept related to the operation of an IMC, and a final chapter reuniting experimental results.

First, Chapter 2 presents a mathematical model for the converter, using both continuous and discrete models to model the converter dynamic. A static analysis is then introduced, analyzing the operation of each converter stage and the power flow between input and output.

Next, Chapter 3 discusses different modulation strategies and presents four different space vector modulation schemes, as well as a comparison between each scheme. The modulation strategies are based in the static analysis previously presented, and is further explored in Appendix C.

Chapter 4 review some algorithms which are useful for implementing the modulation schemes presented previously. Block diagrams of the algorithms and/or FPGA implementations are presented to further elucidate the process of the IMC operation.

Finally, Chapter 5 presents some experimental results of the proposed algorithms as well as the operation of an Indirect Matrix Converter.

Three appendix were presented at the end of this work, which are useful to elucidate some of the concepts used throughout this thesis. Appendix A presents a method do discretize continuous state-space models, while Appendix B presents some concepts, definitions and conventions, like Clarke and Park transformations and sequence components. Appendix C presents a detailed mathematical analysis of the modulation schemes presented in Chapter 3.

2 MATRIX CONVERTER MODELLING

2.1 INTRODUCTION

This chapter describes a mathematical analysis of the indirect matrix converter shown in Figure 1.6. The topology can be divided into two different stages. The rectifier stage is composed by twelve four-quadrant switches and possesses the same structure as a CSI, whereas the inverter stage is composed by two quadrant switches in a three-phase bridge configuration similar to a VSI.

A fundamental characteristic of the topology is the possibility to operate with power flux reversibility, i.e, the converter can operate as a voltage *step-down* (*Buck* mode) or as a voltage *step-up* (*Boost* mode), given that the VSI and CSI are also bidirectional. This trait can be explored in different applications, such as the following:

- *Buck* mode (Voltage *step-down*): The converter is supplied by a voltage source, and the load possesses a current source profile. This operation mode is widely used in variable voltage motor drives, as demonstrated in [19, 20, 21].

- *Boost* mode (Voltage *step-up*): As opposed to the previous mode, the converter is supplied by a current source, and the load possesses a voltage source profile. This mode can be used in grid tied applications, where the power flux flows from a variable frequency generator to the grid [1, 22, 23].

Contrary to the CMC, the IMC is called indirect due to the decoupling between rectifier and inverter switching states, forming a bus composed by nodes p and n between both stages, which is commonly referred as a virtual DC-link. The rectifier stage is connected to a voltage source, in this case a capacitor C_f, while the inverter stage is connected to a current source, in this case the inductor L_m. The *high-side* is defined as the input of the LC filter connected to the rectifier stage, while the *low-side* is defined as the output of the L filter connected to the inverter stage.

For modelling purposes, an ideal model will be adopted for each switch, but prohibited states generated by the switches will be taken into account, since the virtual DC-link voltage must be positive valued to avoid shot-circuits in the inverter stage. A simplified topology using ideal switches is presented in Figure 2.1.

A *Buck* mode operation will be adopted for modelling the converter, although the obtained model is valid for both modes. Therefore, the *high-side* will be referred as the input, while the *low-side* will be referred as the output. A continuous and a discrete dynamic model, as well as a static model will be presented in the following sections.

2.2 SWITCHED MODEL

In this section, a dynamic switched model for the indirect matrix converter is presented. This model consider ideal switches which possess two distinct states: enabled and disabled. The subscript r henceforth denotes variables pertaining to the rectifier stage, and the subscript i to variables belonging to the inverter stage.

The *high-side* and the *low-side* voltage and current vectors can be defined by (2.1) and (2.2), respectively.

$$\begin{aligned} \vec{v}_r &= \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^T \\ \vec{i}_r &= \begin{bmatrix} i_A & i_B & i_C \end{bmatrix}^T \end{aligned} \tag{2.1}$$

$$\begin{aligned} \vec{v}_i &= \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T \\ \vec{i}_i &= \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \end{aligned} \tag{2.2}$$

Similarly, the voltage and current input vectors and the voltage output vector can be defined, as described by (2.3) and (2.4), respectively.

$$\begin{aligned} \vec{u}_r &= \begin{bmatrix} u_A & u_B & u_C \end{bmatrix}^T \\ \vec{i}_r^{\,s} &= \begin{bmatrix} i_A^s & i_B^s & i_C^s \end{bmatrix}^T \end{aligned} \tag{2.3}$$

$$\vec{u}_i = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \tag{2.4}$$

The indirect matrix converter switched model previously presented possesses twelve ideal switches. According to the switched model presented in Figure 2.1, a switching function s_{ij} can be expressed for the state of each switch S_{ij}, as described by (2.5), where $i \in \{A, B, C, a, b, c\}$ and $j \in \{p, n\}$.

$$s_{ij} = \begin{cases} 1, & \text{Switch } S_{ij} \text{ enabled} \\ 0, & \text{Switch } S_{ij} \text{ disabled.} \end{cases} \tag{2.5}$$

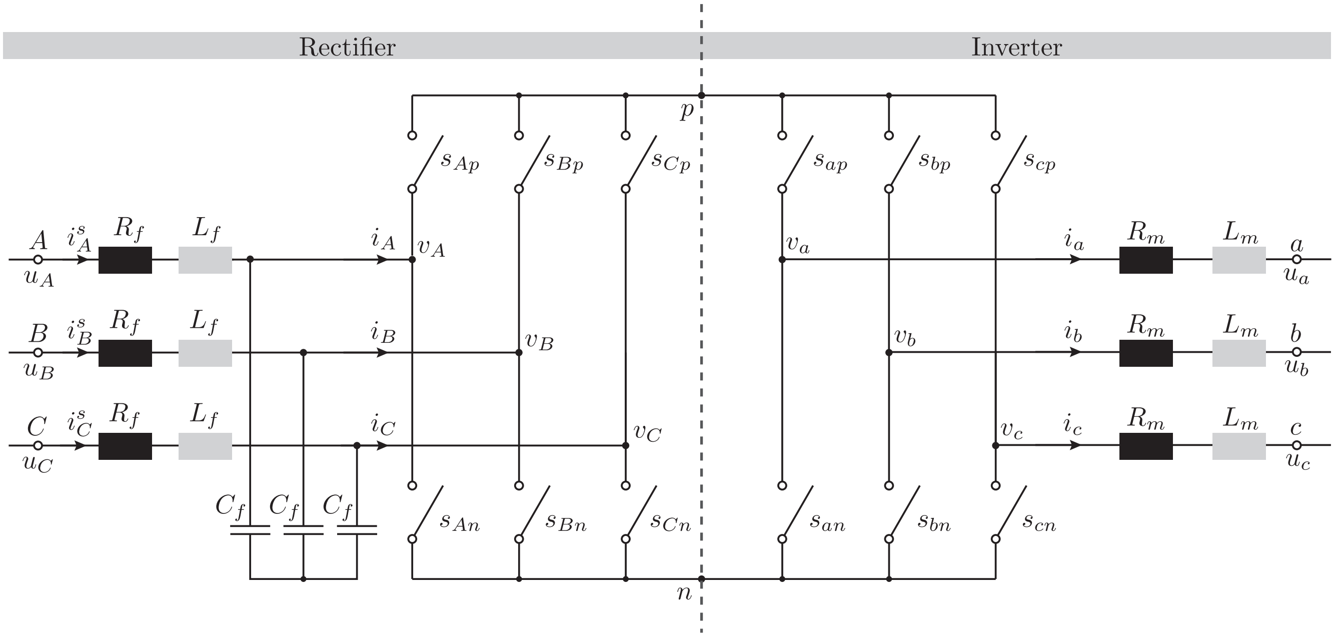

Rectifier
Inverter
A
u_A
i_A^s
B
u_B
i_B^s
C
u_C
i_C^s
R_f
L_f
C_f
i_A
i_B
i_C
v_A
v_B
v_C
s_{Ap}
s_{Bp}
s_{Cp}
s_{An}
s_{Bn}
s_{Cn}
p
n
s_{ap}
s_{bp}
s_{cp}
s_{an}
s_{bn}
s_{cn}
v_a
v_b
v_c
i_a
i_b
i_c
R_m
L_m
a
u_a
b
u_b
c
u_c

Figure 2.1 – Inverse matrix converter switched model, composed by twelve ideal switches, as well as filtering elements. The *high-side* voltage is defined by $\{u_A, u_B, u_C\}$ and the *low-side* voltage is defined by $\{u_a, u_b, u_c\}$.

Therefore, it is possible to obtain switching vectors for the rectifier and inverter stage, as defined by (2.6) and (2.7), respectively.

$$[\mathbf{s}_r] = \begin{bmatrix} s_{Ap} - s_{An} & s_{Bp} - s_{Bn} & s_{Cp} - s_{Cn} \end{bmatrix} \tag{2.6}$$

$$[\mathbf{s}_i] = \begin{bmatrix} s_{ap} - s_{an} & s_{bp} - s_{bn} & s_{cp} - s_{cn} \end{bmatrix} \tag{2.7}$$

For simplicity, the switching vectors can be redefined as in (2.8) and (2.9), where $s_i \in (-1, 0, 1)$.

$$[\mathbf{s}_r] = \begin{bmatrix} s_A & s_B & s_C \end{bmatrix} \tag{2.8}$$

$$[\mathbf{s}_i] = \begin{bmatrix} s_a & s_b & s_c \end{bmatrix} \tag{2.9}$$

Consequently, the virtual DC-link voltage and current can be described as a function of the switching vectors, as shown in (2.10).

$$\begin{aligned} u_{pn} &= [\mathbf{s}_r]\,\vec{v}_r \\ i_{pn} &= [\mathbf{s}_i]\,\vec{i}_i \end{aligned} \tag{2.10}$$

Similarly, the the *low-side* voltage and the *high-side* current vectors can be expresse by (2.11) and (2.12).

$$\vec{v}_i = [\mathbf{s}_r]^T\, u_{pn} \tag{2.11}$$

$$\vec{i}_r = [\mathbf{s}_{ABC}]^T\, i_{pn} \tag{2.12}$$

The *low-side* voltage and the *high-side* current vectors can be expressed in terms of the switching vectors pertaining to both rectifier and inverter stages by substituting (2.10) in (2.11) and (2.12), according to (2.13) and (2.14).

$$\vec{v}_i = [\mathbf{s}_i]^T\,[\mathbf{s}_r]\,\vec{v}_r \tag{2.13}$$

$$\vec{i}_r = [\mathbf{s}_r]^T\,[\mathbf{s}_i]\,\vec{i}_i \tag{2.14}$$

It is possible to obtain a switched transformation matrix for the indirect matrix converter, which directly relates voltage and current input and output, defined by (2.15).

$$[\mathbb{T}_M] = [\mathbf{s}_i]^T [\mathbf{s}_r] = \begin{bmatrix} s_a s_A & s_a s_B & s_a s_C \\ s_b s_A & s_b s_B & s_b s_C \\ s_c s_A & s_c s_B & s_c s_C \end{bmatrix} \tag{2.15}$$

Therefore, the equations for *low-side* voltage and the *high-side* current described in (2.13) and (2.14) can be rewritten as (2.16) and (2.17), respectively.

$$\vec{v}_i = [\mathbb{T}_M]\, \vec{v}_r \tag{2.16}$$

$$\vec{i}_r = [\mathbb{T}_M]^T \vec{i}_i \tag{2.17}$$

The modelling can be divided between the rectifier and inverter stages. Since equations (2.16) and (2.17) describe a relation between the two stages, it is possible to simplify the switched model shown in Figure 2.1 using controlled voltage and current sources, as illustrated in Figure 2.2.

Therefore, the system can be described by two separated state-space representation. The output voltages $\{u_a, u_b, u_c\}$ can be described according to the different load characteristics. For example, if a motor is connected to the *low-side*, its voltage equations can be coupled into the model. For a resistive load, the resistance value can be grouped with R_m and the voltage vector $\vec{u}_i$ is null valued.

Since the rectifier stage voltage vector $\vec{v}_r$ and the inverter stage current vector $\vec{i}_i$ are linearly dependant, two new switching matrices can be defined according to equations (2.18) and (2.19), resulting in (2.20) and (2.21). Rectifier voltage v_C and inverter current i_c can be expressed as a linear combination of the expressed vectors, hence the suppression in the new set of equations.

$$[\mathbb{T}_r] = \begin{bmatrix} s_a s_A - s_a s_C & s_a s_B - s_a s_C \\ s_b s_A - s_b s_C & s_b s_B - s_b s_C \\ s_c s_A - s_c s_C & s_c s_B - s_c s_C \end{bmatrix} \tag{2.18}$$

$$[\mathbb{T}_i] = \begin{bmatrix} s_a s_A - s_c s_A & s_b s_A - s_c s_A \\ s_a s_B - s_c s_B & s_b s_B - s_c s_B \end{bmatrix} \tag{2.19}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = [\mathbb{T}_r] \begin{bmatrix} v_A \\ v_B \end{bmatrix} \tag{2.20}$$

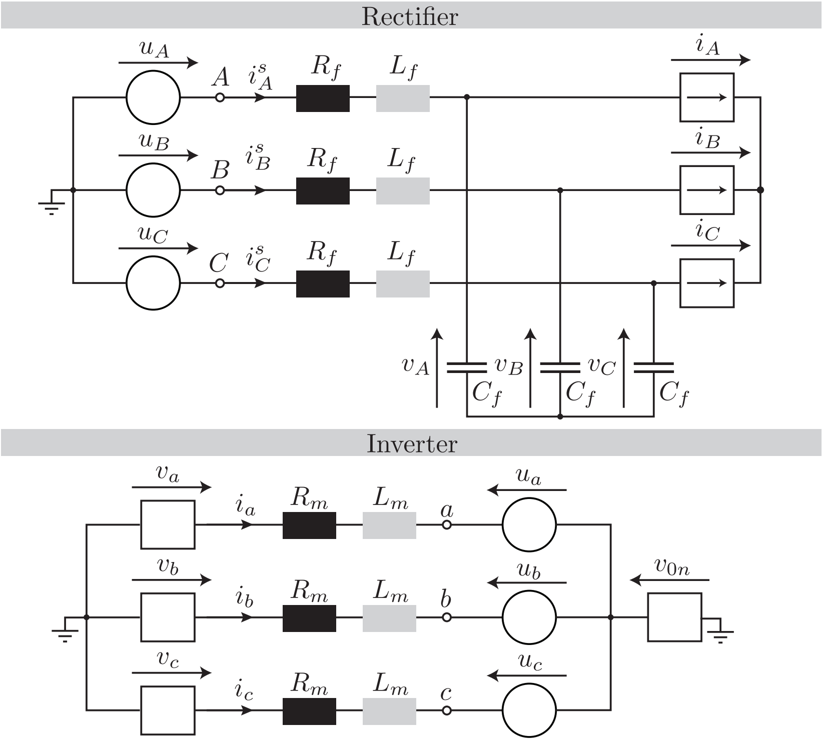

Rectifier
u_A
A
i_A^s
R_f
L_f
i_A
u_B
B
i_B^s
R_f
L_f
i_B
u_C
C
i_C^s
R_f
L_f
i_C
v_A
C_f
v_B
C_f
v_C
C_f
Inverter
v_a
i_a
R_m
L_m
a
u_a
v_b
i_b
R_m
L_m
b
u_b
v_{0n}
v_c
i_c
R_m
L_m
c
u_c

Figure 2.2 – Switched model circuit. The switched transformation matrix describes the coupling between both rectifier and inverter stages.

$$\begin{bmatrix} i_A \\ i_B \end{bmatrix} = [\mathbb{T}_i] \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{2.21}$$

2.2.1 Rectifier Stage

The rectifier stage can be modelled as a fourth order system with three inputs and two state versus inputs. Since the inputs versus states given by the controlled current sources are coupled with the inverter stage, they are separated for a partial representation of the system, resulting in a time invariant system representation. The chosen state-space state variables are shown in (2.22), and the stage inputs are described by (2.23) and the state versus input vector is demonstrated in (2.24).

$$\mathbf{x}_r = \begin{bmatrix} i_A^s & i_B^s & v_A & v_B \end{bmatrix}^T \tag{2.22}$$

$$\mathbf{u}_r = \vec{u}_r = \begin{bmatrix} u_A & u_B & u_C \end{bmatrix}^T \tag{2.23}$$

$$\mathbf{w}_r = \begin{bmatrix} i_A & i_B \end{bmatrix}^T \tag{2.24}$$

From the circuit shown in Figure 2.2, it is possible to obtain an expression for the inductor L_f voltages for phases pertaining to the set $\{A, B\}$, as demonstrated by (2.25).

$$\begin{bmatrix} v_{L_f,A} \\ v_{L_f,B} \end{bmatrix} = \begin{bmatrix} u_{AB} \\ u_{BC} \end{bmatrix} - \begin{bmatrix} v_{AB} \\ v_{BC} \end{bmatrix} - R_f \begin{bmatrix} i_A^s \\ i_B^s \end{bmatrix} + R_f \begin{bmatrix} i_B^s \\ i_C^s \end{bmatrix} + \begin{bmatrix} v_{L_f,B} \\ v_{L_f,C} \end{bmatrix} \tag{2.25}$$

Similarly, it is possible to obtain an expression for the capacitor C_f current, according to (2.26).

$$\vec{i}_{C_f,r} = \vec{i}_r^s - \vec{i}_r \tag{2.26}$$

From the circuit shown in Figure 2.2, it is possible to conclude that some voltages and currents of magnetic devices are linearly dependent. Such dependancy is demonstrated in (2.27).

$$\begin{aligned} i_C^s &= -i_A^s - i_B^s \\ i_C &= -i_A - i_B \\ v_C &= -v_A - v_B \end{aligned} \tag{2.27}$$

Therefore, the rectifier stage circuit can be expressed by the state-space model described by (2.28), with state-space matrices defined by (2.29).

$$\dot{\mathbf{x}}_r = [\mathbf{A}_r]\,\mathbf{x}_r + [\mathbf{B}_r]\,\mathbf{u}_r + [\mathbf{E}_r]\,\mathbf{w}_r \tag{2.28}$$

$$
\begin{aligned}
[\mathbf{A}_r] &= \begin{bmatrix} -\frac{R_f}{L_f}\mathbb{I}_{2\text{x}2} & -\frac{1}{L_f}\mathbb{I}_{2\text{x}2} \\ \frac{1}{C_f}\mathbb{I}_{2\text{x}2} & \mathbb{O}_{2x2} \end{bmatrix} \\
[\mathbf{B}_r] &= \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \frac{1}{3L_f} \\
[\mathbf{E}_r] &= \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{bmatrix} \frac{1}{C_f}
\end{aligned}
\tag{2.29}
$$

2.2.2 Inverter Stage

Similarly to the methodology previously presented, a circuit representing the inverter stage is also presented in Figure 2.2. Differently from the rectifier stage, the common-mode voltage v_{0n} is strongly present, according to equation (2.30), resulting in a non-null valued instantaneous common-mode voltage generated by the modulated inverter voltage vector $\vec{v}_i$.

$$
v_{0n} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \end{bmatrix}(\vec{v}_i - \vec{u}_i) \tag{2.30}
$$

Furthermore, the rectifier stage can be modelled as a second order system possessing three inputs and three state versus inputs, which are coupled with the rectifier stage as shown previously. The chosen state-space state variables and stage input vector are described by (2.31) and (2.32), respectively, while the state versus input vector is shown in (2.33).

$$
\mathbf{x}_i = \begin{bmatrix} i_a & i_b \end{bmatrix}^T \tag{2.31}
$$

$$
\mathbf{u}_i = \vec{u}_i = \begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T \tag{2.32}
$$

$$
\mathbf{w}_i = \vec{v}_i = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T \tag{2.33}
$$

The inductor voltage can be expressed by (2.34).

$$\begin{aligned}\begin{bmatrix} v_{L_m,a} \\ v_{L_m,b} \end{bmatrix} &= \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}(\vec{v}_i - \vec{u}_i) - R_m \begin{bmatrix} i_a - i_b \\ i_b - i_c \end{bmatrix} \\ &+ \begin{bmatrix} v_{L_m,b} \\ v_{L_m,c} \end{bmatrix}\end{aligned} \tag{2.34}$$

Furthermore, the phase c current can be expressed as a linear combination of the currents pertaining to the set $\{a, b\}$, according to equation.

$$i_c = -i_a - i_b \tag{2.35}$$

Therefore, the inverter stage state-space model can be described by (2.36), with state-space matrices defined by (2.37).

$$\dot{\mathbf{x}}_i = [\mathbf{A}_i]\,\mathbf{x}_i + [\mathbf{B}_i]\,\mathbf{u}_i + [\mathbf{E}_i]\,\mathbf{w}_i \tag{2.36}$$

$$\begin{aligned}[\mathbf{A}_i] &= -\frac{R_m}{L_m}\mathbb{I}_{\text{2x2}} \\ [\mathbf{B}_i] &= \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}\frac{1}{3L_m} \\ [\mathbf{E}_i] &= \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}\frac{1}{3L_m}\end{aligned} \tag{2.37}$$

2.2.3 Complete Model

Since both rectifier and inverter stage models are coupled by the switched transformation matrix defined in (2.20) and (2.21). The rectifier and inverter state equations can be rewritten according to (2.39), with $[\mathbb{T}_r']$ defined in (2.40).

$$\dot{\mathbf{x}}_r = \begin{bmatrix} -\frac{R_f}{L_f}\mathbb{I}_{\text{2x2}} & -\frac{1}{L_f}\mathbb{I}_{\text{2x2}} & \mathbb{O}_{2x2} \\ \frac{1}{C_f}\mathbb{I}_{\text{2x2}} & \mathbb{O}_{2x2} & -\frac{1}{C_f}\mathbb{T}_i \end{bmatrix}\begin{bmatrix} \mathbf{x}_r \\ \mathbf{x}_i \end{bmatrix} \tag{2.38}$$

$$\dot{\mathbf{x}}_i = \begin{bmatrix} \mathbb{O}_{2x2} & \frac{1}{3L_m}\mathbb{T}_r' & -\frac{R_m}{L_m}\mathbb{I}_{\text{2x2}} \end{bmatrix}\begin{bmatrix} \mathbf{x}_r \\ \mathbf{x}_i \end{bmatrix} \tag{2.39}$$

$$\mathbb{T}_r' = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}\mathbb{T}_r \tag{2.40}$$

The complete state variables vector is a combination of both stages. The state-space state vector, input and disturbance are described by (2.41) and (2.42), respectively. The index t indicates variables pertaining to the complete model.

$$\mathbf{x}_t = \begin{bmatrix} \mathbf{x}_r \\ \mathbf{x}_i \end{bmatrix} = \begin{bmatrix} i_A^s & i_B^s & v_A & v_B & i_a & i_b \end{bmatrix}^T \tag{2.41}$$

$$\mathbf{u}_t = \begin{bmatrix} \vec{u}_r \\ \vec{u}_i \end{bmatrix} = \begin{bmatrix} u_A & u_B & u_C & u_a & u_b & u_c \end{bmatrix}^T \tag{2.42}$$

It is possible to combine the systems described in (2.28) and (2.36), resulting in a complete system depicted by (2.43). The state-space system matrices are shown in (2.44).

$$\dot{\mathbf{x}}_t = [\mathbf{A}_t]\,\mathbf{x}_t + [\mathbf{B}_t]\,\mathbf{u}_t \tag{2.43}$$

$$\begin{aligned}
[\mathbf{A}_t] &= \begin{bmatrix} -\frac{R_f}{L_f}\mathbb{I}_{2\text{x}2} & -\frac{1}{L_f}\mathbb{I}_{2\text{x}2} & \mathbb{O}_{2x2} \\ \frac{1}{C_f}\mathbb{I}_{2\text{x}2} & \mathbb{O}_{2x2} & -\frac{1}{C_f}\mathbb{T}_i \\ \mathbb{O}_{2x2} & \frac{1}{3L_m}\mathbb{T}'_r & -\frac{R_m}{L_m}\mathbb{I}_{2\text{x}2} \end{bmatrix} \\
[\mathbf{B}_t] &= \frac{1}{3}\begin{bmatrix} \frac{2}{L_f} & -\frac{1}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\ -\frac{1}{L_f} & \frac{2}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{2}{L_m} & \frac{1}{L_m} & \frac{1}{L_m} \\ 0 & 0 & 0 & \frac{1}{L_m} & -\frac{2}{L_m} & \frac{1}{L_m} \end{bmatrix}
\end{aligned} \tag{2.44}$$

2.2.4 Discrete Switched Model

For a discrete time representation, a discrete time switched model can be obtained by using a discretization method, be it *Euler*, *Tustin* or *Runge-Kutta*, on the continuous state-space model.

This model is important for many different applications, such as *hardware-in-the-loop* simulations and some control strategies, such as the Finite Control Set Model Predictive Control (FCS-MPC). The FCS-MPC uses a discrete state-space representation to estimate the state variables for all the possible combination of switching states, and uses a cost function to choose the next switching state based on the result of this function [19].

Assuming a sampling period T_a, the model is valid for time instants which are integer multiples of this sampling period, here denoted as nT_a. The converter discrete switched model equation can then be expressed by (2.45).

$$\mathbf{x}_t\left(n+1\right) = \left[\mathbf{G}_t\right]\mathbf{x}_t\left(n\right) + \left[\mathbf{H}_t\right]\mathbf{u}_t\left(n\right) \tag{2.45}$$

A simple method for discretizing the system is the *Backward Euler* method, presented on Appendix A. However, the discussed method is only valid for time invariant systems. Fortunately, the separated system described by equations (2.28) and (2.36) is time-invariant, as the time-variant switching matrix which couples both systems is not explicitly present. This method was chosen due to its low computational-burden for real-time applications.

Therefore, it is possible to obtain a new set of equations, given by (2.46), which describes a discretized state-space model for the indirect matrix converter. Equation (2.47) shows the system matrices, according to the method proposed on Appendix A, and (2.48) couples both systems.

$$\begin{cases}\mathbf{x}_r\left(n+1\right) = \left[\mathbf{G}_r\right]\mathbf{x}_r\left(n\right) + \left[\mathbf{H}_r\right]\mathbf{u}_r\left(n\right) + \left[\mathbf{R}_r\right]\mathbf{w}_r\left(n\right)\\ \mathbf{x}_i\left(n+1\right) = \left[\mathbf{G}_i\right]\mathbf{x}_i\left(n\right) + \left[\mathbf{H}_i\right]\mathbf{u}_i\left(n\right) + \left[\mathbf{R}_i\right]\mathbf{w}_i\left(n\right)\end{cases} \tag{2.46}$$

$$\begin{gathered}\left[\mathbf{G}_r\right] = e^{\left[\mathbf{A}_r\right]T_a}, \quad \left[\mathbf{G}_i\right] = e^{\left[\mathbf{A}_i\right]T_a}\\ \left[\mathbf{H}_r\right] = \left[\mathbf{A}_r\right]^{-1}\left(\left[\mathbf{G}_r\right] - \mathbb{I}_{6\text{x}6}\right)\left[\mathbf{B}_r\right]\\ \left[\mathbf{H}_i\right] = \left[\mathbf{A}_i\right]^{-1}\left(\left[\mathbf{G}_i\right] - \mathbb{I}_{3\text{x}3}\right)\left[\mathbf{B}_i\right]\\ \left[\mathbf{R}_r\right] = \left[\mathbf{A}_r\right]^{-1}\left(\left[\mathbf{G}_r\right] - \mathbb{I}_{6\text{x}6}\right)\left[\mathbf{E}_r\right]\\ \left[\mathbf{R}_i\right] = \left[\mathbf{A}_i\right]^{-1}\left(\left[\mathbf{G}_i\right] - \mathbb{I}_{3\text{x}3}\right)\left[\mathbf{E}_i\right]\end{gathered} \tag{2.47}$$

$$\begin{gathered}\mathbf{w}_r\left(n\right) = \left[\mathbb{T}_i\left(n\right)\right]\mathbf{x}_i\left(n\right)\\ \mathbf{w}_i\left(n\right) = \begin{bmatrix}\mathbb{O}_{3\text{x}2} & \mathbb{T}_r\left(n\right)\end{bmatrix}\mathbf{x}_r\left(n\right)\end{gathered} \tag{2.48}$$

2.3 AVERAGED MODEL

From the switched state-space model, it is possible to obtain an averaged model using results presented in Appendix B. An averaged switching function can be defined by (2.49), where T_s is the switching time and $i \in \{A, B, C, a, b, c\}$. It is important to notice that the averaged switching function is bounded, as $\delta_i \in [-1, 1]$.

$$\delta_i = \langle s_{ip} - s_{in} \rangle_{T_s} = \int_t^{t+T_s} s_{ip}(t) - s_{in}(t)\mathrm{d}t \tag{2.49}$$

Similarly to the switched model, it is possible to obtain averaged switching vectors for the rectifier and inverter stages, as defined by (2.50) and (2.51), respectively.

$$[\mathbf{\Delta}_r] = \begin{bmatrix} \delta_A & \delta_B & \delta_C \end{bmatrix} \tag{2.50}$$

$$[\mathbf{\Delta}_i] = \begin{bmatrix} \delta_a & \delta_b & \delta_c \end{bmatrix} \tag{2.51}$$

Consequently, an averaged switching matrix can be defined by (2.52). This matrix couples the rectifier and inverter stages in the same way as the switching matrix in the switched model, according to (2.53) and (2.54).

$$\langle [\mathbb{T}_M] \rangle_{T_s} = [\mathbf{\Delta}_i]^T [\mathbf{\Delta}_r] = \begin{bmatrix} \delta_a\delta_A & \delta_a\delta_B & \delta_a\delta_C \\ \delta_b\delta_A & \delta_b\delta_B & \delta_b\delta_C \\ \delta_c\delta_A & \delta_c\delta_B & \delta_c\delta_C \end{bmatrix} \tag{2.52}$$

$$\vec{v}_i = \langle [\mathbb{T}_M] \rangle_{T_s} \vec{v}_r \tag{2.53}$$

$$\vec{i}_r = \langle [\mathbb{T}_M]^T \rangle_{T_s} \vec{i}_i \tag{2.54}$$

Therefore, by a process similar to the obtention of the complete system defined by (2.43), the averaged switched model can be defined by (2.55). The system input as well as the system matrix are expressed by (2.56), respectively. An extended version of (2.55) is presented in (2.57), where $\mathbf{Q}_{ij}^{r,i}$ are the elements of matrices $\left[\mathbf{Q}^{r,i}\right]$ defined in (2.58).

$$\langle \dot{\mathbf{x}}_t \rangle_{T_s} = [\mathbf{A}_{avg}] \langle \mathbf{x}_t \rangle_{T_s} + [\mathbf{B}_{avg}] \langle \mathbf{u}_t \rangle_{T_s} \tag{2.55}$$

$$\begin{aligned}
\langle \mathbf{x}_t \rangle_{T_s} &= \left[\langle i_A^s \rangle_{T_s} \quad \langle i_B^s \rangle_{T_s} \quad \langle v_A \rangle_{T_s} \quad \langle v_B \rangle_{T_s} \quad \langle i_a \rangle_{T_s} \quad \langle i_b \rangle_{T_s} \right]^T \\
\langle \mathbf{u}_t \rangle_{T_s} &= \left[\langle u_A \rangle_{T_s} \quad \langle u_B \rangle_{T_s} \quad \langle u_C \rangle_{T_s} \quad \langle u_a \rangle_{T_s} \quad \langle u_b \rangle_{T_s} \quad \langle u_c \rangle_{T_s} \right]^T
\end{aligned} \tag{2.56}$$

$$
\begin{bmatrix}
\langle \dot{i}^s_A(t)\rangle_{T_s} \\
\langle \dot{i}^s_B(t)\rangle_{T_s} \\
\langle \dot{v}_A(t)\rangle_{T_s} \\
\langle \dot{v}_B(t)\rangle_{T_s} \\
\langle \dot{i}_a(t)\rangle_{T_s} \\
\langle \dot{i}_b(t)\rangle_{T_s}
\end{bmatrix}
=
\begin{bmatrix}
-\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\
0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 \\
\frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f}\mathbf{Q}^i_{11} & -\frac{1}{C_f}\mathbf{Q}^i_{12} \\
0 & \frac{1}{C_f} & 0 & 0 & -\frac{1}{C_f}\mathbf{Q}^i_{21} & -\frac{1}{C_f}\mathbf{Q}^i_{22} \\
0 & 0 & \frac{1}{3L_m}\mathbf{Q}^r_{11} & \frac{1}{3L_m}\mathbf{Q}^r_{12} & -\frac{R_m}{L_m} & 0 \\
0 & 0 & \frac{1}{3L_m}\mathbf{Q}^r_{21} & \frac{1}{3L_m}\mathbf{Q}^r_{22} & 0 & -\frac{R_m}{L_m}
\end{bmatrix}
\begin{bmatrix}
\langle i^s_A(t)\rangle_{T_s} \\
\langle i^s_B(t)\rangle_{T_s} \\
\langle v_A(t)\rangle_{T_s} \\
\langle v_B(t)\rangle_{T_s} \\
\langle i_a(t)\rangle_{T_s} \\
\langle i_b(t)\rangle_{T_s}
\end{bmatrix}
$$

$$
+
\begin{bmatrix}
\frac{2}{L_f} & -\frac{1}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\
-\frac{1}{L_f} & \frac{2}{L_f} & -\frac{1}{L_f} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -\frac{2}{L_m} & \frac{1}{L_m} & \frac{1}{L_m} \\
0 & 0 & 0 & \frac{1}{L_m} & -\frac{2}{L_m} & \frac{1}{L_m}
\end{bmatrix}
\begin{bmatrix}
\langle u_A(t)\rangle_{T_s} \\
\langle u_B(t)\rangle_{T_s} \\
\langle u_C(t)\rangle_{T_s} \\
\langle u_a(t)\rangle_{T_s} \\
\langle u_b(t)\rangle_{T_s} \\
\langle u_c(t)\rangle_{T_s}
\end{bmatrix}
\tag{2.57}
$$

$$
\left[\mathbf{Q}^i\right] = \begin{bmatrix} \delta_a\delta_A - \delta_c\delta_A & \delta_b\delta_A - \delta_c\delta_A \\ \delta_a\delta_B - \delta_c\delta_B & \delta_b\delta_B - \delta_c\delta_B \end{bmatrix}, \quad \left[\mathbf{Q}^r\right] = \begin{bmatrix} (2\delta_a - \delta_b - \delta_c)(\delta_A - \delta_C) & (2\delta_a - \delta_b - \delta_c)(\delta_B - \delta_C) \\ (2\delta_b - \delta_a - \delta_c)(\delta_A - \delta_C) & (2\delta_b - \delta_a - \delta_c)(\delta_B - \delta_C) \end{bmatrix} \tag{2.58}
$$

2.4 STATIC ANALYSIS

The previous sections presented a detailed analysis of the converter considering multiple switching states. A model was obtained, which precisely reproduces the converter. The static analysis aims to present a steady-state converter analysis while ignoring state transients.

For a safe operation of the indirect matrix converter, there are some conditions which must be satisfied and limit the possible switching states:

- Any two phases of the rectifier stage cannot be short circuited;
- Any phase of the inverter stage cannot be open circuited;
- The virtual DC link voltage must be positive.

These conditions limit the possible switching states to nine in the rectifier stage and to eight in the inverter stage.

According to the averaged model, the virtual DC link voltage and current can be expressed by (2.59).

$$\begin{aligned}\langle u_{pn}\rangle_{T_s} &= \delta_A v_A + \delta_B v_B + \delta_C v_C \\ \langle i_{pn}\rangle_{T_s} &= \delta_a i_a + \delta_b i_b + \delta_c i_c\end{aligned} \tag{2.59}$$

The sum of the averaged switching function is unitary in each state due to fixed frequency operation, according to (2.60).

$$\begin{cases}\delta_A + \delta_B + \delta_C = 1 \\ \delta_a + \delta_b + \delta_c = 1\end{cases} \tag{2.60}$$

The system input power is approximately constant considering ideal conditions. Therefore, the virtual DC link current can be expressed according to (2.61), assuming that both voltage and current averaged values are approximately constants.

$$\langle i_{pn}\rangle_{T_s} \approx \frac{P_{pn}}{\langle u_{pn}\rangle_{T_s}} \tag{2.61}$$

The converter behaviour aims to find a combination of averaged switching vectors which satisfy the condition given by (2.62).

$$P_{ABC} \approx P_{abc} \tag{2.62}$$

Therefore, it is possible to impose voltage and current profiles by altering the switching vectors. The following section presents a more detailed analysis of the switching vectors.

Since the switched model has a total of twelve switches, there is a total of four thousand and ninety-six different combinations. However, in order to comply with the conditions presented previously, the number of possible switching states is reduced to nine in the rectifier and eight in the inverter stage, totalizing seventy-two possible switching states for the indirect matrix converter. However, it is easier to analyze each stage separately, since both stages are independent.

For this analysis, the system will be represented using the *Clarke* transformation in its complex notation, according to (2.63), where $\bar{r}_{r,i}$ is a vector pertaining to the three-reference frame in phasor notation and $\bar{r}_{\alpha\beta}$ is a complex valued vector in $\alpha\beta$ coordinates. Details regarding this transformation are described in Appendix B. This transformation is used to reduce the system dimention, since the common-mode voltage analysis will be suppressed. Through this transformation, a three-phase system will be described using the projection of the three-phase phasors on a two-dimensional two-dimensional stationary axis.

$$\bar{r}_{\alpha\beta} = \begin{bmatrix} 1 & e^{j\frac{2\pi}{3}} & e^{-j\frac{2\pi}{3}} \end{bmatrix} \bar{r}_{r,i} \tag{2.63}$$

For this analysis, the rectifier and inverter voltage and current are defined by (2.64) and (2.65), respectively.

$$\begin{aligned} \vec{v}_r &= \begin{bmatrix} V_{pk}^r \cos\left(\omega_r t\right) \\ V_{pk}^r \cos\left(\omega_r t - \frac{2\pi}{3}\right) \\ V_{pk}^r \cos\left(\omega_r t + \frac{2\pi}{3}\right) \end{bmatrix} \\ \vec{i}_r &= \begin{bmatrix} I_{pk}^r \cos\left(\omega_r t\right) \\ I_{pk}^r \cos\left(\omega_r t - \frac{2\pi}{3}\right) \\ I_{pk}^r \cos\left(\omega_r t + \frac{2\pi}{3}\right) \end{bmatrix} \end{aligned} \tag{2.64}$$

$$\begin{aligned} \vec{v}_i &= \begin{bmatrix} V_{pk}^i \cos\left(\omega_i t\right) \\ V_{pk}^i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ V_{pk}^i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix} \\ \vec{i}_i &= \begin{bmatrix} I_{pk}^i \cos\left(\omega_i t\right) \\ I_{pk}^i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ I_{pk}^i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix} \end{aligned} \tag{2.65}$$

Table 2.1 – Current source inverter switching states.

Type	**Vector** $\vec{I}_k$	S_{Ap} S_{An}	S_{Bp} S_{Bn}	S_{Cp} S_{Cn}	i_A	i_B	i_C	$\lVert\bar{i}_i\rVert$	$\angle\bar{i}_i$	u_{pn}
Active	$\vec{I}_1$	1 0	0 1	0 0	i_{pn}	$-i_{pn}$	0	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{\pi}{6}$	v_{AB}
	$\vec{I}_2$	1 0	0 0	0 1	i_{pn}	0	$-i_{pn}$	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{\pi}{6}$	$-v_{CA}$
	$\vec{I}_3$	0 0	1 0	0 1	0	i_{pn}	$-i_{pn}$	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{\pi}{2}$	v_{BC}
	$\vec{I}_4$	0 1	1 0	0 0	$-i_{pn}$	i_{pn}	0	$\frac{2}{\sqrt{3}}i_{pn}$	$\frac{5\pi}{6}$	$-v_{AB}$
	$\vec{I}_5$	0 1	0 0	1 0	$-i_{pn}$	0	i_{pn}	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{5\pi}{6}$	v_{CA}
	$\vec{I}_6$	0 0	0 1	1 0	0	$-i_{pn}$	i_{pn}	$\frac{2}{\sqrt{3}}i_{pn}$	$-\frac{\pi}{2}$	$-v_{BC}$
Null	$\vec{I}_7$	1 1	0 0	0 0	–	–	–	0	–	0
	$\vec{I}_8$	0 0	1 1	0 0	–	–	–	0	–	0
	$\vec{I}_9$	0 0	0 0	1 1	–	–	–	0	–	0

2.4.1 Rectifier Stage

The rectifier stage can be analyzed as a current source inverter. Therefore, there are nine possible switching states states which satisfy the previously discussed operation conditions, which can be subdivided into active and null states. Null states produces a null valued output, while active states produces a non-zero output. Since the null state is redundant, it will be depicted by $\vec{I}_0$ henceforth.

Assuming a constant virtual DC link current i_{pn}, the states can be described by Table 2.1, and a graphic representation of the space-vector map is illustrated by Figure 2.3. In a CSI, the DC link current is fed by a large inductance, which guarantees a low current ripple. However, the IMC virtual DC link current averaged value is not constant. Therefore, the current vector amplitude varies according to the inverter stage behaviour.

Furthermore, it is possible to infer that the virtual DC link voltage will always be composed of segments of the line-to-line voltages. Therefore, for each sector there will be always three possible current

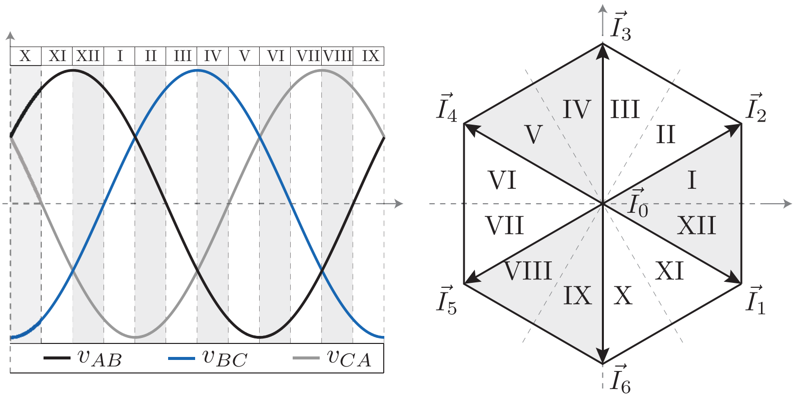


Figure 2.3 – Current source inverter space-vector map.

vectors which leads to a positive valued DC link voltage.

2.4.2 Inverter Stage

Differently from the rectifier stage, the inverter stage can be analyzed as a voltage source inverter. There are eight possible switching states, which can also be divided into active and null states. Since there are two redundant null states, they will be referred as $\vec{V}_0$ henceforth. Furthermore, the switching function s_{ip} and s_{in} are linear dependent, according to (2.66). Therefore, the switching vector $[\mathbf{s}_i]$ can be expressed by (2.67).

$$s_{in} = 1 - s_{ip} \tag{2.66}$$

$$[\mathbf{s}_i] = \begin{bmatrix} 2s_{ap} - 1 & 2s_{cp} - 1 & 2s_{cp} - 1 \end{bmatrix} \tag{2.67}$$

Assuming a constant virtual DC link voltage u_{pn}, the switching states can be described by Table 2.2, and a graphic representation of the space-vector map is shown in Figure 2.4. In a VSI, the DC link voltage is almost constant, given that it is fed by a large capacitance, which guarantees a small voltage ripple. However, the IMC virtual DC link voltage is not constant, similarly to the rectifier stage. The voltage vector amplitude is not constant and varies according to one of the *High-side* line-to-line voltage, depending on the switching state of

Table 2.2 – Voltage source inverter switching states.

Type	**Vector** $\vec{I}_k$	S_{ap} S_{an}	S_{bp} S_{bn}	S_{cp} S_{cn}	v_a	v_b	v_c	$\|\bar{v}_r\|$	$\angle\bar{v}_r$	i_{pn}
Active	$\vec{V}_1$	1 0	0 1	0 1	u_{pn}	$-u_{pn}$	$-u_{pn}$	$\frac{2}{3}u_{pn}$	0	i_a
	$\vec{V}_2$	1 0	1 0	0 1	u_{pn}	u_{pn}	$-u_{pn}$	$\frac{2}{3}u_{pn}$	$\frac{\pi}{3}$	$-i_c$
	$\vec{V}_3$	0 1	1 0	0 1	$-u_{pn}$	u_{pn}	$-u_{pn}$	$\frac{2}{3}u_{pn}$	$\frac{2\pi}{3}$	i_b
	$\vec{V}_4$	0 1	1 0	1 0	$-u_{pn}$	u_{pn}	u_{pn}	$\frac{2}{3}u_{pn}$	$-\pi$	$-i_a$
	$\vec{V}_5$	0 1	0 1	1 0	$-u_{pn}$	$-u_{pn}$	u_{pn}	$\frac{2}{3}u_{pn}$	$-\frac{2\pi}{3}$	i_c
	$\vec{V}_6$	1 0	0 1	1 0	u_{pn}	$-u_{pn}$	u_{pn}	$\frac{2}{3}u_{pn}$	$-\frac{\pi}{3}$	$-i_b$
Null	$\vec{V}_7$	1 0	1 0	1 0	u_{pn}	u_{pn}	u_{pn}	0	–	0
	$\vec{V}_8$	0 1	0 1	0 1	$-u_{pn}$	$-u_{pn}$	$-u_{pn}$	0	–	0

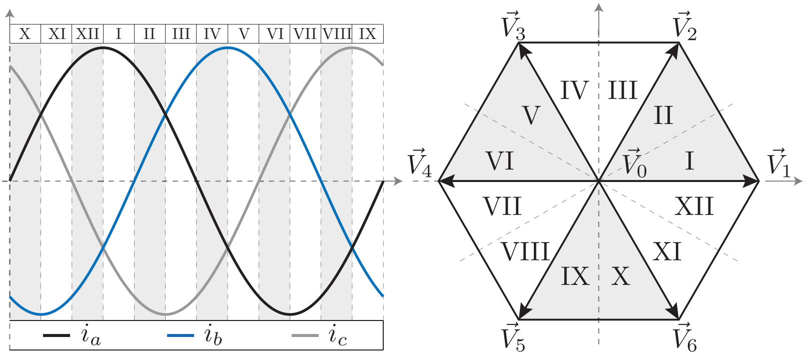

X
XI
XII
I
II
III
IV
V
VI
VII
VIII
IX
i_a
i_b
i_c
$\vec{V}_3$
$\vec{V}_2$
$\vec{V}_4$
$\vec{V}_1$
$\vec{V}_0$
$\vec{V}_5$
$\vec{V}_6$
IV
III
V
II
VI
I
VII
XII
VIII
XI
IX
X

Figure 2.4 – Voltage source inverter space-vector map.

the rectifier stage.

Since four-quadrant switches are used to define the rectifier state, i_{pn} can assume positive and negative values. Therefore, there is no limitation regarding which vector can be applied in the inverter stage.

A complete space vector map can be expressed as a combination of both stages, as shown in Figure 2.5. During a single sampling time,

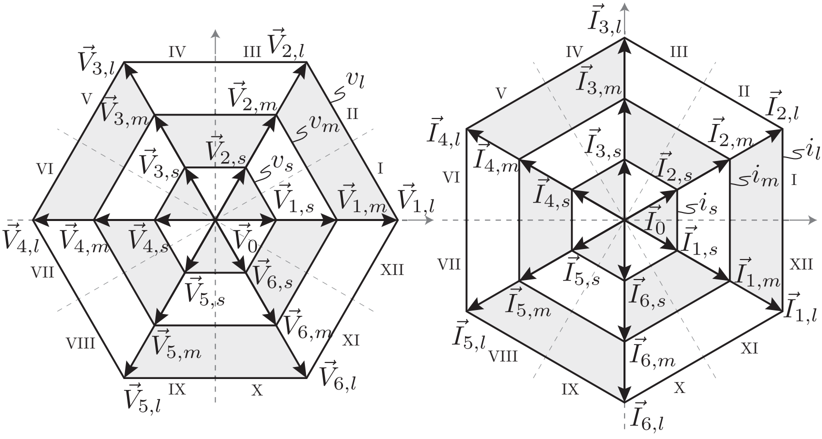

$\vec{V}_{3,l}$
IV
III
$\vec{V}_{2,l}$
v_l
V
$\vec{V}_{3,m}$
$\vec{V}_{2,m}$
v_m
II
VI
$\vec{V}_{3,s}$
$\vec{V}_{2,s}$
v_s
I
$\vec{V}_{1,s}$
$\vec{V}_{1,m}$
$\vec{V}_{1,l}$
$\vec{V}_{4,l}$
$\vec{V}_{4,m}$
$\vec{V}_{4,s}$
$\vec{V}_0$
VII
$\vec{V}_{6,s}$
XII
$\vec{V}_{5,s}$
$\vec{V}_{6,m}$
VIII
$\vec{V}_{5,m}$
XI
$\vec{V}_{6,l}$
$\vec{V}_{5,l}$
IX
X
$\vec{I}_{3,l}$
IV
III
V
$\vec{I}_{3,m}$
II
$\vec{I}_{2,l}$
$\vec{I}_{4,l}$
$\vec{I}_{3,s}$
$\vec{I}_{2,m}$
i_l
$\vec{I}_{4,m}$
$\vec{I}_{2,s}$
i_m
VI
I
$\vec{I}_{4,s}$
i_s
$\vec{I}_0$
$\vec{I}_{1,s}$
VII
XII
$\vec{I}_{5,s}$
$\vec{I}_{1,m}$
$\vec{I}_{6,s}$
$\vec{I}_{5,m}$
$\vec{I}_{1,l}$
$\vec{I}_{5,l}$
VIII
$\vec{I}_{6,m}$
XI
IX
X
$\vec{I}_{6,l}$

Figure 2.5 – Indirect matrix converter current and voltage space-vector map.

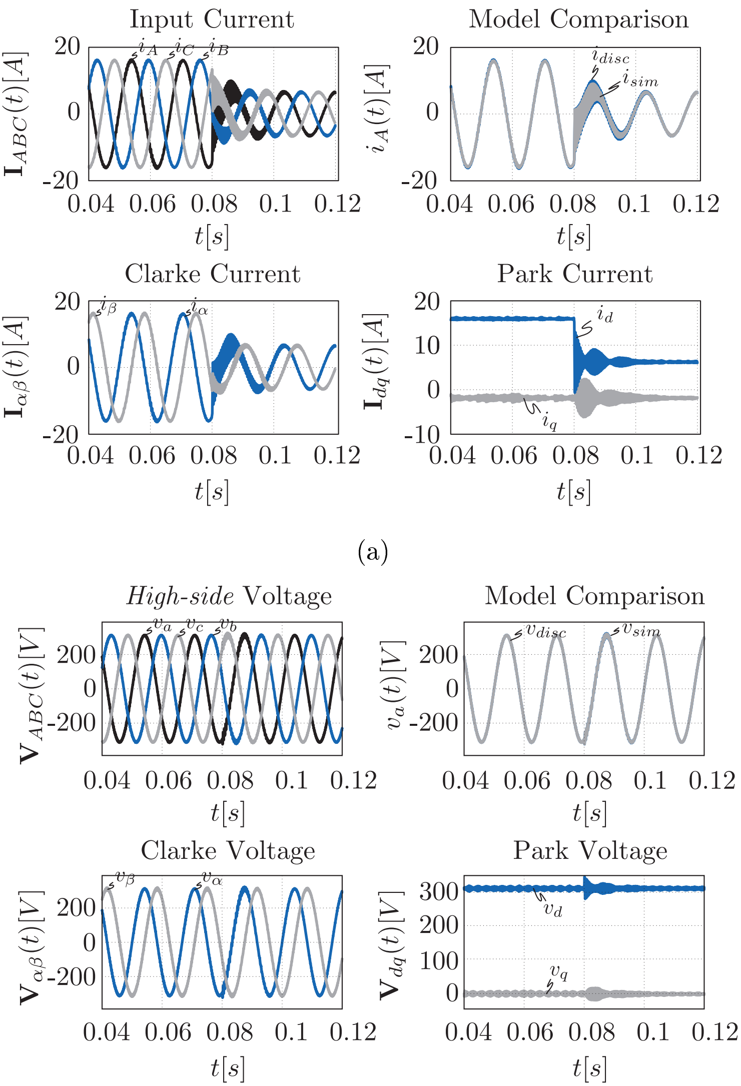
three line-to-line voltages are positive valued, which are classified from the highest to the lowest amplitude as $\{v_l, v_m, v_s\}$.

Since u_{pn} is positive valued, the power flow direction is controlled by the inverter side, according to (2.61). Therefore, there are only three possible currents for each direction of the power flow, which are classified from the highest to lowest amplitude as $\{i_l, i_m, i_s\}$.

2.5 SIMULATION ANALYSIS

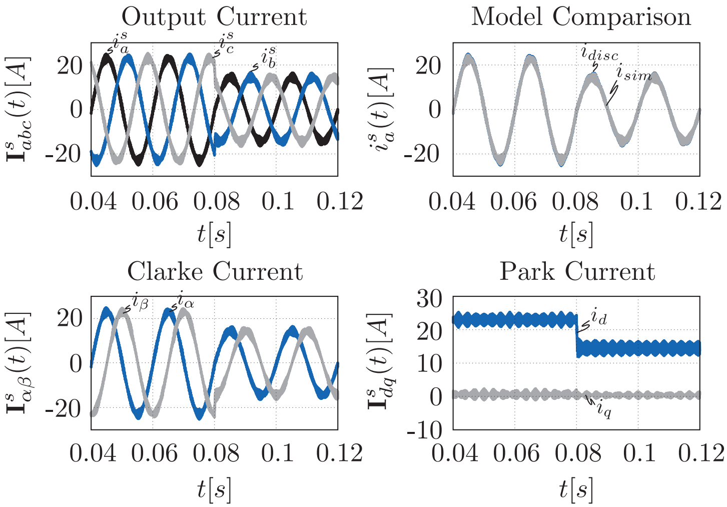
This sections aims to verify the validity of indirect matrix converter models obtained in this chapter. The discretized state-space model as well as the converter circuit were implemented using Matlab® and Simulink®.

The parameters used for simulations are described in Table 2.3. Figure 2.6 shows a simulation for the nine state variables. The results were presented in *abc* coordinates and using *Clarke* and *Park* transformations, which are presented in Appendix B. Details regarding modulation strategy implementation will be presented in the subsequent chapters.


Input Current
$\mathbf{I}_{ABC}(t)[A]$
i_A
i_C
i_B
20
0
-20
0.04 0.06 0.08 0.1 0.12
$t[s]$
Model Comparison
$i_A(t)[A]$
i_{disc}
i_{sim}
20
0
-20
0.04 0.06 0.08 0.1 0.12
$t[s]$
Clarke Current
$\mathbf{I}_{\alpha\beta}(t)[A]$
i_β
i_α
20
0
-20
0.04 0.06 0.08 0.1 0.12
$t[s]$
Park Current
$\mathbf{I}_{dq}(t)[A]$
i_d
i_q
20
10
0
-10
0.04 0.06 0.08 0.1 0.12
$t[s]$
High-side Voltage
$\mathbf{V}_{ABC}(t)[V]$
v_a
v_c
v_b
200
0
-200
0.04 0.06 0.08 0.1 0.12
$t[s]$
Model Comparison
$v_a(t)[V]$
v_{disc}
v_{sim}
200
0
-200
0.04 0.06 0.08 0.1 0.12
$t[s]$
Clarke Voltage
$\mathbf{V}_{\alpha\beta}(t)[V]$
v_β
v_α
200
0
-200
0.04 0.06 0.08 0.1 0.12
$t[s]$
Park Voltage
$\mathbf{V}_{dq}(t)[V]$
v_d
v_q
300
200
100
0
0.04 0.06 0.08 0.1 0.12
$t[s]$

(a)

(b)



(c)

Figure 2.6 – Simulated discretized state-space model of the indirect matrix converter using HVZCS modulation strategy, with modulation index varying from 0.8 to 0.5 at $t = 80$ ms. The amplitude invariant *Clarke* and *Park* transformations were used for clarity. (a) *High-side* Input current. (b) *High-side* Voltage. (c) *Low-side* Current.

Table 2.3 – Simulation parameters.

Parameter	**Symbol**	**Value**
Modulation Strategy	–	HVZCS [1]
Modulation index	m	0.8–0.5
High-side RMS voltage	V_r^{rms}	220 V
Low-side RMS voltage	V_i^{rms}	152.4–95.3 V
High-side frequency	f_{ABC}	60 Hz
Low-side frequency	f_{abc}	50 Hz
High-side Inductance	L_f	250 μH
High-side Capacitance	C_f	16 μF
High-side Resistance	R_f	10 mΩ
Low-side Inductance	L_m	750 μH
Low-side Resistance	R_m	9.375 Ω
Switching Frequency	f_s	24.424 kHz
Simulation Step	T_{step}	80 ns

2.6 CONCLUSION

This section presented mathematical models which describes accurately the static and dynamic behaviour of the indirect matrix converter. A discretized switched model was presented, which can be used in different control strategies, as well as *hardware-in-the-loop* simulations. The presented models are valid for both *step-down*, which is commonly used in motor driving operation, and *step-up* mode, which can be used for grid-tied applications.

A static analysis was presented, separating the converter into a rectifier and an inverter stage, or into a current and a voltage source inverter. An analysis of the switching vector was performed. In the following chapters, the analysis of matrix converter operation will be based on the models and static analysis here presented.

3 MODULATION STRATEGIES

3.1 INTRODUCTION

This chapter presents a review on different modulation strategies. Following the static analysis presented in the previous chapter, different modulation techniques can be applied to the indirect matrix converter, while preserving the power balance between rectifier and inverter stages.

Carrier-based modulation strategies have been explored by a few authors in [24, 25, 26] for operation under unbalanced voltage condition. This type of modulation uses carriers and pulse-width modulators to generate an averaged switching matrix with a pre-determined behaviour. The main advantage of this modulation strategy is the reduced computational burden. Since this work proposes a fast and low computational effort implementation of the space-vector modulation, carrier-based strategies will not be further discussed.

An advantage of the IMC is that some modulation strategies do not require multi-step commutation for the rectifier stage, which usually adds another layer of complexity to the implementation. However, multi-step commutation for the IMC is much simpler than on the CMC, since the current values are known for all the switches. *Dead-time* and *overlap-time* are still required for a safe converter operation.

Since the matrix converter possesses seventy-two possible switching states, space-vector modulation can be quite complex, since many different combinations of vectors are possible. This chapter discusses some of the possible combinations.

The SVM strategies presented in this chapter are derived using a sequential approach, separating the converter into rectifier and inverter stages, as presented in the last chapter. With regards to the modulation, the IMC topology, depicted in Figure 3.1, represents a combination of a CSI for the rectifier stage and a VSI for the inverter stage.

The principle of space-vector modulation is to calculate the time of appliance for different voltage or current vectors during a determined switching time such that the averaged value of the applied voltage or current follows a reference, according to (3.1), where $\bar{r}_n$ is a voltage or current vector in phasor form, N is the number of applied vectors, and t_n is the time of which each vector is applied. The vector times must suffice the condition set by (3.2).

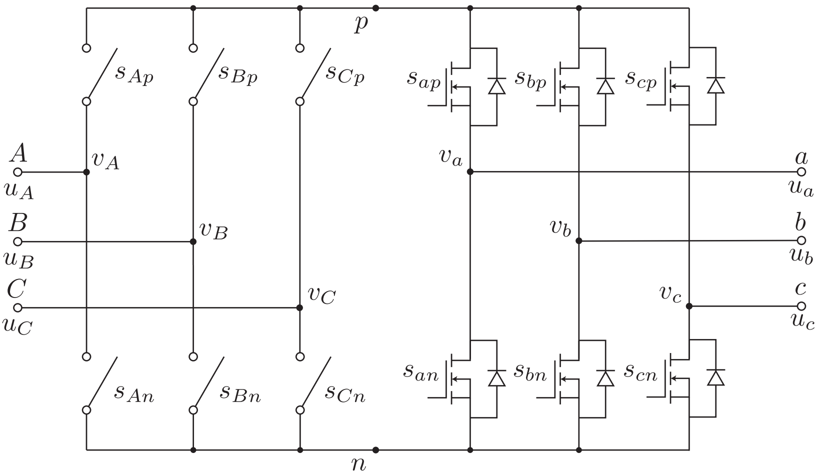


Figure 3.1 – Indirect Matrix Converter (IMC) topology. The four-quadrant switches denoted with indexes $\{A, B, C\}$ compose the rectifier-stage, while the switches denoted with indexes $\{a, b, c\}$ compose the inverter stage.

$$\langle \bar{r} \rangle_{T_s} = \frac{1}{T_s} \sum_{n=0}^{N} \bar{r}_n t_n \tag{3.1}$$

$$\sum_{n=0}^{N} t_n = T_s \tag{3.2}$$

The sequence of application of each vector does not alter the averaged value. Consequently, the order can be chosen in such way to reduce switching losses. According to the static analysis in the previous chapter, u_{pn} and i_{pn} are dependent the rectifier and inverter switching state, respectively. If one is null, it is possible to have soft-switching on one stage. Therefore, according to [1], the main space-vector modulations for the IMC can be classified according to:

- *Zero Current Switching* (ZCS) – The null vector is always synthesized on the inverter stage. The virtual DC link current is zero during this instant. During this time instant, the rectifier stage can commute with no losses.
- *Zero Voltage Switching* (ZVS) – Contrary to the ZCS modulation,

the null vector is synthesized in the rectifier stage. The switches on the inverter side commute no losses due to a null virtual DC link voltage. In general, ZVS modulation strategies require multi-step commutation schemes, which increase the implementation complexion.

Furthermore, the IMC space-vector modulation can be classified by which vectors are used when synthesizing the reference vector, according to the vector map presented in the previous chapter in Figure 2.5. The author in [2] further classifies modulation strategies for the IMC according to Table 3.1.

The ZCS and ZVS modulation schemes aim to reduce switching losses in an indirect matrix converter and can be classified according to which voltage or current vector, according to the three possible vector and current vectors $\{v_l, v_m, v_s\}$ and $\{i_l, i_m, i_s\}$ applied. HVSVM uses the large vectors, denoted by l subscript, and medium vectors, denoted by m subscript. LVSVM uses medium and small vector, the last denoted by s subscript. A graphic representation of the possible switching states for the HVSVM and LVSVM are presented in Figure 3.2.

Three-level modulation schemes uses the three available vectors, demonstrating the "quasi three-level" characteristic of the IMC. The TLSVM uses all the available switching vectors in both rectifier and inverter stages, with the exception of the null vector in the rectifier

Table 3.1 – Indirect matrix converter space vector modulation strategies [2].

Modulation Scheme	**Reference**
ZCS Modulation Strategies (ZCS)	
High Voltage ZCS (HVZCS)	[27, 28]
Low Voltage ZCS (LVZCS)	[29]
Three-Level ZCS (TLZCS)	[8, 30]
ZVS Modulation Strategies (ZCS)	
High Voltage ZVS (HVZVS)	[27, 31]
Low Voltage ZVS (LVZVS)	[8]
Three-Level ZVS (TLZVS)	[8]
Switching Losses Shifting (SLS)	
High Voltage SLS (HVSLS)	[29, 8, 32]
Low Voltage SLS (LVSLS)	[29, 8]
Conventional SVM (CSVM)	[33, 34]
Non-Zero SVM (NZSVM)	[35]
Reactive Power SVM (RPSVM)	[8]

stage for ZCS and in the inverter stage for ZVS scheme, resulting in a vector map which utilizes all the possible switching states, as discussed in the previous chapter. This modulation strategy is patented [30] and its mathematical derivation can be found in [8]. However, its FPGA implementation is not practical and will not be further discussed in this work.

Unfortunately, the strategies based on ZCS and ZVS concentrate losses on one stage, leading to a non-uniform semiconductor loss distribution. The Switching Loss Shifting (SLS) modulation strategies [8, 32] provide an alternative scheme which aim to balance the switching losses by applying the null vector in both stages. A disadvantage of this scheme is the complexity of the implementation, as multi-step commutation might be needed for a proper operation.

An alternative for the proposed ZCS and ZVS modulation schemes are modulations which were originally developed for the CMC can be applied to the IMC. The CSVM proposed in [34], and its improved version ISVM are examples of modulations originally conceived for the CMC. These modulation schemes also result in a better semiconductor loss distribution. However, such modulation patterns require multi-step commutation schemes and possesses increased switching losses.

Also, some modulation strategies aim for CM voltage reduction, such as the NZSVM presented in [35], which possesses an increased number of voltage transitions in a switching time if compared to the modulations previously presented.

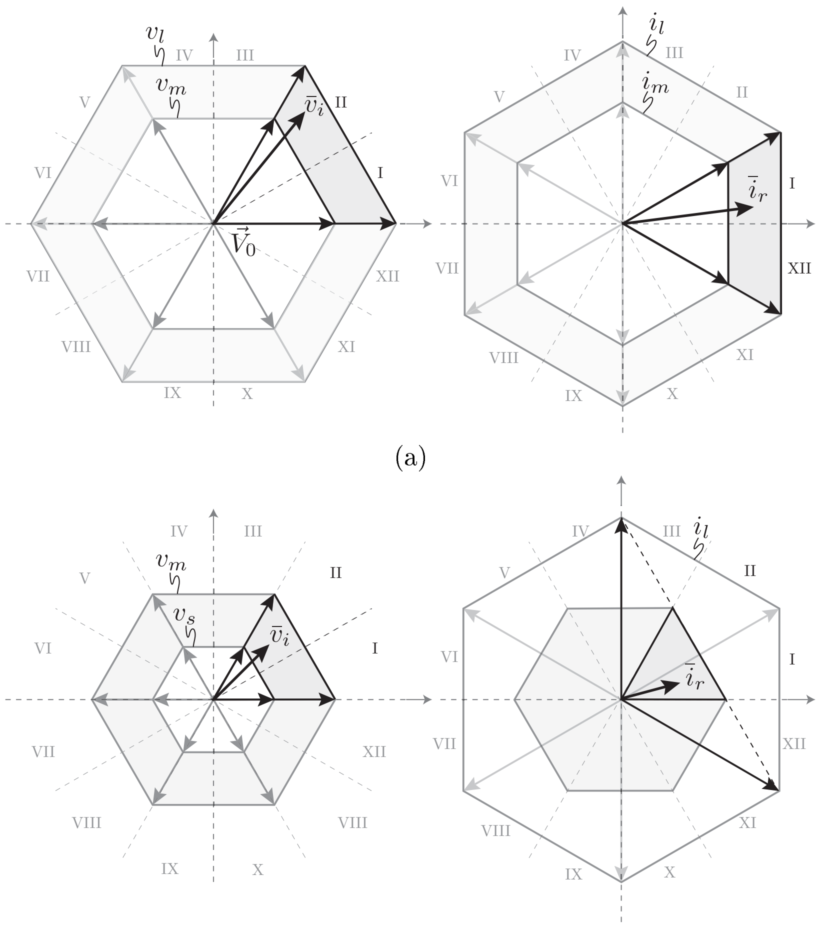
The next sections present a detailed analysis of some modulation schemes. Detailed calculations for the discussed schemes are presented in Appendix C.

3.2 SPACE VECTOR MODULATION STRATEGIES

3.2.1 High Voltage Zero Current Switching Modulation

The ZCS modulation strategies aims to commute the switches in the rectifier stage without losses. The null vector is always applied in the inverter stage. Table 3.2 shows the voltage vectors for each sector considering *high-side* voltage and *low-side* current three phase vectors given by (3.3) and (3.4), respectively.

Since the four-quadrant switches commute with zero current, a multi-step commutation scheme is not required. Therefore, the implementation of ZCS strategies are simpler and preferable for MOSFET


v_l
v_m
$\bar{v}_i$
$\vec{V}_0$
i_l
i_m
$\bar{i}_r$
v_s
I
II
III
IV
V
VI
VII
VIII
IX
X
XI
XII

(a)

(b)

Figure 3.2 – Inverter and rectifier stage space vector map for different ZCS and ZVS modulation schemes. (a) High Voltage Space Vector Modulation (HVSVM) (b) Low Voltage Space Vector Modulation (LVSVM).

based converters. The ZVS modulation strategies are indicated for IGBT based converters, as a longer *dead-time* is needed due to the tail current for ZCS schemes, resulting in a higher voltage and current distortion.

$$\vec{v}_r = V_r^{pk} \begin{bmatrix} \cos(\varphi_r) \\ \cos\left(\varphi_r - \frac{2}{3}\pi\right) \\ \cos\left(\varphi_r + \frac{2}{3}\pi\right) \end{bmatrix} \tag{3.3}$$

$$\vec{i}_i = I_i^{pk} \begin{bmatrix} \cos(\varphi_i) \\ \cos\left(\varphi_i - \frac{2}{3}\pi\right) \\ \cos\left(\varphi_i + \frac{2}{3}\pi\right) \end{bmatrix} \tag{3.4}$$

The HVZCS modulation scheme consists of applying the large and medium amplitude voltage vectors $\{v_l, v_m\}$ in the rectifier stage, limiting the number of possible vectors according to Figure 3.2a. The virtual DC link voltage is then formed by segments of line-to-line voltages v_l and v_m, illustrated by Figure 3.3.

A modulation index directly tied to the converter gain can be expressed by (3.5). From this equation, it is possible to infer that the maximum converter gain is approximately equal to 0.866 for *Buck* mode operation. An immediate implication is that this modulation scheme cannot be used to drive a three-phase motor with a rated voltage equal to the input voltage.

Table 3.2 – *High-side* line-to-line voltages sorted by magnitude for each sector.

Sector	φ_r	v_l	v_m	v_s
I	$\left[0, \frac{\pi}{6}\right]$	$-v_{CA}$	v_{AB}	v_{BC}
II	$\left[\frac{\pi}{6}, \frac{\pi}{3}\right]$	$-v_{CA}$	v_{BC}	v_{AB}
III	$\left[\frac{\pi}{3}, \frac{\pi}{2}\right]$	v_{BC}	$-v_{CA}$	$-v_{AB}$
IV	$\left[\frac{\pi}{2}, \frac{2\pi}{3}\right]$	v_{BC}	$-v_{AB}$	$-v_{CA}$
V	$\left[\frac{2\pi}{3}, \frac{5\pi}{6}\right]$	$-v_{AB}$	v_{BC}	v_{CA}
VI	$\left[\frac{5\pi}{6}, \pi\right]$	$-v_{AB}$	v_{CA}	v_{BC}
VII	$\left[-\pi, -\frac{5\pi}{6}\right]$	v_{CA}	$-v_{AB}$	$-v_{BC}$
VIII	$\left[-\frac{5\pi}{6}, -\frac{2\pi}{3}\right]$	v_{CA}	$-v_{BC}$	$-v_{AB}$
IX	$\left[-\frac{2\pi}{3}, -\frac{\pi}{2}\right]$	$-v_{BC}$	v_{CA}	v_{AB}
X	$\left[-\frac{\pi}{2}, -\frac{\pi}{3}\right]$	$-v_{BC}$	v_{AB}	v_{CA}
XI	$\left[-\frac{\pi}{3}, -\frac{\pi}{6}\right]$	v_{AB}	$-v_{BC}$	$-v_{CA}$
XII	$\left[-\frac{\pi}{6}, 0\right]$	v_{AB}	$-v_{CA}$	$-v_{BC}$

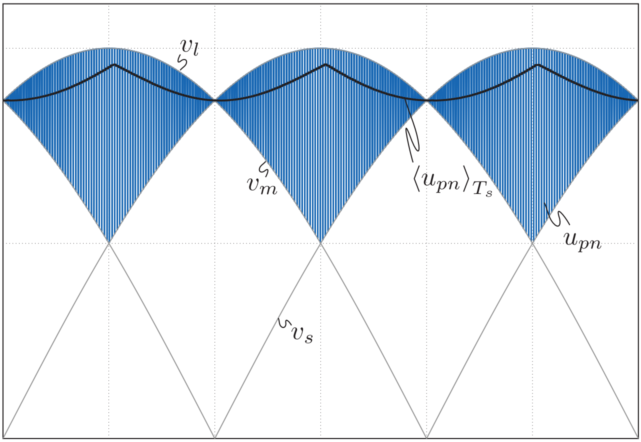


Figure 3.3 – Virtual DC link voltage waveform for the HVZCS modulation scheme.

$$m = \frac{2}{\sqrt{3}} \frac{V_i^{pk}}{V_r^{pk}} \in [0, 1] \tag{3.5}$$

Using the modulation index defined in (3.5), the vector times can be calculated according to (3.6).

$$\begin{aligned}
\tau_{1,l}^{i} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right) \cos\left(\varphi_i + \tfrac{\pi}{6}\right) \\
\tau_{1,m}^{i} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right) \cos\left(\varphi_i + \tfrac{\pi}{6}\right) \\
\tau_{2,l}^{i} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right) \sin\left(\varphi_i\right) \\
\tau_{2,m}^{i} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right) \sin\left(\varphi_i\right)
\end{aligned} \tag{3.6}$$

The null vector choice differentiates ZCS and ZVS strategies. For ZCS modulation schemes, the application of the null vector occurs in the inverter stage, and the rectifier stage switches commute during this instant. Since the order of application of switching vectors does not alter the final averaged values, Figure 3.4 presents two different vector sequences. Both schemes present the same switching number in a period, albeit the nine-segment and eleven-segment schemes possess half-wave symmetry, minimizing even harmonics. The eleven-segment scheme guarantees null current on sector changes, guaranteeing a safe

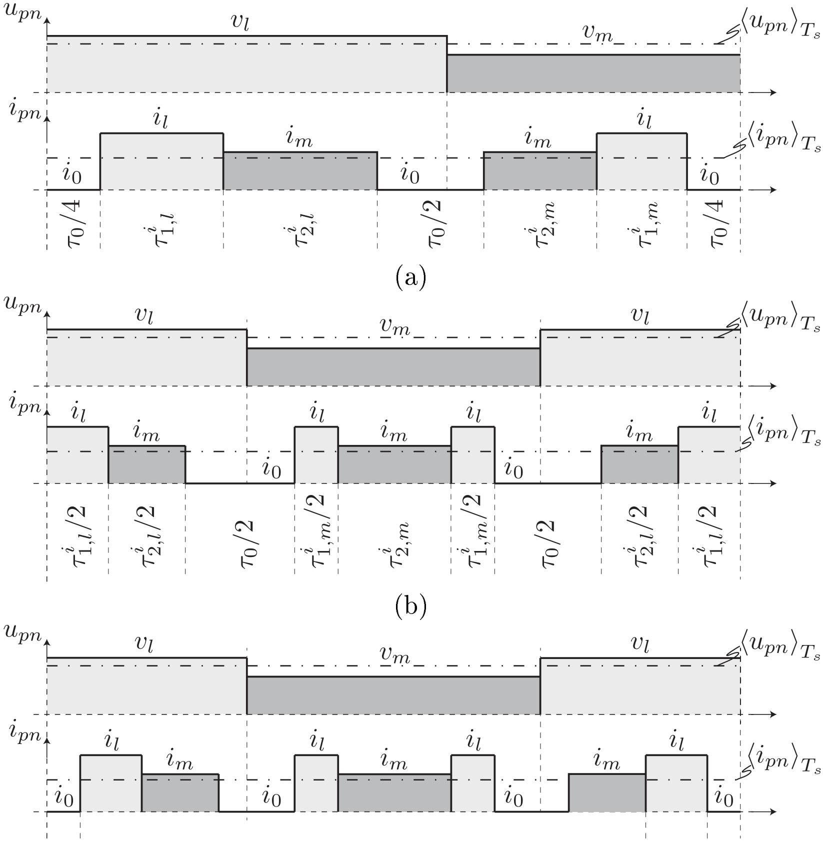
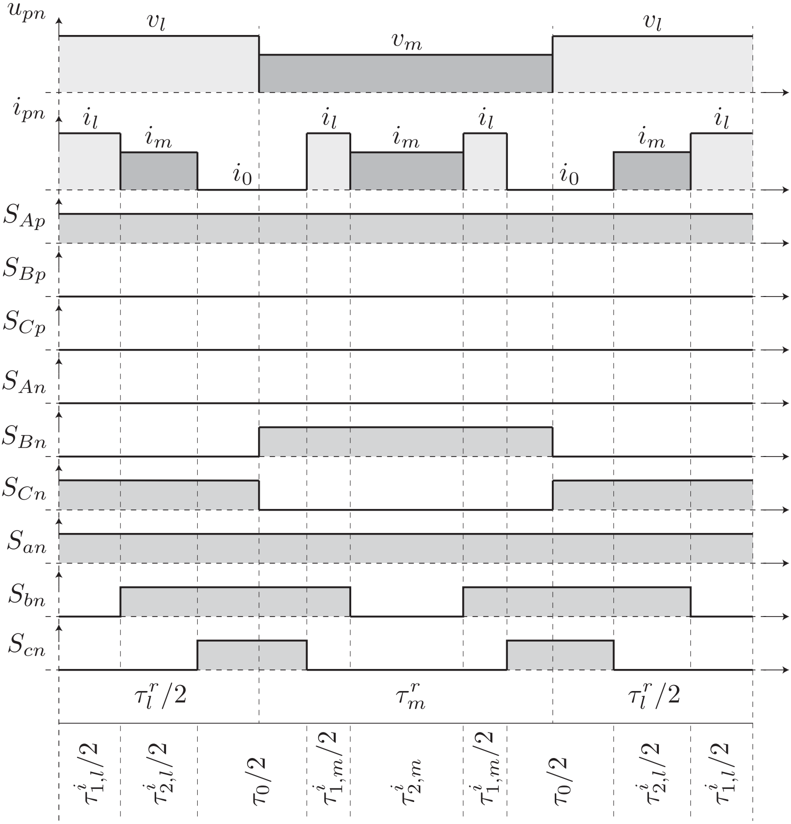

u_{pn}
v_l
v_m
$\langle u_{pn} \rangle_{T_s}$
i_{pn}
i_l
i_m
i_0
$\langle i_{pn} \rangle_{T_s}$
$\tau_0/4$
$\tau^i_{1,l}$
$\tau^i_{2,l}$
$\tau_0/2$
$\tau^i_{2,m}$
$\tau^i_{1,m}$
$\tau_0/4$
(a)
$\tau^i_{1,l}/2$
$\tau^i_{2,l}/2$
$\tau_0/2$
$\tau^i_{1,m}/2$
$\tau^i_{2,m}$
$\tau^i_{1,m}/2$
$\tau_0/2$
$\tau^i_{2,l}/2$
$\tau^i_{1,l}/2$
(b)
(c)

Figure 3.4 – HVZCS modulation schemes. (a) Seven-segment scheme. (b) Nine-segment scheme. (c) Eleven-segment scheme.

operation for double update, as v_l can change between sectors, resulting in a small number of non-ZCS switching in a grid period. This scheme is proposed in [36] for the modulated model predictive control (M^{2}PC), as it is not guaranteed that v_l is the same for each switching time window.

The null vector application time can be defined by (3.7). The switching frequency in the inverter stage is two times higher than the switching frequency of the rectifier stage. A diagram of the switching pattern for the nine-segment HVZCS modulation scheme considering


u_{pn}
v_l
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v_l
i_{pn}
i_l
i_m
i_0
i_l
i_m
i_l
i_0
i_m
i_l
S_{Ap}
S_{Bp}
S_{Cp}
S_{An}
S_{Bn}
S_{Cn}
S_{an}
S_{bn}
S_{cn}
$\tau_l^r/2$
τ_m^r
$\tau_l^r/2$
$\tau_{1,l}^i/2$
$\tau_{2,l}^i/2$
$\tau_0/2$
$\tau_{1,m}^i/2$
$\tau_{2,m}^i$
$\tau_{1,m}^i/2$
$\tau_0/2$
$\tau_{2,l}^i/2$
$\tau_{1,l}^i/2$

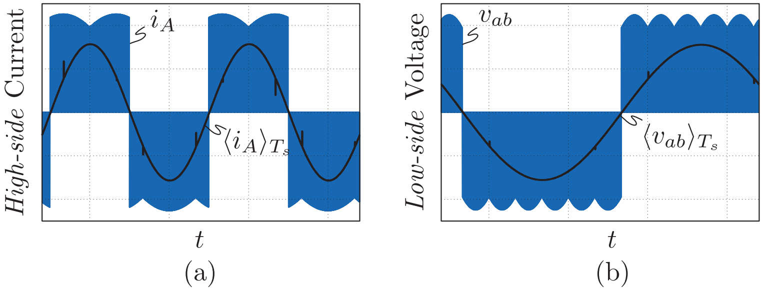
Figure 3.5 – Switching pattern of the nine-segment HVZCS modulation scheme considering both stages in the first quadrant.

both stages in the first sector is shown in Figure 3.5.

$$\tau_0 = T_s - \tau_{1,l}^i - \tau_{1,m}^i - \tau_{2,l}^i - \tau_{2,m}^i \tag{3.7}$$

The rectifier stage current and inverter stage voltage waveforms for a modulation index of 0.8, along with their average value, are presented in Figure 3.6. It is possible to notice that the average value of both quantities possess a sinusoidal form.

According to [27, 28], HVZCS modulation presents the most advantages for nominal operation, since a lower *low-side* voltage ripple can be achieved. Furthermore, since the virtual DC link voltage has a



(a) (b)

Figure 3.6 – Electrical quantities waveform for HVZCS modulation scheme for a modulation index of 0.8. (a) Rectifier stage current. (b) Inverter stage line-to-line-to-line voltage.

lower ripple if compared other strategies, the *high-side* current ripple is lower for this scheme.

The main disadvantage for this modulation scheme is that all switches commute with the highest and medium amplitude line-to-line voltage, switching losses are higher if compared to the LVSVM modulation scheme, whose switches commute with lower voltage levels. However, this modulation scheme is still the most viable for higher modulation index operation.

3.2.2 Low Voltage Zero Current Switching Modulation

Differently from the previously presented scheme, the LVZCS modulation strategy consists of applying the medium and low amplitude line-to-line voltage vectors $\{v_m, v_s\}$ in the rectifier stage, limiting the number of switching vectors according to the diagram presented in Figure 3.2b. Consequently, the virtual DC link voltage waveform is composed of segments of the *high-side* line-to-line voltage as illustrated in Figure 3.7.

A modulation index directly tied to the converter gain is described in (3.8). Therefore, the maximum voltage gain of this modulation scheme is equal to 0.5 for *Buck-mode* operation.

$$m = \frac{2}{\sqrt{3}}\frac{V_i^{pk}}{V_r^{pk}} \in \left[0, \frac{1}{\sqrt{3}}\right] \tag{3.8}$$

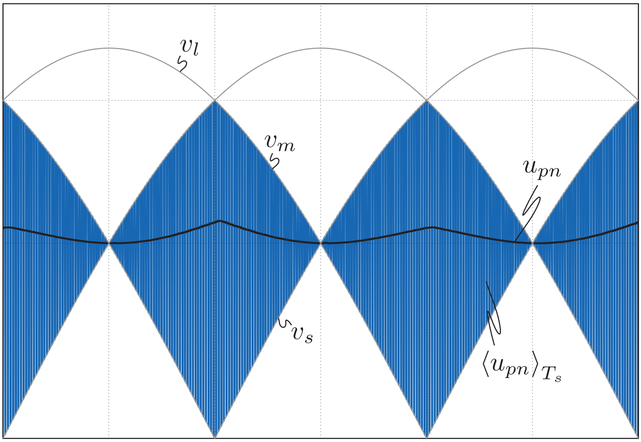


Figure 3.7 – Virtual DC link voltage waveform for the LVZCS modulation scheme.

Using the modulation index defined in (3.8), the vector times can be defined according to (3.9).

$$\begin{aligned} \tau^i_{1,m} &= mT_s \cos(\varphi_r)\cos\left(\varphi_i + \tfrac{\pi}{6}\right) \\ \tau^i_{1,s} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\cos\left(\varphi_i + \tfrac{\pi}{6}\right) \\ \tau^i_{2,m} &= mT_s \cos(\varphi_r)\sin(\varphi_i) \\ \tau^i_{2,s} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\sin(\varphi_i) \end{aligned} \tag{3.9}$$

Similarly to the HVZCS scheme, a null vector time can be defined by (3.10).

$$\tau_0 = T_s - \tau^i_{1,m} - \tau^i_{1,s} - \tau^i_{2,m} - \tau^i_{2,s} \tag{3.10}$$

Once again, the null vector choice differentiates ZCS and ZVS schemes. Similarly to the HVZCS modulation scheme, Figure 3.8 illustrates a nine-segment LVZCS modulation scheme. It is important to notice that the switching frequency in the inverter stage is two times higher than in the rectifier stage, similarly to the previous scheme.

The waveform for the rectifier stage current and inverter stage line-to-line-to-line voltage is presented in Figure 3.9, which demonstrates the operation of the converter operating using the LVZCS mod-

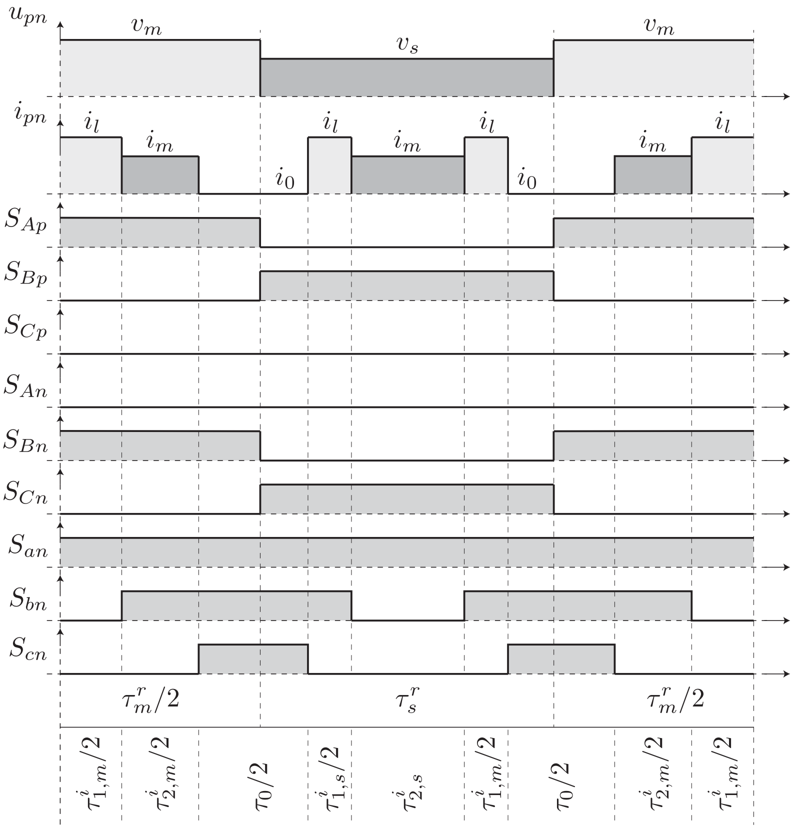
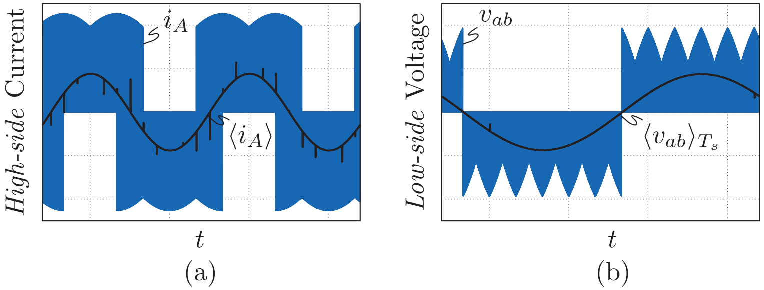

u_{pn}
v_m
v_s
v_m
i_{pn}
i_l
i_m
i_0
i_l
i_m
i_l
i_0
i_m
i_l
S_{Ap}
S_{Bp}
S_{Cp}
S_{An}
S_{Bn}
S_{Cn}
S_{an}
S_{bn}
S_{cn}
$\tau^r_m/2$
τ^r_s
$\tau^r_m/2$
$\tau^i_{1,m}/2$
$\tau^i_{2,m}/2$
$\tau_0/2$
$\tau^i_{1,s}/2$
$\tau^i_{2,s}$
$\tau^i_{1,m}/2$
$\tau_0/2$
$\tau^i_{2,m}/2$
$\tau^i_{1,m}/2$

Figure 3.8 – Switching pattern of the nine-segment HVZCS modulation scheme considering both stages in the first quadrant.

ulation scheme.

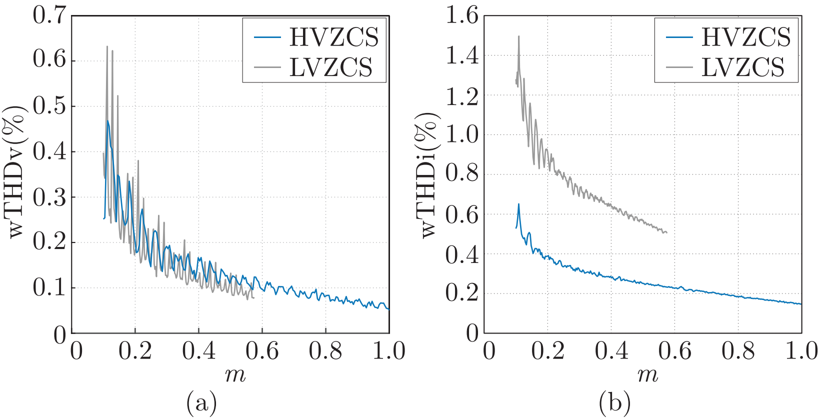
Since the amplitude of the virtual DC link voltage is lower, this scheme has lower switching losses if compared to the HVZCS modulation. According to the graphic presented in Figure 3.10, the ***high-side*** current harmonic content is higher, since the voltage ripple in the virtual DC link voltage is higher in the LVZCS scheme.

A practical problem of the LVZCS modulation scheme is that switching must be disabled during the time regions when v_l is close to zero to avoid eventual short-circuits due to the application of negative valued voltages on the virtual DC-link. Another solution would be to operate with a different modulation scheme during these intervals,



(a) (b)

Figure 3.9 – Electrical quantities waveform for HVZCS modulation scheme for a modulation index of 0.45. (a) Rectifier stage current. (b) Inverter stage line-to-line-to-line voltage.



(a) (b)

Figure 3.10 – Weighted total harmonic distortion of HVZCS and LVZCS modulation schemes. (a) *Low-side* voltage wTHDv (b) *High-side* current wTHDi.

which leads to a more complex implementation.

3.2.3 Zero Voltage Switching Modulation

The HVZVS and LVZVS modulation schemes are analogous to the HVZCS and LVZCS modulation schemes, and the vector times used for the ZCS are the same for the ZVS strategies.

The difference between the previous modulation schemes and ZVS schemes is in the application of the null vector. Contrary to the previous strategies, ZVS SVM aim to commute the switches of the inverter stage by applying the null vector in the rectifier stage. Therefore, the difference between ZCS and ZVS modulation schemes only lies in which of the stages apply the null vector.

3.3 CONCLUSION

This section presented a review on different modulation strategies applied to the IMC. Some of the innate characteristics of the topology enable modulation schemes with reduced switching losses, as demonstrated by ZCS and ZVS modulation schemes. However, such strategies possesses some operation limits and disadvantages, which might be solved with other modulation schemes.

The SLS modulation schemes aim to solve the distribution of losses problem of ZVS and ZCS modulation by alternating between the two modulation schemes. Therefore, its understanding and mathematical formulation is directly tied to the formulation presented in this chapter.

Some modulation strategies based on the CMC SVM are useful for reduced harmonic distortion. However, the decreased converter efficiency due to increased switching losses might limit the application of such strategies on the IMC, as conduction losses on CMCs are significantly lower [34].

Some non-linear control strategies applied to the IMC, such as the M^2PC [36], also uses some of the reduced switching losses principles presented in this chapter.

4 ALGORITHMS APPLIED TO MATRIX CONVERTERS

4.1 INTRODUCTION

This chapter presents some algorithms which are useful for a safe operation of matrix converters, and vary from trigonometric function calculations to frequency and phase estimation, while focusing on their FPGA implementations.

Traditionally, of modulation strategies and algorithms necessary for the operation of power converters are implemented using Digital Signal Processors (DSPs), as function libraries and look-up tables generally facilitate the implementation of such algorithms. However, more complex power converters might demand the use of an FPGA allied with the DSP, especially for space-vector modulation techniques. The communication between DSP–FPGA is usually implemented through SPI protocols, which are slow and very susceptible to external noise, reducing the converter reliability.

One alternative is the use of SoC implementations, which usually possesses a microprocessor and a FPGA embedded on the same chip, enabling a parallel communication, albeit increasing the cost. Another alternative is to directly implement these algorithms in the FPGA, which usually represents a complex implementation while eliminating the need for a digital processor. This work aims to develop such solution, while aiming to reduce the resource usage of the FPGA. However, there is a need to develop some ideas of auxiliary algorithms to perform basic tasks, such as the calculation of trigonometric functions.

The calculation of trigonometric functions is present in most of power electronics algorithms, varying from reference generation for carrier-based modulation, space-vector modulation and synchronism algorithms such as FLLs and PLLs. The precision of those algorithms is generally directly related to the resolution of these calculations. The fastest way to perform those functions is through look-up tables. However, the memory usage of those tables is quite large. Another approach is through series expansion. However, the problem lies in the number of multipliers used by the equivalent series, as low-cost FPGAs usually possesses a limited number of DSP blocks to perform fast multiplications. The alternative presented in this chapter is the CORDIC algorithm, which possesses a fast and simple FPGA implementation, since it is composed mostly by additions and bitwise operations.

After introducing a method to calculate trigonometric functions, a discussion on synchronism algorithms and frequency estimators will be presented. These type of algorithms are extremely useful for the interface between two different time-variant systems, as the modulation strategies presented in the previous chapter uses the electrical quantities phase. Also, these algorithms are useful for control strategies, which are usually based on stationary or synchronous reference frames.

Control system of grid connected converters can be grouped into two modes of operation: connected to grid and isolated mode (islanding). The control system is intended to regulate the stability of grid operation, maintaining stability while facing changes in load and assuring a safe interconnection between different networks. A variety of methods and algorithm have been proposed, such as zero crossing methods, Phase/Frequency-Locked Loops (PLLs/FLLs), adaptive filtering-based frequency estimators and recursive state estimation via non-linear estimators.

The study of synchronism algorithms is also important in the study of matrix converters, since the IMC must be able to accurately track the frequency on both rectifier and inverter stages, and is very susceptible to sudden variations. On of the biggest challenges of grid-connected matrix converters is the need for frequency and phase estimation for a wide freuquency range. Usually, the frequency of the rectifier stage might vary around 50 or 60 Hz for the electrical grid. However, the MEAs introduce a need for the converter to operate in a range of frequency between 300 – 800 MHz, and a instant variation of this frequency might damage the converter if the algorithm is not quick enough to perceive such perturbations. Also, the frequency of the inverter stage current stage varies according to the generator rotor velocity for this type of application. Therefore, fast and precise algorithms are indispensable for a correct operation of matrix converters.

4.2 CORDIC ALGORITHM

The CORDIC (COrdinate Rotation DIgital Computer) is a digital signal processing algorithm which enables the implementation of hyperbolic and trigonometric functions without the use of long look-up tables, multipliers and dividers. This method consists of adders and rotations, which possesses an extremely fast and simple FPGA implementation.

This algorithm was initially proposed by J. Volder in 1959 [37], and since then has suffered a few modifications. However, the main idea is to perform a series of rotations of a vector as the following derivation.

In cartesian coordinates, the rotation of a vector $\vec{v}_i$ pertaining to the vector space $\mathbb{R}^2$ by an angle θ can be expressed according to (4.1).

$$\vec{v}_f = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \vec{v}_i \tag{4.1}$$

So, equation (4.1) can be rewritten according to (4.2).

$$\frac{1}{\cos(\theta)} \vec{v}_f = \begin{bmatrix} 1 & -\tan(\theta) \\ \tan(\theta) & 1 \end{bmatrix} \vec{v}_i \tag{4.2}$$

The rotation angles of each iteration must satisfy equation (4.3). This choice replaces the tangent function by a power of two division, which can be translated as a rotation of an integer number in binary representation.

$$\theta_i = \tan^{-1}\left(2^{-i}\right) \tag{4.3}$$

It is possible to define a function σ_i which determines the rotation direction. The rotation equation (4.1) can be rewritten as (4.4), where the iteration number is given by $i \in \mathbb{N}$.

$$\vec{v}_i = \cos\left(\tan^{-1}\left(2^{-i}\right)\right) \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \vec{v}_{i-1} \tag{4.4}$$

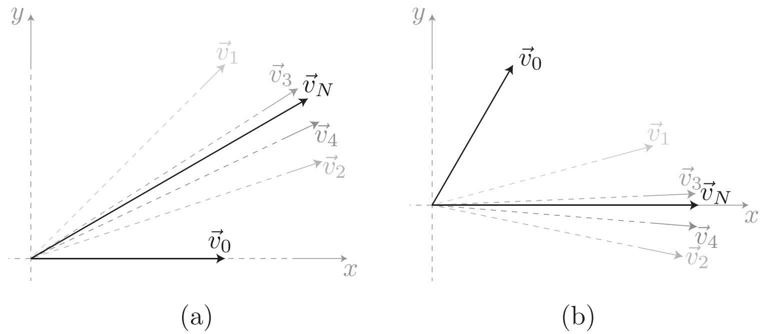
For a number N of iterations, the final vector is defined by equation (4.5), where $\vec{v}_0$ is an initial point.

$$\vec{v}_N = \left(\prod_{i=0}^{N} \cos\left(\tan^{-1}\left(2^{-i}\right)\right) \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \right) \vec{v}_0 \tag{4.5}$$

The constant term of equation (4.5) can be rewritten according to (4.6), and converges after approximately nine iterations to 0.607253. Since the algorithm consists of performing sums and bitwise operations, the gain introduced by each iteration is not taken into account, resulting in a final gain given by k_N^{-1}.

$$k_N = \prod_{i=0}^{N} \cos\left(\tan^{-1}\left(2^{-i}\right)\right) = \prod_{i=0}^{N} \frac{1}{\sqrt{1+2^{-2i}}} \tag{4.6}$$

A third coordinate for $\vec{v}_i$ can be used to obtain the angle, and



(a) (b)

Figure 4.1 – CORDIC algorithm in both rotation and vectoring mode graphic representation. (a) Rotation mode with $\vec{v}_0 = k_N, 0$ and z_0 equal to 30°. (b) Vectoring mode with v_0 as a unitary phasor with angle equal to 30° and z_0 equal to zero.

the method to determine the rotation direction determines which function is performed by the algorithm. The CORDIC algorithm can be described by (4.7).

$$\begin{aligned}\vec{v}_N = \begin{bmatrix} x_N \\ y_N \end{bmatrix} &= k_N \left(\prod_{i=0}^{N} \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \right) \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \\ z_N &= z_0 - \sum_{i=0}^{N} \sigma_i \theta_i \end{aligned} \tag{4.7}$$

The following derivations present two distinct operation modes, resulting two different function sets, traditionally called rotation and vectoring mode.

4.2.1 Rotation Mode

By forcing $\lim_{N\to\infty} z_N$ to zero, the final vector $\vec{v}_N$ results in a rotation of initial vector $\vec{v}_0$ by an angle z_0, according to equation (4.8).

$$\vec{v}_N = k_N^{-1} \begin{bmatrix} \cos(z_0) & -\sin(z_0) \\ \sin(z_0) & \cos(z_0) \end{bmatrix} \vec{v}_0 \tag{4.8}$$

The rotation direction function can be defined according to (4.9) to force the convergence of z_N to zero.

$$\sigma_i = \begin{cases} +1, & z_i \geq 0 \\ -1, & z_i < 0 \end{cases} \tag{4.9}$$

The main idea of this operation mode is illustrated in Figure 4.1a. By forcing $\vec{v}_0 = \{k_N, 0\}$, the algorithm results in a conversion from polar to rectangular of an unitary vector with angle z_0.

4.2.2 Vectoring Mode

The idea of this is to force $\lim_{N\to\infty} y_N$ to zero, obtaining equation (4.10).

$$\begin{aligned} x_N &= k_N^{-1} \left\| \vec{v}_0 \right\|_2 \\ z_N &= z_0 + \tan^{-1} \angle \vec{v}_0 \end{aligned} \tag{4.10}$$

Algorithm 4.1 Fixed-Point CORDIC Algorithm

```
Input: Initial Vector Coordinates $\{x_0, y_0\}$, Initial Angle $z_0$, Rotation Angles $\{\theta_0, \ldots, \theta_N\}$
Output: Output Vector Coordinates $\{v_0, v_1\}$, Output Angle $z$
$\theta \leftarrow \{\theta_0, \ldots, \theta_N\}$
$v \leftarrow \{x_0, y_0\}$
$z \leftarrow z_0$
for $i \leftarrow 0$ to $N$ do
    $w \leftarrow v$
    if rotation mode then
        $\sigma \leftarrow \mathrm{sgn}(z_0)$
    else if vectoring mode then
        $\sigma \leftarrow -\mathrm{sgn}(w_0 w_1)$
    end if
    $v_0 \leftarrow w_0 - \sigma(w_1 >> i)$
    $v_1 \leftarrow w_1 + \sigma(w_0 >> i)$
    $z \leftarrow z - \sigma\theta_i$
end for
```

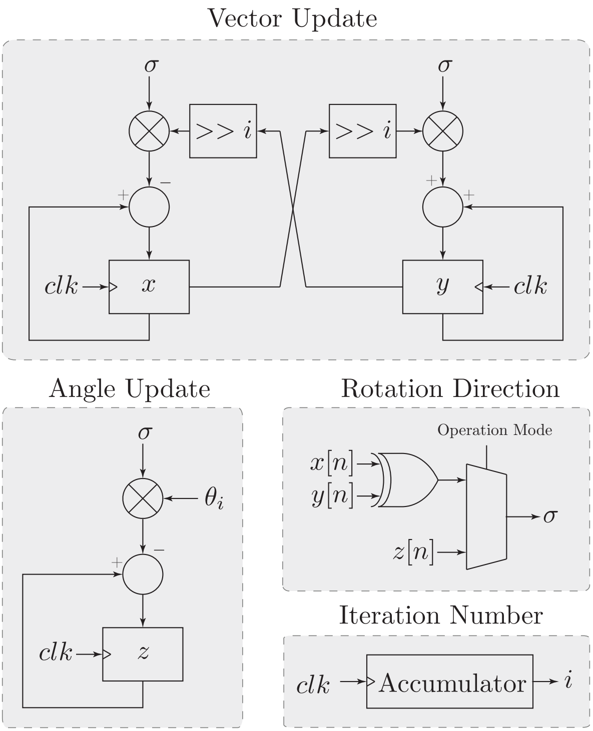

Vector Update
σ
σ
>> i
>> i
−
+
+
+
clk
x
y
clk
Angle Update
σ
θ_i
−
+
clk
z
Rotation Direction
Operation Mode
x[n]
y[n]
z[n]
σ
Iteration Number
clk
Accumulator
i

Figure 4.2 – Recursive CORDIC algorithm FPGA implementation. Variable n indicates the total number of bits.

The rotation direction function can be defined according to (4.11) to force the convergence of y_N.

$$\sigma_i = \begin{cases} +1, & x_i y_i \leq 0 \\ -1, & x_i y_i > 0 \end{cases} \tag{4.11}$$

This operation mode is illustrated in Figure 4.1b. By forcing z_0 to zero, it is possible to directly calculate the norm and angle of a vector.

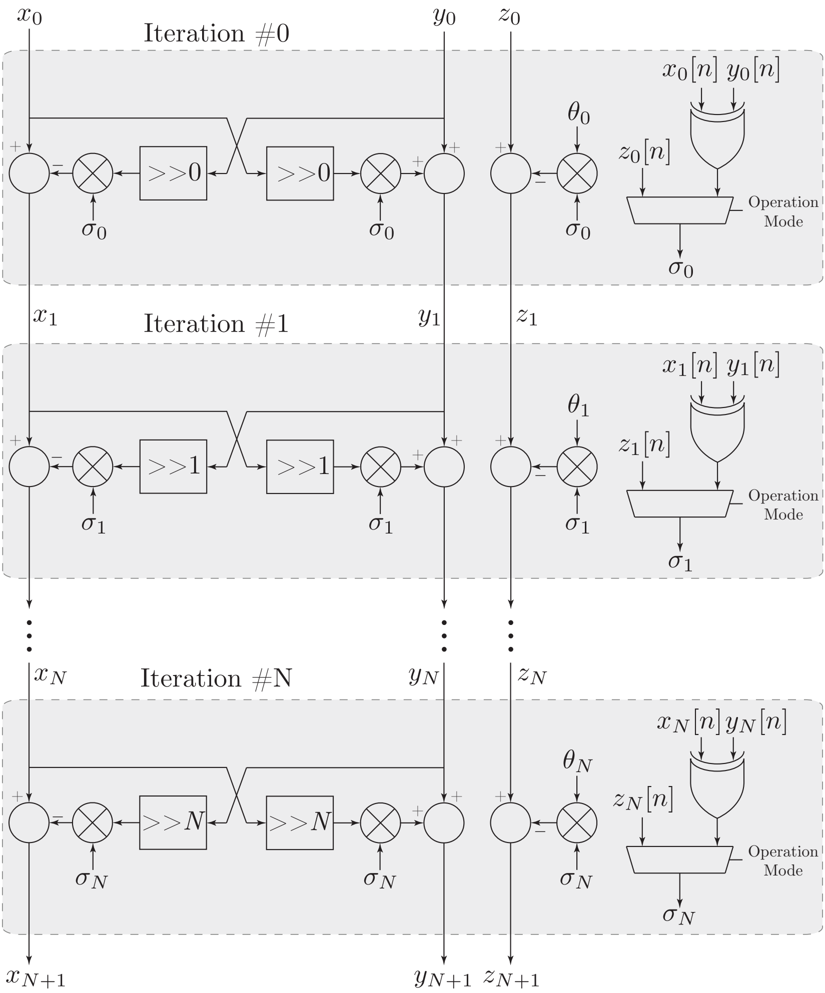

x_0
Iteration #0
y_0
z_0
$x_0[n]$ $y_0[n]$
θ_0
$z_0[n]$
$>>0$
$>>0$
σ_0
Operation Mode
x_1
Iteration #1
y_1
z_1
$x_1[n]$ $y_1[n]$
θ_1
$z_1[n]$
$>>1$
$>>1$
σ_1
x_N
Iteration #N
y_N
z_N
$x_N[n]$ $y_N[n]$
θ_N
$z_N[n]$
$>>N$
$>>N$
σ_N
x_{N+1}
y_{N+1}
z_{N+1}

Figure 4.3 – Pipelined CORDIC algorithm FPGA implementation. Variable n indicates the total number of bits.

4.2.3 Algorithm Implementation

The CORDIC algorithm can be described according to Algorithm 4.1 for a fixed point representation. The rotation angles for this algorithm are always fixed according to equation (4.3) and must be previously calculated.

Since the algorithm uses a fixed-point representation, we can assume that the variables uses a generic Q_n base. For small angles, the trigonometric function $\tan x$ is approximately equal to the angle x. Therefore, θ_n is equal to $1Q_n$, which is the smallest possible representation, limiting the maximum number of iterations to $n+1$.

A possible FPGA implementation, illustrated by Figure 4.2 uses three n-bit registers for v and and z, as well as N n-bit registers for angles $\{\theta_0, \ldots, \theta_n\}$. The greatest advantage of this implementation is the resource usage, although the algorithm performance is hindered, since the execution time is always known and equal to Nt_{clk}, where t_{clk} is the inverse of clock frequency f_{clk}.

For a faster implementation, a pipelined structure is recommended, which is illustrated in Figure 4.3. Since the algorithm execution time depends on the delay of each operation, as well as the path defined by the compiler, although time estimations can be performed. However, the proposed implementation is significantly faster than the recursive strategy, but the resource usage is much larger. An execution time of approximately 100 ns was verified for a nineteen iteration pipelined algorithm. Since the delay between input and output might not satisfy timing constraints, the proposed strategy may require pipeline registers to guarantee the implementation stability.

4.3 PHASE-LOCKED LOOPS

Phase-Locked Loops are synchronism algorithms originated in communication theory and are widely used in Power Electronics in grid-tied connections. These algorithms aim to estimate frequency and phase of electrical quantities, and are widely used in grid tied applications. There is a wide range of different strategies, although most follow a generic structure.

One of the advantages of three-phase power systems is the obtention of two orthogonal vectors by using a stationary reference frame through the use of the Clarke transformation, resulting in the pq theory, which will be further discussed in this section, improving the dynamic behaviour of traditional PLLs.

As previously discussed, the use of such algorithms are also fundamental for the correct operation of the indirect matrix converter, as the presented modulation strategies are dependant on the estimated phase to accurately synthesize the electric quantities.

4.3.1 General Phase-Locked Loop Analysis

The phase-locked loop is an algorithm for phase and frequency estimation based on the generation of an orthogonal component, according to Figure 4.4. The structure contains a phase detector, a loop filter (in this case a low-pass filter) to reject noise and perturbations of the estimated quantities, as well as a voltage controlled oscillator (VCO) to generate a component orthogonal to the reference signal.

Let $\bar{v}$ a pure sinusoidal input signal and $\hat{v}$ the PLL output signal according to (4.12).

$$\begin{aligned} \bar{v} &= V^{pk}\sin\left(\omega t+\varphi\right) \\ \hat{v} &= V^{pk}\cos\left(\hat{\omega} t+\hat{\varphi}\right) \end{aligned} \tag{4.12}$$

The output of the phase detector is given by (4.13), and since line filter eliminates the high frequency component, the VCO input is given by (4.14).

$$\xi_{pd} = \frac{1}{2}k_{pd}V^{pk}\big(\underbrace{\sin\left(\left(\omega-\hat{\omega}\right)t+\varphi-\hat{\varphi}\right)}_{\text{Low Frequency}}+\underbrace{\sin\left(\left(\omega+\hat{\omega}\right)t+\varphi+\hat{\varphi}\right)}_{\text{High Frequency}}\big) \tag{4.13}$$

$$\xi_{lf} = \frac{1}{2}k_{pd}V^{pk}\sin\left(\left(\omega-\hat{\omega}\right)t+\varphi-\hat{\varphi}\right) \tag{4.14}$$

Assuming that the frequency estimation error is sufficiently small, the VCO input can be approximated according to (4.15).

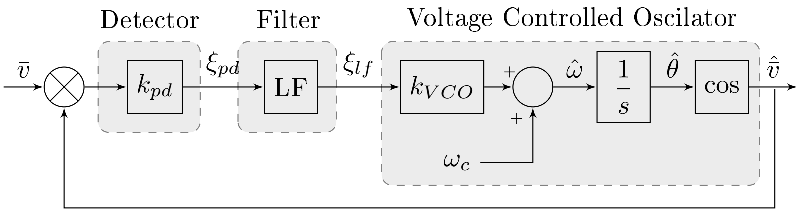


Figure 4.4 – Block diagram of a generic PLL, which is base for the SRF-PLL, as the input can be obtained through the Park transformation.

$$\xi_{lf} = \frac{1}{2} k_{pd} V^{pk} \sin\left(\varphi - \hat{\varphi}\right) \tag{4.15}$$

Using the first term of the Taylor series of equation (4.15) centred in the origin yields (4.16), thus obtaining a system linearization valid for a sufficiently small difference between phase angles.

$$\underline{\xi}_{lf} \approx \frac{1}{2} k_{pd} V^{pk} \left(\theta - \hat{\theta}\right) \tag{4.16}$$

Equation (4.17) thus presents an expression for the estimated frequency.

$$\underline{\hat{\omega}} = \omega_c + \frac{1}{2} k_{pd} k_{VCO} V^{pk} \left(\theta - \hat{\theta}\right) \tag{4.17}$$

An inherent phase-displacement θ_{dis} is inserted in the system by the input filter, which can be calculated through the Fourier transform of the filter according to (4.18).

$$\theta_{dis} = \angle k_{pd} k_{VCO} \overline{\mathrm{LF}}(\omega_c) \tag{4.18}$$

According to classical control theory, the SRF-PLL has a good performance around its equilibrium point. Since linearization techniques were used around an equilibrium point, the dynamic response of the Loop Filter must be able to satisfy the frequency variations given by (4.17). The IMC electric quantities possesses variable frequency, resulting in a constant change in the operation point, thus creating a need for different structures which may operate without a fixed point of operation.

4.3.2 pq Theory-based Phase-Locked Loop

Using the results presented in Appendix B, unitary voltage phasor $\bar{v}$ and current phasor $\bar{i}$ can be expressed according to equation (4.19).

$$\begin{aligned} \bar{v} &= v_\alpha + j v_\beta = e^{j(\omega t + \varphi)} \\ \bar{i} &= i_\alpha + j i_\beta = e^{j(\hat{\omega} t + \hat{\varphi})} \end{aligned} \tag{4.19}$$

A power phasor $\bar{s}$ can be obtained multiplying both voltage and current phasors, according to (4.20).

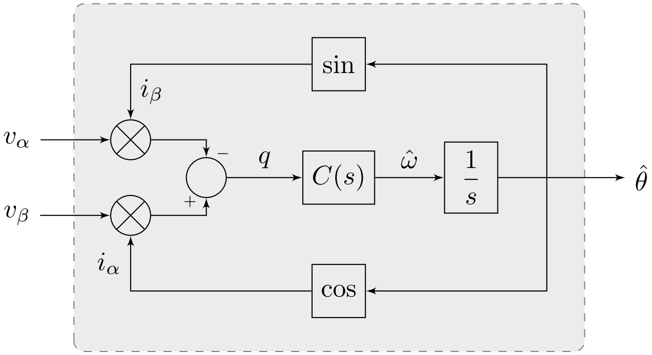


Figure 4.5 – qPLL implementation block diagram.

$$\bar{s} = \bar{v}\bar{i}^* = e^{j((\omega-\hat{\omega})t+\varphi-\hat{\varphi})} \tag{4.20}$$

The power phasor can be further decomposed into (4.21).

$$\begin{aligned} \bar{s} &= p + jq \\ p &= \cos\left((\omega-\hat{\omega})\,t + \varphi - \hat{\varphi}\right) \\ q &= \sin\left((\omega-\hat{\omega})\,t + \varphi - \hat{\varphi}\right) \end{aligned} \tag{4.21}$$

Algorithm 4.2 qPLL Algorithm with a Second Order Line Filter

```
Input: Voltage Components $v_\alpha$ and $v_\beta$, Line Filter Constants $A$ and $B$, Sampling Time $T_a$
Output: Estimated Angle $\theta_0$
$\theta_1 \leftarrow \theta_0$
for $i \leftarrow 2$ to $1$ do
    $q_i \leftarrow q_{i-1}$
    $\omega_i \leftarrow \omega_{i-1}$
end for
$v \leftarrow \{v_\alpha, v_\beta\}$
$q \leftarrow v_1 \cos\theta_0 - v_0 \sin\theta_0$
$\omega_0 \leftarrow A_0 q_0 + A_1 q_1 + A_2 q_2 + B_1 \omega_1 + B_2 \omega_2$
$\theta_0 \leftarrow \theta_1 + 0.5 T_a (\omega_0 + \omega_1)$
if $(\theta_0 > 2\pi)$ then
    $\theta_0 \leftarrow \theta_0 - 2\pi$
end if
```

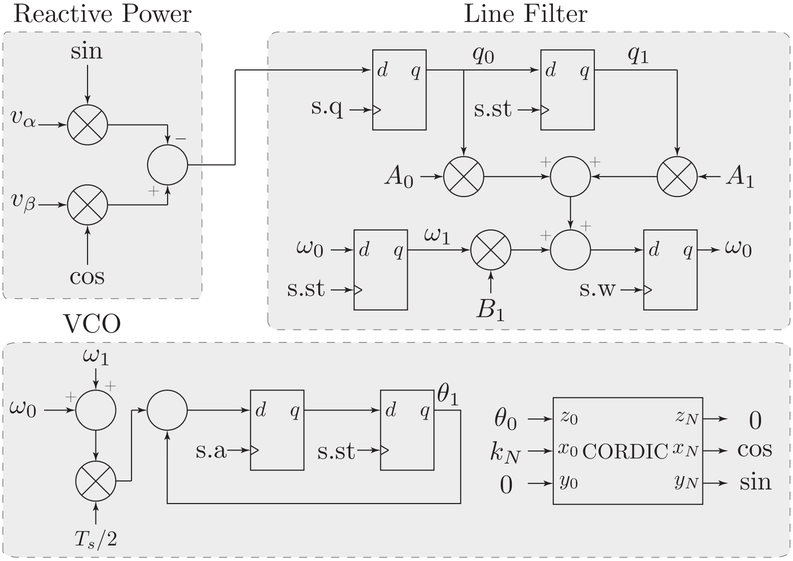

Reactive Power
sin
v_α
v_β
cos
−
+
Line Filter
d q
q_0
q_1
s.q
s.st
A_0
A_1
+
ω_0
ω_1
s.st
B_1
s.w
ω_0
VCO
ω_1
ω_0
$T_s/2$
θ_1
s.a
s.st
θ_0
k_N
0
z_0
x_0
y_0
CORDIC
z_N
x_N
y_N
0
cos
sin

Figure 4.6 – FPGA implementation of a qPLL using CORDIC.

The pq theory-based PLLs uses the naturally orthogonal components present in voltage and current phasors to reduce the constraints on the line filter, obtaining in (4.21) a similar equation to (4.14) on the output of the line filter. Two different topologies can be obtained from this theory, the pPLL based on the three-phase active power and the qPLL based on the reactive power, presented in Figure 4.5. Since the active power is different from zero in steady-state, the qPLL topology is preferred.

The algorithm for the qPLL implementation is described in Algorithm 4.2. The CORDIC algorithm in rotation mode previously presented can be used for the calculation trigonometric functions needed by the qPLL algorithm in an FPGA implementation. Figure 4.6 presents a block diagram of the FPGA implementation, while Figure 4.7 presents the finite-state machine (FSM) which manages the algorithm. The whole system waits for an interruption, going from state *s.hold* to state *s.st*, which is responsible to store the previous values of $\{q, \omega, \theta\}$. During state $s.q$, the present reactive power register updates its value. After that, the current frequency and angle values are update in states $s.w$ and $s.a$, respectively.

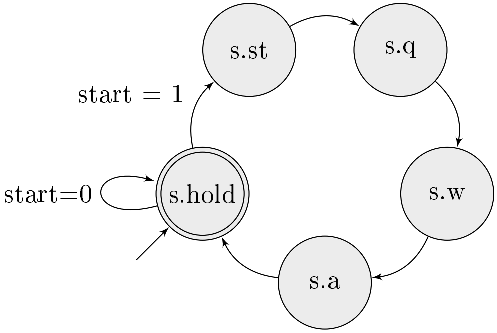


Figure 4.7 – Finite-state machine of the qPLL FPGA implementation.

Similarly to the SRF-PLL, the qPLL possesses the same problems due to a linearization performed in the VCO stage. However, the effects are much smaller since the equilibrium point is dynamic. Also, this algorithm is not valid for unbalanced voltage grids, since equation (4.19) is only valid for circular trajectories, object of study of the next section.

4.4 FREQUENCY DETECTION ALGORITHMS

Frequency detections algorithms are useful for different control strategies, such as resonant controllers, and for fault detections. A reliable algorithm must be able to detect the grid frequency under fault conditions and for a wide range frequency in some special cases, such as the More Electric Aircrafts (MEAs).

The least mean squares (LMS) are a class of adaptive filter which uses the mean square error of an estimated signal to mimic a determined system behaviour. It was invented in 1960 by Bernard Widrow and Ted Hoff [38], and is widely used due to its similar characteristics to the Kalmann Filter, providing a fast adaptive response and noise rejection. Algorithms based on the LMS filter inherit its fast response, while facing stability issues and internal noise due to limit cycle and quantization noise.

The estimated frequency can be used as a feed-forward compensation of the VCO of the PLL strategies previously presented or used for syntonization of low-pass filters.

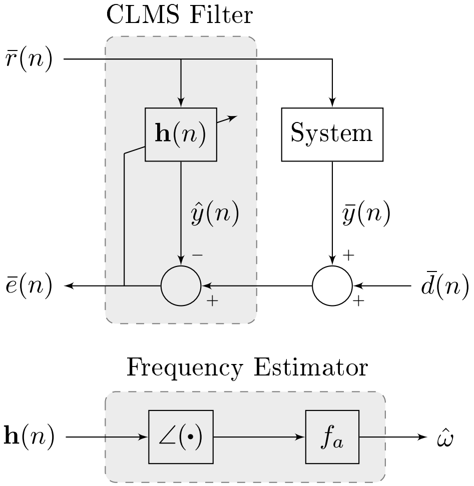

CLMS Filter
$\bar{r}(n)$
$\mathbf{h}(n)$
System
$\hat{y}(n)$
$\bar{y}(n)$
$-$
$+$
$+$
$+$
$\bar{e}(n)$
$\bar{d}(n)$
Frequency Estimator
$\mathbf{h}(n)$
$\angle(\bullet)$
f_a
$\hat{\omega}$

Figure 4.8 – CLMS based frequency detector block diagram.

4.4.1 Complex Least Mean Squares Filter-based Frequency Estimator

Since the projection of a vector pertaining to a three-phase system on the $\alpha\beta$ plane can be described by a complex phasor $\bar{r}$, a complex version of the LMS (CLMS) filter must be used. Concepts used as basis for the formulation of the estimator are presented in Appendix B.

The CLMS formulation is given by (4.22) according to [38], where e is the error between the output $\bar{y}$ and the estimated output, given by the estimated system $\mathbf{h}$ and the input $\bar{r}$.

$$\begin{aligned} \hat{y}(n) &= \mathbf{h}^H(n)\bar{r}(n) \\ \bar{e}(n) &= \bar{y}(n) - \hat{y}(n) \\ \mathbf{h}(n+1) &= \mathbf{h}(n) + \mu\bar{e}^*(n)\bar{r}(n) \end{aligned} \tag{4.22}$$

Let $\bar{r}$, given by equation (4.23), which describes a circular trajectory in the $\alpha\beta$ plane, represent a three-phase system under balanced conditions.

$$\bar{r}(n) = \frac{3}{2}k_m R^{pk} e^{j\omega k T_a} \tag{4.23}$$

The estimated system output can be written as (4.24) by using a strictly linear estimator (SLE).

$$\hat{y}(n) = \bar{r}(n+1) = \frac{3}{2} k_m R^{pk} e^{j\hat{\omega}(n+1)T_a} \tag{4.24}$$

By inspection, the system $\mathbf{h}$ can be expressed by (4.25), and describes a rotation by an angle $\hat{\omega}T_a$.

$$\mathbf{h}(n) = e^{j\hat{\omega}T_a} \tag{4.25}$$

The grid frequency can be estimated by rewriting equation (4.25), obtaining expression (4.26).

$$\hat{\omega} = f_a \tan^{-1} \frac{\Im\{\mathbf{h}(n)\}}{\Re\{\mathbf{h}(n)\}} \tag{4.26}$$

However, if the the system is unbalanced, then $\bar{r}$ will be described by (4.27). Therefore, equation (4.25) is not valid anymore, since the input trajectory is non-circular.

$$\begin{aligned} \bar{r}(n) &= \frac{1}{2} k_m \left(R_a + R_b + R_c\right) e^{j\omega k T_a} \\ &+ \left(\frac{1}{2} k_m \left(2R_a - R_b - R_c\right) + j\frac{\sqrt{3}}{2} k_m \left(R_c - R_b\right)\right) e^{-j\omega k T_a} \end{aligned} \tag{4.27}$$

The algorithm for implementing the CLMS frequency estimator is described in Algorithm 4.3, and the block diagram is presented in Figure 4.8. The CORDIC algorithm operating in vectoring mode can be used to compute the inverse trigonometrical function, which normally possesses a high computational burden.

4.4.2 Augmented Complex Least Mean Squares Filter-based Frequency Estimator

Differently from the CLMS-based algorithm, the ACLMS-based frequency detector uses a widely linear estimator (WLE) to estimate the system output [39].

Since the input vector positive and negative sequence components are orthogonal, this technique provides a mean to estimate two distinct orthogonal system, here called $\mathbf{h}$ and $\mathbf{g}$, for each sequence component. The algorithm formulation changes from (4.22) to (4.28).

Algorithm 4.3 CLMS-based Frequency Estimator

```
Input: Voltage Vector $\bar{v} = \{v_\alpha, v_\beta\}$, Sampling Frequency $f_a$
Output: Grid Frequency $\hat{\omega}$
Comments: Index 0 indicates the real part and index 1 indicates imaginary part.
$e_0 \leftarrow y_0 - h_0 v_0 - h_1 v_1$
$e_1 \leftarrow y_1 + h_1 v_0 - h_0 v_1$
$h_0 \leftarrow h_0 + \mu\left(e_0 v_0 + e_1 v_1\right)$
$h_1 \leftarrow h_1 + \mu\left(e_0 v_1 - e_1 v_0\right)$
$\hat{\omega} \leftarrow f_a \tan^{-1}\left(h_1/h_0\right)$
```

$$\begin{aligned} \hat{y}(n) &= \mathbf{h}^H(n)\bar{r}(n) + \mathbf{g}^T(n)\bar{r}^*(n) \\ \bar{e}(n) &= \bar{y}(n) - \hat{y}(n) \\ \mathbf{h}(n+1) &= \mathbf{h}(n) + \mu\bar{e}^*(n)\bar{r}(n) \\ \mathbf{g}(n+1) &= \mathbf{g}(n) + \mu\bar{e}^*(n)\bar{r}^*(n) \end{aligned} \tag{4.28}$$

So, a generic input phasor $\bar{r}$ can be written as Figure 4.29. Keeping in mind that such vector possesses the same formulation as (4.27).

$$\bar{r}(n) = \bar{r}_p(n)e^{j\omega k T_a} + \bar{r}_n(n)e^{-j\omega k T_a} \tag{4.29}$$

The output y can be written as the next-step input, according to (4.30).

$$\bar{y}(n) = \bar{r}_p(n+1)e^{j\omega(n+1)T_a} + \bar{r}_n(n+1)e^{-j\omega(n+1)T_a} \tag{4.30}$$

According to the ACLMS filter formulation described in (4.28), the estimated output can be written as (4.31) using a widely linear estimator.

$$\begin{aligned} \hat{y}(n) = &\left(\bar{r}_p(n)\mathbf{h}(n) + \bar{r}_n^*(n)\mathbf{g}(n)\right)e^{j\hat{\omega}(n+1)T_a} \\ &+ \left(\bar{r}_p^*(n)\mathbf{g}(n) + \bar{r}_n(n)\mathbf{h}(n)\right)e^{-j\hat{\omega}(n+1)T_a} \end{aligned} \tag{4.31}$$

Equaling (4.30) and (4.31) results in a set of two equations given by (4.32) and (4.33).

$$e^{j\hat{\omega}T_a} = \frac{\bar{r}_p(n)\mathbf{h}(n) + \bar{r}_n^*(n)\mathbf{g}(n)}{\bar{r}_p(n+1)} \tag{4.32}$$

$$e^{-j\hat{\omega}T_a} = \frac{\bar{r}_p^*(n)\mathbf{g}(n) + \bar{r}_n(n)\mathbf{h}(n)}{\bar{r}_n(n+1)} \tag{4.33}$$

Equation (4.34) can be rewritten as by taking the conjugate on both sides of the equation.

$$e^{j\hat{\omega}T_a} = \frac{\bar{r}_p(n)\mathbf{g}^*(n) + \bar{r}_n^*(n)\mathbf{h}^*(n)}{\bar{r}_n^*(n+1)} \tag{4.34}$$

Assuming an operation in steady-state, the sequence components $\bar{r}_p$ and $\bar{r}_n$ can be considered constants, together with the fact that $\bar{r}_p$ is real valued, equaling equations (4.32) and (4.34) result in a second order system given by (4.35).

$$\begin{aligned} \mathbf{g}(n)a^2(n) + \left(\mathbf{h}(n) - \mathbf{h}^*(n)\right)a(n) - \mathbf{g}^*(n) = 0 \\ a(n) = \left(\frac{\bar{r}_n(n)}{\bar{r}_p(n)}\right)^* \end{aligned} \tag{4.35}$$

An analysis of the discriminant of equation (4.35) is given by (4.36).

$$\begin{aligned} \Delta &= \sqrt{\left(\mathbf{h}(n) - \mathbf{h}^*(n)\right)^2 + 4\left\|\mathbf{g}(n)\right\|^2} \\ &= 2\sqrt{-\Im\left\{\mathbf{h}(n)\right\}^2 + \left\|\mathbf{g}(n)\right\|^2} \end{aligned} \tag{4.36}$$

So, equation (4.35) possesses two solutions, as described in (4.37). For complex valued solutions, the discriminant must be complex valued.

$$\begin{aligned} a_1(n) &= -j\frac{\Im\left\{\mathbf{h}(n)\right\} - \sqrt{-\Im\left\{\mathbf{h}(n)\right\}^2 + \left\|\mathbf{g}(n)\right\|^2}}{\mathbf{g}(n)} \\ a_2(n) &= -j\frac{\Im\left\{\mathbf{h}(n)\right\} + \sqrt{-\Im\left\{\mathbf{h}(n)\right\}^2 + \left\|\mathbf{g}(n)\right\|^2}}{\mathbf{g}(n)} \end{aligned} \tag{4.37}$$

The imaginary part of $e^{j\hat{\omega}T_a}$ is positive-valued, as the sampling frequency is much lower than the grid frequency. The grid frequency can be estimated according to (4.38).

$$\hat{\omega}(n) = f_a \tan^{-1}\left(\frac{\Im\left\{\mathbf{h}(n) + a_1(n)\mathbf{g}(n)\right\}}{\Re\left\{\mathbf{h}(n) + a_1(n)\mathbf{g}(n)\right\}}\right) \tag{4.38}$$

Equation (4.38) can be further simplified for a complex valued

Algorithm 4.4 ACLMS-based Frequency Estimator

```
Input: Voltage Vector $\bar{v} = \{v_\alpha, v_\beta\}$, Sampling Frequency $f_a$
Output: Grid Frequency $\hat{\omega}$
Comments: Index 0 indicates the real part and index 1 indicates imaginary part.
$e_0 \leftarrow y_0 - (h_0 + g_0)v_0 - (h_1 - g_1)v_1$
$e_1 \leftarrow y_1 + (h_1 + g_1)v_0 - (h_0 - g_1)v_1$
$h_0 \leftarrow h_0 + \mu\,(e_0 v_0 + e_1 v_1)$
$h_1 \leftarrow h_1 + \mu\,(e_0 v_1 - e_1 v_0)$
$g_0 \leftarrow g_0 + \mu\,(e_0 v_0 - e_1 v_1)$
$g_1 \leftarrow g_1 - \mu\,(e_0 v_1 + e_1 v_0)$
$b \leftarrow h_1^2 - g_0^2 - g_1^2$
if $b > 0$ then
    $\hat{\omega} \leftarrow f_a \tan^{-1}\left(\sqrt{b}/h_0\right)$
else
    $\hat{\omega} \leftarrow 0$
end if
```

discriminant, resulting in (4.39).

$$\hat{\omega}(n) = f_a \tan^{-1}\left(\frac{\sqrt{\Im\{\mathbf{h}(n)\}^2 - \|\mathbf{g}(n)\|^2}}{\Re\{\mathbf{h}(n)\}}\right) \tag{4.39}$$

The complexity of the ACLMS algorithm implementation is quite higher than the CLMS, since there is a need to compute the square root function besides the inverse trigonometric function, although it is possible to alter the CORDIC algorithm presented in this work to calculate the function. Otherwise, there needs to be a lookup-table to perform such calculations. The algorithm for the widely linear frequency estimator is described in Algorithm 4.4. If **g** vanishes, the ACLMS based algorithms turns into the CLMS.

4.4.3 Simulation and Analysis of LMS-based Frequency Estimation Algorithms

The presented CLMS and ACLMS-based algorithms inherit the fast response and noise rejection inherent to the LMS filter. The ACLMS algorithm assumes a complex rotation of the projection on the $\alpha\beta$ plane, which turns into a simple rotation of the positive sequence us-

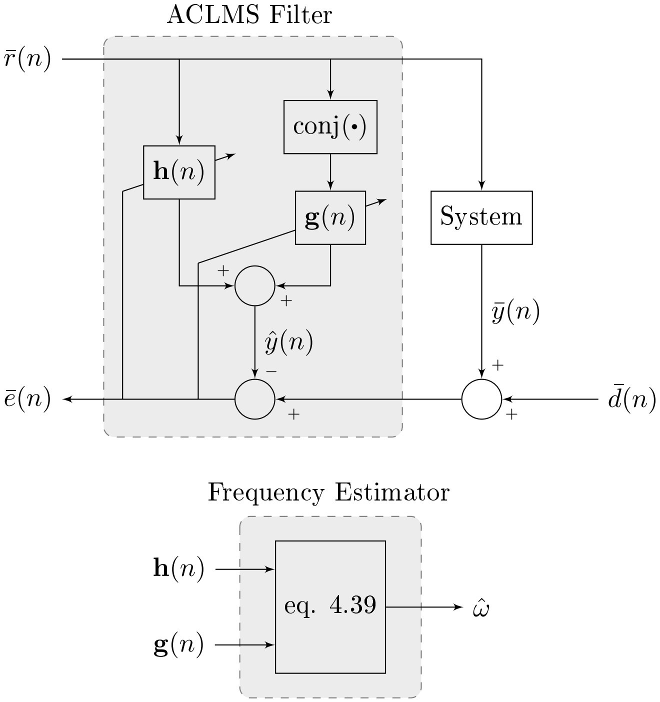

ACLMS Filter
$\bar{r}(n)$
conj(•)
$\mathbf{h}(n)$
$\mathbf{g}(n)$
System
+
+
$\hat{y}(n)$
−
$\bar{y}(n)$
+
$\bar{e}(n)$
+
+
$\bar{d}(n)$
Frequency Estimator
$\mathbf{h}(n)$
eq. 4.39
$\hat{\omega}$
$\mathbf{g}(n)$

Figure 4.9 – ACLMS based frequency detector block diagram.

ing the symmetric components theory presented in Appendix B. If the negative sequence component vanishes, the voltage vector has a circular trajectory, and the CLMS algorithm can be used to accurately estimate the frequency. An example of trajectories is shown in Figure 4.10.

Choosing an optimal adaptive gain μ proves to be difficult, since the signal amplitude is time variant. So, a smaller gain must be chosen to guarantee a safe operation. An alternative is the use of a normalized LMS filter, which solves some of the instabilities, albeit increasing the computational effort.

Figure 4.11 shows a complete simulation of the parameters of the ACLMS-based algorithm for an adaptive gain of 0.1, demonstrating that the algorithm accurately estimates the grid frequency in unbalanced conditions. The settling time for the estimated frequency is approximately one cycle of the grid voltage, which can be further improved by elevating the adaptive gain and/or sampling frequency.

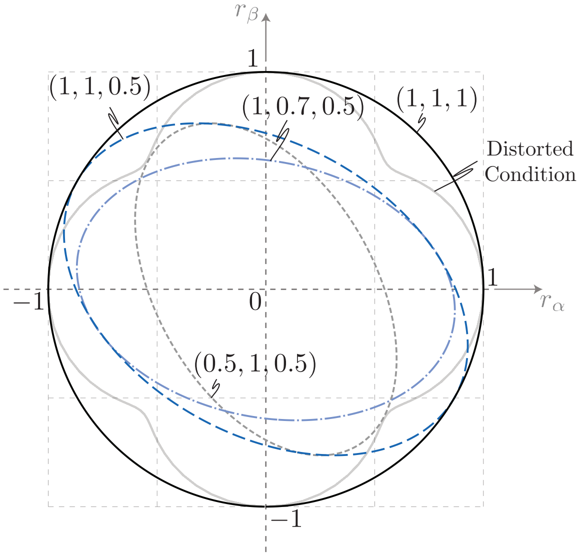


Figure 4.10 – Trajectory of the projection $\bar{r}$ of a generic three-phase vector with amplitudes (R_a, R_b, R_c) on the $\alpha\beta$ plane. Emphasis on the non-circularity of the voltage vector under unbalanced or distorted conditions.

A comparison between the CLMS and ACLMS-based methods using the same adaptive gain is presented in Figure 4.12 for four different conditions: voltage unbalanced voltage, phase unbalanced voltages, frequency step and under distorted conditions. The ACLMS-based frequency estimator has a better performance if compared to the other method for most of the cases presented. However, it is possible to notice that the algorithm performs poorly under distorted grid voltages.

One of the issues of the proposed algorithm is that the input was assumed as a perfect sinusoidal signal, which is an idealized condition. Since the LMS filter possesses a fast dynamic response, low frequency harmonics induce a variation in the estimated frequency, and analog filters introduce a slower dynamic.

The greatest difficulty of implementing the algorithms lies in performing the inverse trigonometric and square root functions with a sufficient precision. The grid frequency can be described as a functions of the method and the sampling frequency, as shown in (4.40). The sampling frequency is much higher than the grid frequency, as the gain

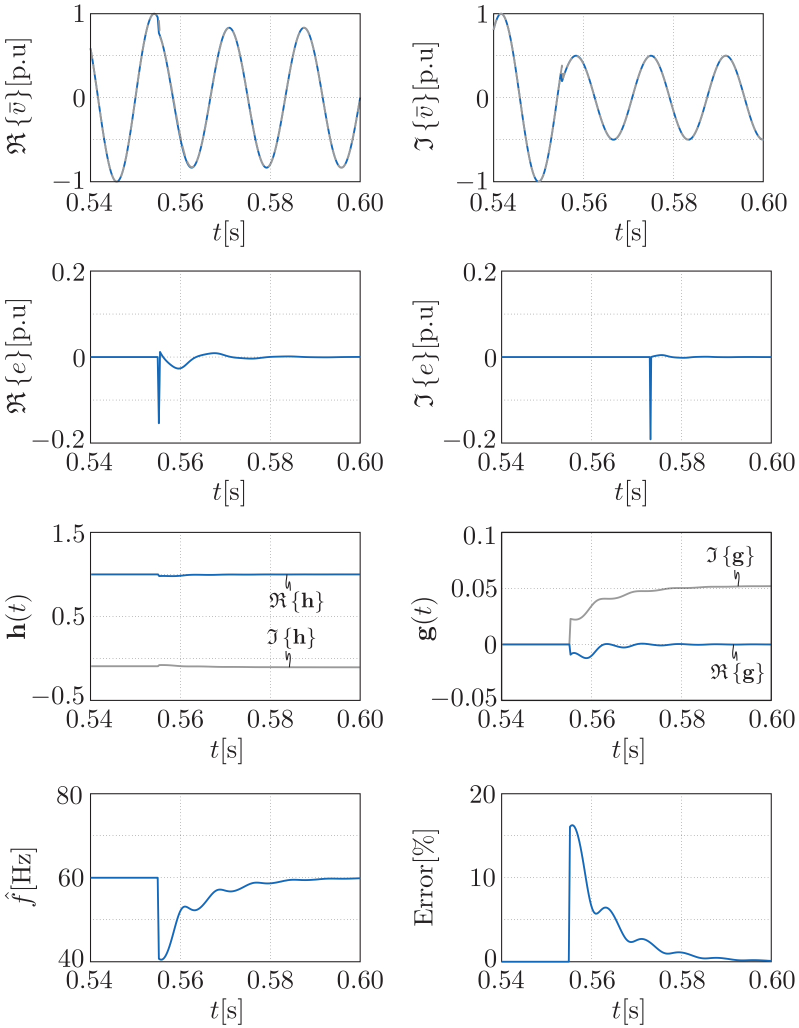


Figure 4.11 – Simulation of the ACLMS-based frequency estimator with sampling frequency of 3.84 kHz and grid frequency of 60 Hz for a voltage step of (1,1,1) p.u. to (1,0.5,0.5) p.u. at $t = 0.555$s and an adaptive gain μ equal to 0.1.

k_{LMS} is very small, and the higher the sampling frequency the smaller the gain. Therefore, a higher sampling frequency results in more bits

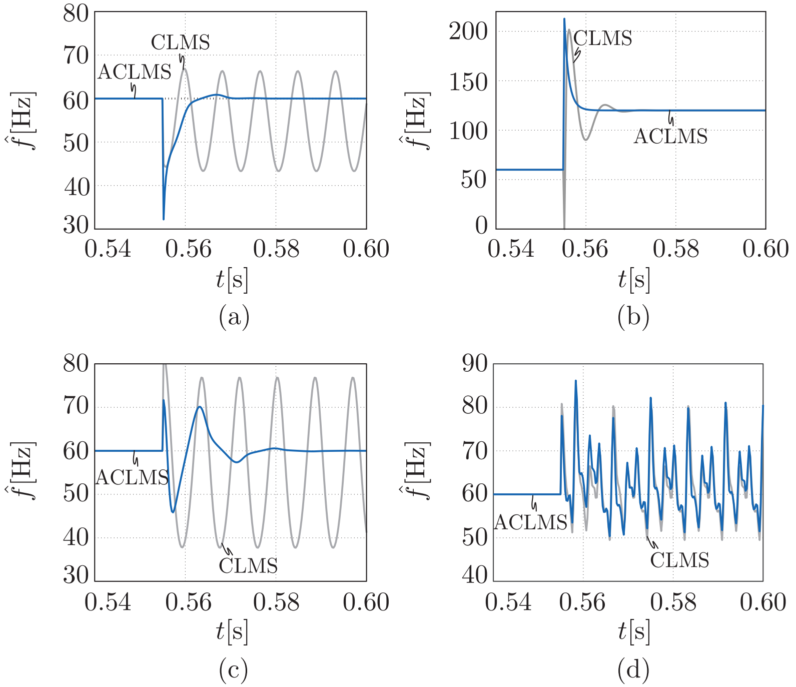


Figure 4.12 – Simulation of the CLMS and ACLMS-based frequency estimator with sampling frequency equal to 3.84 kHz under different conditions. (a) Voltage unbalance from $(1, 1, 1)$ p.u. to $(1, 0.5, 0.5)$ p.u. (b) Frequency step from 60 Hz to 120 Hz. (c) Phase unbalance of $+30^{o}$ for phase b and -30^{o} for phase c. (d) Distorted grid with 5% 5th harmonic, 4% 7th harmonic, 3% 11th harmonic, 2% 13th harmonic and 1% 17th harmonic.

necessary to accurately represent the estimated frequency.

$$k_{LMS} = \frac{\hat{\omega}}{f_s} \tag{4.40}$$

Since the gain is a result of an inverse trigonometric function, the resolution of the CORDIC algorithm and the square root function directly affects the resolution of the estimation. However, the implemented estimation was able to accurately estimate the frequency under unbalanced conditions.

An FPGA implementation of the ACLMS-based algorithm was proposed in [40]. A 15-bit input 16-bit output look-up table was implemented to calculate the square root function and a 18-bit CORDIC algorithm was used to calculate the inverse trigonometric function, with signals implemented using a Q_{18} fixed point representation. The experimental results for three different cases are presented in Figure 4.13. It is possible to notice that the LSB does not vary due to the precision of the 16-bit look-up table.

4.5 CONCLUSION

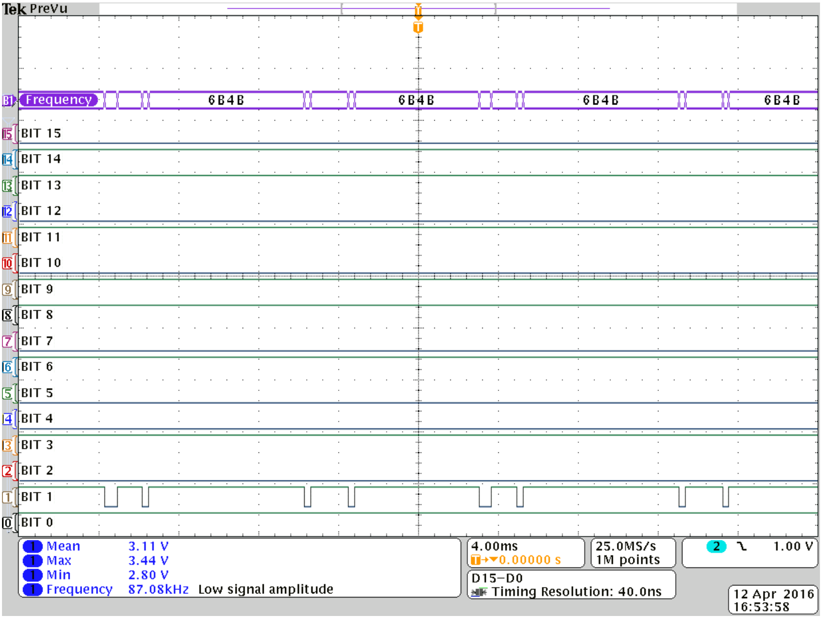
This chapter presented a collection of algorithms which are useful for the operation of an indirect matrix converter. A pseudo-code along with the FPGA implementation were presented for most of the discussed algorithms.

The CORDIC algorithm is useful for many different algorithms, and can perform many different functions. The operation modes described in the previous section were the used to implement the calculation of vector times and phase estimations in a FPGA. The use of the proposed structure to perform trigonometric functions eliminates the need for look up tables, hence reducing the resource usage, and provides a way to perform very precise calculations with a short execution time.

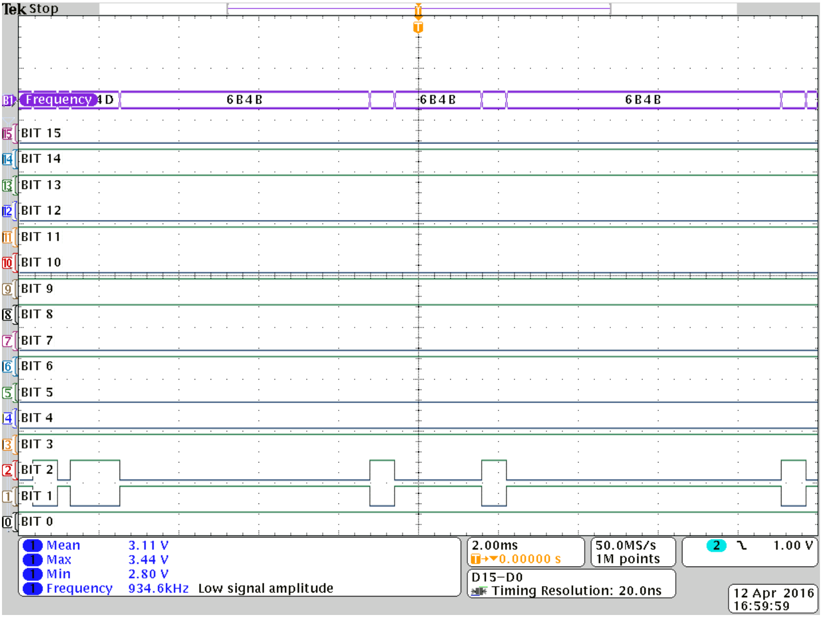
The synchronism algorithms presented in this chapter are useful for phase estimation, which is employed by the space vector modulation presented in the previous chapter. The presented PLL structures are a base for many different algorithms. However, the problem of the operation around a single operation point as demonstrated for the SRF-PLL limits its use for frequency varying grids, such as the ones present in MEAs, thus creating a need for algorithms which do not operate around a point of equilibrium.

One alternative are the LMS-based algorithms, which possesses a inherent fast response. However, due to its fast response, these algorithms are very susceptible to grid distortions, as shown in simulations considering voltage harmonics, as the trajectory of the positive sequence is not circular under distorted conditions.

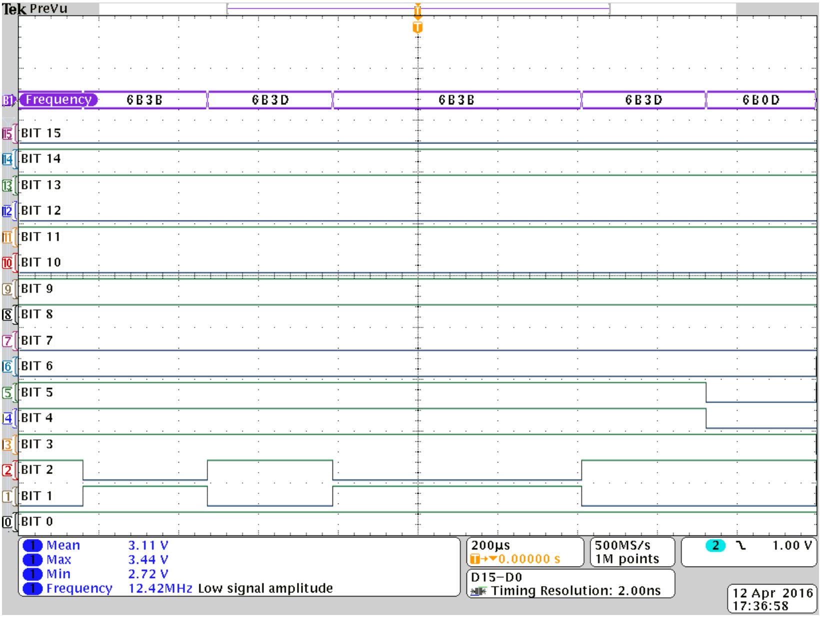
The collections of algorithms shown in this chapter serves as a base for the indirect matrix converter modulation implementation, which is the topic of the next chapter. Therefore, experimental results for the proposed algorithms will be further discussed.


Tek PreVu
Frequency
6B4B
6B4B
6B4B
6B4B
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
Mean 3.11 V
Max 3.44 V
Min 2.80 V
Frequency 87.08kHz Low signal amplitude
4.00ms
0.00000 s
25.0MS/s
1M points
2 1.00 V
D15–D0
Timing Resolution: 40.0ns
12 Apr 2016
16:53:58

(a)


Tek Stop
Frequency
4D
6B4B
6B4B
6B4B
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
Mean 3.11 V
Max 3.44 V
Min 2.80 V
Frequency 934.6kHz Low signal amplitude
2.00ms
0.00000 s
50.0MS/s
1M points
2 1.00 V
D15–D0
Timing Resolution: 20.0ns
12 Apr 2016
16:59:59

(b)


Tek PreVu
B1 Frequency
6B3B
6B3D
6B3B
6B3D
6B0D
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0

Mean 3.11 V
Max 3.44 V
Min 2.72 V
Frequency 12.42MHz Low signal amplitude
200µs
0.00000 s
500MS/s
1M points
2 1.00 V
D15–D0
Timing Resolution: 2.00ns
12 Apr 2016
17:36:58

(c)

Figure 4.13 – Estimated frequency of a FPGA based widely linear frequency estimation for different conditions. (a) Balanced voltages, with frequency varying between 60.029 Hz ($6B4B_{16}$) and 60.033 Hz ($6B4B_{16}$). (b) Phase unbalance of $+12^{\circ}$ on phase b and -12° on phase c, with the estimated frequency varying between 60.033 Hz ($6B4B_{16}$) and 60.038 Hz ($6B4D_{16}$). (c) Phase and voltage unbalance of $(1, 0.5, 0.5)$, with the estimated frequency varying between 59.998 Hz ($6B3B_{16}$), 60.003 Hz ($6B3D_{16}$), and 59.898 Hz ($6B0D_{16}$).

5 MODULATION DESIGN AND EXPERIMENTAL RESULTS

5.1 INTRODUCTION

This chapter aims to present a design using a FPGA to perform the modulation schemes presented in Chapter 3 while using the algorithms described in Chapter 4. Therefore, concepts discussed in the previous chapter are required for the comprehension of the proposed implementation.

As previously discussed, the correct operation of the Indirect Matrix Converter depends on an accurate estimation of the electric quantities phase, since the converter performs an interface between two distinct AC systems. Therefore, two phase-locked loop algorithm structures are hence used to estimate the rectifier stage voltage and inverter stage current phases. Since there is no need to estimate both angles at the same time using paralleled structures, a finite-state machine can be implemented to use the same structure for both estimations, which then occur sequentially. The LMS-based frequency estimation techniques described in the previous chapter were not used in a primary moment, since these strategies require a high resource usage and are not required for the converter operation in a first moment.

The previous chapter described the need for a voltage-controlled oscillator (VCO) to generate a component orthogonal to the reference signals. This structure was here implemented using the CORDIC algorithm, which is also discussed in Chapter 4.

After estimating the phase of electrical quantities in both rectifier and inverter stages, the vector times for the space-vector modulation must be calculated. The calculation of the vector times depend on the calculation of trigonometric functions and a pulse-width modulator to generate the nine-segment pattern presented in Chapter 3. Since the vector time calculation uses the result of the PLL phase estimation, another finite-state machine must be implemented to manage the data flow. Since a CORDIC algorithm is already used in the PLL structure, the vector times are calculated using the same structure.

The next sections aim to present the implementation of the HVZCS modulation strategy for the Indirect Matrix Converter. The implementations are based on the Altera Cyclone IV EP4CE22F17C6N FPGA, which is present on the Terasic Cyclone IV DE0-Nano Development Kit. The voltage and current acquisitions were performed using a Texas Instruments TMS320F28335 Microcontroller, which communicates with the FPGA through a SPI interface.

5.2 HIGH-RESOLUTION PULSE WIDTH MODULATOR

Over the last few years, several different modulation strategies have been employed in the control of static power converters, and most strategies depend on a pulse width modulator to generate switching functions according to an average reference value. An easy way to generate such functions is to compare the reference value with a carrier, which is usually a periodic triangular or sawtooth function. In a discrete situation, the carrier can be generated by a counter with update frequency f_{clk}. Therefore, for a fixed switching frequency f_s, the number of possible discrete states N defined by (5.1).

$$N = \frac{f_{clk}}{f_s} \tag{5.1}$$

The resolution of the digital pulse width modulator, defined by (5.2), is proportional to the inverse update frequency, which is limited by physical characteristics of the device, hence limited to a maximum update frequency. The main objective of HRPWMs is to obtain a resolution higher than the resolution defined by (5.2) through the use of auxiliary digital circuits.

$$\text{RES} = \frac{1}{f_{clk}} \tag{5.2}$$

An initial idea is to obtain a higher resolution through the use of digitally controlled delays on the output of a modulator [41], or through a chain of logic elements [42], obtaining different modulated pulses. Such strategies are highly dependant on the placement realized by the compiler, and some even propose manual routing of logic elements of a FPGA, which is extremely difficult to perform in larger projects.

An alternative to the aforementioned is to generate different phase-shifted pulses through different modulators fed with phase-shifted clocks [43]. The proposed strategy obtained a resolution eight times higher than with a single modulator, according to (5.3), but with a very limited update frequency. The idea was further developed and is presented in this section, obtaining a resolution of 625 ps with a high monotonic behaviour, equivalent to a digital pulse width modulator with a 1.6 GHz update frequency, thus reducing quantization

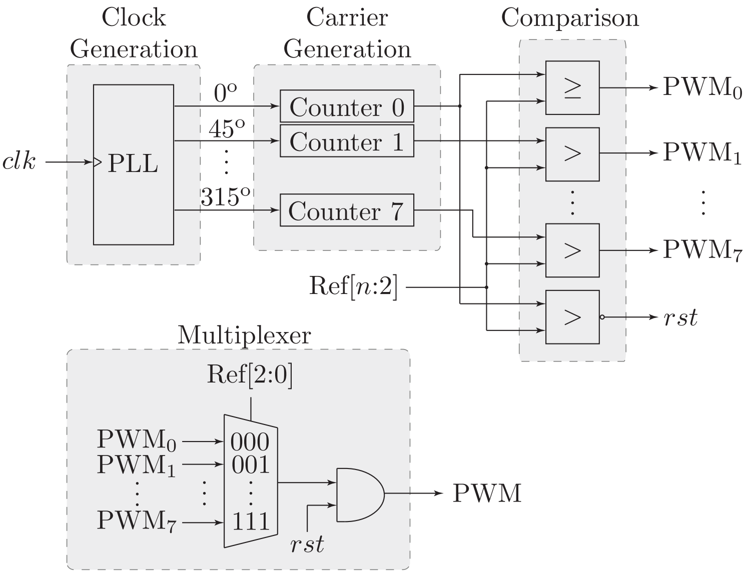

Clock Generation
Carrier Generation
Comparison
clk
PLL
0°
45°
315°
Counter 0
Counter 1
Counter 7
≥
>
>
>
PWM0
PWM1
PWM7
rst
Ref[n:2]
Multiplexer
Ref[2:0]
PWM0
PWM1
PWM7
000
001
111
rst
PWM

Figure 5.1 – Block diagram of the proposed HRPWM FPGA implementation.

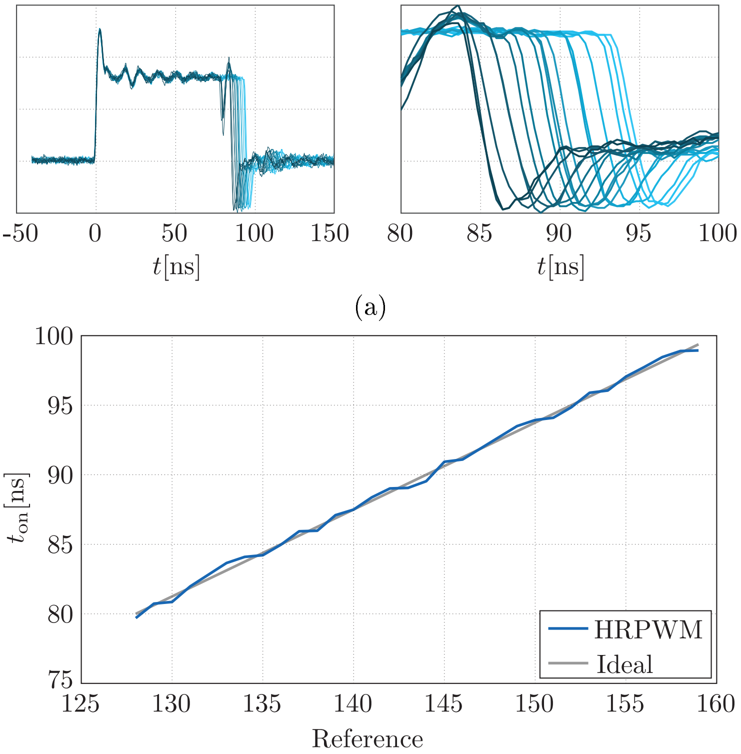
noise. The block diagram presented in Figure 5.1 illustrates the FPGA implementation of the proposed strategy.

$$\mathrm{RES}_{\mathrm{HRPWM}} = \frac{8}{f_{clk}} \tag{5.3}$$

The experimental results are presented in Figure 5.2a for different reference values. Figure 5.2b shows a graphic of the on time for a reference from 128 to 159 along with the ideal characteristic. Ideally, the on time follows a specific proportion, but intrinsic path delays inside the FPGA define the difference between the measured times. However, the modulator still possesses a high monotonic behaviour while operating close to the maximum frequency step.

Since the space vector modulation uses a pulse width modulator to create the modulation schemes discussed in Chapter 3, the proposed strategy can also be used to minimize the quantization noise generated by the pulse width modulation.

In the subsequent experimental results, the proposed modulator represents a gain of three bits of resolution on the vector times



(a)

(b)

Figure 5.2 – High resolution digital pulse width modulator experimental results with 625 ps resolution. (a) Modulated output with reference varying from 136 to 151. (b) Graphic of on time versus reference, showing a monotonic behaviour.

modulation.

5.3 SPACE VECTOR MODULATION DESIGN FLOWCHART

This section aims to demonstrate the design flowchart of the SVM implementation. Three finite-state machines were implemented to control the implementation while aiming to minimize the number of resources used.

A simplified qPLL finite-state machine was presented in Chapter 4. However, since the same structure is used to estimate two different phasor angles, two states were added to better control this behaviour, resulting in a number of six states. The flowchart is presented in Figure 5.3.

A second finite-state-machine was employed to perform the vector times calculation previously described. Therefore, there is a need to calculate four different trigonometric functions, each performed during a determined state, as described by the flowchart presented in Fig-

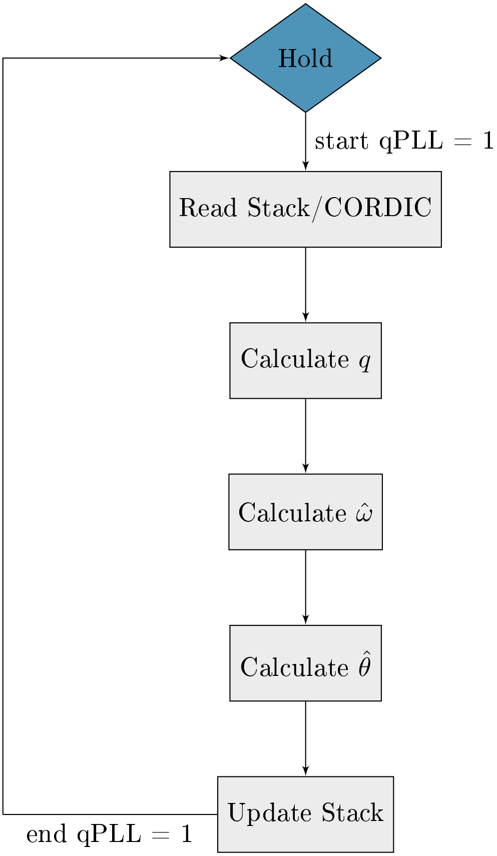

Hold
start qPLL = 1
Read Stack/CORDIC
Calculate q
Calculate $\hat{\omega}$
Calculate $\hat{\theta}$
Update Stack
end qPLL = 1

Figure 5.3 – Flowchart for qPLL FPGA finite-state machine implementation.

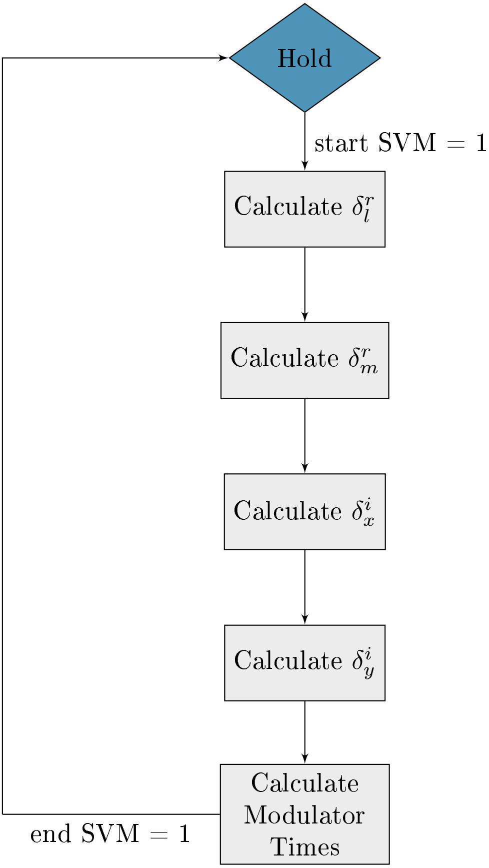

Hold
start SVM = 1
Calculate δ_l^r
Calculate δ_m^r
Calculate δ_x^i
Calculate δ_y^i
Calculate Modulator Times
end SVM = 1

Figure 5.4 – Flowchart of the SVM vector times finite-state machine.

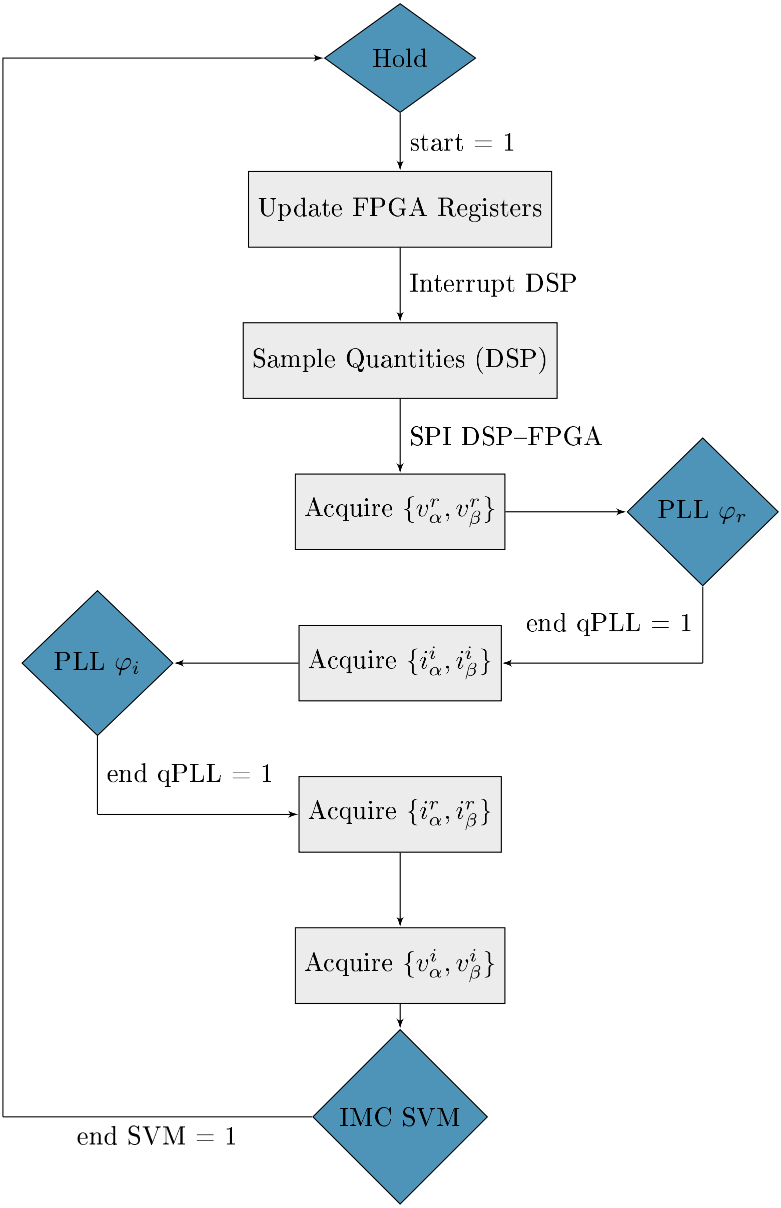

Hold
start = 1
Update FPGA Registers
Interrupt DSP
Sample Quantities (DSP)
SPI DSP–FPGA
Acquire $\{v^r_\alpha, v^r_\beta\}$
PLL φ_r
end qPLL = 1
Acquire $\{i^i_\alpha, i^i_\beta\}$
PLL φ_i
end qPLL = 1
Acquire $\{i^r_\alpha, i^r_\beta\}$
Acquire $\{v^i_\alpha, v^i_\beta\}$
IMC SVM
end SVM = 1

Figure 5.5 – IMC space vector modulation design main flowchart.

ure 5.4. The main finite-state-machine, which controls the whole system, possesses fourteen different states. Its flowchart is presented in Figure 5.5.

The subsequent section presents some details regarding the FPGA implementation, as well as results acquired directly from the FPGA using the Altera SignalTap II Logic Analyzer.

5.4 IMPLEMENTATION OF THE INDIRECT MATRIX CONVERTER SPACE VECTOR MODULATION

The space vector modulation of an IMC for grid tied applications was implemented using some concepts presented in the previous chapters as well as some of the algorithms presented previously. There is a need for two synchronism structures, means to calculate the vector times described in Chapter 3 and a control structure.

On a first moment, the control structure was not implemented, but its implementation results in an extra states in the flowchart proposed in Figure 5.5. A FPGA was used to perform all the calculations and algorithms presented, while a Digital Signal Processor (DSP) was used to perform voltage and current acquisitions and communicates with the FPGA through a serial data interface.

The HVZCS modulation scheme was implemented to verify the converter behaviour since it presents the most advantages, as discussed in the previous chapter. It is possible to rewrite the time equations obtained in Appendix C according to (5.4).

$$\begin{aligned}
\delta^i_{x,l} &= m\delta^r_l\delta^i_x \\
\delta^i_{x,m} &= m\delta^r_m\delta^i_x \\
\delta^i_{y,l} &= m\delta^r_l\delta^i_y \\
\delta^i_{y,m} &= m\delta^r_m\delta^i_y \\
\delta_0 = 1 - \delta^i_{x,l} &- \delta^i_{x,m} - \delta^i_{y,l} - \delta^i_{y,m}
\end{aligned} \tag{5.4}$$

The vector times presented in (5.4) were then implemented using a CORDIC algorithm with a multiplexed input, with rectifier and inverter auxiliary functions defined by (5.5), which varies according to the sector in which the reference phasor is present.

A qPLL algorithm was implemented to obtain the estimated phasor angles θ_r and θ_i, which ideally are equal to φ_r and φ_i, respectively. Since two synchronism algorithms are used, the structure of the qPLL

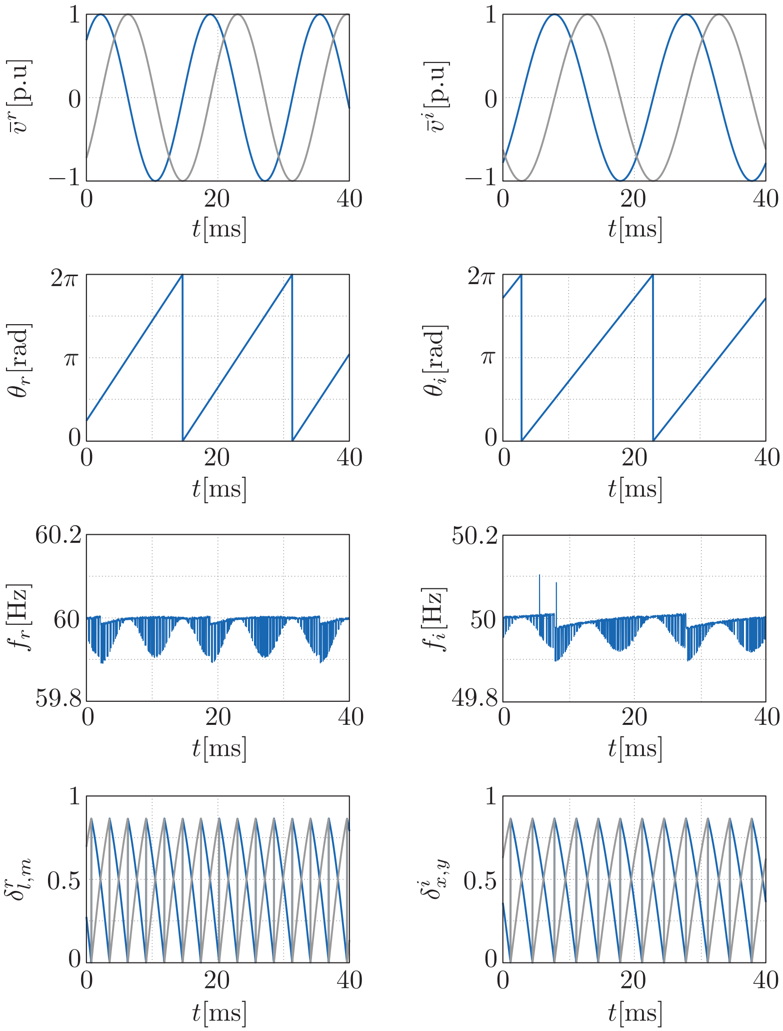


Figure 5.6 – Experimental results of the CORDIC-based qPLL structure implementation shared by both rectifier and inverter stages with voltage vectors with frequency equal to 60 Hz and 50 Hz, respectively.

is shred for the rectifier and inverter stage. Two stacks were created to store the previous time instant signals for each of the PLLs, and a FSM was implemented to control the PLL input multiplexer, reducing the number of resources utilized. The general finite-state machine also controls which of the angles from the stack serves as the CORDIC input.

From equation (5.5), there is a need to calculate four different trigonometric functions. A single 19-iteration pipelined CORDIC structure was implemented in the FPGA, which is shared by all structures which need to perform these functions in the FPGA. A finite-state machine was then implemented according to the flowchart presented in Figure 5.5 and Figure 5.4 to control a multiplexer connected to the structure input. The general finite-state machine control if the the CORDIC input comes from the SVM or the PLL algorithm, while the SVM finite-state machine controls which of the four duty-cycles is calculated. Figure 5.6 shows the estimated frequencies, angles and vector times calculated using equation (5.5).

$$\begin{aligned}
\delta_l^r &= \begin{cases} \cos\left(\varphi_r - \dfrac{\pi}{3}\right), & \text{rectifier sector is odd} \\ \cos\left(\varphi_r + \dfrac{\pi}{3}\right), & \text{rectifier sector is even} \end{cases} \\
\delta_m^r &= \begin{cases} \cos\left(\varphi_r + \dfrac{\pi}{3}\right), & \text{rectifier sector is odd} \\ \cos\left(\varphi_r - \dfrac{\pi}{3}\right), & \text{rectifier sector is even} \end{cases} \\
\delta_x^i &= \begin{cases} \cos\left(\varphi_r + \dfrac{\pi}{6}\right), & \text{inverter sector is odd} \\ \sin\left(\varphi_r\right), & \text{inverter sector is even} \end{cases} \\
\delta_y^i &= \begin{cases} \sin\left(\varphi_r\right), & \text{inverter sector is odd} \\ \cos\left(\varphi_r + \dfrac{\pi}{6}\right), & \text{inverter sector is even} \end{cases}
\end{aligned} \tag{5.5}$$

The nine-segment modulation scheme was implemented, since it possesses quarter-wave symmetry with reduced number of switching. Nine different references for the inverter stage and three references for the rectifier stage must be calculated for the pulse width modulator to obtain the modulation scheme, according to (5.6) and (5.7). The modulator duty cycles are shown in Figure 5.7.

$$\begin{aligned}
\delta_1^r &= \frac{1}{2}\left(\delta_{x,l}^i + \delta_{y,l}^i + \frac{1}{2}\delta_0\right) \\
\delta_2^r &= \frac{1}{2}\left(1 + \delta_1^r + \delta_{x,m}^i + \delta_{y,m}^i + \frac{1}{2}\delta_0\right) \\
\delta_3^r &= \delta_1^r + \delta_2^r = 1
\end{aligned} \tag{5.6}$$

$$
\begin{aligned}
\delta_1^i &= \frac{1}{2}\delta_{x,l}^i \\
\delta_2^i &= \delta_1^i + \frac{1}{2}\delta_{y,l}^i \\
\delta_3^i &= \delta_2^i + \frac{1}{4}\delta_0 \\
\delta_4^i &= \delta_3^i + \frac{1}{2}\delta_{y,m}^i \\
\delta_5^i &= \delta_4^i + \delta_{x,m}^i \\
\delta_6^i &= \delta_5^i + \frac{1}{2}\delta_{y,m}^i \\
\delta_7^i &= \delta_6^i + \frac{1}{4}\delta_0 \\
\delta_8^i &= \delta_7^i + \frac{1}{2}\delta_{y,l}^i \\
\delta_9^i &= \delta_8^i + \frac{1}{2}\delta_{x,l}^i = 1
\end{aligned}
\tag{5.7}
$$

A vector of modulated pulses $\vec{p}_{r,i}$ was then created concatenating the modulated signals, with each signal resulting from the comparison between the references $\delta_j^{r,i}$ described in (5.7) and (5.6), as illustrated in Figure 5.8. The resulting $\vec{p}_i$ can be represented as a hexadecimal number which varies from 1_{16} to $1FF_{16}$ and $\vec{p}_r$ is a number from 1_{16} to 7_{16} which can be directly translated into a vector depending on the current rectifier and inverter sector. The generated pulses for rectifier and inverter stage are shown in Figure 5.9.

The results here presented were obtained using a Digital-Signal Processor to generate two voltage phasors for each converter stage with the object of testing the design flow.

5.5 INDIRECT MATRIX CONVERTER RESULTS

An indirect matrix converter described in [1] was used for testing, which is presented in Figure 5.10. With the objective of testing the topology and modulation strategy, the Δ-Switch was not used. Therefore, the topology is composed by eighteen Cree CMF2012D SiC MOSFETs. The converter parameters and test conditions are presented in Table 5.1. The experimental results for this point of operation is presented in Figure 5.11.

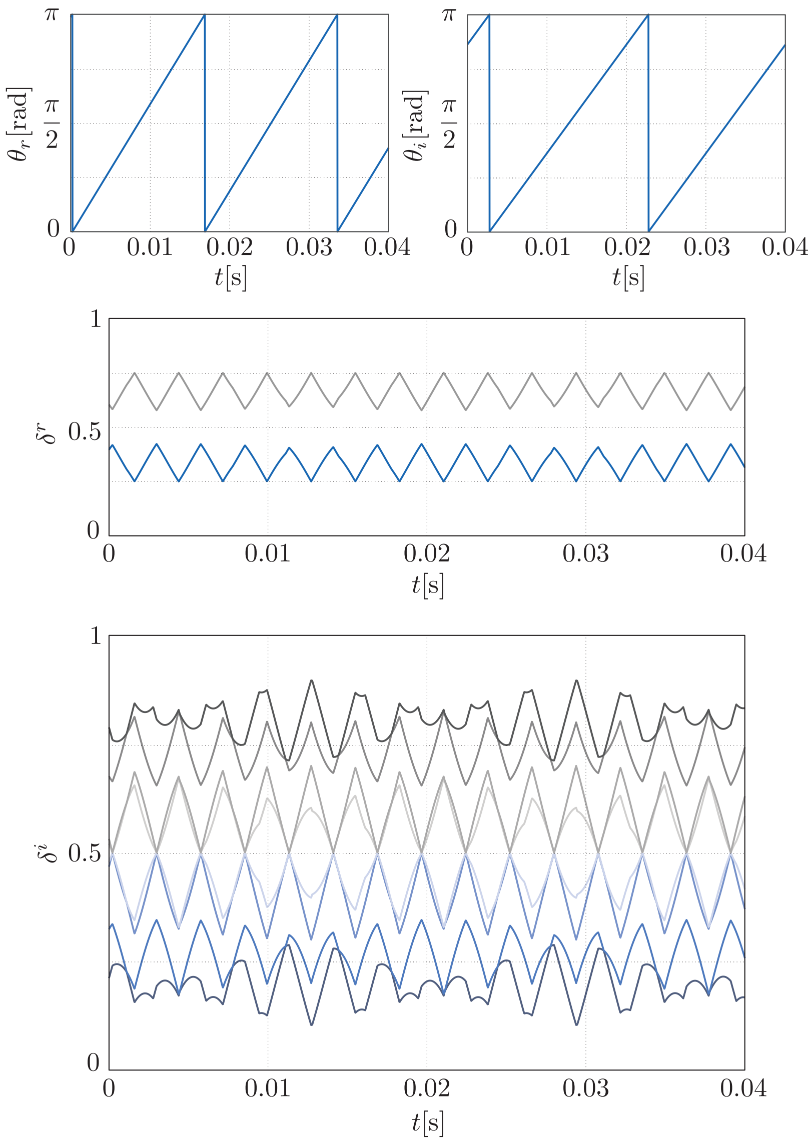


Figure 5.7 – Pulse width modulator duty-cycles for a nine-segment HVZCS modulation scheme for a 60 Hz frequency reference for the rectifier stage and 50 Hz frequency reference for the inverter stage.

Table 5.1 – Experimental result parameters.

Parameter	**Symbol**	**Value**
Modulation Strategy	–	HVZCS
Modulation index	m	0.8
High-side RMS phase voltage	V_r^{rms}	127 V
Low-side RMS phase voltage	V_i^{rms}	88 V
High-side frequency	f_r	60 Hz
Low-side frequency	f_i	50 Hz
High-side Inductance	L_f	250 μH
High-side Capacitance	C_f	16 μF
High-side Resistance	R_f	10 mΩ
Low-side Inductance	L_m	750 μH
Low-side Resistance	R_m	50 Ω (Y)
Switching Frequency	f_s	24.424 kHz

During experimental test, a resonance was detected between voltage source and input filter, as it can be seen in the input current. This resonance can be damped by adding a passive damping structure to the input filter. Since the converter point of operation is different than the projected one, as the converter is processing approximately 5% of its nominal capacity, the projected current ripples are hard to achieve. The input current also presents a large phase displacement caused by the input filter. This issue drastically reduces when the converter processes more power.

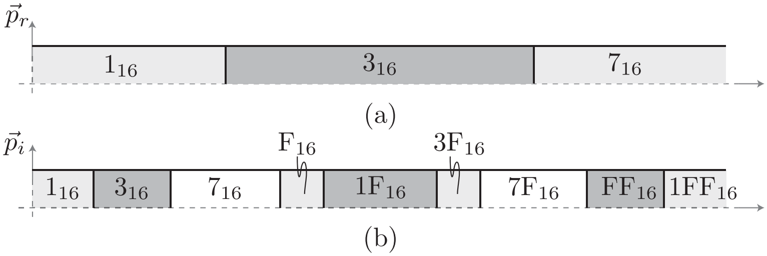


Figure 5.8 – Modulated switching state with vector times for space vector modulation using a nine-segment scheme, concatenating the modulated signals into two vectors. (a) Rectifier switching state vector. (b) Inverter switching state vector.

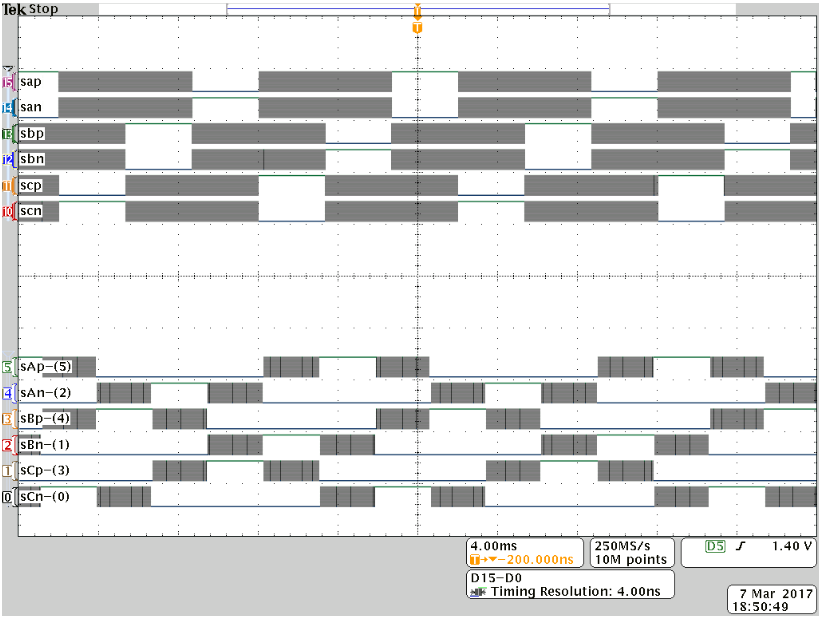

Tek Stop
15 sap
14 san
13 sbp
12 sbn
11 scp
10 scn
5 sAp−(5)
4 sAn−(2)
3 sBp−(4)
2 sBn−(1)
1 sCp−(3)
0 sCn−(0)
4.00ms
−200.000ns
250MS/s
10M points
D5 1.40 V
D15−D0
Timing Resolution: 4.00ns
7 Mar 2017
18:50:49

Figure 5.9 – Experimental result of the HVZCS modulation scheme pulses implementation for the switches of rectifier and inverter stage. Channels D0–D7 shows the switching signals for the rectifier stage, while Channels D10–D15 shows the switching signals for the inverter stage.

5.6 CONCLUSION

This chapter demonstrated the operation of some of the algorithms presented in Chapter 4, such as the CORDIC for the calculation of trigonometric functions and the qPLL to estimate the angle of voltage phasors. A FPGA based design of the HVZCS modulation was then presented.

The structure presented makes use of a single CORDIC structure to perform calculations, which is then multiplexed by both the qPLL and modulation structure. The qPLL is also multiplexed by inverter and rectifier stage voltages, resulting in a significant reduction of resource usage.

The CORDIC implementation represents approximately 50% of the resource usage on the project, since many structures are based on this implementation. The numbers of multipliers is scarce in low-cost FPGAs, which proves to be a problem for large projects. The presented implementation aimed to reduce the number of resource usage while focusing on sharing resources between algorithm. Therefore, three finite-state machine was implemented to manage the implementation behaviour.

The proposed modulation design was tested in a prototype, and an experimental result was obtained for a low power point of operation, proving the functionality of the FPGA implementation.

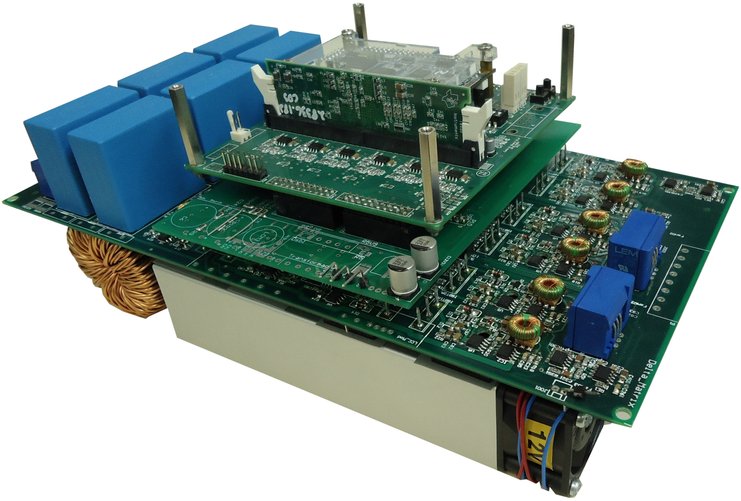
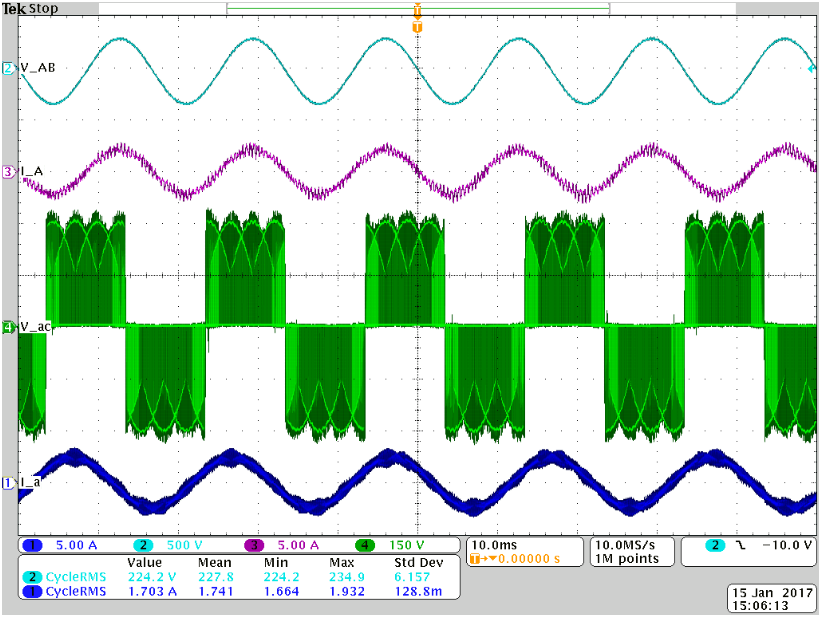


Figure 5.10 – Ultra Sparse Matrix Converter prototype photography. This topology also include a Δ-Switch, which can reduce conduction losses as proposed in [1].



	Value	Mean	Min	Max	Std Dev
2 CycleRMS	224.2 V	227.8	224.2	234.9	6.157
1 CycleRMS	1.703 A	1.741	1.664	1.932	128.8m

Figure 5.11 – Experimental results of an indirect matrix converter operating in *Buck*-mode with with parameters given by Table 5.1.

6 CONCLUSION

Static power converters are the main object of study of Power Electronics, and the development of new technologies applied power converters enables more efficient energy conversion solutions. These power converters can be used in many different areas, such as electricity micro-generation and motor drives. The power electronics field of study is extensive, varying from the construction of these converter to techniques and algorithms for their appropriate operation. A correct operation of a power converter is dependent on the comprehension of many different concepts, as shown in this thesis.

The development of new semiconductor technologies and the search for a more efficient energy conversion between two AC systems may result in more complex topologies, such as the presented indirect matrix converter. The main advantages of this topology is high efficiency, extensive life cycle and reduced volume and weight. However, the number of semiconductor devices is quite high if compared to the most commonly used solutions previously presented. Also, the operation of these type of converters is very complex and demand additional countermeasures to faults which might occur during normal operation. The absence of a DC-link energy storage device (capacitor, inductor) reduces the system inertia. For example, the capacitor of a VL-BBC provides energy for a large torque variation while operating as a motor drive, reducing the input current efforts and provoking a voltage sag in the DC-link voltage. Since the matrix converter does not possess energy storage devices, the energy for the sudden torque variation comes from the input, resulting in elevated current peaks, restricting applications for the matrix converter.

A mathematical model for the indirect matrix converter was obtained, and the state-space matrix for the complete system possesses very non-linear behaviour, proving hard to select a single operation point for a linearization. The design of a linear controller might prove to be quite difficult, since the the plant shows constant variations of the operating point. The behaviour of linear controllers are also hindered for non-linear loads. Therefore, many non-linear approaches are currently being studied to solve some of the converter problems, as well as guaranteeing a safe operation under faults. Some authors propose strategies around the FCS-MPC, since the possible converter states are always known. The use of a correct discrete model is necessary for a correct state estimation. A theoretical discrete model was also discussed, and simulations demonstrated the model accuracy. However, parametric variations, as well as non-linearities might hinder the accuracy of such model. Therefore, a parameter estimation method might prove to have a better efficacy for this type of control.

A FPGA implementation of the modulation and synchronism strategies was proposed and verified experimentally. A resource reduced implementation was discussed, as many of the design structures were shared by different algorithms. The main disadvantage is the complexity of the finite state machine implemented to control the design behaviour, increasing the computational time. However, the execution time of the proposed strategy is much lower than the design constraints set by the switching frequency. Such implementation possesses a high sequential design flow, which tends towards the reduced resource usage based on a trade-off between using the FPGA capabilities and reducing the area of the design. An experimental result was presented, demonstrating the modulation implementation and verifying the behaviour of the converter.

As recommendations for future works, the following topics present some research lines based on the information contained in this thesis:

- Investigation of different linear and non-linear control strategies;
- Research on control techniques for active damping for grid-tied applications;
- Survey on different synchronism algorithms which possess fast response and operate for a wide range of frequency;
- Exploration of the IMC operation under unbalanced/distorted conditions and operation under system faults;
- Study of frequency estimation methods employing different adaptive filters with harmonic rejection.

REFERENCES

[1] JAPPE, T. K. *Conversores Matriciais Indiretos Alimentados em Corrente*. PhD. Dissertation — INEP/UFSC, 2015.

[2] FRIEDLI, T. *Comparative Evaluation of Three-Phase Si and SiC AC-AC Converter Systems*. PhD. Dissertation — ETH Zurich, 2010.

[3] AKAGI, H. The state-of-the-art of power electronics in japan. *IEEE Transactions on Power Electronics*, v. 13, n. 2, p. 345–356, Mar 1998. ISSN 0885-8993.

[4] WANG, H. et al. Design for reliability in power electronics in renewable energy systems 2013; status and future. In: *4th International Conference on Power Engineering, Energy and Electrical Drives*. 2013. p. 1846–1851. ISSN 2155-5516.

[5] WHEELER, P. W. et al. Matrix converters: a technology review. *IEEE Transactions on Industrial Electronics*, v. 49, n. 2, p. 276–288, Apr 2002. ISSN 0278-0046.

[6] FRIEDLI, T.; KOLAR, J. W. Comprehensive comparison of three-phase ac-ac matrix converter and voltage dc-link back-to-back converter systems. In: *The 2010 International Power Electronics Conference - ECCE ASIA -*. 2010. p. 2789–2798.

[7] WHEELER, P. W. et al. Power supply loss ride-through and device voltage drop compensation in a matrix converter permanent magnet motor drive for an aircraft actuator. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*. 2004. v. 1, p. 149–154 Vol.1. ISSN 0275-9306.

[8] SCHAFMEISTER, F. *Indirekte Sparse Matrix Konverter*. PhD. Dissertation — ETH Zurich, 2008.

[9] SCHONBERGER, J. et al. An ultra sparse matrix converter with a novel active clamp circuit. In: *2007 Power Conversion Conference - Nagoya*. 2007. p. 784–791.

[10] LIPO, T. A. Recent progress in the development in solid-state ac motor drives. *IEEE Transactions on Power Electronics*, v. 3, n. 2, p. 105–117, Apr 1988. ISSN 0885-8993.

[11] BORGONOVO, D. *Análise Modelagem e Controle de Retificadores PWM Trifásicos.* PhD. Dissertation — INEP/UFSC, 2005.

[12] MUSSA, S. A. *Controle de um Conversor CA-CC Trifásico PWM de Três Níveis com Fator de Potência Unitário Utilizando DSP.* PhD. Dissertation — INEP/UFSC, 2003.

[13] SINGH, B. et al. A review of three-phase improved power quality ac-dc converters. *IEEE Transactions on Industrial Electronics*, v. 51, n. 3, p. 641–660, June 2004. ISSN 0278-0046.

[14] WILSON, J. W. A. The forced-commutated inverter as a regenerative rectifier. *IEEE Transactions on Industry Applications*, IA-14, n. 4, p. 335–340, July 1978. ISSN 0093-9994.

[15] GYUGYI, L.; PELLY, B. R. *Static Power Frequency Changers. Theory, performance and applications.* : Wiley, 1976.

[16] BLAND, M. J. et al. Comparison of bi-directional switch components for direct ac-ac converters. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551).* 2004. v. 4, p. 2905–2909 Vol.4. ISSN 0275-9306.

[17] VENTURINI, M.; ALESINA, A. The generalised transformer: A new bidirectional, sinusoidal waveform frequency converter with continuously adjustable input power factor. In: *1980 IEEE Power Electronics Specialists Conference.* 1980. p. 242–252. ISSN 0275-9306.

[18] MALEKJAMSHIDI, Z.; JAFARI, M.; ZHU, J. Analysis and comparison of direct matrix converters controlled by space vector and venturini modulations. In: *2015 IEEE 11th International Conference on Power Electronics and Drive Systems.* 2015. p. 635–639. ISSN 2164-5256.

[19] FORMENTINI, A. et al. Speed finite control set model predictive control of a pmsm fed by matrix converter. *IEEE Transactions on Industrial Electronics*, v. 62, n. 11, p. 6786–6796, Nov 2015. ISSN 0278-0046.

[20] AYDOGMUS, O.; DENIZ, E. Design and implementation of two-phase permanent magnet synchronous motor fed by a matrix converter. *IET Power Electronics*, v. 10, n. 9, p. 1054–1060, 2017. ISSN 1755-4535.

[21] ZHANG, J. et al. Hysteresis band current controller based field-oriented control for an induction motor driven by a direct matrix converter. In: *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*. 2017. p. 4633–4638.

[22] SAYGIN, A.; AKSOZ, A.; YILMAZ, E. N. A different model of wecs connected to smart grid through matrix converter. In: *2016 4th International Istanbul Smart Grid Congress and Fair (ICSG)*. 2016. p. 1–5.

[23] BASAK, A.; MUKHERJEE, K.; SYAM, P. Effect of matrix converter on the speed control scheme of a grid connected doubly-fed induction generator system. In: *2016 2nd International Conference on Control, Instrumentation, Energy Communication (CIEC)*. 2016. p. 319–323.

[24] ZHANG, J. et al. Carrier-based modulation strategy of indirect matrix converters for common-mode voltage reduction. In: *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*. 2017. p. 534–538.

[25] WANG, B.; VENKATARAMANAN, G. A carrier based pwm algorithm for indirect matrix converters. In: *2006 37th IEEE Power Electronics Specialists Conference*. 2006. p. 1–8. ISSN 0275-9306.

[26] TRAN, Q. H.; NGUYEN, N. V.; LEE, H. H. A carrier-based modulation method to reduce switching losses for indirect matrix converters. In: *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*. 2014. p. 4828–4833. ISSN 1553-572X.

[27] KOLAR, J. W. et al. The essence of three-phase ac/ac converter systems. In: *2008 13th International Power Electronics and Motion Control Conference*. 2008. p. 27–42.

[28] KOLAR, J. W. et al. Novel three-phase ac-dc-ac sparse matrix converter. In: *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*. 2002. v. 2, p. 777–791 vol.2.

[29] KOLAR, J. W.; SCHAFMEISTER, F. Novel modulation schemes minimizing the switching losses of sparse matrix converters. In: *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*. 2003. v. 3, p. 2085–2090 Vol.3.

[30] FRIEDLI, T.; KOLAR, J. W. Swiss Patent 698 914, *Verfahren zur Dreipunkt-Modulation eines quasi-direkten Dreiphasen AC/AC-Pulsumrichters*. Swiss Patent 698 914, Nov. 7, 2006.

[31] ITOH, J. I. et al. A novel control method to reduce an inverter stage loss in an indirect matrix converter. In: *2009 35th Annual Conference of IEEE Industrial Electronics*. 2009. p. 4475–4480. ISSN 1553-572X.

[32] SOEIRO, T. B.; HELDWEIN, M. L. High efficiency indirect matrix converter topologies. In: *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. 2013. p. 4856–4861. ISSN 1553-572X.

[33] NIELSEN, P.; BLAABJERG, F.; PEDERSEN, J. K. Space vector modulated matrix converter with minimized number of switchings and a feedforward compensation of input voltage unbalance. In: *Proceedings of International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth*. 1996. v. 2, p. 833–839 vol.2.

[34] JUSSILA, M. *Comparison of Space-Vector-Modulated Direct and Indirect Matrix Converters in Low-Power Applications*. PhD. Dissertation — Tampere University of Technology, 2007.

[35] LEE, K.-B.; BLAABJERG, F.; LEE, K.-W. A simple dtc-svm method for matrix converter drives using a deadbeat scheme. In: *2005 European Conference on Power Electronics and Applications*. 2005. p. 10 pp.–P.10.

[36] TARISCIOTTI, L. et al. Modulated predictive control for indirect matrix converter. *IEEE Transactions on Industry Applications*, v. 53, n. 5, p. 4644–4654, Sept 2017. ISSN 0093-9994.

[37] VOLDER, J. E. The cordic trigonometric computing technique. *IRE Transactions on Electronic Computers*, EC-8, n. 3, p. 330–334, Sept 1959. ISSN 0367-9950.

[38] MANDIC, D. P.; KANNA, S.; DOUGLAS, S. C. Mean square analysis of the clms and aclms for non-circular signals: The approximate uncorrelating transform approach. In: *2015 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*. 2015. p. 3531–3535. ISSN 1520-6149.

[39] XIA, Y.; MANDIC, D. P. Widely linear adaptive frequency estimation of unbalanced three-phase power systems. *IEEE Transactions on Instrumentation and Measurement*, v. 61, n. 1, p. 74–83, Jan 2012. ISSN 0018-9456.

[40] GRABOVSKI, E. F. C.; MUSSA, S. A. Three-phase frequency estimator in smart grid applications: Practical issues using fpga. In: *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*. 2017. p. 175–179.

[41] HUERTA, S. C. et al. Fpga-based digital pulsewidth modulator with time resolution under 2 ns. *IEEE Transactions on Power Electronics*, v. 23, n. 6, p. 3135–3141, Nov 2008. ISSN 0885-8993.

[42] WU, J.; SHI, Z. The 10-ps wave union tdc: Improving fpga tdc resolution beyond its cell delay. In: *2008 IEEE Nuclear Science Symposium Conference Record*. 2008. p. 3440–3446. ISSN 1082-3654.

[43] GRABOVSKI, E. F. C.; MUSSA, S. A. High resolution fpga-based symmetrical digital pulse width modulator. In: *2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. 2017. p. 1–5.

[44] ERICKSON, R. W.; MAKSIMOVIĆ, D. *Fundamentals of Power Electronics.* : Kluwer Academic Publishers, 2001.

[45] DUESTERHOEFT, W. C.; SCHULZ, M. W.; CLARKE, E. Determination of instantaneous currents and voltages by means of alpha, beta, and zero components. *Transactions of the American Institute of Electrical Engineers*, v. 70, n. 2, p. 1248–1255, July 1951. ISSN 0096-3860.

[46] RAO, N. D.; RAO, H. N. R. Study of symmetrical and related components through the theory of linear vector spaces. *Electrical Engineers, Proceedings of the Institution of*, v. 113, n. 6, p. 1057–1062, June 1966. ISSN 0020-3270.

Appendix A – Discretization of Continuous State Space Models

A.1 INTRODUCTION

This appendix presents a discretization method for state space models, employed during the discretization of power converter models and *hardware-in-the-loop* simulation. Hence, the objective of this brief mathematical proof is to explain some results used which might not seem trivial.

The discretization method here presented is the *Backward Euler* method, or the zero-order holder equivalent, which possesses a simple mathematical representation, as well as a low computational effort, since the state equation is substituted by a first-order approximation.

A.2 MATHEMATICAL ANALYSIS

Let a system be described by (A.1), where $\mathbf{x}$ is the state vector, $\mathbf{u}$ is the system input vector and $\mathbf{y}$ is the output vector. Also, the sampling time is defined as T_a.

$$\begin{cases} \dot{\mathbf{x}} = [\mathbf{A}]\,\mathbf{x} + [\mathbf{B}]\,\mathbf{u} \\ \mathbf{y} = [\mathbf{C}]\,\mathbf{x} + [\mathbf{D}]\,\mathbf{u} \end{cases} \tag{A.1}$$

Therefore, manipulating the expression for the derivative of the state vector in (A.1) results in (A.2).

$$\dot{\mathbf{x}}(t) - [\mathbf{A}]\,\mathbf{x}(t) = [\mathbf{B}]\,\mathbf{u}(t) \tag{A.2}$$

The next step is to multiply the term $e^{-[\mathbf{A}]t}$ on both sides of the equation (A.2), resulting in (A.3).

$$e^{-[\mathbf{A}]t}\dot{\mathbf{x}}(t) - e^{-[\mathbf{A}]t}\,[\mathbf{A}]\,\mathbf{x}(t) = e^{-[\mathbf{A}]t}\,[\mathbf{B}]\,\mathbf{u}(t) \tag{A.3}$$

Hence, equation (A.3) can be rewritten as (A.4). It is important to notice that the system matrix were considered time-invariant, otherwise (A.4) is not valid.

$$\frac{\mathrm{d}}{\mathrm{d}t}e^{-[\mathbf{A}]t}\mathbf{x}(t) = e^{-[\mathbf{A}]t}\,[\mathbf{B}]\,\mathbf{u}(t) \tag{A.4}$$

Thus, integrating both sides of equation (A.4) in a sampling time, as in (A.5), and multiplying both sides of the equation by $e^{[\mathbf{A}](n+1)T_a}$ results in (A.6).

$$\int_{nT_a}^{(n+1)T_a} \frac{\mathrm{d}}{\mathrm{d}t} e^{-[\mathbf{A}]t}\mathbf{x}(t)\mathrm{d}t = \int_{nT_a}^{(n+1)T_a} e^{-[\mathbf{A}]t}\left[\mathbf{B}\right]\mathbf{u}(t)\mathrm{d}t \tag{A.5}$$

$$\begin{aligned} \mathbf{x}\left((n+1)T_a\right) &= e^{[\mathbf{A}]T_a}\mathbf{x}\left(nT_a\right) \\ &+ \int_{nT_a}^{(n+1)T_a} e^{-[\mathbf{A}]((n+1)T_a-t)}\left[\mathbf{B}\right]\mathbf{u}(t)\mathrm{d}t \end{aligned} \tag{A.6}$$

However, the output vector in equation (A.6) is still inside the integral. Nonetheless, since this model describes a zero-order holder equivalent, the input is constant during this time interval and equal to its initial value. Therefore, (A.6) can be rewritten as (A.7).

$$\begin{aligned} \mathbf{x}\left((n+1)T_a\right) &= e^{[\mathbf{A}]T_a}\mathbf{x}\left(nT_a\right) \\ &+ \int_0^{T_a} e^{-[\mathbf{A}]\lambda}\left[\mathbf{B}\right]\mathrm{d}\lambda\,\mathbf{u}\left(nT_a\right) \end{aligned} \tag{A.7}$$

By supressing the sampling time notation, and rewriting (A.7), the Discrete State Space Model can be described by (A.8), where the system matrices are given by (A.9).

$$\mathbf{x}\left(n+1\right) = \left[\mathbf{G}\right]\mathbf{x}\left(n\right) + \left[\mathbf{H}\right]\mathbf{u}\left(n\right) \tag{A.8}$$

$$\begin{aligned} \left[\mathbf{G}\right] &= e^{[\mathbf{A}]T_a} \\ \left[\mathbf{H}\right] &= \int_0^{T_a} e^{-[\mathbf{A}]\lambda}\left[\mathbf{B}\right]\mathrm{d}\lambda \end{aligned} \tag{A.9}$$

If matrix $[\mathbf{A}]$ is non-singular, matrix $[\mathbf{H}]$ can be calculated using (A.10), where η is the system order.

$$\left[\mathbf{H}\right] = \left[\mathbf{A}\right]^{-1}\left(\left[\mathbf{G}\right] - \mathbb{I}_{\eta \mathrm{x} \eta}\right)\left[\mathbf{B}\right] \tag{A.10}$$

A.3 CONCLUSION

This appendix described complementary information about state-space model discretization using the *Backward Euler* method. The proposed method was used to discretize the indirect matrix converter state-space system. This method is based on a Zero-Order holder, and is valid for time-invariant state-space matrices.

For time-variant state-space matrices, the equation derivation follows the same steps, with minor alterations. However, since the converter equations can be written using time-invariant matrices, they were not discussed.

Appendix B – Definitions, Conventions and Pertinent Concepts

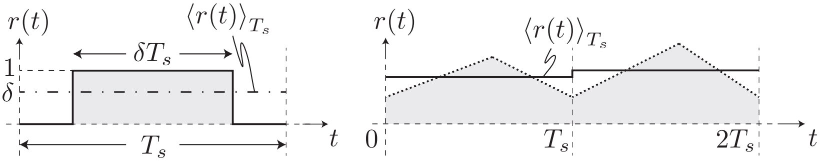
B.1 INTRODUCTION

This appendix presents some definitions, concepts and conventions adopted throughout this document, while aiming to clarify some concepts adopted recalling definitions widely used by the power electronics literature and fundamental to understand the theory proposed by this thesis.

B.2 AVERAGE VALUE

The average value of a signal of a time variant signal $r(t)$ on a determined time interval T_s approach is widely used in power converter modelling, and can be determined according to (B.1). This approach reduces the complexity of mathematical model by transforming time variant signals into a time invariant system, sacrificing the model validity for time intervals lower than two times the considered time interval, according to Shannon's Theorem [44]. An example of this concept is illustrated in Figure B.1.

$$\langle r \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s}^{t} r(\tau)\mathrm{d}\tau \tag{B.1}$$



(a)

(b)

Figure B.1 – Average value of a time variant signal. (a) Representation of a signal pertaining to $\{0, 1\}$ and its average value in a determined time interval. (b) Time variant signal with varying average value.

B.3 CLARKE TRANSFORMATION

Assuming three-phase vector and current vectors, belong to a three-dimensional vector subspace *abc*. Hence, the set $R_{abc} = \{\hat{r}_a, \hat{r}_b, \hat{r}_c\}$ defined by equation (B.2) can be defined as a basis of *abc*. By inspection, it is possible to infer that the vectors belonging to the set R_{abc} are linearly independent.

$$R_{abc} = \left\{ \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}^T, \quad \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}^T, \quad \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}^T \right\} \tag{B.2}$$

A generic vector, here referred as $\vec{r}_{abc} \in abc$, can be written as a linear combination of the basis as in (B.3).

$$\vec{r}_{abc} = r_a \hat{r}_a + r_b \hat{r}_b + r_c \hat{r}_c \tag{B.3}$$

The Clarke (or $\alpha\beta\gamma$) transformation is a linear transformation proposed during the first world war by Edith Clarke [45], and aims to express the vector subspace abc in a stationary reference frame according to equation (B.4).

$$\vec{r}_{\alpha\beta\gamma} = \left[\mathbb{T}_{\frac{\alpha\beta\gamma}{abc}} \right] \vec{r}_{abc} \tag{B.4}$$

The transformation possesses two distinct forms, which are classified as power and amplitude invariant, according to equation (B.5) and table Table B.1. The power invariant transformation aims to obtain an orthonormal set of vector as basis for the vector subspace, while the constant amplitude aims to maintain the amplitude of a vector in both coordinates.

$$\left[\mathbb{T}_{\frac{\alpha\beta\gamma}{abc}} \right] = k_m \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \\ k_0 & k_0 & k_0 \end{bmatrix} \tag{B.5}$$

Table B.1 – Power and amplitude invariant Clarke transformation constants.

Classification	k_m	k_0	$\left\| \left[\mathbb{T}_{\frac{\alpha\beta\gamma}{abc}} \right] \right\|_\infty$	k_t
Power Invariant	$\sqrt{\frac{2}{3}}$	$\frac{1}{\sqrt{2}}$	1	$\sqrt{\frac{3}{2}}$
Amplitude Invariant	$\frac{2}{3}$	1	$\sqrt{\frac{3}{2}}$	1

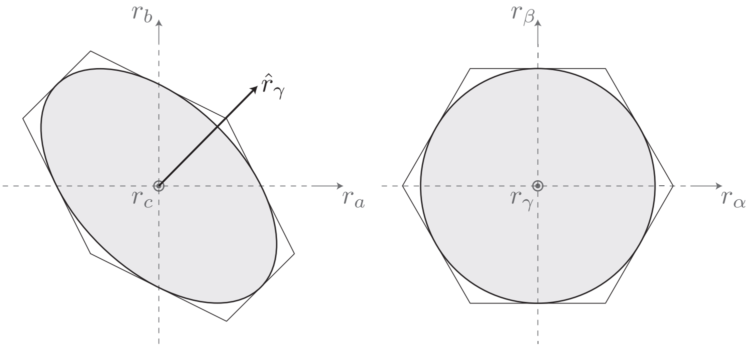


Figure B.2 – Projection of a plane in *abc* coordinates onto a stationary axis $\alpha\beta$.

The set $R_{\alpha\beta\gamma} = \{\hat{r}_\alpha, \hat{r}_\beta, \hat{r}_\gamma\}$, which is also a basis of $\mathbb{R}^3$, is given by (B.6).

$$R_{\alpha\beta\gamma} = \left\{ \begin{bmatrix} k_m \\ 0 \\ k_0 k_m \end{bmatrix}, \begin{bmatrix} -\frac{1}{2}k_m \\ \frac{\sqrt{3}}{2}k_m \\ k_0 k_m \end{bmatrix}, \begin{bmatrix} -\frac{1}{2}k_m \\ -\frac{\sqrt{3}}{2}k_m \\ k_0 k_m \end{bmatrix} \right\} \tag{B.6}$$

Using the set $R_{\alpha\beta\gamma}$ as basis for $\alpha\beta\gamma$, the vector $\vec{r}_{\alpha\beta\gamma}$ can be written as (B.7), where r_α, r_β and r_γ are given by (B.4).

$$\vec{r}_{\alpha\beta\gamma} = r_\alpha \hat{r}_\alpha + r_\beta \hat{r}_\beta + r_\gamma \hat{r}_\gamma \tag{B.7}$$

The coordinate given by the term $r_\gamma \hat{r}_\gamma$ is called zero sequence component. According to equation (B.8). Hence, it affects the axis orthogonal to the plane described by the stationary axis, as illustrated by Figure B.2.

$$\vec{r}_{\gamma,abc} = \left[\mathbb{T}_{\frac{\alpha\beta\gamma}{abc}}\right] r_\gamma \hat{r}_\gamma = \frac{1}{3k_m k_0} r_\gamma \left(\hat{r}_a + \hat{r}_b + \hat{r}_c\right) \tag{B.8}$$

Suppressing the effect of the zero sequence component, it is possible to represent the previous three-dimensional vector subspace by a two dimensional vector subspace described by a stationary axis, here called $\alpha\beta$. Thus, a generic vector $\vec{r}_{\alpha\beta}$ pertaining to $\alpha\beta$ can be described by (B.9).

$$\begin{aligned}\vec{r}_{\alpha\beta} &= r_\alpha \hat{r}_\alpha + r_\beta \hat{r}_\beta \\ \vec{r}_{\alpha\beta} &= k_m \left(r_a - \frac{1}{2} r_b - \frac{1}{2} r_c \right) \hat{r}_\alpha + \frac{\sqrt{3}}{2} k_m \left(r_b - r_c \right) \hat{r}_\beta\end{aligned} \tag{B.9}$$

A stationary axis vector can also be represented by a phasor $\bar{r}$ defined by (B.10) for simplicity, where $\|\vec{r}_{\alpha\beta}\| = \|\vec{r}_{\alpha\beta}\|_2$, considering the set $R_{\alpha\beta} = \{1, j\}$ basis of $\alpha\beta$.

$$\begin{aligned}\bar{r} &= r_\alpha \cos\varphi_r + j r_\beta \sin\varphi_r \\ \bar{r} &= \|\vec{r}_{\alpha\beta}\| \, e^{j\varphi_r} = \|\vec{r}_{\alpha\beta}\| \left(\cos\varphi_r + j \sin\varphi_r \right) \\ \varphi_r &= \angle\vec{r}_{\alpha\beta} = \tan^{-1} \frac{r_\beta}{r_\alpha}\end{aligned} \tag{B.10}$$

The norm and angle of vector $\vec{r}_{\alpha\beta}$ is given by (B.11).

$$\begin{aligned}\|\vec{r}_{\alpha\beta}\| &= k_m \sqrt{r_a^2 + r_b^2 + r_c^2 - r_a r_b - r_b r_c - r_c r_a} \\ \varphi_r &= \tan^{-1} \sqrt{3} \frac{r_b - r_c}{2r_a - r_b - r_c}\end{aligned} \tag{B.11}$$

A generic grid voltage vector can be defined according to (B.12).

$$\vec{u}_{abc} = \begin{bmatrix} U_a \cos\omega_u t \\ U_b \cos\left(\omega_u t - \frac{2\pi}{3}\right) \\ U_c \cos\left(\omega_u t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{B.12}$$

The vector $\vec{u}_{\alpha\beta} \in \alpha\beta$ can be described by (B.13).

$$\begin{aligned}\vec{u}_{\alpha\beta} &= u_\alpha \hat{u}_\alpha + u_\beta \hat{u}_\beta \\ u_\alpha &= \left(U_a + \frac{1}{4} \left(U_b + U_c \right) \right) k_m \cos\omega_u t + \frac{\sqrt{3}}{4} \left(U_c - U_b \right) k_m \sin\omega_u t \\ u_\beta &= \frac{\sqrt{3}}{4} \left(U_c - U_b \right) k_m \cos\omega_u t + \frac{3}{4} \left(U_b + U_c \right) k_m \sin\omega_u t\end{aligned} \tag{B.13}$$

If the system is operating under balanced conditions, it is possible to infer that the voltage amplitude is the same for phases a, b and c. Therefore, (B.13) can be simplified into (B.14).

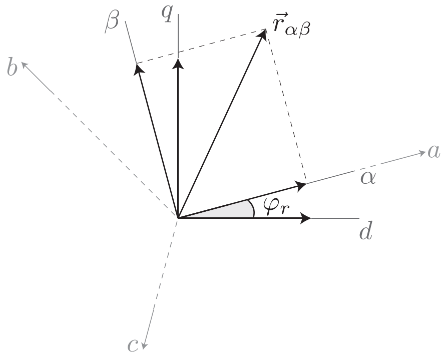


Figure B.3 – Projection of a vector in $\alpha\beta$ coordinates onto the synchronous axis.

$$\vec{u}_{\alpha\beta} = \frac{3}{2} k_m U_{pk} \left(\cos\left(\omega_u t\right) \hat{u}_\alpha + \sin\left(\omega_u t\right) \hat{u}_\beta \right) \tag{B.14}$$

B.4 PARK TRANSFORMATION

The Park transformation is a mathematical manipulation proposed in 1929 by Robert H. Park which aims to represent represent a three-dimensional time-variant vector in a two-dimensional stationary (or synchronous) axis [46]. Hence, this transformation consists in rotating the vector subspace basis $R_{\alpha\beta}$ at a fixed frequency, here called $dq0$.

Hence, a vector belonging to $\alpha\beta\gamma$ can be expressed in the $dq0$ vector subspace according to (B.15), where the transformation matrix is given by (B.16). Figure B.3 shows the projection of a vector in $\alpha\beta$ coordinates in the synchronous axis.

$$\vec{r}_{dq0} = \left[\mathbb{T}_{\frac{dq0}{\alpha\beta\gamma}} \right] \vec{r}_{\alpha\beta\gamma} \tag{B.15}$$

$$\left[\mathbb{T}_{\frac{dq0}{\alpha\beta\gamma}} \right] = \begin{bmatrix} \sin\varphi_r & \cos\varphi_r & 0 \\ \cos\varphi_r & -\sin\varphi_r & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{B.16}$$

Therefore, it is possible to express a transformation matrix from abc to $dq0$ according to (B.17).

$$\left[\mathbb{T}_{\frac{dq0}{abc}}\right] = k_m \begin{bmatrix} \sin\left(\varphi_r\right) & \sin\left(\varphi_r - \frac{2\pi}{3}\right) & \sin\left(\varphi_r + \frac{2\pi}{3}\right) \\ \cos\left(\varphi_r\right) & \cos\left(\varphi_r - \frac{2\pi}{3}\right) & \cos\left(\varphi_r + \frac{2\pi}{3}\right) \\ k_0 & k_0 & k_0 \end{bmatrix} \tag{B.17}$$

B.5 SEQUENCE COMPONENTS

The main idea of sequence components is to decompose an unbalanced system into two rotational systems, one in the counter-clockwise (positive) direction and the other in the clockwise (negative) direction. This is achieved by using the set $R_{\alpha\beta,sym} = \{\hat{r}_p, \hat{r}_n\} \in \alpha\beta$ given by equation (B.18) as a vector space basis for the stationary coordinates.

$$R_{\alpha\beta,sym} = \{\hat{r}_p, \hat{r}_n\} = \left\{e^{j\varphi_r}, e^{-j\varphi_r}\right\} \tag{B.18}$$

Considering a generic grid voltage vector given by (B.12), the Euler identity can be written as in (B.19).

$$\begin{aligned} \cos\omega_u t &= \frac{\hat{u}_p + \hat{u}_i}{2} \\ \sin\omega_u t &= -j\frac{\hat{u}_p - \hat{u}_i}{2} \end{aligned} \tag{B.19}$$

By applying the Euler identity in (B.13), while using the phasor notation as in (B.10), it is possible to obtain (B.20).

$$\begin{aligned} \bar{u} = &\left(U_a + \frac{1}{4}\left(U_b + U_c\right)\right) k_m \frac{\hat{u}_p + \hat{u}_i}{2} - j\frac{\sqrt{3}}{4}\left(U_c - U_b\right) k_m \frac{\hat{u}_p - \hat{u}_i}{2} \\ &+ j\frac{\sqrt{3}}{4}\left(U_c - U_b\right) k_m \frac{\hat{u}_p + \hat{u}_i}{2} + \frac{3}{4}\left(U_b + U_c\right) k_m \frac{\hat{u}_p - \hat{u}_i}{2} \end{aligned} \tag{B.20}$$

Therefore, the voltage phasor $\bar{u}$ can be expressed as in (B.21).

$$\begin{aligned} \bar{u} &= \bar{u}_p \hat{u}_p + \bar{u}_n \hat{u}_n \\ \bar{u}_p &= \frac{1}{2} k_m \left(U_a + U_b + U_c\right) \\ \bar{u}_n &= \frac{1}{2} k_m \left(2U_a - U_b - U_c\right) + j\frac{\sqrt{3}}{2} k_m \left(U_c - U_b\right) \end{aligned} \tag{B.21}$$

From (B.21), it is possible to infer that $\Im\{\bar{u}_p\}$ is null. Therefore, while the trajectory of $\bar{u}$ is non-circular, the trajectory of $\bar{u}_p$ is always circular. However, if the system is operating under balanced voltage conditions, $\bar{u}_n$ is null valued and the trajectory of $\bar{u}$ is circular.

B.6 CONCLUSION

This appendix presented some concepts and definitions which are widely used throughout this thesis, such as Clarke and Park transformations, sequence components and the concept of average value, which is widely used for modelling power converters.

Appendix C – Space Vector Modulation Strategies

C.1 INTRODUCTION

The objective of this appendix is to provide a detailed mathematical analysis for different space-vector modulation strategies applied to the IMC. The following material is based on SVM schemes presented in Chapter 3, and the analysis is based on the switching states proposed in Chapter 2. The converter topology is presented in Figure C.1, and the analysis is based on [8].

The *High-side* voltage and *Low-side* current values are defined by (C.1) and (C.2), respectively. Another important consideration is that $\vec{i}_r$ is proportional to $\vec{v}_r$, i.e, the phase between current and voltage vectors is null. Table C.1 and Table C.2 provide the switching states for the rectifier and inverter stage, respectively.

$$\vec{v}_r = V_r^{pk} \begin{bmatrix} \cos\left(\varphi_r\right) \\ \cos\left(\varphi_r - \frac{2}{3}\pi\right) \\ \cos\left(\varphi_r + \frac{2}{3}\pi\right) \end{bmatrix} \tag{C.1}$$

$$\vec{i}_i = I_i^{pk} \begin{bmatrix} \cos\left(\varphi_i\right) \\ \cos\left(\varphi_i - \frac{2}{3}\pi\right) \\ \cos\left(\varphi_i + \frac{2}{3}\pi\right) \end{bmatrix} \tag{C.2}$$

Table C.1 – Rectifier stage switching states

$\vec{I}_k$	S_{Ap}	S_{Bp}	S_{Cp}	S_{An}	S_{Bn}	S_{Cn}
$\vec{I}_1$	1	0	0	0	1	0
$\vec{I}_2$	1	0	0	0	0	1
$\vec{I}_3$	0	1	0	0	0	1
$\vec{I}_4$	0	1	0	1	0	0
$\vec{I}_5$	0	0	1	1	0	0
$\vec{I}_6$	0	0	1	0	1	0
$\vec{I}_7$	1	0	0	1	0	0
$\vec{I}_8$	0	1	0	0	1	0
$\vec{I}_9$	0	0	1	0	0	1

C.2 HIGH VOLTAGE SPACE VECTOR MODULATION

The HVSVM modulation applies the highest and amplitude and medium amplitude line voltages on the rectifier stage, here called v_l and v_m, respectively. The calculations are made considering a single sector for both stages, i.e. $\varphi_r \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$ and $\varphi_i \in \left[0, \frac{\pi}{3}\right]$. Therefore, v_l and v_m can be described by (C.3).

$$\begin{aligned} v_l &= \sqrt{3} V_r^{pk} \cos\left(\varphi_r - \tfrac{\pi}{6}\right) \\ v_m &= \sqrt{3} V_r^{pk} \cos\left(\varphi_r + \tfrac{\pi}{6}\right) \end{aligned} \tag{C.3}$$

The rectifier stage current average value can be described by (C.4).

$$\langle \vec{i}_r \rangle_{T_s} = \begin{bmatrix} \delta_l^r + \delta_m^r \\ -\delta_m^r \\ -\delta_l^r \end{bmatrix} \langle i_{pn} \rangle_{T_s} \tag{C.4}$$

Thus, the rectifier duty cycles are defined by (C.5) referring to Sector I, while considering the static analysis presented in Chapter 2

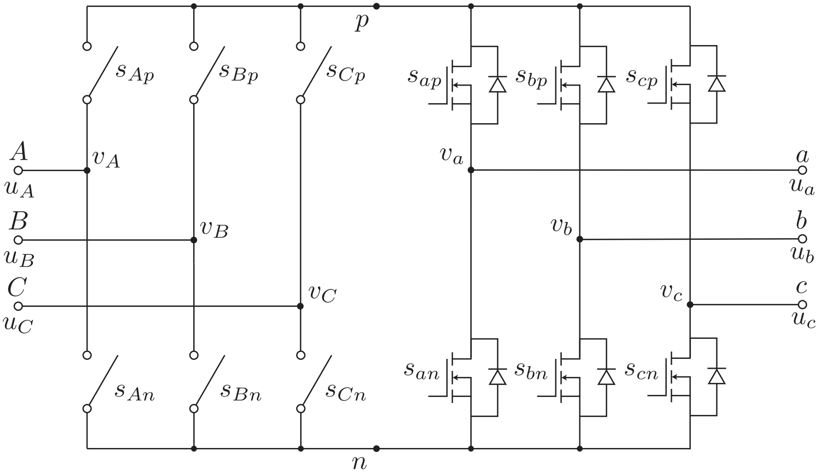


Figure C.1 – Indirect Matrix Converter (IMC) topology. The four-quadrant switches denoted with indexes $\{A, B, C\}$ compose the rectifier-stage, while the switches denoted with indexes $\{a, b, c\}$ compose the inverter stage.

Table C.2 – Inverter stage switching states

$\vec{V}_k$	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}
$\vec{V}_1$	1	0	0	0	1	1
$\vec{V}_2$	1	1	0	0	0	1
$\vec{V}_3$	0	1	0	1	0	1
$\vec{V}_4$	0	1	1	1	0	0
$\vec{V}_5$	0	0	1	1	1	0
$\vec{V}_6$	1	0	1	0	1	0
$\vec{V}_7$	1	1	1	0	0	0
$\vec{V}_8$	0	0	0	1	1	1

and a null phase displacement in the rectifier stage.

$$\begin{aligned} \delta_l^r &= -\frac{\langle i_C \rangle_{T_s}}{\langle i_A \rangle_{T_s}} = \frac{\cos\left(\varphi_r - \frac{\pi}{3}\right)}{\cos\left(\varphi_r\right)} \\ \delta_m^r &= -\frac{\langle i_B \rangle_{T_s}}{\langle i_A \rangle_{T_s}} = \frac{\cos\left(\varphi_r + \frac{\pi}{3}\right)}{\cos\left(\varphi_r\right)} \end{aligned} \tag{C.5}$$

Defined the rectifier times, it is possible to define the average virtual DC link voltage according to (C.6).

$$\langle u_{pn} \rangle_{T_s} = \delta_l^r v_l + \delta_m^r v_m \tag{C.6}$$

The voltage vectors $\vec{V}_1$ and $\vec{V}_2$ can be described by (C.7) in phasorial notation, according to Table C.2.

$$\bar{v}_1^i = \tfrac{2}{3} u_{pn}, \quad \bar{v}_2^i = \tfrac{2}{3} u_{pn} e^{j\frac{\pi}{3}} \tag{C.7}$$

In order to fully utilize the voltage vectors, equation (C.8) guarantees the same relative application time for each vector.

$$\begin{aligned} \delta_1^i &= \frac{\tau_{1,l}^i}{\tau_l^r} = \frac{\tau_{1,m}^i}{\tau_m^r} \\ \delta_2^i &= \frac{\tau_{2,l}^i}{\tau_l^r} = \frac{\tau_{2,m}^i}{\tau_m^r} \end{aligned} \tag{C.8}$$

The inverter stage averaged voltage vector can be calculated by (C.9).

$$\left\langle \bar{v}^i \right\rangle_{T_s} = \left\langle \bar{v}_1^i \right\rangle_{T_s} + \left\langle \bar{v}_2^i \right\rangle_{T_s} \tag{C.9}$$

By substituting (C.7) and (C.8) in (C.9), expression (C.10) can be obtained, and further developed into (C.11).

$$\left\langle \bar{v}^i \right\rangle_{T_s} = \frac{2}{3} \left\langle u_{pn} \right\rangle_{T_s} \left(\delta_1^i + \delta_2^i e^{j\frac{\pi}{3}}\right) \tag{C.10}$$

$$\left\langle \bar{v}^i \right\rangle_{T_s} = \frac{2}{3} \left(\delta_l^r v_l + \delta_m^r v_m\right) \left(\delta_1^i + \delta_2^i e^{j\frac{\pi}{3}}\right) \tag{C.11}$$

The inverter stage reference voltage can be defined by (C.12).

$$\left\langle \bar{v}^i \right\rangle_{T_s} = V_i^{pk} e^{j\varphi_i} \tag{C.12}$$

Therefore, (C.8) can be further derived as (C.13).

$$\begin{aligned} \delta_1^i &= \frac{\sqrt{3}}{2} \frac{V_i^{pk}}{\frac{1}{2}\left\langle u_{pn} \right\rangle_{T_s}} \cos\left(\varphi_i + \tfrac{\pi}{6}\right) \\ \delta_2^i &= \frac{\sqrt{3}}{2} \frac{V_i^{pk}}{\frac{1}{2}\left\langle u_{pn} \right\rangle_{T_s}} \sin\left(\varphi_i\right) \end{aligned} \tag{C.13}$$

The averaged virtual DC link voltage can be rewritten as (C.14).

$$\left\langle u_{pn} \right\rangle_{T_s} = \frac{3}{2} V_r^{pk} \frac{1}{\sin\left(\varphi_r\right)} \tag{C.14}$$

The minimum average virtual DC link voltage is defined by (C.15).

$$\min\left(\left\langle u_{pn} \right\rangle_{T_s}\right) = \frac{3}{2} V_r^{pk} \tag{C.15}$$

The converter gain is limited according to (C.16).

$$\max\left(V_i^{pk}\right) = \frac{1}{\sqrt{3}} \min\left(\left\langle u_{pn} \right\rangle_{T_s}\right) = \frac{\sqrt{3}}{2} V_r^{pk} \tag{C.16}$$

Finally, by substituting the voltage relations in (C.8) in (C.13), as well as (C.14), a modulation index can be written as (C.17), and the inverter vector times can be written as (C.18).

$$m = \frac{2}{\sqrt{3}} \frac{V_i^{pk}}{V_r^{pk}} \in [0,1] \tag{C.17}$$

$$\begin{aligned}
\tau^i_{1,l} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\cos\left(\varphi_i + \tfrac{\pi}{6}\right)\\
\tau^i_{1,m} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right)\cos\left(\varphi_i + \tfrac{\pi}{6}\right)\\
\tau^i_{2,l} &= mT_s \cos\left(\varphi_r - \tfrac{\pi}{3}\right)\sin\left(\varphi_i\right)\\
\tau^i_{2,m} &= mT_s \cos\left(\varphi_r + \tfrac{\pi}{3}\right)\sin\left(\varphi_i\right)
\end{aligned} \tag{C.18}$$

The null vector time can be defined by (C.19).

$$\tau_0 = T_s - \tau^i_{1,l} - \tau^i_{1,m} - \tau^i_{2,l} - \tau^i_{2,m} \tag{C.19}$$

The difference between HVZCS and HVZVS modulation is that the null vector is applied by the inverter stage in the ZCS modulation scheme, and by the rectifier stage in the ZVS modulation. However, the equations obtained in this section are valid for both cases.

C.3 LOW VOLTAGE SPACE VECTOR MODULATION

The LVSVM modulation scheme is very similar to the HVSVM scheme previously presented. The main difference is that the medium and lowest amplitude voltage vectors are applied in the rectifier stage, here called v_m and v_s, defined by (C.20) respectively. Again, the calculations are made considering a single sector for both stages, i.e. $\varphi_r \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$ and $\varphi_i \in \left[0, \frac{\pi}{3}\right]$.

$$\begin{aligned}
v_m &= \sqrt{3}V_r^{pk}\cos\left(\varphi_r + \tfrac{\pi}{6}\right)\\
v_s &= \sqrt{3}V_r^{pk}\cos\left(\varphi_r - \tfrac{\pi}{2}\right)
\end{aligned} \tag{C.20}$$

The rectifier stage current average value can be described by (C.21).

$$\langle \vec{i}_r \rangle_{T_s} = \begin{bmatrix} \delta^r_m \\ \delta^r_s - \delta^r_m \\ -\delta^r_s \end{bmatrix} \langle i_{pn} \rangle_{T_s} \tag{C.21}$$

The rectifier vector duty cycle can be obtained through (C.22), considering a null phase displacement between voltage and current on the rectifier stage and assuming $\delta^r_m + \delta^r_s = 1$

$$\begin{aligned}\delta_m^r &= \frac{\langle i_A\rangle_{T_s}}{\langle i_B\rangle_{T_s}+2\langle i_A\rangle_{T_s}} = \frac{\cos(\varphi_r)}{\sqrt{3}\cos\left(\varphi_r-\frac{\pi}{6}\right)}\\ \delta_s^r &= -\frac{\langle i_C\rangle_{T_s}}{\langle i_B\rangle_{T_s}+2\langle i_A\rangle_{T_s}} = \frac{\cos\left(\varphi_r-\frac{\pi}{3}\right)}{\sqrt{3}\cos\left(\varphi_r-\frac{\pi}{6}\right)}\end{aligned} \tag{C.22}$$

The average virtual DC link voltage can be written as (C.23).

$$\langle u_{pn}\rangle_{T_s} = \delta_m^r v_m + \delta_s^r v_s = \frac{\sqrt{3}}{2}V_r^{pk}\frac{1}{\cos\left(\varphi_r-\frac{\pi}{6}\right)} \tag{C.23}$$

Therefore, the inverter voltage vector maximum amplitude is given by (C.24).

$$\max\left(V_i^{pk}\right) = \frac{1}{\sqrt{3}}\min\left(\langle u_{pn}\rangle_{T_s}\right) = \frac{1}{2}V_r^{pk} \tag{C.24}$$

Following the same procedure as the HVZCS vector time derivation, the modulation index and vector times for the inverter side is given by (C.25) and (C.26), respectively.

$$m = \frac{2}{\sqrt{3}}\frac{V_i^{pk}}{V_r^{pk}} \in \left[0, \frac{1}{\sqrt{3}}\right] \tag{C.25}$$

$$\begin{aligned}\tau_{1,m}^i &= mT_s\cos(\varphi_r)\cos\left(\varphi_i+\frac{\pi}{6}\right)\\ \tau_{1,s}^i &= mT_s\cos\left(\varphi_r-\frac{\pi}{3}\right)\cos\left(\varphi_i+\frac{\pi}{6}\right)\\ \tau_{2,m}^i &= mT_s\cos(\varphi_r)\sin(\varphi_i)\\ \tau_{2,s}^i &= mT_s\cos\left(\varphi_r-\frac{\pi}{3}\right)\sin(\varphi_i)\end{aligned} \tag{C.26}$$

Similarly to the previous case, the null vector time can be defined by (C.27).

$$\tau_0 = T_s - \tau_{1,l}^i - \tau_{1,m}^i - \tau_{2,l}^i - \tau_{2,m}^i \tag{C.27}$$

Once again, the greatest difference between LVZCS and LVZVS is that in the LVZCS modulation scheme, the null vector is applied by the inverter stage, while in the LVZVS scheme the null vector is applied in the rectifier stage.

C.4 CONCLUSION

This appendix presented the derivation of the vector times presented in Chapter 2, as well as the operation limits of HVSVM and LVSVM. The times here obtained serve as basis for many different modulation schemes, such as ZVS, ZCS and SLS and serves as a basis for TLSVM, which is presented in [8].