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ANALYSIS AND DESIGN OF A SUBTHRESHOLD CMOS SCHMITT TRIGGER CIRCUIT

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"*Well, there is only one mind expanding drug this man enjoys, and that's called school.*" – Sheldon Cooper, The Big Bang Theory.

RESUMO

Nesta tese, o disparador Schmitt (ou Schmitt *trigger*) CMOS clássico (ST) operando em inversão fraca é analisado. A transferência de tensão DC completa é determinada, incluindo expressões analíticas para as tensões dos nós internos. A transferência de tensão DC resultante do ST apresenta um comportamento contínuo mesmo na presença da histerese. Nesse caso, a característica da tensão de saída entre os limites da histerese é formada por um segmento metaestável, que pode ser explicado em termos das resistências negativas dos subcircuitos NMOS e PMOS do ST. A tensão mínima para o aparecimento da histerese é determinada fazendo-se a análise de pequenos sinais. A análise de pequenos sinais também é utilizada para a estimativa da largura do laço de histerese. É mostrado que a histerese não aparece para tensões de alimentação menores que 75 mV em 300 K. A análise do ST operando como amplificador também foi feita. A razão ótima dos transistores foi determinada com o objetivo de se maximizar o ganho de tensão. A comparação do disparador Schmitt com o inversor CMOS convencional destaca as vantagens e desvantagens de cada um para aplicações de ultra-baixa tensão. Também é mostrado que o ST é teoricamente capaz de operar (com ganho de tensão absoluto ≥ 1) com uma tensão de alimentação tão baixa quanto 31.5 mV, a qual é menor do que o conhecido limite prévio de 36 mV, para o inversor convencional. Como amplificador, o ST possui ganho de tensão absoluto consideravelmente maior que o inversor convencional na mesma tensão de alimentação. Três circuitos integrados foram projetados e fabricados para estudar o comportamento do ST com tensões de alimentação entre 50 mV e 1000 mV.

Palavras-chave: Schmitt trigger. Disparador Schmitt. Ultra-Baixa Tensão. Inversão Fraca. Ultra-Baixa Potência. Inversor CMOS.

RESUMO EXPANDIDO

1 INTRODUÇÃO

Nos últimos anos, desenvolvimentos significativos direcionados a ultra-baixa tensão foram feitos, com foco principal em aplicações autônomas que dependem de mini ou micro baterias ou que captam a energia do meio ambiente. Tais fontes de energia incluem sinais de radiofrequência, vibradores mecânicos, geradores termoelétricos (TEG), células de combustível de glicose e células fotovoltaicas. Ao mesmo tempo, avanços contínuos na eletrônica em geral, com mais e melhores funcionalidades, permitiram um aumento tremendo em diversos tipos de equipamentos, incluindo sistemas para comunicação, processamento da informação, entretenimento, computação ubíqua, redes de sensores e sistemas médicos.

Fontes ambientais de energia (*energy harvesting*) representam uma importante fonte de potência. No entanto, o nível de tensão disponível é muito baixo, geralmente em torno de 100 mV. Por exemplo, geradores termoelétricos, que dependem da diferença de temperatura entre o corpo e o ambiente, fornecem uma tensão entre 50 mV e 75 mV, na faixa de 1-3 K. Células fotovoltaicas fornecem centenas de milivolts em ambientes escuros. E, finalmente, uma fonte interessante de energia é proveniente das árvores, focando em aplicações de monitoramento climático e da vida selvagem. A tensão disponível é devida a diferença de pH entre o caule da árvore e o solo.

Uma vez que a tensão disponível é extremamente baixa, os métodos convencionais para alcançar alto ganho de tensão não são apropriados devido à dificuldade de impor a saturação aos transistores. Uma técnica interessante para minimizar esse problema é o uso de realimentação positiva para aumentar o ganho do amplificador. Nessa tese, optamos pela utilização da realimentação positiva presente no disparador Schmitt (Schmitt *trigger*) para se obter um amplificador de alto ganho.

A operação de circuitos digitais CMOS com tensão em torno de 500 mV, ou abaixo disso, força os transistores operarem no regime de inversão fraca ou sublimiar. Esse regime é caracterizado pela relação exponencial entre correntes e tensões dos terminais do transistor.

Diversas aplicações foram desenvolvidas com o objetivo de se minimizar a tensão de alimentação dos circuitos como, por exemplo, um circuito digital operando com $V_{DD} = 4\ kT/q$ (= 103 mV a 300 K), cadeias de 1000 inversores alimentado com 50 mV, um filtro 8x8 tipo

FIR funcionando com alimentação de 85 mV, memórias SRAM baseadas no disparador Schmitt (ST) funcionais até o limite de 150 mV e, finalmente, um multiplicador 8x8 baseado em estruturas derivadas do disparador Schmitt operando com alimentação de 62 mV. Esta última aplicação inspirou o desenvolvimento desta tese.

2 OBJETIVO

Embora alguns autores afirmem que a cascata de 4 transistores entre alimentação e terra presente no disparador Schmitt clássico não seja apropriado para aplicações de ultra-baixa tensão, ele tem sido empregado como o elemento principal em diversos circuitos de ultra-baixa tensão. O disparador Schmitt clássico é um dos circuitos mais úteis tanto para aplicações digitais quanto analógicas. Analisando o circuito, os transistores de realimentação funcionam como uma fonte de corrente controlada por tensão para os nós intermediários. Nesse sentido, a cascata de 4 transistores é de fundamental importância para o funcionamento do circuito.Além disso, a cascata de transistores já foi utilizada para redução das correntes de fuga.

O disparador Schmitt foi analisado extensivamente em inversão forte. Entretanto, em inversão fraca somente alguns estudos parciais foram realizados, como por exemplo, circuitos lógicos baseados no disparador Schmitt, com o objetivo de se maximizar a razão entre a corrente dos transistores ligados e desligados.

Esta tese tem como objetivo a completa análise do disparador Schmitt operando em inversão fraca. O comportamento estático do disparador Schmitt é analisado em profundidade, são determinadas as tensões nodais, as dimensões ótimas dos transistores que maximiza o ganho quando funcionando como amplificador são calculadas, é explicada a histerese, com comprovações dos resultados através de medidas em circuitos projetados e fabricados especialmente com esses objetivos.

3 RESULTADOS

Teoricamente os inversores CMOS podem funcionar até o limite de 36 mV (em 300K) de tensão de alimentação. Porém, resultados analíticos mostram que o disparador Schmitt otimizado pode funcionar com uma tensão de alimentação de até 31.5 mV (em 300 K), representando um novo limite para circuitos de ultra-baixa tensão.

Se comparado com o inversor convencional CMOS, o ST tem muitas vantagens para aplicações de ultra-baixa tensão. A primeira é que a presença de histerese resulta num circuito comparador de dois níveis com boa eficiência na presença de ruído. Ao mesmo tempo, seu consumo de potência é consideravelmente menor que comparadores baseados em amplificadores operacionais.

A segunda vantagem é que o ganho de tensão do ST é muito maior do que o do inversor convencional quando não há histerese. Entretanto, a desvantagem do ST é que a área ocupada pelo ST é grande, o que resulta em uma frequência de operação menor.

Nos dois casos quando há e quando não há histerese, a margem de ruído estático do ST é maior do que a do inversor convencional. Adicionalmente, o ST é menos susceptível a variações dos parâmetros tecnológicos e de temperatura. Esses dois fatos permitem que o ST seja operacional para tensões de alimentação extremamente baixas.

ABSTRACT

In this thesis, the classical CMOS Schmitt trigger (ST) operating in weak inversion is analyzed. The complete DC voltage transfer characteristic is determined, including analytical expressions for the internal node voltage. The resulting voltage transfer characteristic of the ST presents a continuous output behavior even when hysteresis is present. In this case, the output voltage characteristic between the hysteresis limits is formed by a metastable segment, which can be explained in terms of the negative resistance of the NMOS and PMOS subcircuits of the ST. The minimum supply voltage at which hysteresis appears is determined carrying out small-signal analysis, which is also used to estimate the hysteresis width. It is shown that hysteresis does not appear for supply voltages lower than 75 mV at 300 K. The analysis of the ST operating as a voltage amplifier was also carried out. Optimum transistor ratios were determined aiming at voltage gain maximization. The comparison of the ST with the standard CMOS inverter highlights the relative benefits and drawbacks of each one in ULV applications. It is also shown that the ST is theoretically capable of operating (voltage gain ≥ 1) at a supply voltage as low as 31.5 mV, which is lower than the well-known limit of 36 mV, for the standard CMOS inverter. As an amplifier, the ST shows considerable higher absolute voltage gains than those showed by the conventional inverter at the same supply voltages. Three test chips were designed and fabricated to study the operation of the ST at supply voltages between 50 mV and 1000 mV.

Keywords: Schmitt trigger. Ultralow Voltage. Subthreshold Operation. Ultralow Power. CMOS Inverter.

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LIST OF ABBREVIATIONS

B	Bulk terminal
BB	Body Bias
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
CMOS	Complementary MOS
D	Drain terminal
DC	Direct Current
FBB	Forward Body Bias
FDSOI	Fully Depleted Silicon on Insulator
FET	Field Effect Transistor
FF	Fast NMOS and PMOS transistors
FIR	Finite Impulse Response
FS	Fast NMOS and slow PMOS transistors
G	Gate terminal
Ge	Germanium
IC	Integrated Circuit
IoE	Internet of Everything
IoT	Internet of Things
ITRS	International Roadmap for Semiconductors
KCL	Kirchhoff Current Law
LER	Line Edge Roughness
NMOS	N-type MOST
NBB	No Body Bias
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOST	Metal Oxide Semiconductor Transistor
OP-AMP	Operational Amplifier
PDN	Pull Down Network
PMOS	P-type MOST
PUN	Pull Up Network
PVT	Process, Voltage, and Temperature
RBB	Reverse Body Bias
RDF	Random Dopant Fluctuations
RO	Ring Oscillator
RSCE	Reverse Short Channel Effect
S	Source terminal
SF	Slow NMOS and fast PMOS transistors
Si	Silicon
SNM	Signal-to-Noise Margin

SoS	Silicon-on-sapphire
SRAM	Static Random Access Memory
SS	Slow NMOS and PMOS transistors
ST	Schmitt Trigger
TEG	Thermo-electric generator
TT	Typical NMOS and PMOS threshold voltage transistors
ULP	Ultralow Power
ULV	Ultralow Voltage
VTC	Voltage Transfer Characteristic
VTC^{-1}	Inverted Voltage Transfer Characteristic
ZBB	Zero Body Bias

LIST OF SYMBOLS

2ε	Output voltage swing
ϕ_t	Thermal voltage
μ	Carrier mobility
$c_{0\text{-}4}$	Coefficients of the 4th degree ST transfer function
C'_{OX}	Gate capacitance per unit area
C_O	Output capacitance
C_L	Load capacitance
clk	Clock signal
$d_{0\text{-}4}$	Coefficients of the ST output voltage swing
G	Voltage gain
g_m	Gate transconductance
g_{md}	Drain transconductance
g_{ms}	Source transconductance
I	Current strength of the transistor
i_d	Small-signal drain current
I_D	Drain current of the transistor
$I_{F(R)}$	Forward (reverse) current
$i_{f(r)}$	Forward (reverse) inversion level
I_O	Current scaling factor of the transistor
I_{ON}	On or driving current
I_{OFF}	Off or leakage current
I_{SQ}	Specific current of the transistor
k	Boltzmann constant
L	Transistor length
m	Number of inputs of a digital gate
n	Slope factor
$N(P)$	N(P)-type transistor
q	Electron charge
Q'_{IS}	Normalized inversion charge at the source
Q'_{IX}	Normalized inversion charge along the channel
S	Aspect ratio of the transistor
T	Absolute temperature
V_{DD}	Positive supply voltage
V_{DDmin}	Minimum supply voltage
V_{DB}	Drain-bulk voltage
V_{DS}	Drain-source voltage
V_{GB}	Gate-bulk voltage
V_H	High-level voltage
V_I	Input voltage

v_I	Small-signal input voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_L	Hysteresis width voltage of the Schmitt trigger
V_M	Threshold, trip or transition voltage of the gate
V_O	Output voltage
v_O	Small-signal output voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_P	Pinch-off voltage of the transistor
V_{SB}	Source-bulk voltage
V_{T0}	Threshold voltage
V_X	Voltage at node X
v_X	Small-signal voltage at node X
V_W	Body bias compensation voltage
V_Y	Voltage at node Y
v_Y	Small-signal voltage at node Y
W	Transistor width

1 INTRODUCTION

In recent years, significant developments towards ultralow voltage have been made, mainly focusing on autonomous applications that rely on miniature batteries or that harvest energy from the environment [1],[2]. Such sources of energy include RF signals, mechanical vibrators, body-worn thermo-electric generators (TEG), glucose fuel cells and photovoltaic cells. At the same time, continuous advances in general electronics, with more and better functionalities, allowed tremendous increase in several kinds of equipments, including systems for communication, information processing, entertainment, ubiquitous computing, sensor networks, and medical systems.

In 2009, electronic devices accounted for 15 % of household electricity consumption, and it may double by 2020, and triple by 2030 [3]. Even for those applications that do not rely on batteries but are always connected to the wall plug, any technique which reduces power consumption is welcome. Consequently, not only voltage constrained applications may benefit from ultralow voltage techniques; all electronic devices shall benefit from them, consuming less energy and in a more efficient way. For applications that rely on or need a battery such as implantable devices, hearing-aid devices, or environment sensors, ultralow voltage is required in order to extend battery life and avoid or postpone surgical interventions or trips to places of difficult access such as the middle of a forest. In this sense, Professor Jan Rabaey predicts that in the near future the majority of objects will have a wireless connection, resulting in billions, or even trillions of connected devices, called the sensory swarm [4]. This will be enabled by the pervasive wireless networking and ultralow power technologies. Gartner, Inc. predicts that Internet of Things (IoT), the network of physical objects that contain embedded technology to communicate and sense or interact with their internal states or the external environment and which excludes portable computers, tablets and smart phones, will grow to 26 billion units in 2020 [5]. At the same time, ABI Research states that ultralow power technologies, the key enabler of the Internet of Everything (IoE), will allow 30 billion devices by 2020 [6], following the same trend. All these devices must capture their own energy, once it is just impossible for all of them to use batteries. Moreover, the environment just cannot handle all the quantity of batteries after their disposal.

Ambient energy-harvesting sources represent an important source of power. However, the voltage level available from them is very low,

generally below 100 mV. For example, thermo-electric generators (TEG) based on bismuth telluride, Bi_2Te_3 [7], that rely on the temperature difference between the human body and the environment, in the range of 1-3 K, sources a voltage between 50 mV and 75 mV [8]. Similarly, photovoltaic cells provide hundreds of milivolts in dark office environments [9]. Finally, an interesting source of energy is available from trees, focusing applications for climatic and wildlife monitoring, as shown in Fig.1. Supplied voltage is due to pH difference between the tissue of the tree (points X or Y above the soil) and the soil (point B), and is in the range of 20 mV to 200 mV [10].

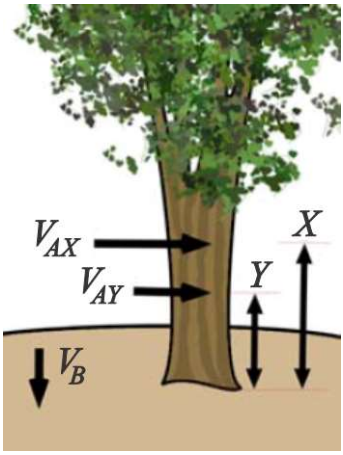


Figure 1 – Energy harvested from a tree, measured at V_{AX} or V_{AY}, away X or Y from the reference voltage V_B. From [10].

As the supply voltage of digital circuits is reduced to extremely low values, in the range of tens of millivolts, the output voltages corresponding to the logic levels '0' and '1' deviates significantly from the supply rails. This situation characterizes ultralow voltage operation [11]. However, this concept is not widely accepted and here we consider ultralow voltage simply the operation of the circuits in the subthreshold regime.

In the ultralow voltage context, DC-DC converters are widely used to convert one voltage level into another in both discrete and integrated circuits (IC). However, these converters suffer from poor efficiency (around 20 % in ultralow voltage regime), may require non-integrated inductors and capacitors and some of them need considerable startup voltages (in the range of 200-700 mV) [10],[12]. Consequently,

it is very interesting to supply digital circuits directly from the input source or through a step down low dropout linear regulator, without the need of a step up converter. The drawback of the linear step down regulators is that they reduce the (already low) voltage available for the digital circuits; so, supplying the circuits directly from the input source is the preferred option.

Now, considering the technologies available in the present and given the dynamics of the semiconductor industry, the commercial off-the-shelf electronics nowadays and in the near future will continue to use CMOS technology. As predicted by the Moore law, to keep costs within acceptable range, CMOS technology is the preferred one or even the mandatory solution for ultralow power and ultralow voltage applications [13],[14]; bulk CMOS technology based on silicon (Si) substrate is the cheapest and most used one. Since ultralow voltage applications do not really respond at high speed, mature bulk CMOS technologies are suitable and preferred in terms of costs [15].

The operation of digital logic and memories in subthreshold regime requires device, circuit and architectural design optimizations, different of those normally used in strong inversion [16]. Circuits that operate in subthreshold regime suffer from low speed. However, these circuits are intended for ultralow power and ultralow voltage applications and not high performance ones [16]. Actually, the most crucial challenges faced by the circuits operating in subthreshold are: degradation of performance, ensure energy efficiency under performance/voltage range, reduction of yield due to process, voltage or temperature (PVT) variations, increased leakage to overall energy budget ratio, large design effort to ensure performance/energy constraints [17]. All these topics are of great importance and have been addressed along the years, even though a lot of research still needs to be done.

1.1 CIRCUITS WITH FEEDBACK

Under extremely low supply voltages, conventional methods for achieving high voltage gain are not appropriate due to the difficulty of imposing that the transistors operate in saturation [18]-[20]. An interesting technique to mitigate this drawback is the use of positive feedback to generate a compensating negative conductance for the purpose of enhancing the amplifier gain [21]-[23]. However, the structures proposed in [21]-[23] rely on the existence of differential signals to generate a negative resistance to compensate the positive

resistance at the output. Generating differential voltages with low supply voltages is not an easy task.

The arrangement of Fig. 2 (a) represents the basic diagram of feedback circuits. A linear amplifier with gain A receives as input the sum of the input voltage and a fraction of the output multiplied by the feedback factor, k. The resulting static gain is given by $G = V_O / V_I = A / (1 - kA)$.

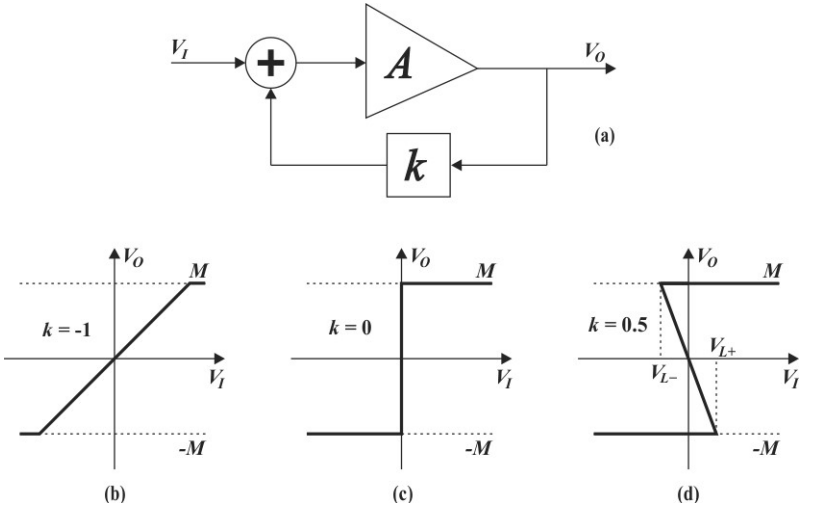


Figure 2 – (a) Basic structure of a feedback circuit; transfer characteristic of a feedback circuit with (b) $k = -1$; (c) $k = 0$; (d) $k = 0.5$. From [24].

Figure 2 (b)-(d) shows the input-output transfer characteristic of the circuit of Fig. 2 (a) for different values of the feedback factor [24].

Negative feedback occurs when $k < 0$. Assuming a high gain linear amplifier ($A \to \infty$), the circuit operates with a positive gain of $-1/k$. For $k = -1$, the circuit operates as a voltage follower ($G = 1$). The circuit operates as an ideal discriminator when no feedback is present ($k = 0$); the output assumes positive saturation M when $V_I > 0$, and negative saturation $-M$ when $V_I < 0$.

Positive feedback occurs when $k > 0$. Little changes on the input are amplified in a self-supporting loop until the output saturates at either a positive or a negative value. The loop feeds back a voltage of Mk (or $-Mk$) that must be surpassed by the input voltage, *i.e.* $V_I < -Mk$ (or $V_I > Mk$) in order to move the output to the other direction, where it saturates again. The transitions from the two output levels are considerably sharp

for reasonable high supply voltages. Within the hysteresis limits (V_{L+} and V_{L-}), the output has two stable levels and one metastable level, which is prone to move to one of the stable levels. The transition from the metastable level to any of the stable levels is represented by a negative resistance. The transition from one stable output to the other stable output is a dynamic phenomenon [25],[26], not considered in Fig. 2 (a).

In this thesis we have opted to make use of the positive feedback present in the Schmitt trigger to obtain a high gain amplifier.

1.2 LOGIC CIRCUITS FOR ULTRALOW VOLTAGE OPERATION

Different techniques and approaches can be used to implement logic functions in CMOS technology, considering the ease of implementation, robustness, area, density, speed, and power dissipation [13]. However, there is no specific or single solution that solves all these issues at the same time.

Pseudo-NMOS logic working in subthreshold regime was first proposed in [27]. It requires an always on PMOS transistor as an active load, which actually represents the main drawback of this logic family. The logic function is determined by a series/parallel association of NMOS transistors. Although pseudo-NMOS logic exhibits lower delays and lower power-delay product (PDP) if compared to the static CMOS counterpart in subthreshold regime of operation, it is less attractive when total energy per cycle is considered [28]. Also, note that the NMOS transistors that evaluate the logic function are fighting against a single PMOS transistor. If local and global process variations are taken into account, this logic style provides higher output level variability when operating in subthreshold regime, resulting in low yield.

Sub-Domino logic is the Domino logic operating in the subthreshold regime and was proposed in [29] as an alternative for ultralow voltage applications. Sub-Domino logic is a dynamic and dual-phase logic in which a clock signal controls the precharge and the evaluate phases. At the precharge phase, the output node can be charged to either a high (logic function is determined by series/parallel array of NMOS transistors) or a low (logic function is determined by series/parallel array of PMOS transistors) level, depending on the circuit topology. However, note that, depending on the input signal pattern, at the precharge phase the output of the gate is charged (or discharged) to immediately be discharged (or charged) at the evaluation phase. Thus, the activity of the output signal can be high, leading to a high

dissipation of energy, if compared to the static logic [30]. The main drawbacks of the Sub-Domino logic are: it requires an inverter at the output in order to allow cascading of the gates, it is highly sensitive to noise [29], and due to the fact that the evaluate phase can be quite long in subthreshold regime of operation, the dynamic node may lose charge because of the leakage currents, resulting in logic errors.

CMOS static logic is the most common logic style in subthreshold regime of operation due to its robustness [31] and simplicity. It requires no clock or differential signals for proper operation, it has good static noise margins, it does not have dynamic nodes, and it can be cascaded very easily. For these reasons, static logic is the best general-purpose option in subthreshold [32] among other available techniques such as the ones presented in the previous paragraphs. The design of static logic gates can be automated with a high degree of confidence.

However, as the supply voltage is reduced, the dependence of the performance on PVT variations reduces and degrades the usage of the conventional CMOS static logic gates in subthreshold (with no body bias – NBB, or zero body bias – ZBB), to the same extension of other logic families. For example, a variation in the threshold voltage, which can be in the range of ±30 mV for current technologies, can shift right or left the voltage transfer characteristic (VTC) and, so, degrade the static noise margin (SNM) of the standard inverter. Threshold voltage variation is also responsible for the increase in the minimum operating supply voltage of the SRAMs. To minimize the effects of PVT variations, a number of compensation techniques have been developed, some of which include body-bias (BB) compensation [33]-[35], and tunable supply and body biasing [36] voltages. The idea behind all the compensations techniques is to equalize or tune the currents of the MOSFETs, with the application of a proper bias voltage to the body of each transistor, as shown in Fig. 3. The bias voltage applied to the p-channel transistors, V_{BP}, and n- channel transistors, V_{BN}, can be equal or not, depending on the bias voltage generator, design and application.

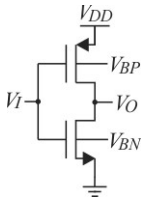
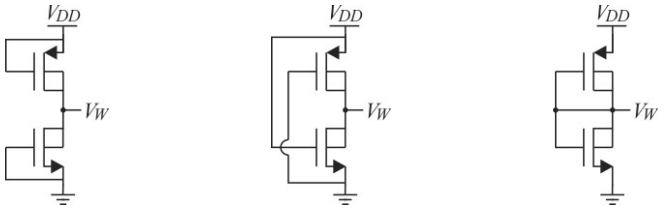


Figure 3 – CMOS inverter with body bias.

Body-bias compensation techniques can be divided into two groups. The first one is the Forward Body Bias (FBB) technique, which uses bias voltages that lie between the supply rails. The main advantages of FBB are the simplicity to generate the bias voltages and the increase in the maximum operating frequency of the transistor [35]. However, the technique has a stringent drawback: the parasitic source-bulk and drain-bulk diodes are forward biased, thus increasing power dissipation [35]. FBB is limited to 600-700 mV of supply voltage. The second technique is the Reverse Body Bias (RBB), which uses bias voltages that are higher than the positive supply voltage for the PMOS transistors and lower than the negative supply voltage (generally ground) for the NMOS transistors. Generating the bias voltages for RBB is not simple and may require charge-pumps or other boost converters. The advantages of RBB is that source-bulk and drain-bulk diodes are always reverse biased and the leakage currents of both NMOS and PMOS transistors are reduced, which in turn, reduces the static power dissipation of the logic gate.

Figure 4 shows three FBB body bias generators; note that the bodies of the transistors are connected to the drains. The bias generator of Fig. 4 (a) generates a voltage V_W which, applied to the NMOS and PMOS bodies of an identical inverter, will (try to) equalize the off or leakage currents of the NMOS and PMOS transistors [36]. The bias generator of Fig. 4 (b) equalizes the on or driving currents of the transistors [35], and so the rise and fall times of a conventional inverter. Finally, the bias generator of Fig. 4 (c) equalizes the currents when the input voltage is equal to the output voltage [35], i.e., it centralizes the voltage transfer characteristic of the inverter (but does not necessarily equalize the rise and fall times). V_W is the generated voltage (to be applied to both NMOS and PMOS transistors in these cases).



(a) (b) (c)

Figure 4 – Body-bias generators that: (a) equalizes off currents [36]; (b) equalizes on currents [35]; (c) centralizes the VTC of the inverter [35].

Body-biasing can be applied to NAND, NOR and other logic gates as well. Note, however, that body-biasing is not limited to CMOS static logic; it can be used by any other circuit, with proper bias generators in order to reduce the effects of PVT variations.

As already stated, static logic is one of the possible techniques intended for ultralow voltage applications. From the logic families mentioned above, static logic gates are the current trend [32] in ultralow voltage applications. Particularly, static logic gates based on the Schmitt trigger (ST) inverter is a promising approach for ULV. Detailed explanation about the ST architectures will be given in Section 1.4.

1.3 ULTRALOW VOLTAGE APPLICATIONS

The operation of CMOS digital circuits from supply voltages of 500mV or lower forces, in many cases, the transistors to operate in the weak inversion, or subthreshold, regime [37]. This regime is characterized by the exponential relationship between currents and terminal voltages. The design of subthreshold circuits has been focused on obtaining minimum energy per logic operation [38], but there are applications for which a reduction of the supply voltage below the value that results in the minimum energy per operation is advantageous [12], [39]. In effect, for applications where most components are often in the sleep mode, reducing the supply voltage to the minimum necessary to maintain the active circuits operational, the standby and total average power values are lower.

Digital circuits operating at $V_{DD} = 4kT/q$ (= 103mV at 300K) were fabricated by IBM in 2001 [34]. A further reduction in the supply voltage is possible because the fundamental limit of low voltage operation for the CMOS inverter, as shown in [40], is 36mV at 300K.

In order to approximate to this limit and in an attempt to compensate for the spreading of process parameters from wafer to wafer, body bias is applied to an 1000-stage inverter chain in [41] and to a 8x8 FIR filter in [42], achieving supply voltages of only 50 mV and 85 mV, respectively. The body bias compensation technique used applies different voltages to the bodies of the PMOS and NMOS transistors. The result is a lower spread of the trip point with PVT variations. With the same purposes, in [43] a post-fabrication step is used to inject charge and correct the within-die threshold voltage variation of the MOSFETs in order to minimize the supply voltage of simple CMOS combinational logic circuits. With this technique, the supply voltage of the circuits was successfully reduced from 94 mV to 74 mV. However, the technique

requires post-fabrication steps, which can be costly in volume applications.

As part of digital systems, static random access memories (SRAM) have a particular importance in both high and low voltage applications since they dissipate as much as 70 % of the total energy as leakage energy [44], and can occupy an area of about 85 % of the die, in some applications. In [45]-[48], a non symmetric Schmitt trigger-based inverter (with no PMOS feedback mechanism) was applied to a SRAM memory (ST-SRAM) comprised of 10 transistors, in order to maximize the static noise margin and reduce power consumption. In [49] the proposed ST-SRAM was compared with other SRAM topologies with 4 to 10 transistors in the cell. The ST memory was proposed because the low supply voltage coupled with intra-die and inter-die process variations of the conventional 6-transistors SRAM and other topologies suffer from memory failures such as read failure, write failure, hold failure and access time failure. The result is that the ST-SRAM cell exhibits built-in process variation tolerance, which results in higher read, write, and hold noise margins. Moreover, as stated in [45], the 6-transistor cell is *de facto* SRAM topology for both high and low voltages (actually, what makes the 6T cell the *de facto* topology is the number of signals to access it, three in total, and not the number of transistors). The ST-SRAM can be readily interchangeable with the 6T SRAM at higher levels of abstraction. The proposed ST-RAM retains data at a supply voltage as low as 150 mV and is able to work at a frequency of 500 Hz [48].

In [50] an energy harvesting system that accommodates both discrete-time and continuous-time energy sources was designed and validated. The system is basically formed by a pulse transformer boost converter. The startup voltage is only 36 mV, and generates an output voltage as high as ±2.5 V. As part of the system, there is a voltage supervisor circuit, which is composed of a voltage reference, a voltage monitor, a voltage comparator made of a 6T Schmitt trigger, and an output stage. The ST is the main component of the supervisor circuit.

The same authors of [50] propose a shunt voltage regulator in [7], as part of a voltage source for energy harvesting systems intended for smart homes and environment monitoring. The system can work with one or more input sources such as photovoltaic cells, piezoelectric harvester, and thermoelectric generator. The minimum input voltage is 86 mV, and the voltage regulator is capable of sourcing ±3 V output. The shunt voltage regulator uses a Schmitt trigger inverter as a

comparator and, due to the ST binary nature, quiescent current is essentially zero, except for the leakage current.

Lastly, in [39], a 62 mV supply voltage is applied to an 8x8-bit multiplier based on Schmitt trigger structures optimized for on-to-off current ratio maximization. The operating frequency is only 5.2 kHz, but the consumption is 17.9 nW. The NAND and NOR gates used in the multiplier were derived from the Schmitt trigger inverter aiming at the exploration of the minimum possible supply voltage for digital circuits with no post-silicon optimizations like charge injection or body biasing. The minimum supply voltage at which the circuit was fully operational was 62 mV. This remarkable result inspired the development of our research and, finally, of this thesis.

1.4 SCHMITT TRIGGER ARCHITECTURES

Many Schmitt trigger architectures have been proposed along the years, in which the main active components were valves, bipolar junction transistors and MOSFETs. Valve circuits were supplied by voltages as high as 200 V, but as technology evolved and applications required lower power consumption, the supply voltages were also reduced to 12 V, 5 V, and 3.3 V. More recently, architectures and topologies intended for ultralow voltage and ultralow power applications were proposed, aiming at supply voltages in the range of 100-200 mV, or even lower. In this sense, old ST topologies or ST circuits that rely on technologies or components not proper for ultralow voltage operation such as vacuum tubes, BJTs, OP-AMPs will not be dealt with in this thesis.

Two examples Schmitt trigger topologies are shown in Fig. 5. The one in Fig. 5 (a) was proposed in [49] whereas the one in Fig. 5 (b) was proposed in [51]. For convenience the ST circuit of Fig. 5 (a) will be explained, and is as follows: transistors P_1 and N_1 work as a standard inverter. However, note the parallel association of P_1 and P_2, and N_1 and N_2, which effectively changes the trip point of the inverter formed by N_1 and P_1. For proper operation of the circuit as a Schmitt trigger, N_2 and P_2 must form a weak inverter if compared to the output inverter [52], formed by N_3 and P_3. Actually, transistors N_2 and P_2 and N_3 and P_3 form a latch circuit, which determines the hysteretic behavior of the circuit. The analysis of the circuit of Fig. 5 (b) is similar to the one of Fig. 5 (a), considering the fact that the effective trip point of the input inverter formed by N_1 and P_1 depends on whether N_2 is on or off.

Both the circuits in Fig. 5 (a) and (b) work as a buffer; so, in order to make these circuits invert the input signal, an additional inverter stage is required at the output, increasing area and power dissipation.

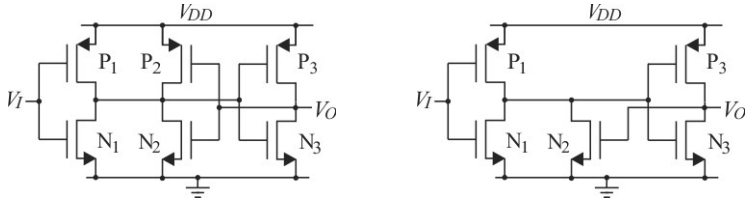


Figure 5 – Schmitt trigger buffer with parallel association of transistors: (a) latch circuit with inverters [49]; (b) NMOS network parallel association [51].

A very simple non-inverting Schmitt trigger, proposed in [53], is shown in Fig 6. The circuit is composed of two inverters with distinct transition voltages, V_{M1} and V_{M2}, and two output transistors, M_1 and M_2. The hysteresis width is given by V_{M2}–V_{M1}, which is effectively determined by the aspect ratios of the transistors that compose the inverters.

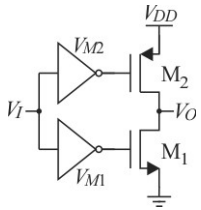


Figure 6 – Schmitt trigger buffer with different trip point inverters [53].

Body biasing can also be employed to change the trip point of the inverters, which form the Schmitt trigger buffers shown in Fig. 7 (a)-(b) [54].

The 4-transistor ST circuit of Fig. 7 (a) dynamically adjusts the bias voltage applied to the body of the input transistors N_0 and P_0, which form an inverter. When the output voltage is low, the bias voltage applied to the body of the transistors N_0 and P_0 increases the trip point of the ST. On the other hand, when the output voltage is high, the trip point of the ST is decreased.

The circuit in Fig. 7 (b) is formed by three inverters, two of which are cross-coupled, forming a latch, similar to the ST from Fig. 5 (a). DTMOS transistors are employed in the first stage (N_0 and P_0) in order to vary the transconductance of the gate and to increase the speed. The second stage has two functions: first, to speed up the transition of the output voltage, and second to control the bias voltage of the third stage, since they are cross-coupled connected. The third stage (N_2 and P_2) is responsible for generating the bias voltage for the other stages. The idea of this circuit is also to vary the trip point of the topology by the application of a variable bias voltage.

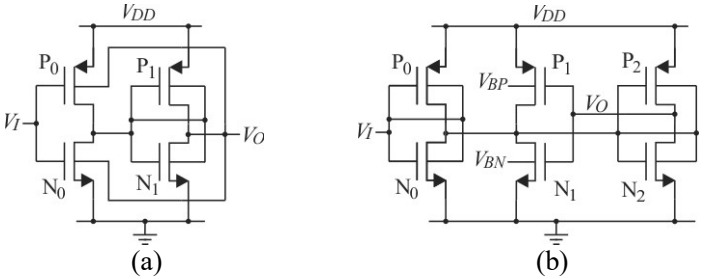


Figure 7 – Schmitt trigger for ULV [54] with; (a) dynamic body-biasing; (b) cross-coupled inverters with body-biasing.

Even though some authors [53], [55] have claimed that the pile-up of four transistors between power and ground rails means that the classical CMOS Schmitt trigger, shown in Fig. 8, is not appropriate for low-voltage applications, it has been employed as the key element in several ultralow voltage (ULV) circuits as shown in Section 1.3. The classical 6T Schmitt trigger is one of the most useful circuits for both analog and digital applications [56]. Analyzing the circuit, transistors N_2 and P_2 provide voltage controlled current feedback to the middle nodes formed by transistors N_0-N_1 and P_0-P_1. In this sense, the 4-transistor stacking (N_0-N_1-P_1-P_0) is of paramount importance for correct operation of the circuit since the nodes between N_0 and N_1, and P_0 and P_1 provide a connection summing point for the feedback current. Moreover, transistor stacking has been used in [15] and [57] to reduce leakage currents effectively, while [5] claims that transistor stacking can reduce leakage current by an order of magnitude.

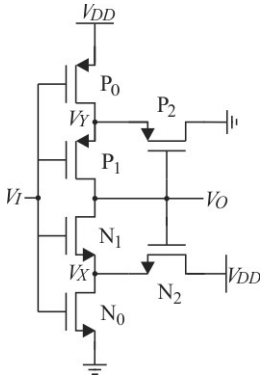


Figure 8 – Classical 6-transistor Schmitt trigger inverter [58].

The classical 6-transistor Schmitt trigger logic circuit, first proposed in [58], has been extensively analyzed in strong inversion in [58]-[63]. It operates roughly as follows: when the input voltage is high, both N_0 and N_1 are on, and the output voltage is low since there is a path between the output and the ground rail [64]. Transistor N_2 is off and transistor P_2 is on. However, no current flows through P_2 since both P_0 and P_1 are off. When the input voltage is low, the transistors work in the opposite way. However, note that for a negative-going transition of the input, initially N_2 is off and P_2 is on, while for a positive-going transition of the input, initially N_2 is on and P_2 is off. Effectively, these two situations represent different strengths of the PMOS and NMOS networks, which results in two different trip points of the ST. This characterizes the hysteretic operation of the ST, when the supply voltage is high enough, as will be discussed later.

The Schmitt trigger inverter is well suited for ultralow voltage and ultralow power applications. In contrast to the bipolar and OP-AMP based ST, which have been analyzed in detail in the literature [58]-[63], little effort has been put into analyzing the ST in weak inversion, with a few in-depth studies [39],[46],[63]. In [39], the ST-based logic gates were designed for the maximization of the on-to-off current ratio, and were able to operate at a supply voltage as low as 62 mV.

One of the benefits of the ST of Fig. 8 is that, although it does not reduce leakage, it shifts the leakage path so that the output voltage is not loaded. Therefore, when the input is at 0 V and the output is high, N_2 pulls V_X to a high potential. Thus, the gate-to-source voltage of N_1 becomes negative biased and its drain to source voltage is close to zero.

For these two reasons, the current flowing in N_1 is greatly reduced and the output voltage deviation is lower [39].

As a matter of comparison, the two ST topologies of Fig. 5 and Fig. 8 are analyzed. Although both circuits have the same number of transistors, the 4-transistors pile-up of the ST of Fig. 8, which is responsible for the feedback mechanism, provides higher voltage gain, higher noise immunity, and considerable lower dependence on process, voltage and temperature variations [65], [66]. Moreover, the ST of Fig. 5 is based on the conventional inverter, so theoretical minimum operating voltage is 36 mV. As will be detailed latter, the theoretical minimum supply voltage of the ST of Fig. 8 is 31.5 mV. Finally, the feedback mechanism present in the classical ST helps reducing the output voltage loading due to the fact that leakage current flows through transistors N_0 and N_2, and P_0 and P_2.

Also, note that body biasing can also be applied to the Schmitt trigger inverter and logic gates, with all benefits that the technique provides.

Other topologies of ST with discrete components, BiCMOS technology, transmission gates, variable hysteresis width control, time varying hysteresis width control, and other technologies can be found in [51], [54]-[56], and [67]-[70]. However, the main and most common topologies for ULV were presented and described here.

2 SCHMITT TRIGGER CONVENTIONAL OPERATION

2.1 WEAK INVERSION OPERATION

The behavior of the Schmitt trigger in strong inversion is well known. However, in weak inversion only partial formulations have been developed in [39]. Here, the complete analytical expressions for the Schmitt trigger operating in weak inversion are derived.

The MOSFET drain current in weak inversion is given [37], [71] by

$$I_{DN(P)} = I_{N(P)} \cdot e^{\frac{V_{GB(BG)}}{n_{N(P)} \cdot \phi_t}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi_t}} - e^{-\frac{V_{DB(BD)}}{\phi_t}} \right) \tag{1}$$

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C'_{ox} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{T0N(P)}|}{n_{N(P)} \cdot \phi_t}+1} \tag{2}$$

where $I_{N(P)}$ is the NMOS(PMOS) transistor strength, or current scaling factor, which is dependent on the aspect ratio W/L and the technological parameters $\mu_{N(P)}$ (mobility), C'_{ox} (oxide capacitance per unit area), and $V_{T0N(P)}$ (threshold voltage). $\phi_t = kT/q$ is the thermal voltage (25.9 mV at 300 K) and $n_{N(P)}$ is the slope factor, usually between 1 and 2. G, S, D, and B are the gate, source, drain, and bulk nodes, respectively. For n-channel transistors, the nodal voltages referred to the bulk are positive while, for p-channel transistors, they are negative.

The classical 6-transistor Schmitt trigger loaded by capacitor C_O is shown in Fig. 9.

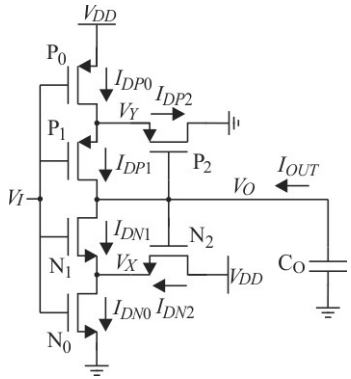


Figure 9 – Currents and voltages in the classical 6-transistor Schmitt trigger.

The DC equation for node V_X is:

$$I_{DN0} = I_{DN1} + I_{DN2}. \tag{3}$$

Calculating the currents I_{DN0}, I_{DN1}, and I_{DN2} from (1) results in

$$I_{N0} \cdot e^{\frac{V_I}{n_N \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_X}{\phi_t}}\right) = I_{N1} \cdot e^{\frac{V_I}{n_N \cdot \phi_t}} \cdot \left(e^{-\frac{V_X}{\phi_t}} - e^{-\frac{V_O}{\phi_t}}\right) + \\ + I_{N2} \cdot e^{\frac{V_O}{n_N \cdot \phi_t}} \cdot \left(e^{-\frac{V_X}{\phi_t}} - e^{-\frac{V_{DD}}{\phi_t}}\right). \tag{4}$$

Rearranging (4) for V_X, results in

$$e^{\frac{V_X}{\phi_t}} = \frac{I_{N0} + I_{N1} + I_{N2} \cdot e^{\frac{V_O - V_I}{n_N \cdot \phi_t}}}{I_{N0} + I_{N1} \cdot e^{-\frac{V_O}{\phi_t}} + I_{N2} \cdot e^{\frac{V_O - V_I}{n_N \cdot \phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{5}$$

Similarly, the KCL for node V_Y results in

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_{P0} \cdot e^{\frac{V_{DD}}{\phi_t}} + I_{P1} \cdot e^{\frac{V_O}{\phi_t}} + I_{P2} \cdot e^{\frac{V_I - V_O}{n_P \cdot \phi_t}}}{I_{P0} + I_{P1} + I_{P2} \cdot e^{\frac{V_I - V_O}{n_P \cdot \phi_t}}} \tag{6}$$

At the same time, the KCL for the unloaded node V_O, (I_{OUT} = 0), is

$$I_{DN1} = I_{DP1}. \tag{7}$$

Substituting the values of I_{DN1} and I_{DP1} from (1) into (7), results in

$$e^{\frac{V_I - n_N \cdot V_X}{n_N \cdot \phi_t}} - e^{\frac{V_I - n_N \cdot V_O}{n_N \cdot \phi_t}} = \frac{I_{P1}}{I_{N1}} \cdot e^{\frac{V_{DD} \cdot (1 - n_P)}{n_P \cdot \phi_t}} \cdot \left(e^{\frac{-V_I + n_P \cdot V_Y}{n_P \cdot \phi_t}} - e^{\frac{-V_I + n_P \cdot V_O}{n_P \cdot \phi_t}}\right) \tag{8}$$

The complete calculation of V_X, V_Y and V_O as functions of V_I is given in Appendix A.

The system formed by equations (5), (6), and (8) can be solved numerically for the output voltage, V_O, as a function of the input voltage, V_I, in order to determine the voltage transfer characteristic (VTC) of the ST. For a given input voltage, V_I, in the range of 0 V to V_{DD}, V_X and V_Y are calculated from equations (5) and (6), respectively, for the initial condition $V_O = V_{DD}$. The output voltage V_O is then calculated from equation (8). The process of calculating of V_X, V_Y, and V_O is repeated for a sufficient number of iterations, resulting in the input-output pair (V_I, V_O). The process is repeated for the initial condition $V_O = 0$ V.

Equations (5)-(8) can be used to evaluate the dependence of the VTC on process, voltage, and temperature (PVT) variations and p- and n- networks imbalance or mismatch. Figure 10 plots the output and internal nodes voltages, obtained from equations (5), (6), and (8), solved numerically for V_{DD} = 60 mV and 150 mV, respectively. Since the p- and n- networks are imbalanced, the output voltages are not centered at $V_{DD}/2$, as expected. For the case of V_{DD} = 60 mV the VTC is centered at 24.75 mV, and at 67.53 mV for the case of V_{DD} = 150 mV. The hysteresis width is called V_L. Note that for the latter case, both the output and the internal nodes voltages present hysteresis (V_L = 4.92 mV), whereas for the former case they do not present hysteresis. It will be shown latter in Section 2.1.5 that hysteresis does not appear for supply voltages lower than 75 mV in ideal cases (symmetrical networks and n = 1) and lower than around 100 mV for real cases (asymmetrical networks and $n > 1$).

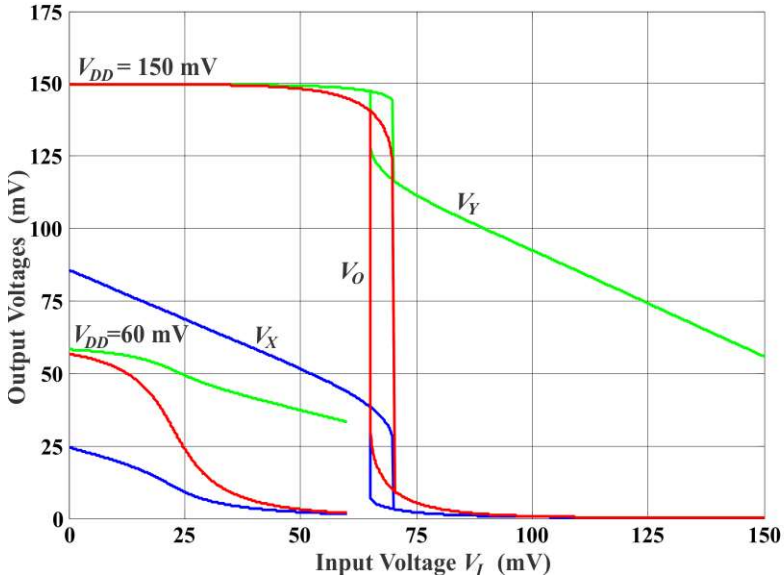


Figure 10 – VTC of the ST, from equations (5), (6), and (8), with imbalanced p- and n- circuits for V_{DD} = 60 mV and 150 mV, with I_{N0} = 3 nA, I_{N1} = 1 nA, I_{N2} = 1 nA, I_{P0} = 1.5 nA, I_{P1} = 0.5 nA, I_{N2} = 0.5 nA, n_N = 1.3, and n_P = 1.2.

However, in this study, for the sake of simplicity unless otherwise stated, we consider in the following that the NMOS and PMOS networks have the same strength and that the slope factors of both NMOS and PMOS transistors are equal to unity ($n_N = n_P = 1$). We write $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, and $I_{N2} = I_{P2} = I_2$. Note that I_0, I_1, and I_2 are the main design parameters of the symmetrical CMOS Schmitt trigger. Thus, equations (5), (6), and (8) can be simplified to (9)-(11), respectively.

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 \cdot e^{-\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}} \tag{9}$$

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}} \tag{10}$$

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}} \quad (11)$$

Figure 11 shows the VTC of the symmetrical ST from equations (9)-(11), with $I_0 = I_1 = I_2 = 1$nA, for supply voltages of 60 mV and 150 mV. Note that, in these cases, the VTCs are perfectly centered at 30 mV and 75 mV, respectively, as expected. For V_{DD} = 150 mV the VTC presents hysteresis (V_L = 15.3 mV), but for V_{DD} = 60 mV it does not.

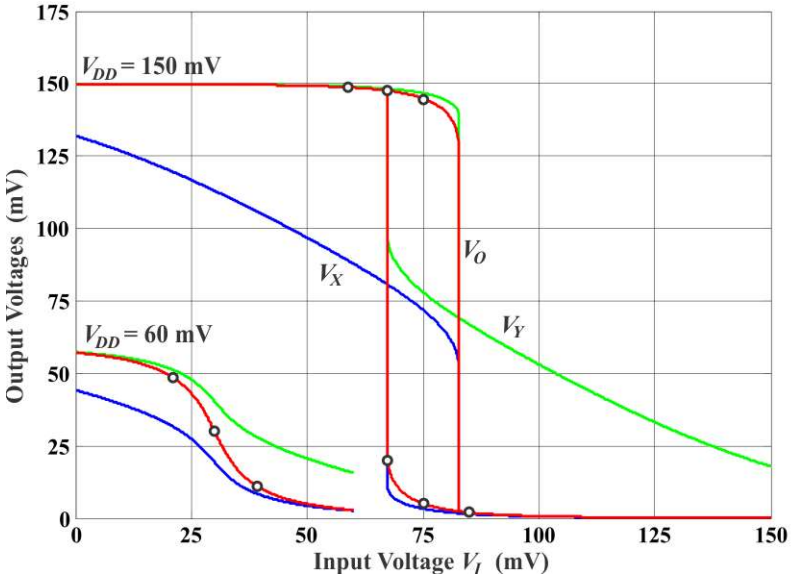


Figure 11 – VTC of the ST, obtained from equations (9)-(11), with balanced p- and n- circuits for V_{DD} = 60 mV and 150 mV.

Another fact that must be noticed is that as the supply voltage is reduced, the output high, V_{OH}, and low, V_{OL}, level voltages do not completely reach the supply rails. The output voltages can be even more degraded for the case of the non-symmetrical ST. Table I shows the output voltages for V_{DD} = 60 mV, for the STs shown in figures 10 and 11. The output low level voltage, V_{OL}, is 4.72% of the supply voltage (60 mV) for the case of the symmetrical ST of the example given, and 3.00% for the case of the non-symmetrical ST. However, the output high level voltage, V_{OH}, is 95.27% of the supply voltage for the symmetrical

case, and 94.52% for the non-symmetrical ST. These differences are low, but under PVT variations, they may cause considerable output voltage deviations and may compromise the circuit operation.

TABLE I – Output high and low level voltages of the non-symmetrical (see Fig. 10) and symmetrical (see Fig. 11) STs for V_{DD} = 60 mV.

	High Output Voltage V_{OH} (mV)	Low Output Voltage V_{OL} (mV)
Non-symmetrical ST	56.71	1.80
Symmetrical ST	57.16	2.83

Equations (9)-(11) form a system, in which V_I and V_O are the input and output variables, respectively. V_X and V_Y are auxiliary variables. The substitution of equations (9) and (10) into (11) results in a single equation of the 4th degree in terms of e^{V_O/ϕ_t} and e^{V_I/ϕ_t}, which can be used to calculate the VTC of the ST. The analysis of the 4th degree equation is given in Appendix B.

2.1.1 Output Voltage Swing

In the case of a large number of cascaded STs or a latch composed of two symmetrical STs connected back-to-back, shown in Fig. 12 (a) and (b), respectively, the output voltage swing $2\mathcal{E}$, with $n_N = n_P = n$, can be calculated similarly to the case of the inverter in [72].

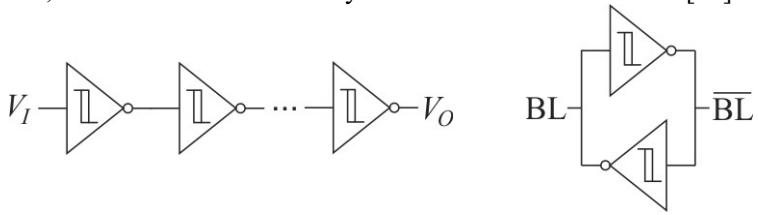


Figure 12 – (a) Odd number of cascaded STs; (b) ST Latch.

Considering the case of a latch composed of two symmetrical STs ($I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$), with $n_N = n_P = n$, when the input voltage, V_I, is high, V_{High}, the output voltage, V_O, is low, V_{Low}. Alternatively, when V_I=V_{Low}, then V_O=V_{High}. The input-output characteristic of the latch is given by the butterfly plot of the ST, as shown in Fig. 13. As can be seen in the figure, the output stable points

of the latch can be calculated from the interception of the VTC and VTC^{-1} of the Schmitt trigger.

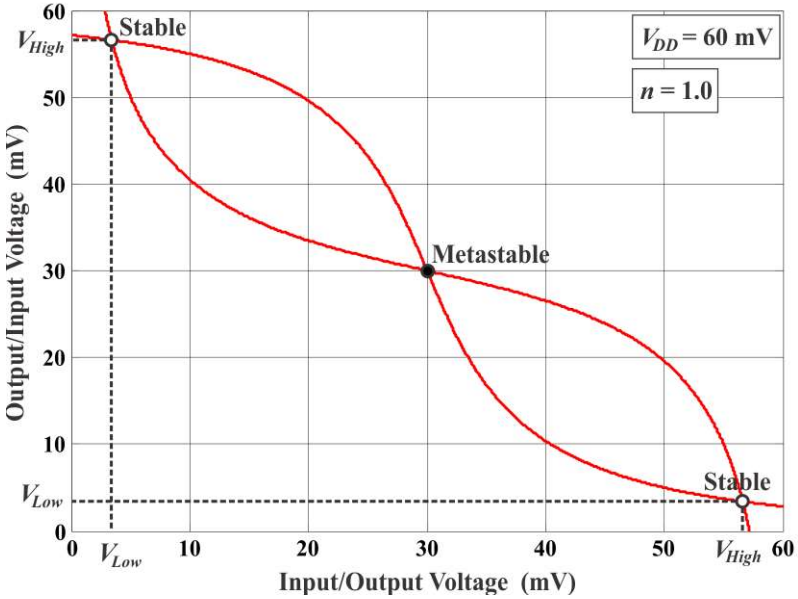


Figure 13 – Butterfly plot of the Schmitt trigger for V_{DD} = 60 mV, $I_0 = I_1 = I_2$, and n=1, used to define V_{Low} and V_{High} output stable points of the ST-based latch.

In this case, V_I and V_O can be written as

$$V_I = V_{Low} = \frac{V_{DD}}{2} - \varepsilon \;\rightarrow\; V_O = V_{High} = \frac{V_{DD}}{2} + \varepsilon\,, \tag{12}$$

$$V_I = V_{High} = \frac{V_{DD}}{2} + \varepsilon \;\rightarrow\; V_O = V_{Low} = \frac{V_{DD}}{2} - \varepsilon\,. \tag{13}$$

The complete calculation of the output voltage swing 2ε is given in Appendix C. The output voltages of a ST, from eq. (C7), with different values of I_0, I_1, I_2, as a function of the supply voltage are shown in Fig. 14 and Fig. 15, for n = 1.0 and n = 1.3, respectively. As the supply voltage is reduced, so is the value of ε (V_{High} and V_{Low} gets closer). The minimum operating supply voltage limit can be determined from (C7), as long as the next stage can distinguish the high and the low output voltage levels. The higher the value of the slope factor, n, the higher the minimum supply voltage required.

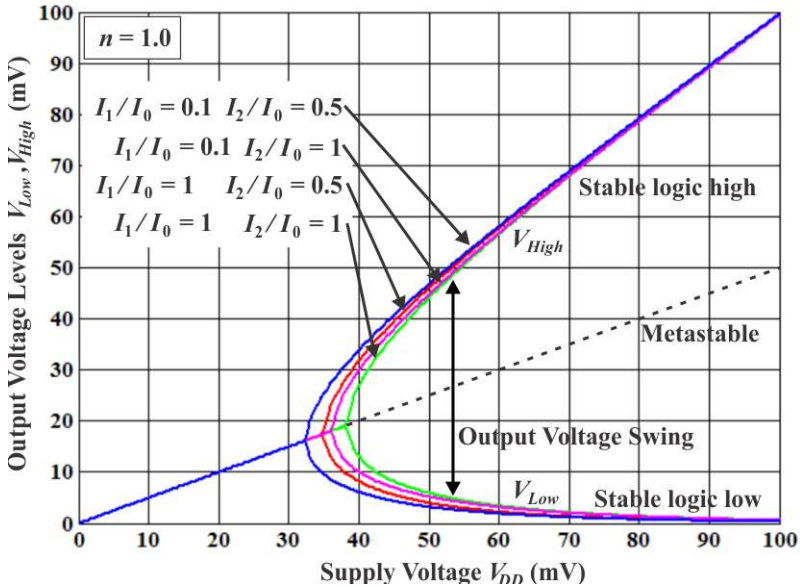


Figure 14 – Output voltage swing of the ST, with $I_1 / I_0 = 0.1$ and $I_1 / I_0 = 1$, $I_2 / I_0 = 0.5$ and $I_2 / I_0 = 1$, for $n = 1.0$, as a function of the supply voltage.

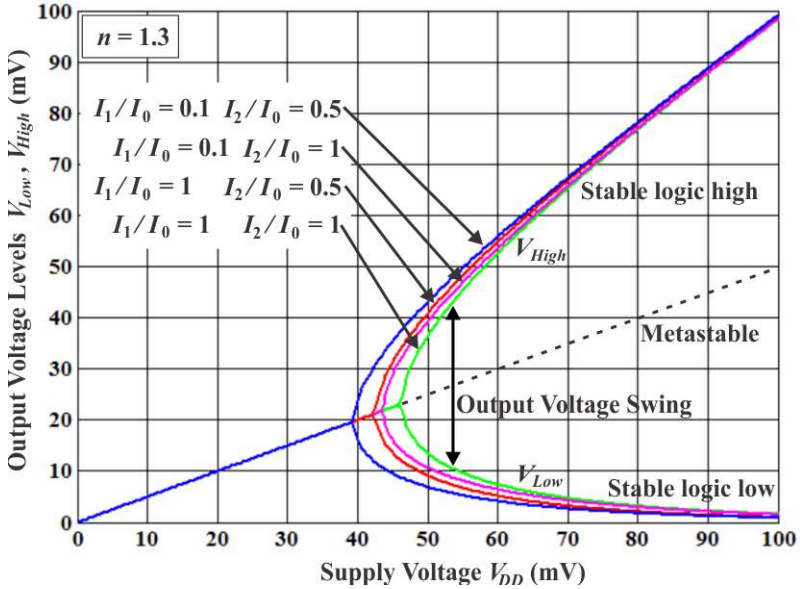


Figure 15 – Output voltage swing of the ST, with $I_1 / I_0 = 0.1$ and $I_1 / I_0 = 1$, $I_2 / I_0 = 0.5$ and $I_2 / I_0 = 1$, for $n = 1.3$, as a function of the supply voltage.

2.1.2 The Effect of the Feedback Strength on the Voltage Transfer Characteristic

Figure 16 shows the VTC of the Schmitt trigger for V_{DD} = 150 mV, and I_1/I_0 = 1, obtained from equations (9)-(11). The feedback strength I_2/I_0 was set equal 1, 10, 15, 20, 30, and 50. For $I_2/I_0 < 15$ hysteresis is present and the ST behaves as an inverter circuit. However, when the feedback is too high, *i.e.* $I_2/I_0 > 15$, hysteresis disappears. The ST is no more an inverter circuit for extremely high feedback, *e.g.* $I_2/I_0 = 50$. The same behavior is shown in Fig. 17 for a supply voltage of 60 mV (no hysteresis is present), and I_2/I_0 varying from 1 to 30.

The undesired behavior of the ST when the feedback strength is too high is verified by simulation, as shown in Fig. 18 and Fig. 19, for V_{DD} = 150 mV, and V_{DD} = 60 mV, respectively. IBM 180 nm technology was used for the simulations. The feedback strength was varied by changing the number of parallel transistor in the feedback branch. In both figures, the curves are not perfectly centered at $V_{DD}/2$ due to the fact that the p- and n- networks are not perfectly matched.

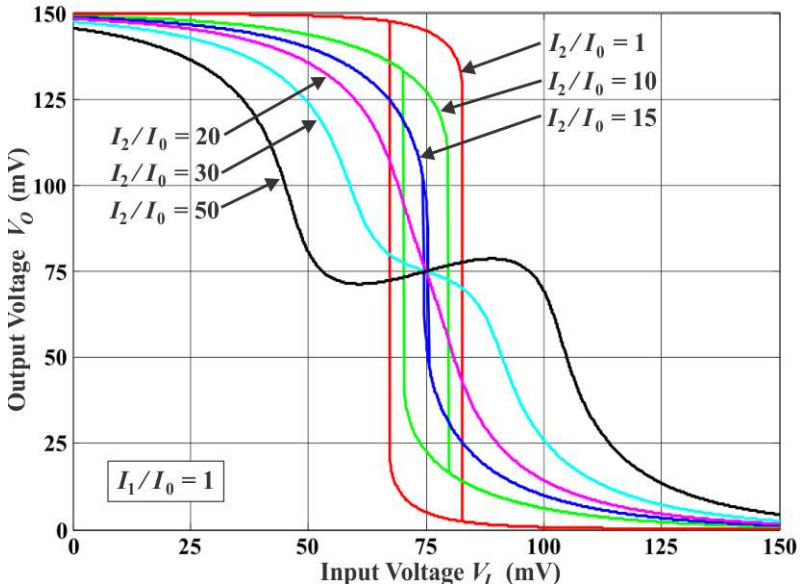


Figure 16 – VTC of the ST, obtained from equations (9)-(11), with I_1/I_0=1 and I_2/I_0 from 1 to 50, for V_{DD} = 150 mV.

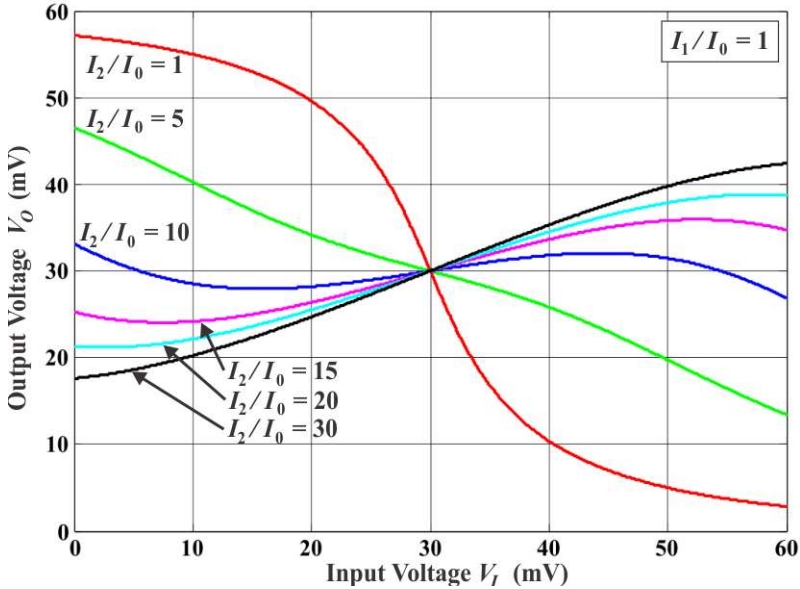


Figure 17 – VTC of the ST, obtained from equations (9)-(11), with I_1/I_0=1 and I_2/I_0 from 1 to 30, for V_{DD} = 60 mV.

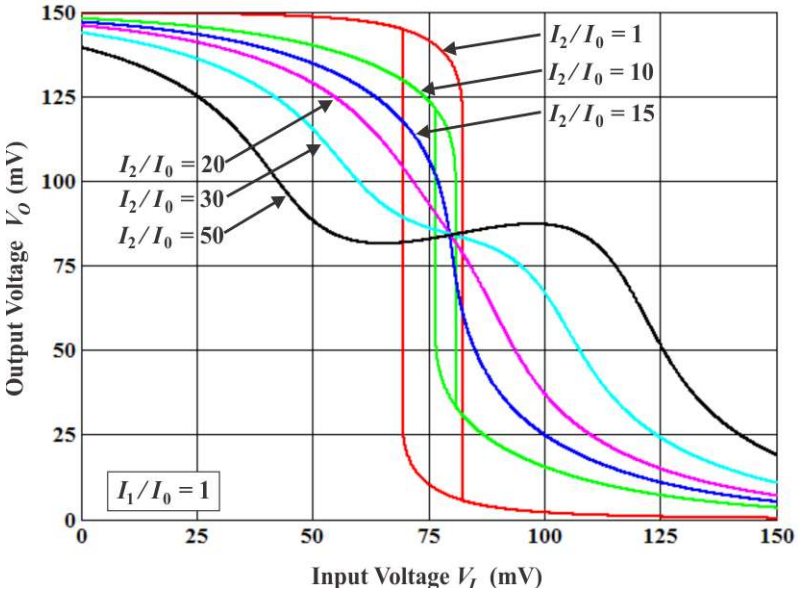


Figure 18 – VTC of the ST, obtained from simulation in 180 nm technology, with I_1/I_0=1 and I_2/I_0 from 1 to 50, for V_{DD} = 150 mV.

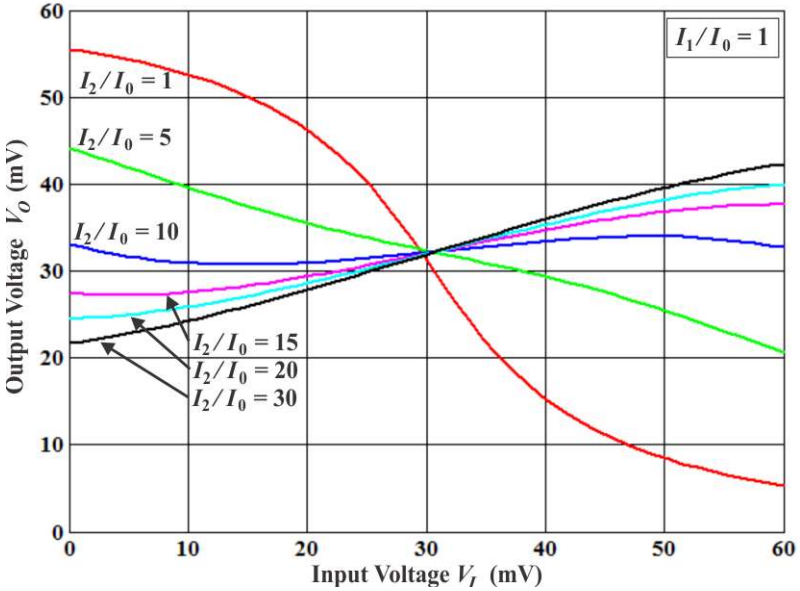


Figure 19 – VTC of the ST, obtained from simulation in 180 nm technology, with I_1/I_0=1 and I_2/I_0 from 1 to 30, for V_{DD} = 60 mV.

2.1.3 The Origin of Hysteresis

In order to understand the origin of hysteresis we follow reference [62] and split the Schmitt trigger into two parts, the PMOS network (PN) and the NMOS network (NN), as show in Fig. 20 (a) and (b), respectively.

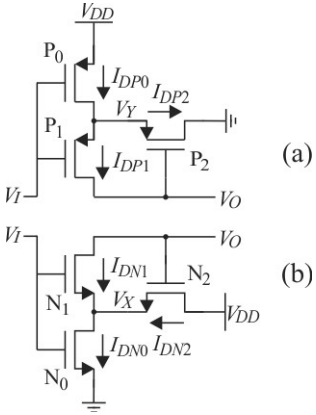


Figure 20 – ST split into PMOS and NMOS networks.

The currents through P_1 and N_1 as functions of both the input and the output voltages are obtained from equations (1)-(2), along with (5) and (6). Figure 21 shows the currents for V_{DD} = 60 mV and $I_0 = I_1 = I_2$ = 1 nA. Note that, for a fixed input voltage, the curves of the currents through P_1 and N_1 intersect at a single point, indicated by the open circles for V_I = 20 mV, 30 mV, and 40 mV. In this example, any value of the input, from 0 to V_{DD}, is mapped into a single value of the output; therefore, hysteresis does not appear. It will be shown latter that, for the parameters chosen in this example, the minimum supply voltage at which hysteresis starts to appear is around 84 mV.

It can also be seen in Fig. 21 that, for a fixed input voltage, above a certain output voltage for the NN and below another output voltage for the PN, the output resistance becomes negative. However, this phenomenon is not pronounced due to the low value of the supply voltage and has no further consequences.

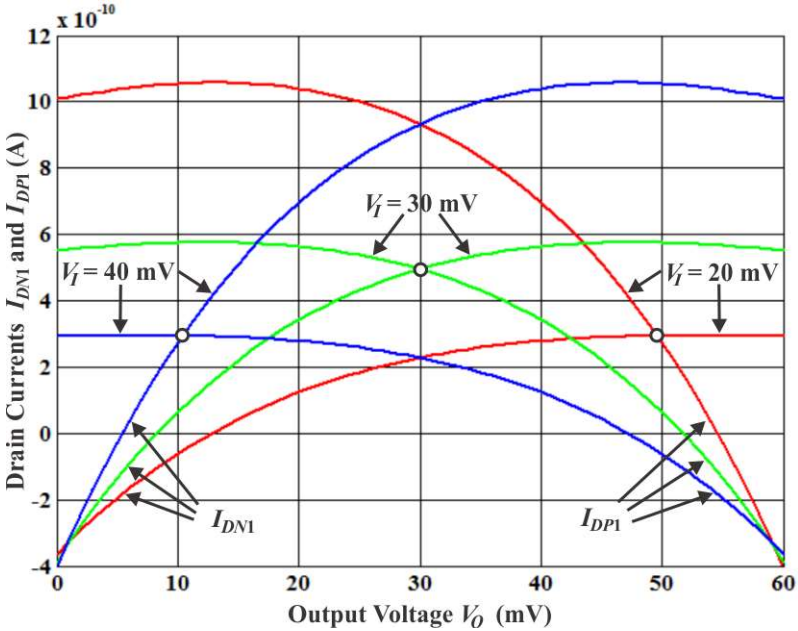


Figure 21 – Drain currents of N_1 and P_1 in terms of the output voltage, V_O, for different input voltages, V_I, with $I_0 = I_1 = I_2 = 1$ nA and $V_{DD} = 60$ mV.

Fig. 22 shows the drain current of the n- and p-subcircuits for $V_{DD} = 150$ mV. It can be noted that, for a fixed input voltage, the drain current that flows through N_1 initially increases with an increase in the output voltage up to a maximum value. Above this value the current decreases, thus presenting a negative resistance characteristic, which is much more pronounced than in the case where $V_{DD} = 60$ mV. In effect, the feedback transistor N_2 pulls up the node voltage V_X as the output voltage increases. The increase in V_X causes the current through N_1 to decrease, whereas the increase in V_O tends to increase the current. The effect of the voltage increase in V_X can overwhelm that due to the V_O increase; thus, the output resistance can become negative. The same conclusion applies to the current flowing through P_1. Hysteresis arises as a consequence of the negative resistance of subcircuits PN and NN. In effect, for a fixed input voltage, the output characteristic of NN and PN intersect at either one or three points. In the latter case, the innermost point is metastable, *i.e.*, any disturbance will move it either to the rightmost or leftmost stable points.

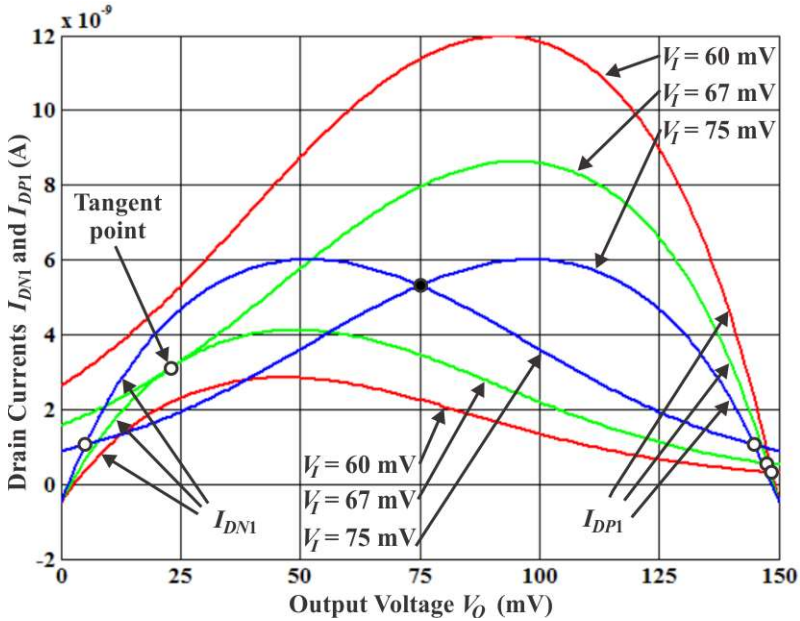


Figure 22 – Drain currents of N_1 and P_1 in terms of the output voltage, V_O, for different input voltages, V_I, with $I_0 = I_1 = I_2 = 1$ nA and $V_{DD} = 150$ mV.

Let us now explain graphically the origin of hysteresis. Initially, consider a negative-going input voltage. When the input voltage is high, *e.g.*, $V_I = 85$ mV, there is only one stable point, for which V_O is close to ground (see Fig. 11). When the input voltage is lower and lies between the hysteresis limits, *e.g.*, $V_I = 75$ mV, two stable outputs (close to ground and close to V_{DD}) and one metastable output point (at $V_O = 75$ mV) exist, as shown in Fig. 22. However, note that there is no physical stimulus to move the output to the high voltage stable point, and the output remains at the stable point close to ground. As the input voltage continues to decrease, the stable output and the metastable output points approximate and eventually become coincident at the hysteresis limit (see the two tangent curves in Fig. 22 for $V_I = 67$ mV). When the input voltage is below the hysteresis limit, e.g., $V_I = 60$ mV, only one operating point exists, which is close to V_{DD}. The transition of the output from the stable point close to ground to that close to V_{DD} is abrupt and is a dynamic phenomenon [25],[26], since the output capacitor, C_O, must be charged or discharged, as shown in Appendix G. The same conclusions can be drawn for a positive-going input voltage.

Fig. 23 shows the output current, $I_{OUT} = I_{DN1} - I_{DP1}$, which charges and discharges the output capacitor, C_O, as a function of the output voltage, V_O. In this example, V_{DD} = 60 mV and the input voltage takes the values 20 mV, 30 mV, and 40 mV. It can be observed that the output current varies monotonically with the output voltage. For each input voltage there is only one stable output voltage (at I_{OUT} = 0 A).

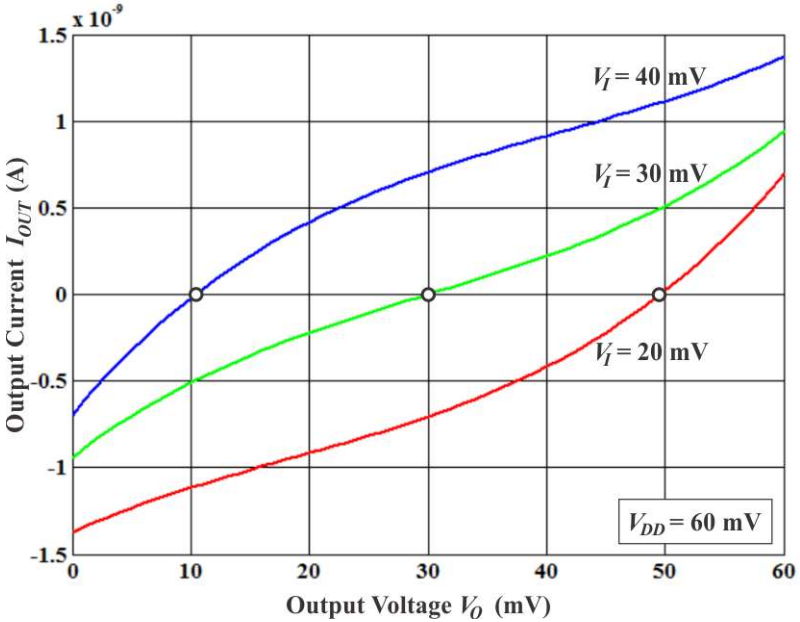


Figure 23 – Output current, I_{OUT}, as a function of the output voltage, V_O, for V_I = 20 mV, 30 mV, and 40 mV, with $I_0 = I_1 = I_2$ = 1 nA, n = 1, and V_{DD} = 60 mV.

If the supply voltage is raised to 150 mV, as shown in Fig. 24, the output driving point characteristic presents a negative resistance region. In this figure, when the input voltage is 60 mV only one stable point exists, which is close to V_{DD}. As the input voltage is raised to 67 mV the curve for the output current is shifted upwards and reaches zero at two points. The leftmost point indicates the appearance of both a second stable point and a metastable point. At an input voltage of 75 mV, three different zeroes exist, one of which is metastable.

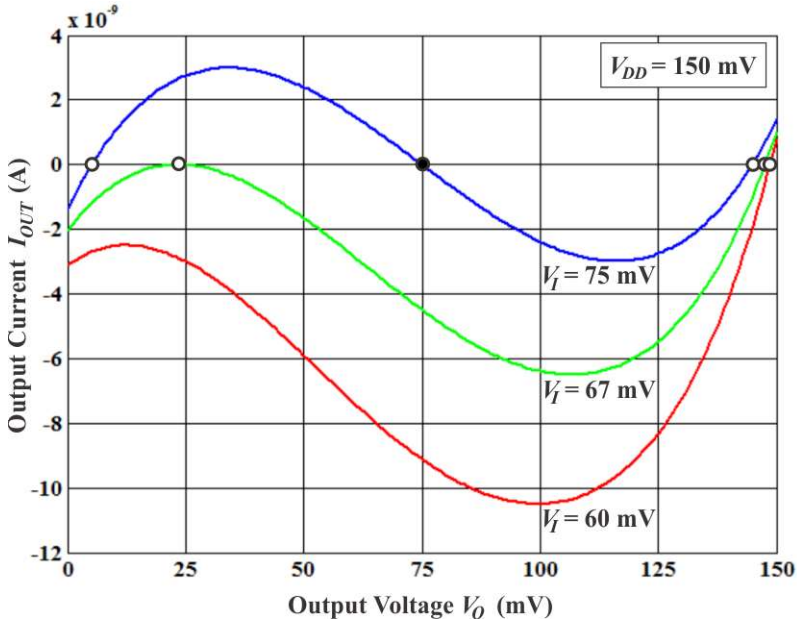


Figure 24 – Output current, I_{OUT}, as a function of the output voltage, V_O, for V_I = 60 mV, 67 mV, and 75 mV, with $I_0 = I_1 = I_2 = 1$ nA, $n = 1$, and $V_{DD} = 150$ mV.

The metastable points of the output characteristic constitute the inner arc of the "Z"-shaped transfer curve shown in Fig. 25. Thus, as for the bipolar and OP-AMP-based ST circuits, the DC voltage transfer characteristic of the classical CMOS ST is an unstable arc within the hysteresis region. The VTC of the Schmitt trigger is actually a single continuous curve [25],[26].

Since the ST circuit under analysis is symmetrical, it is interesting to note that, for any supply voltage, $V_I = V_O = V_{DD}/2$ is either a stable (for non-hysteretic curve) or a metastable (for hysteretic curve) operating point.

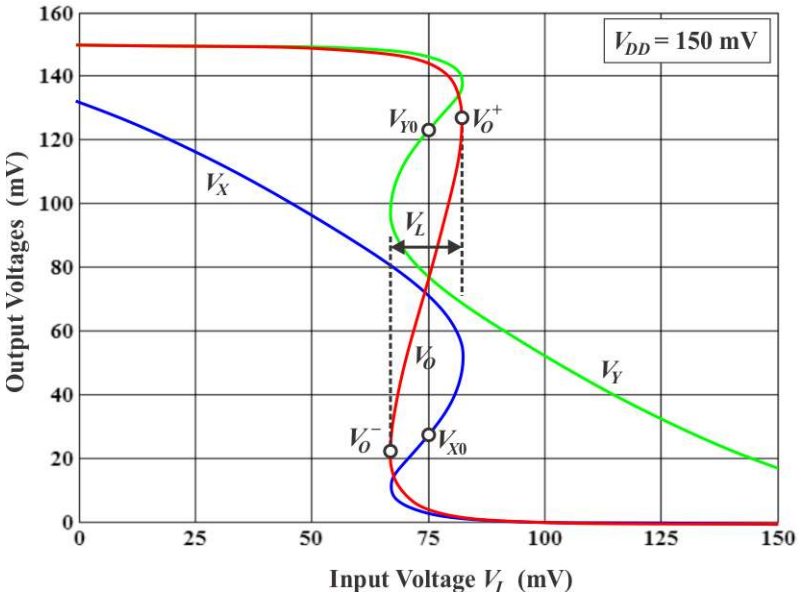


Figure 25 – "Z" curve formed by both stable and metastable points for V_{DD} = 150 mV, n = 1, and $I_1/I_0 = I_2/I_0 = 1$.

2.1.4 Schmitt trigger small-signal voltage gain

The AC gain of the Schmitt trigger is derived by substituting each MOSET with its equivalent small-signal model of three voltage-controlled current sources [71], as show in Fig. 26, where g_m, g_{md}, and g_{ms} are the gate, drain, and source transconductances, respectively.

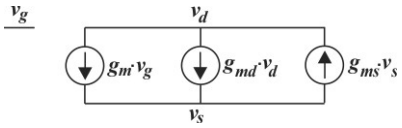


Figure 26 – Small-signal MOSFET model (v_b = 0).

The low-frequency small-signal circuit of a ST with matched n- and p-subcircuits, for $V_I = V_O = V_{DD}/2$, the voltage at which the gain is maximum, is shown in Fig. 27. Here, v_I, v_O, v_X, and v_Y are the small-signal voltages.

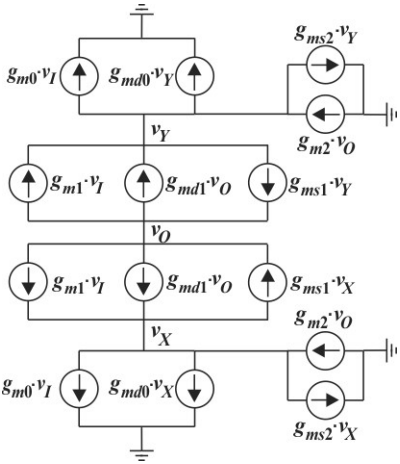


Figure 27 – ST small-signal model.

Applying KCL to v_X, v_Y, and v_O and solving for v_O/v_I, results in $v_X = v_Y$, as expected, and

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{g_{m1}}{g_{md1}}\cdot\frac{1+\dfrac{g_{ms1}\cdot g_{m0}}{g_{m1}\cdot\left(g_{ms2}+g_{md0}\right)}}{1-\dfrac{g_{ms1}\cdot g_{m2}}{g_{md1}\cdot\left(g_{ms2}+g_{md0}\right)}} \tag{14}$$

The small-signal voltage gain given by equation (14) is the actual negative gain of the ST when no hysteresis is present and the positive gain of the metastable curve when the VTC presents hysteresis. We will use the positive gain for estimation of the hysteresis width in Section 2.2.

The transconductances [71] of the Schmitt trigger, calculated in Appendix D, are reproduced in Table II, for $V_I = V_O = V_{DD}/2$.

TABLE II – Transconductances of the Schmitt trigger for $V_O = V_I = V_{DD}/2$.

	g_{ms}	g_{md}	g_m
N_0 or P_0	$\frac{I_0}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\varphi_t}}$	$\frac{I_0}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_0}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(1-e^{-\frac{V_{X0}}{\phi_t}}\right)$
N_1 or P_1	$\frac{I_1}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_1}{\phi_t}\cdot e^{\frac{V_{DD}}{2\phi_t}\left(\frac{1}{n}-1\right)}$	$\frac{I_1}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)$
N_2 or P_2	$\frac{I_2}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$		$\frac{I_2}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}\right)$

Let $V_{X0} = V_X$ ($V_I = V_O = V_{DD}/2$). Thus, equation (9) gives

$$e^{\frac{V_{X0}}{\phi_t}} = \frac{I_0 + I_1 + I_2}{I_0 + I_1\cdot e^{-\frac{V_{DD}}{2\phi_t}} + I_2\cdot e^{-\frac{V_{DD}}{\phi_t}}} \tag{15}$$

By substituting the values of the transconductances from Table II into (14), we obtain, after some lengthy algebra

$$\left.\frac{v_O}{v_I}\right|_{V_I=V_O=\frac{V_{DD}}{2}} = \frac{\left(e^{\frac{V_{DD}}{2\phi_t}}-1\right)\cdot\left(1+\frac{I_1}{I_0}+2\frac{I_2}{I_0}\right)+\left(\frac{I_2}{I_0}\right)^2\cdot\left(e^{-\frac{V_{DD}}{2\phi_t}}-1\right)}{\frac{I_2}{I_0}\cdot\left(e^{\frac{V_{DD}}{2\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)+\frac{I_1}{I_0}\cdot\frac{I_2}{I_0}\cdot\left(1-e^{-\frac{V_{DD}}{2\phi_t}}\right)-n\cdot\left(1+\frac{I_2}{I_0}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)} \tag{16}$$

For the sake of simplicity, when $n = 1$, equation (16) is re-written as

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{\left(2+\frac{I_0}{I_2}+\frac{I_1}{I_2}-\frac{I_2}{I_0}\cdot e^{-\frac{V_{DD}}{2\phi_t}}\right)\cdot\left(1-e^{-\frac{V_{DD}}{2\phi_t}}\right)}{1-\left(2+\frac{I_0}{I_2}+\frac{I_1}{I_2}+\frac{I_2}{I_0}\right)\cdot e^{-\frac{V_{DD}}{2\phi_t}}-\left(1+\frac{I_1}{I_0}\right)\cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{17}$$

2.1.5 Minimum supply voltage V_{DDH} required for the appearance of hysteresis

A zero in the denominator of equation (16) results in an infinite gain, which is associated with the transition between the amplifier and hysteretic operation modes. The minimum supply voltage for hysteresis, V_{DDH}, is given from the denominator of (16), and results in

$$e^{\frac{V_{DDH}}{2\phi_t}} = \frac{n\cdot\left(1+\frac{I_2}{I_0}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)-\frac{I_1}{I_0}\cdot\frac{I_2}{I_0}}{2\frac{I_2}{I_0}}+ \\ +\sqrt{\left[\frac{n\cdot\left(1+\frac{I_2}{I_0}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)-\frac{I_1}{I_0}\cdot\frac{I_2}{I_0}}{2\frac{I_2}{I_0}}\right]^2+\left(1+\frac{I_1}{I_0}\right)}. \tag{18}$$

Neglecting $e^{-V_{DD}/2\phi_t}$ compared to $e^{V_{DD}/2\phi_t}$ from the denominator of eq. (16), V_{DDH} can be approximated as

$$V_{DDH} \approx 2\phi_t\cdot\ln\left[n\cdot\left(1+\frac{I_0}{I_2}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)-\frac{I_1}{I_0}\right] \tag{19}$$

Equation (19) can be further simplified, for $n = 1$, as

$$V_{DDH} \approx 2\phi_t \cdot \ln\left[2 + \frac{I_2}{I_0} + \frac{I_0}{I_2} + \frac{I_1}{I_2}\right] \tag{20}$$

Using (18) to obtain the exact value of the lower bound of V_{DDH}, which is reached for $I_2/I_0 = 1$ and $I_1/I_0 = 0$, results in

$$V_{DDH\min} = 2\phi_t \cdot \ln\left(2 \cdot n + \sqrt{4 \cdot n^2 + 1}\right) \tag{21}$$

Assuming ideal MOSFETs ($n = 1$), at 300K equation (21) results

$$V_{DDH\min} = 2\phi_t \cdot \ln\left(2 + \sqrt{5}\right) = 75\,\text{mV} \tag{22}$$

It is interesting to note that the value of V_{DDHmin} is approximately twice the well-known lower bound of the supply voltage (36 mV) of the CMOS inverter [73] at which the voltage gain is equal to unity.

Figure 28 shows the value of the supply voltage for the appearance of hysteresis, V_{DDH}, from (18) as a function of the feedback strength I_2/I_0 for different values of the series strength, I_1/I_0, and $n = 1$. Figure 29 shows the increase of V_{DDH} from $n = 1.35$, as compared to the case where $n = 1$.

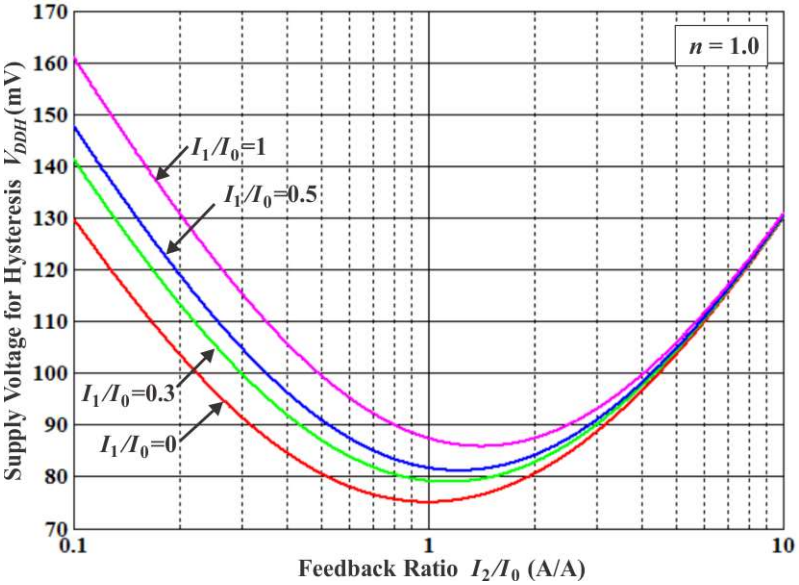


Figure 28 – Minimum supply voltage for the appearance of hysteresis, from equation (18), with $n = 1$.

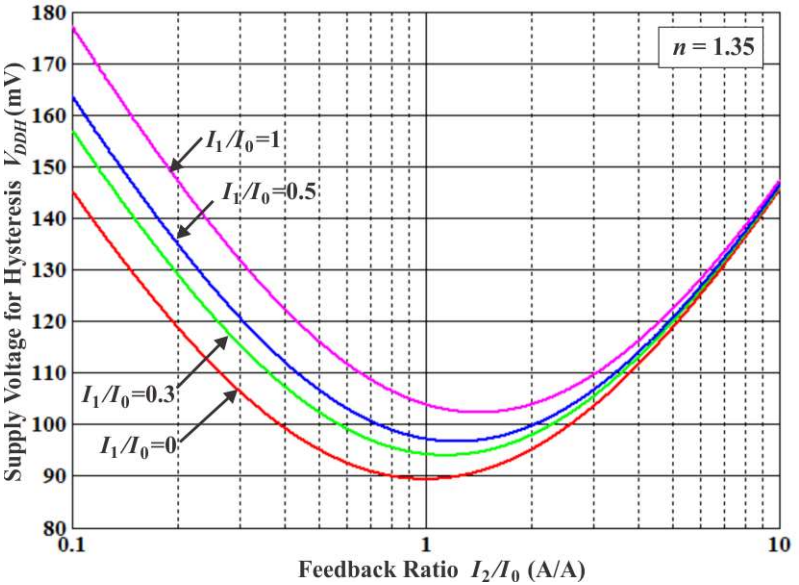


Figure 29 – Minimum supply voltage for the appearance of hysteresis, from equation (18), with $n = 1.35$.

2.2 CALCULATION OF THE HYSTERESIS WIDTH

Assuming that N_1, P_1, N_2, and P_2 are in saturation, it follows that

$$\left.\begin{aligned} g_{md1} &= g_{md2} = 0 \\ g_{m1} &= \frac{g_{ms1}}{n} \\ g_{m2} &= \frac{g_{ms2}}{n} \\ g_{m0} &= \frac{g_{ms0} - g_{md0}}{n} \end{aligned}\right\} \tag{23}$$

and (14) reduces to the remarkable simple result

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = 1 + \frac{g_{ms0}}{g_{ms2}}. \tag{24}$$

By substituting g_{mso} and g_{ms2} by its values from Table II we obtain

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = 1 + \frac{I_0}{I_2} e^{\frac{V_{X0}}{\phi_t}}. \tag{25}$$

V_{X0}, defined in (15), can be approximated as

$$e^{\frac{V_{X0}}{\phi_t}} = \frac{I_0 + I_1 + I_2}{I_0 + I_1 \cdot e^{-\frac{V_{DD}}{2\phi_t}} + I_2 \cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{26}$$

Substituting eq. (20) and eq. (26) into eq. (25), results

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{2+\frac{I_0}{I_2}+\frac{I_1}{I_2}}{1-e^{\frac{V_{DDH}-V_{DD}}{2\phi_t}}}. \tag{27}$$

The sets of metastable points of the VTC, calculated from equations (9)-(11), form the "Z" curves plotted in Fig. 30 and Fig. 31 for V_{DD} in the range 200 mV to 400 mV. In Fig. 30 (a)-(c) the feedback is low (I_2/I_0 = 0.1-0.5) and in Fig. 31 (a)-(c) the feedback is high (I_2/I_0 = 1-5). It can be observed that the metastable arc is roughly linear for high feedback.

For high feedback we can estimate the hysteresis width, V_L, as follows (see Fig. 25):

$$V_L \approx \frac{V_O^+ - V_O^-}{\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}}} \approx \frac{V_{DD}-\Delta V}{\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}}}, \tag{28}$$

where ΔV is a fitting parameter. From Fig. 25, $\Delta V \approx 2 \cdot V_{X0}$. Applying (28) into (29) we can estimate the hysteresis width in weak inversion as

$$V_L \approx \frac{\left(V_{DD}-2V_{X0}\right)\cdot\left(1-e^{\frac{V_{DDH}-V_{DD}}{2\phi_t}}\right)}{2+\frac{I_0}{I_2}+\frac{I_1}{I_2}}, \tag{29}$$

Equation (29) is valid when hysteresis is present ($V_{DD} > V_{DDH}$).

The hysteresis width expression in strong inversion is given in Apendix E for completeness.

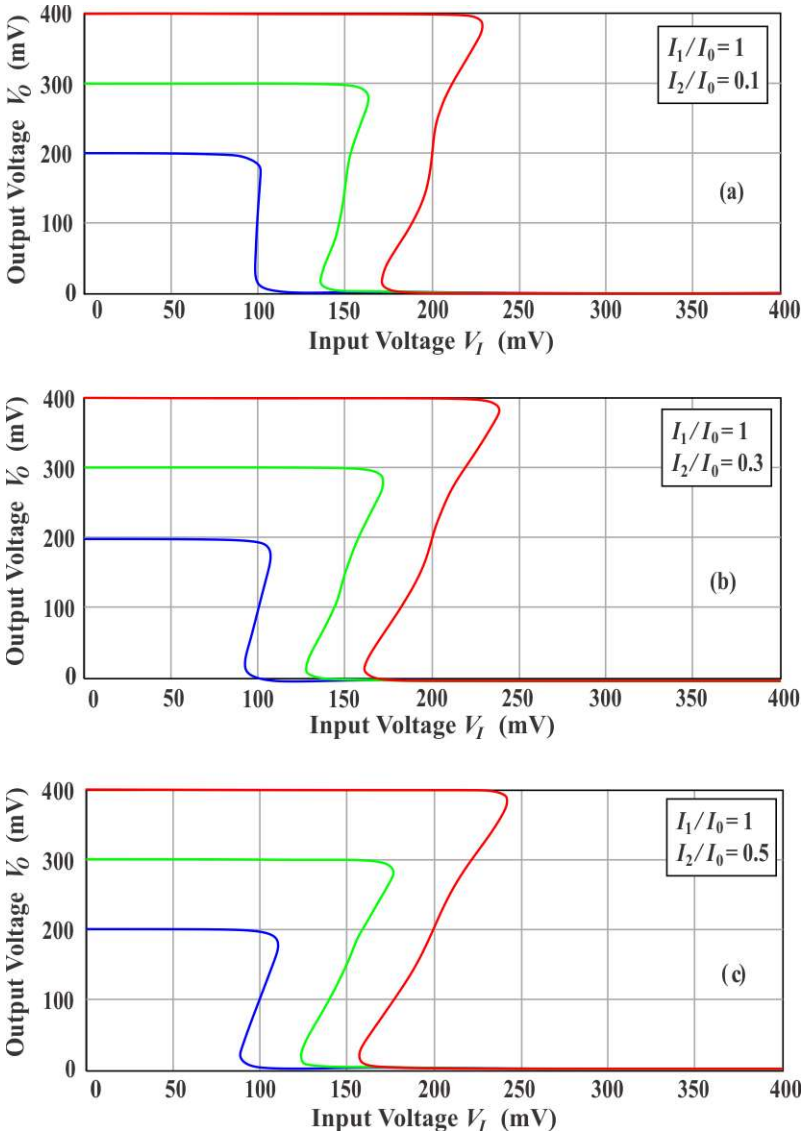


Figure 30 – VTC of the ST for V_{DD} = 200 mV, 300 mV, and 400 mV, I_1/I_0 = 1. Low feedback: (a) I_2/I_0 = 0.1; (b) I_2/I_0 = 0.3; (c) I_2/I_0 = 0.5.

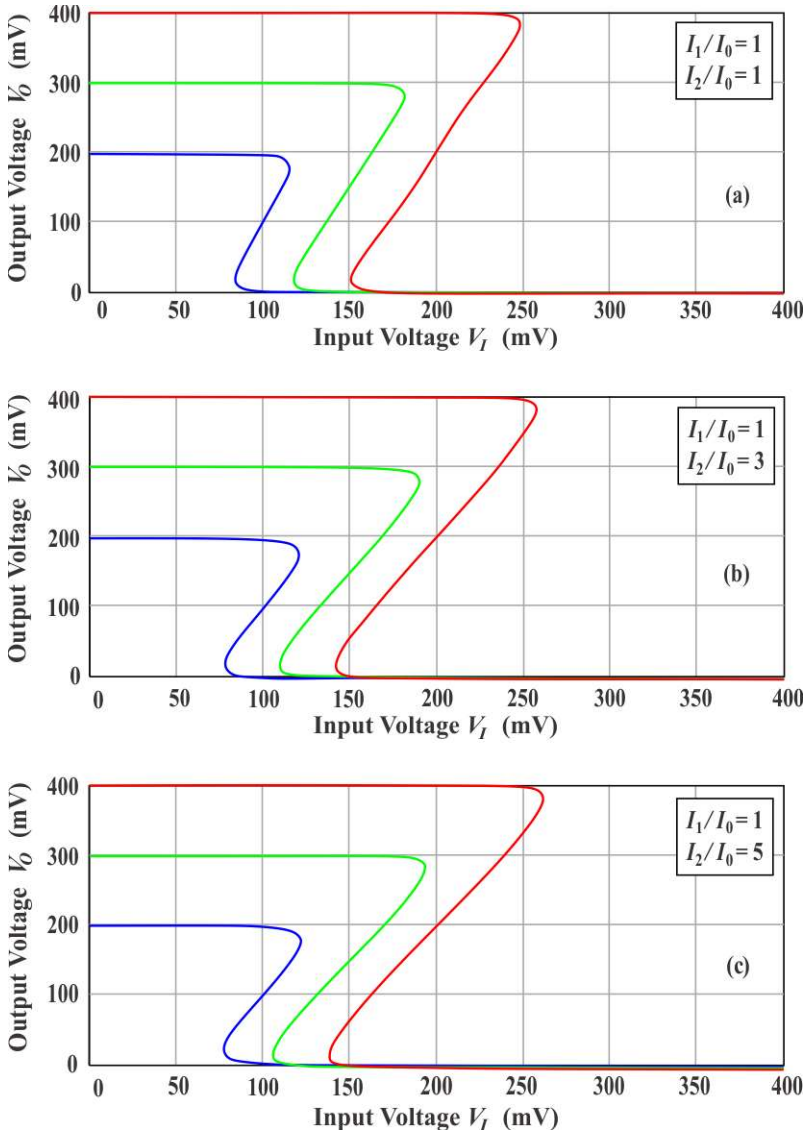


Figure 31 – VTC of the ST for V_{DD} = 200 mV, 300 mV, and 400 mV, I_1/I_0 = 1. High feedback: (a) I_2/I_0 = 1; (b) I_2/I_0 = 3; (c) I_2/I_0 = 5.

2.3 SIMULATION AND EXPERIMENTAL RESULTS

In order to validate the theoretical study of the Schmitt trigger, a test chip was fabricated in a 180 nm technology (V_{TN0} = 397 mV, V_{TP0} = –394 mV, n_N = 1.32, n_P = 1.24, for $L_N = L_P$ = 1.08 µm). Two sets of Schmitt triggers were designed with different transistors sizes in order to evaluate the effect of the relative transistor strength on the hysteresis width. The length of the transistors was fixed at 6 times the minimum transistor length allowed by the technology (L_{MIN} = 180 nm), in order to reduce both the threshold voltage spread and the reverse short channel effect (RSCE) [39],[74],[75]. For the same reason, NMOS and PMOS transistors were separated by a distance higher than the minimum, to avoid line edge roughness (LER) [55], and random dopant fluctuations (RDF), which is the main cause of V_T variations [63],[75]. The transistor length and width were determined by simulation for typical (TT) corner parameters for V_{DD} = 150 mV, in order to have the resulting VTC centered at $V_{DD}/2$. Two sets of Schmitt triggers with I_1/I_0 = 0.4 and I_1/I_0 = 1 and feedback ratios, I_2/I_0, of 0.1, 0.3, 1, and 3 were designed.

The ST with $I_1/I_0 = I_2/I_0 = 1$, where $(W/L)_{P0} = (W/L)_{P1} = (W/L)_{P2}$ = 14 µm / 1.08 µm and $(W/L)_{N0} = (W/L)_{N1} = (W/L)_{N2}$ = 1.08 µm / 1.08 µm, was first used for the measurement of the VTC and output currents. The standard cell layout of the designed ST, which occupies an area of 10.41 µm x 20.37 µm, is shown in Fig. 32. The full chip micrograph and layout are shown in Appendix F, Fig. 72 and Fig. 73, respectively.

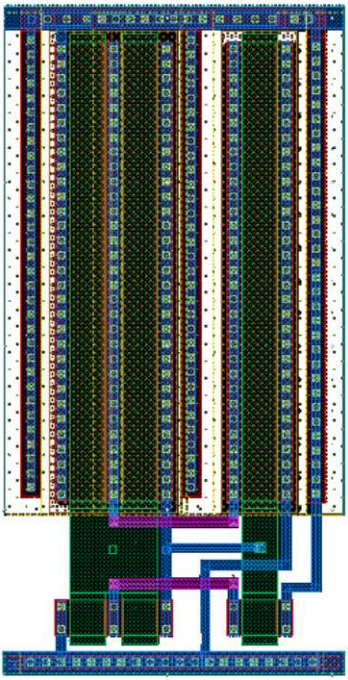


Figure 32 – Layout of the ST with $I_1/I_0 = I_2/I_0 = 1$, where $(W/L)_{P0} = (W/L)_{P1} = (W/L)_{P2} = 14\ \mu m/1.08\ \mu m$ and $(W/L)_{N0} = (W/L)_{N1} = (W/L)_{N2} = 1.08\ \mu m/1.08\ \mu m$

The VTC of the ST for supply voltages of 50 mV, 100 mV, 150 mV, 200 mV, and 250 mV are shown in Fig. 33. For supply voltages below 100 mV hysteresis is not present, in well agreement with eq. (21), which gives V_{DDH} = 99.7 mV, with n = 1.3 extracted from the simulation.

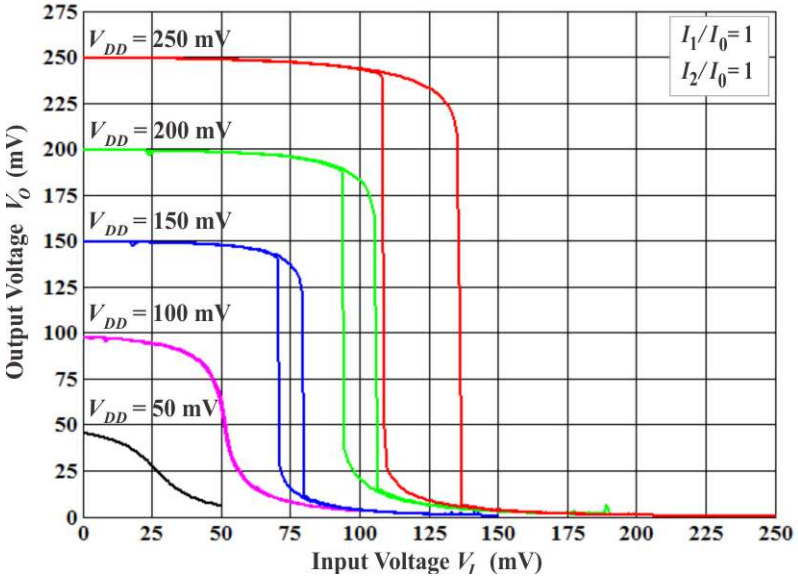


Figure 33 – Measured VTCs of the ST with $I_1/I_0 = I_2/I_0 = 1$, for V_{DD} between 50 mV and 250 mV.

The output current of the ST shown in Fig. 32, measured for V_{DD} = 60 mV, can be seen in Fig. 34. In this example, for fixed input voltages of 20 mV, 30 mV, and 40 mV, there is only one stable point; consequently, no hysteresis is present. Note from simulation that the zero-crossing values (17 mV, 33 mV, and 45 mV) are very close to those measured in the fabricated chip (19 mV, 34 mV, and 46 mV).

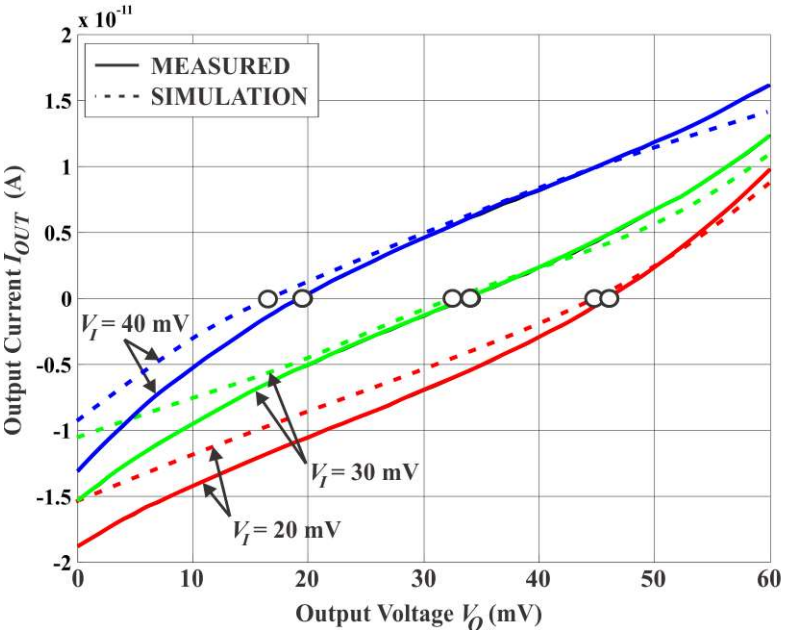


Figure 34 – Measured output current, I_{OUT}, as a function of the output voltage, V_O, for V_I = 20 mV, 30 mV, and 40 mV, for V_{DD} = 60 mV. Open circles are associated with I_{OUT} = 0A.

The measured output current for V_{DD} = 150 mV can be seen in Fig. 35. When the input voltage is 71 mV, the output current is zero for three values of the output voltage. Two of these points are stable, whereas the third is metastable. When the input voltage is lowered to 70 mV the metastable point coincides with the leftmost stable point, which indicates that the low limit of the hysteresis has been reached. For an input voltage V_I = 69 mV, only one stable point exists, clearly showing that this input voltage is not within the hysteresis limits. Analogous conclusions can be drawn for V_I = 78 mV, 79 mV, and 80 mV; in this case, note that V_I = 78 mV is the high limit of the hysteresis curve. When V_I = 75 mV, the metastable point is not exactly at V_O = 75 mV, showing that the p- and n- networks are not perfectly matched.

Note that the experimental curves in Figures 34 and 35 are in close agreement with the theoretical curves of Figures 23 and 24, respectively.

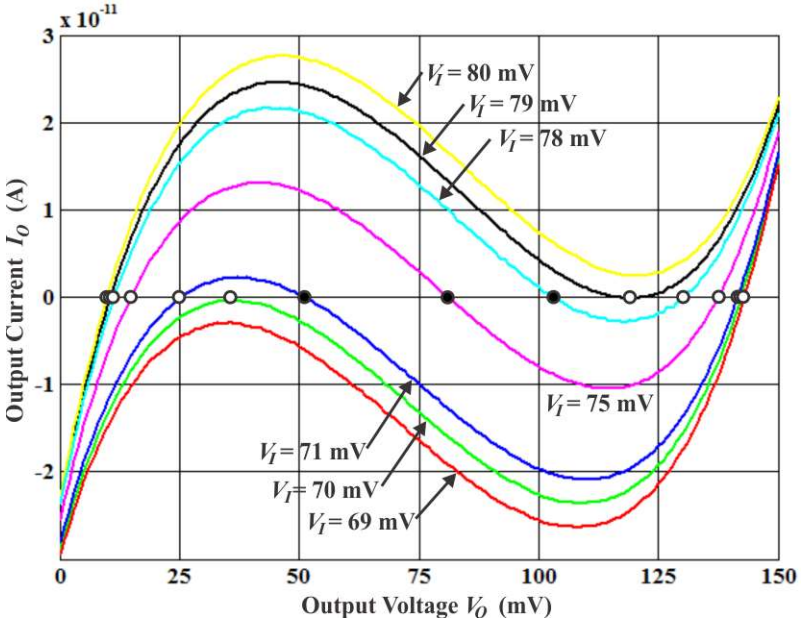
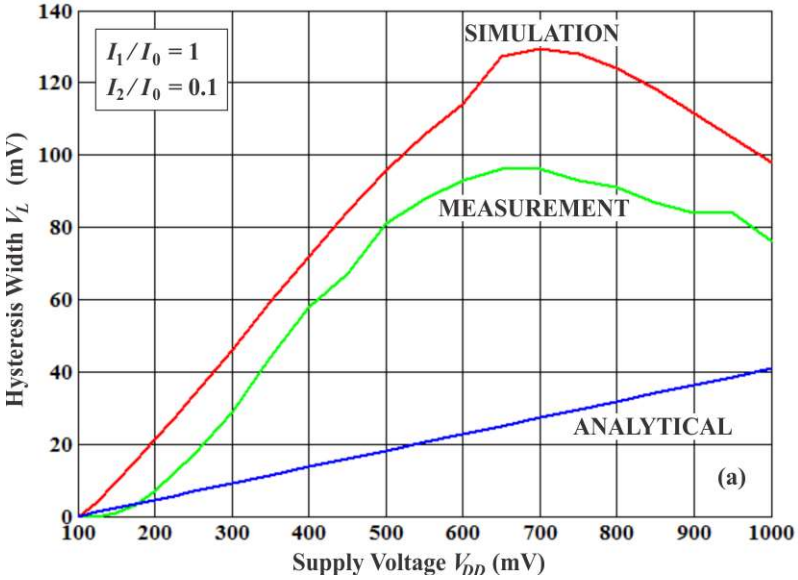


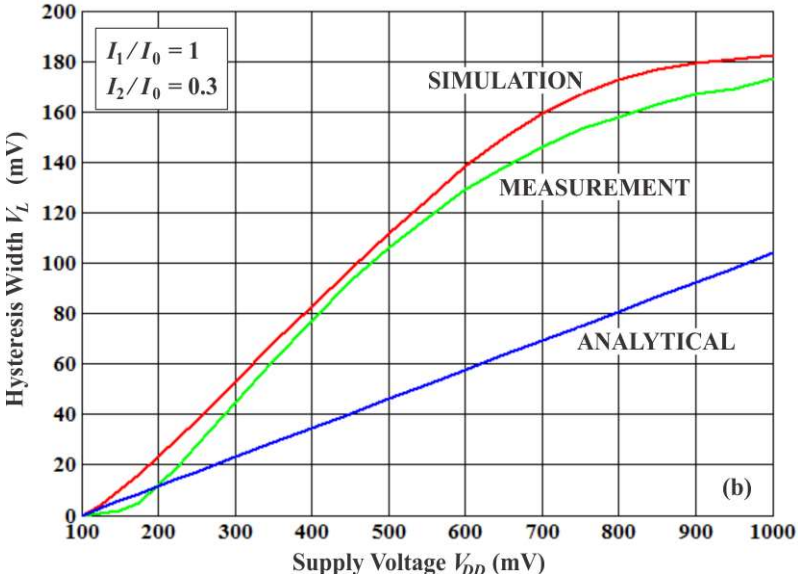
Figure 35 – Measured output current, I_{OUT}, as a function of the output voltage, V_O, for V_I = 69 mV, 70 mV, 71 mV, 75 mV, 78 mV, 79 mV, and 80 mV, for V_{DD} = 150 mV. Open circles are stable points, while closed circles are metastable points.

The hysteresis width was measured for two sets of Schmitt triggers that were integrated and compared with circuit simulations (Cadence Virtuoso, IBM 180 nm design kit) and equation (29). The results in Fig. 36, for the set in which I_1/I_0 = 1, show that hysteresis width varies almost linearly with the supply voltage, for supply voltages higher than around 100 mV. For the cases studied herein, equation (29) shows acceptable results for feedback ratios I_2/I_0 higher than 0.5. For feedback ratios lower than 0.5, the hysteresis width predicted by equation (29) is lower than the measured or simulated value due to the nonlinearity of the metastable arc in the vicinity of the midpoint. For the cases in Fig. 36 (c)-(d) where I_2/I_0 = 1 and I_2/I_0 = 3, respectively, the small difference between the values obtained through simulations, measurements, and equation (29) can be readily explained by variations in the technological parameters and mismatch (mainly associated with the threshold voltage and the width and length of the transistors, which leads to differences in the current strength of the p- and n- networks). Note that in equation (29) the ST is considered to be composed of well-

matched PMOS and NMOS circuits. However, the transistor current is exponentially dependent on both the slope factor and the threshold voltage; therefore, these two factors affect the value of the hysteresis width. The maximum difference in the values for the hysteresis width obtained through measurements and equation (29) were 43 mV (–15.5% at 1V) for the case $I_2/I_0 = 1$, and 36.4 mV (14.5% at 850 mV) for the case $I_2/I_0 = 3$. The results for the set in which $I_1/I_0 = 0.4$ are very similar to those for $I_1/I_0 = 1$, showing difference of only a few millivolts between simulated and measured values. Therefore, the results for $I_1/I_0 = 0.4$ will not be shown here.

Finally, it should be noted that, for supply voltages higher than 500 mV, the analysis of the ST must use the transistor model in either moderate or strong inversion.


$I_1/I_0 = 1$
$I_2/I_0 = 0.1$
SIMULATION
MEASUREMENT
ANALYTICAL
(a)
Hysteresis Width V_L (mV)
Supply Voltage V_{DD} (mV)
0
20
40
60
80
100
120
140
100
200
300
400
500
600
700
800
900
1000


$I_1/I_0 = 1$
$I_2/I_0 = 0.3$
SIMULATION
MEASUREMENT
ANALYTICAL
(b)
Hysteresis Width V_L (mV)
Supply Voltage V_{DD} (mV)
0
20
40
60
80
100
120
140
160
180
200
100
200
300
400
500
600
700
800
900
1000

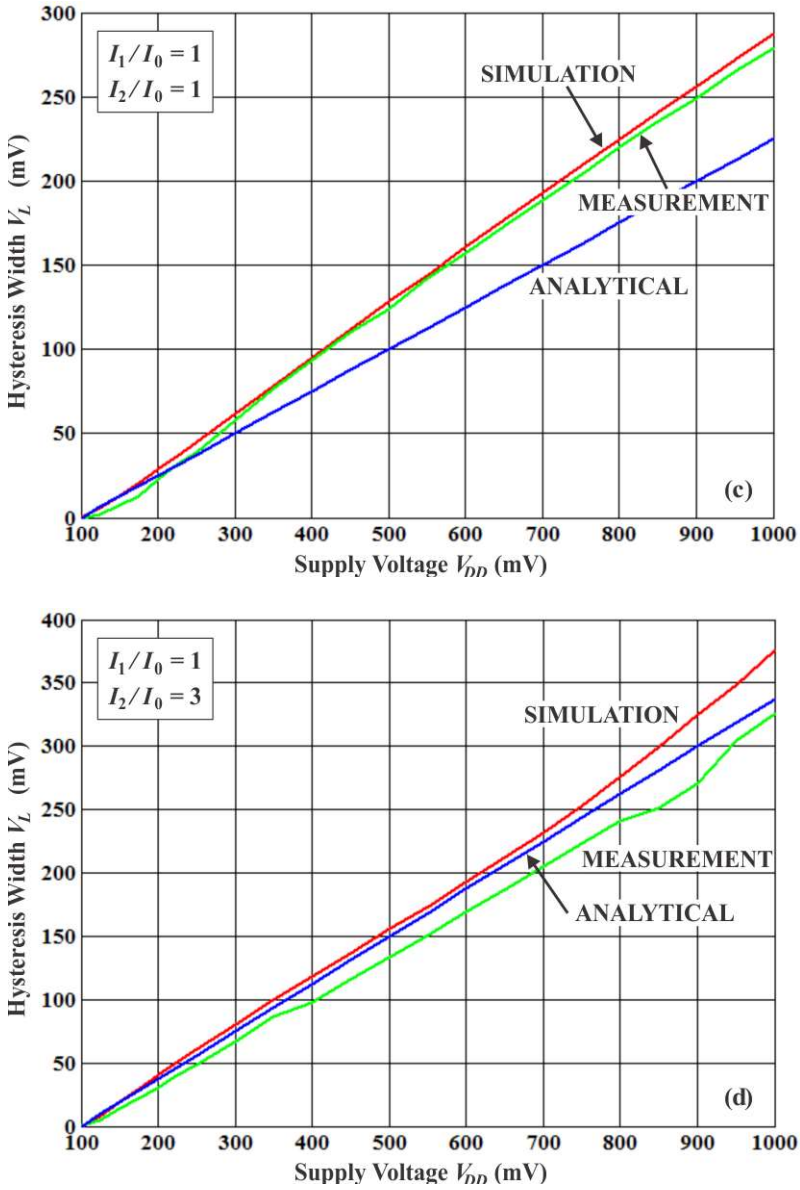


Figure 36 – Comparison of values for the hysteresis width obtained from measurements, simulations and analytical expression, eq. (30), with $I_1/I_0 = 1$, and (a) $I_2/I_0 = 0.1$; (b) $I_2/I_0 = 0.3$; (c) $I_2/I_0 = 1$; and (d) $I_2/I_0 = 3$.

3 OPERATION OF THE SCHMITT TRIGGER AS AN ULTRALOW-VOLTAGE AMPLIFIER

When no hysteresis is present ($V_{DD} < V_{DDH}$), the ST can be used as an ultralow-voltage high-gain amplifier. It has been shown in eq. (22) that, in subthreshold regime, the ST does not present hysteresis for supply voltages of less than 75 mV at room temperature. In real cases, the ST does not exhibit hysteresis for supply voltages of below around 100 mV.

The small-signal circuit of the ST is shown in Fig. 27. The voltage gain of eq. (16) is reproduced here for convenience.

$$\left.\frac{v_O}{v_I}\right|_{V_I=V_O=\frac{V_{DD}}{2}} = \frac{\left(e^{\frac{V_{DD}}{2\phi_t}}-1\right)\cdot\left(1+\frac{I_1}{I_0}+2\frac{I_2}{I_0}\right)+\left(\frac{I_2}{I_0}\right)^2\cdot\left(e^{-\frac{V_{DD}}{2\phi_t}}-1\right)}{\frac{I_2}{I_0}\cdot\left(e^{\frac{V_{DD}}{2\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)+\frac{I_1}{I_0}\cdot\frac{I_2}{I_0}\cdot\left(1-e^{-\frac{V_{DD}}{2\phi_t}}\right)-n\cdot\left(1+\frac{I_2}{I_0}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)} \tag{30}$$

The ST voltage gain of equation (30) is shown in Fig. (37)-(40) as a function of the transistor ratios I_1/I_0 and I_2/I_0, for supply voltages ranging from 40 mV to 70 mV, and $n = 1$. As is clear from the figures, when the feedback strength I_2/I_0 is high, the ST voltage gain is positive and it does not work as an inverter circuit anymore, in agreement with Section 2.1.2. Moreover, it is important to note that there is a maximum absolute gain for $I_0 \sim I_2$ and $I_1 << I_0$. In this sense, there are optimum values of I_2/I_0 and I_1/I_0 that maximize the voltage gain.

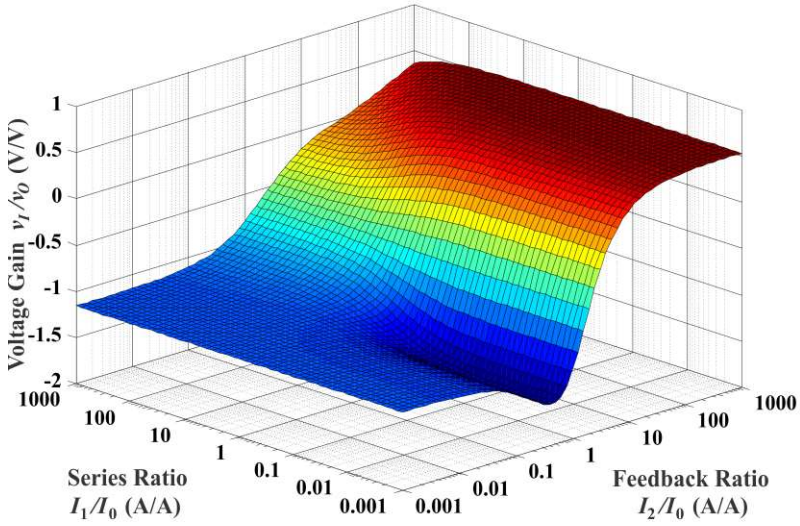


Figure 37 – Small-signal voltage gain of the ST for V_{DD} = 40 mV, n = 1.

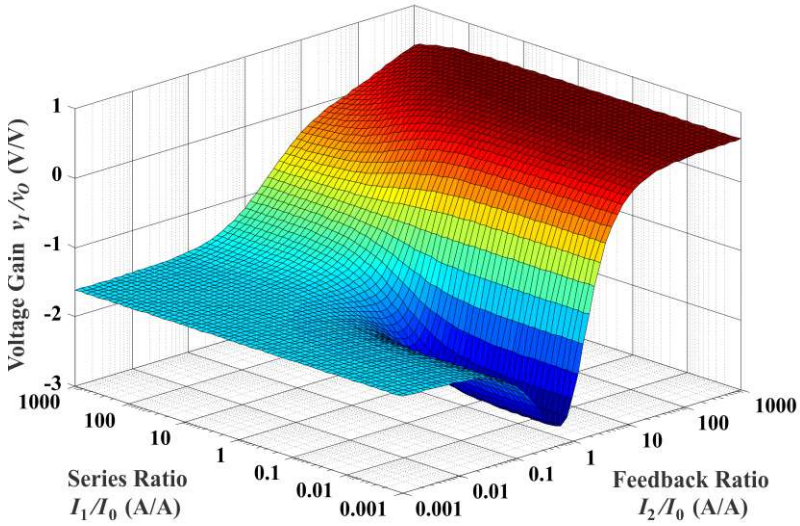


Figure 38 – Small-signal voltage gain of the ST for V_{DD} = 50 mV, n = 1.

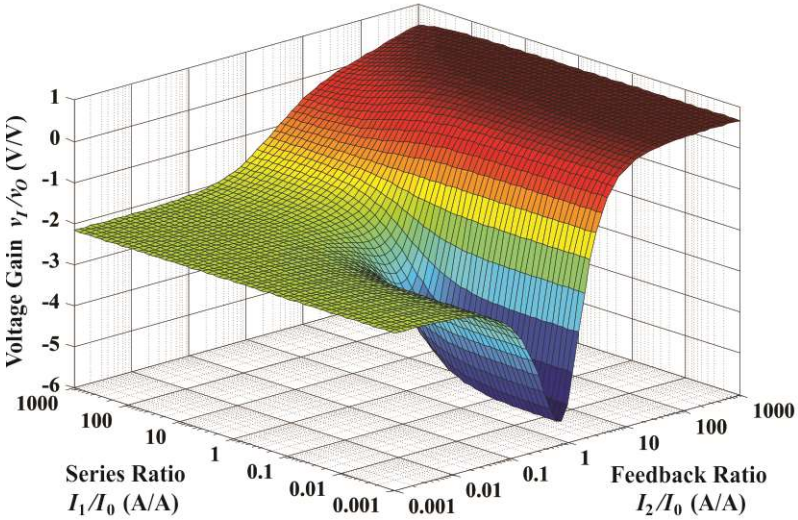


Figure 39 – Small-signal voltage gain of the ST for V_{DD} = 60 mV, n = 1.

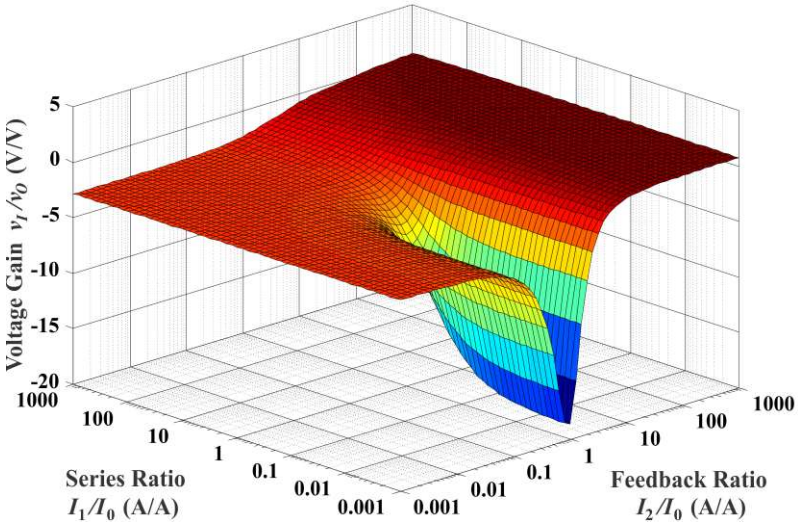


Figure 40 – Small-signal voltage gain of the ST for V_{DD} = 70 mV, n = 1.

3.1 OPTIMUM TRANSISTOR RATIOS

Optimum transistor ratios, I_1/I_0 and I_2/I_0, are defined here as the transistor ratios which maximize the absolute voltage gain of the ST.

3.1.1 Optimum series transistor ratio I_1/I_0

Rearranging eq. (30) in terms of I_1/I_0 results in the bilinear function given in (31), with coefficients A_1, B_1, C_1, and D_1 in (32). Note that A_1, B_1, C_1, and D_1 are dependent on both the supply voltage and I_2/I_0. Function (31) has a singularity for which the result is an infinite gain for a negative value of I_1/I_0 what is not physically possible. Thus, in this case, the maximum absolute gain is obtained when $I_1/I_0 \rightarrow 0$. As an example, this is observed in Fig. 41 for V_{DD} = 60 mV, n = 1 and different values of I_2/I_0, as a function of the I_1/I_0 ratio. However, as can be seen in Fig. 42, values of the series transistor ratio from 0.001 to 0.1 do not have significant effect on the maximum achievable gain.

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{\frac{I_1}{I_0}\cdot A_1 + B_1}{\frac{I_1}{I_0}\cdot C_1 + D_1} \tag{31}$$

$$\left.\begin{aligned} A_1 &= e^{\frac{V_{DD}}{2\phi_t}} - 1 \\ B_1 &= \left(e^{\frac{V_{DD}}{2\phi_t}} - 1\right)\cdot\left(1 + 2\frac{I_2}{I_0}\right) + \left(\frac{I_2}{I_0}\right)^2 \cdot \left(e^{-\frac{V_{DD}}{2\phi_t}} - 1\right) \\ C_1 &= \frac{I_2}{I_0}\cdot\left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right) - n\cdot\left(1 + \frac{I_2}{I_0}\right) \\ D_1 &= \frac{I_2}{I_0}\cdot\left(e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}\right) - n\cdot\left(1 + \frac{I_2}{I_0}\right)^2 \end{aligned}\right\} \tag{32}$$

$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} \rightarrow 0 \tag{33}$$

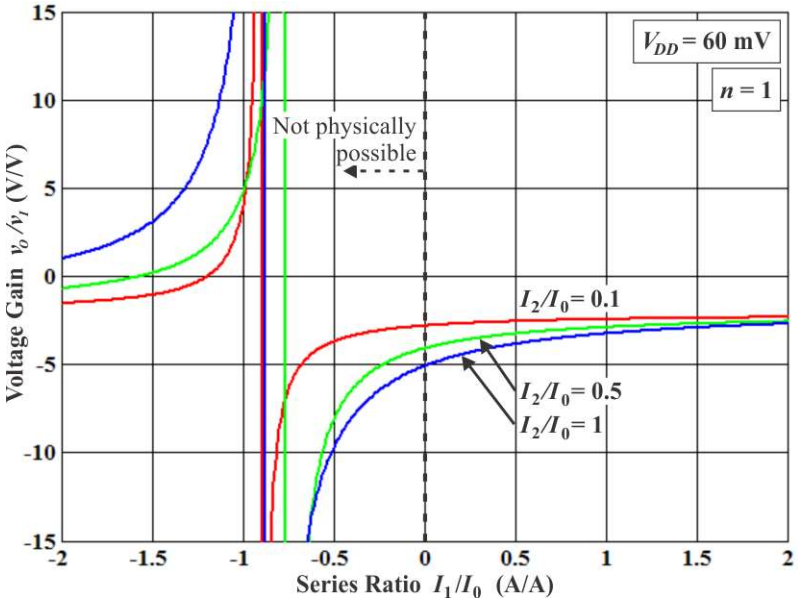


Figure 41 – Small-signal voltage gain of the ST for V_{DD} = 60 mV, n = 1, for different I_2/I_0 ratios, as a function of the I_1/I_0 ratio.

Clearly, I_1/I_0 = 0 is not feasible, so practical values of the series transistors ratio range from 0.01 to 1, with some penalty in terms of the gain.

Figure 42 shows a comparison of the voltage gain, for different I_1/I_0 ratios, with V_{DD} = 60 mV. Note that a I_1/I_0 ratio higher than 0.1 results in a considerable reduction in the maximum achievable voltage gain, which is –5.0 V/V and –3.3 V/V, for I_1/I_0 = 0.1 and I_1/I_0 = 1, respectively.

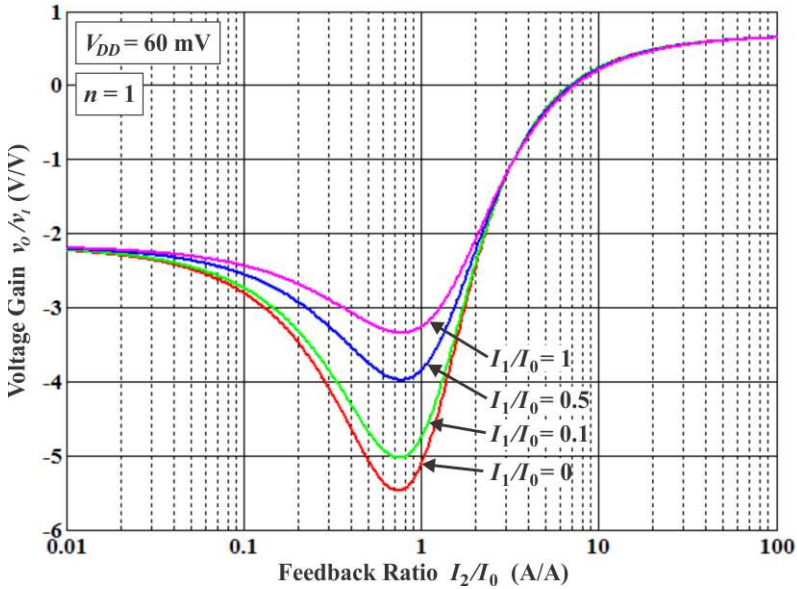


Figure 42 – Small-signal voltage gain of the ST for V_{DD} = 60 mV, n = 1, for different I_1/I_0 ratios, as a function of the I_2/I_0 ratio.

3.1.2 Optimum feedback transistor ratio I_2/I_0

Similarly, rearranging eq. (30) in terms of I_2/I_0 results in (34), with coefficients in (35), for $I_1/I_0 = 0$.

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{\left(\frac{I_2}{I_0}\right)^2 \cdot A_2 + \frac{I_2}{I_0} B_2 + C_2}{\left(\frac{I_2}{I_0}\right)^2 \cdot D_2 + \frac{I_2}{I_0} E_2 + F_2} \tag{34}$$

$$\left.\begin{aligned} A_2 &= e^{-\frac{V_{DD}}{2\phi_t}} - 1 \\ B_2 &= C_2 = e^{\frac{V_{DD}}{2\phi_t}} - 1 \\ D_2 &= F_2 = -n \\ E_2 &= e^{\frac{V_{DD}}{\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}} - 2 \cdot n \end{aligned}\right\} \tag{35}$$

Taking the partial derivative of (34) with respect to I_2/I_0 to find the maximum absolute gain, results in:

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{\left(n^2 - n + 1\right) + e^{\frac{V_{DD}}{2\phi_t}} \cdot \left(2 \cdot n - 1\right) - e^{-\frac{V_{DD}}{2\phi_t}}} - n}{2 \cdot n - 1 + e^{-\frac{V_{DD}}{2\phi_t}}}, \tag{36}$$

The slope factor, n, has little influence on the value of the optimum value of I_2/I_0 at a given supply voltage. So, eq. (36) can be simplified to

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{1 + e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}} - 1}{1 + e^{-\frac{V_{DD}}{2\phi_t}}}, \tag{37}$$

for $n = 1$. Table III shows, for $I_1/I_0 = 0$ and $n = 1$, the optimum values of I_2/I_0, which results in the maximum absolute voltage gain, for different supply voltages.

TABLE III – Optimum values of I_2/I_0 for different supply voltages, with I_1/I_0 = 0 and n = 1.

V_{DD} (mV)	Optimum I_2/I_0	Optimum gain (V/V)
75	0.998	$-\infty$
70	0.905	– 19.076
60	0.732	– 5.581
50	0.577	– 2.764
40	0.438	– 1.574
31.5	0.333	– 1.000
30	0.315	– 0.919

4 THE SCHMITT TRIGGER AS AN ULTRALOW-VOLTAGE LOGIC INVERTER

4.1 THE 6-TRANSISTOR SCHMITT TRIGGER AS A LOGIC INVERTER: STATIC AND DYNAMIC ANALYSIS

The conventional CMOS inverter, shown in Fig. 43, can be treated as a particular case of the Schmitt trigger, with no feedback (I_2 = 0).

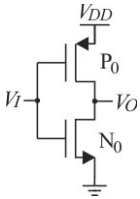


Figure 43 – Conventional CMOS inverter.

The voltage gain of the CMOS inverter, for $V_I = V_O = V_{DD}/2$, derived from the ST voltage gain, eq. (16), is

$$\left.\frac{v_O}{v_I}\right|_{V_I=V_O=\frac{V_{DD}}{2}} = -\frac{e^{\frac{V_{DD}}{2\phi_t}}-1}{n}. \tag{38}$$

Thus, the minimum operating supply voltage, V_{DDmin} [73], for regenerative logic is obtained by making the voltage gain in (38) equal to –1, which yields

$$V_{DD\,\min} = 2\phi_t \cdot \ln(n+1). \tag{39}$$

Assuming that the inverter is composed of ideal MOSFETs (n = 1), eq. (39) reduces to the well-known value [73] of

$$V_{DD\,\min} = 2\phi_t \cdot \ln(2) = 35.9\ \text{mV, at 300K}\ . \tag{40}$$

In the case of the ST, on substituting the optimum values of I_1/I_0 and I_2/I_0 from (33) and (37), respectively, into (18) the minimum value of the supply voltage for a voltage gain equal to –1 V/V is

$$V_{DD\min} = 2\phi_t \cdot \ln\left(\frac{8+\sqrt{73}}{9}\right) = 31.5\,\text{mV, at } 300\text{K}\,, \qquad (41)$$

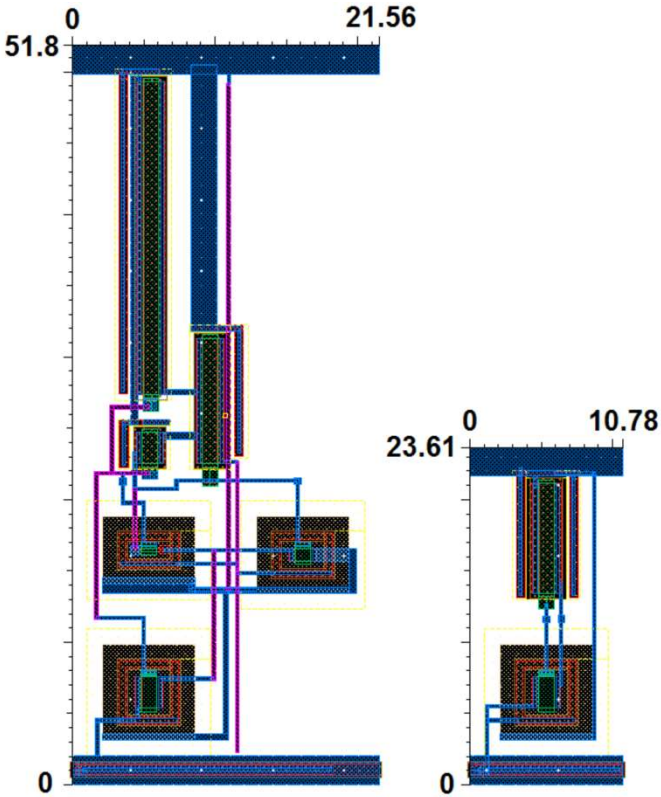
which is achieved for $I_1/I_0 = 0$ and $I_2/I_0 = 1/3$.

It is remarkable that the ST is theoretically capable of operating as a unity-gain amplifier at a supply voltage as low as 31.5 mV. Although the difference between the minimum supply voltage of the inverter, regarded as *the fundamental limit* [73], and that of the Schmitt trigger is small (12.2%), only 4.4 mV at 300 K, it is of paramount importance because it exceeds the previously stated limit for the low-voltage operation of CMOS logic, motivating the continued quest for different circuits and topologies intended for ultralow-voltage operation.

4.1.1 Comparison of the minimum supply voltage for the Schmitt trigger and conventional inverter – Experimental results

In order to compare the Schmitt trigger and the inverter, a test chip was designed and fabricated using IBM 180 nm technology. A total of 40 chips were fabricated and 30 of them were used for measurements; 10 of them were malfunctioning due to bad handling or fabrication problems. Chips were designed comprising a set of 5 STs with different pull up and pull down capabilities, with the purpose to pre-compensate possible threshold voltage variations. One ST was designed in order to compensate the SF corner, another one to compensate halfway between SF and TT corners, another one for the TT corner, another one to compensate halfway between FS and TT corners, and, finally, another one to compensate the FS corner. The same strategy was used for a set of 5 conventional inverters. The result of this design strategy is that at least one ST and one inverter have their VTCs centered close to $V_{DD}/2$ after fabrication. The STs were optimized for a supply voltage equal 40 mV, so that, $I_1/I_0 = 0.1$ and $I_2/I_0 = 0.4$. After the VTC measurements of all the STs and all the inverters in a single chip, the ST with SF pre-compensation and the inverter with halfway SF and TT corners pre-compensation resulted in VTCs closest to $V_{DD}/2$ and were chosen for complete measurements in the rest of the chips. The test chip micrograph and layout are shown in Appendix F, Fig. 70 and Fig. 71,

respectively. The length of the transistors were fixed at 6 times the minimum transistor length allowed by the technology (L_{min} = 180 nm), in order to minimize threshold voltage spread and short channel effects. The layout of the ST and the inverter follow a standard cell style, as shown in Fig. 44 (a) and (b), respectively. The sizes of the ST's transistors are: $(W/L)_{P0}$ = 22 µm/1.08 µm, $(W/L)_{P1}$ = 2.2 µm/1.08 µm, $(W/L)_{P2}$ = 8.8 µm/1.08 µm, $(W/L)_{N0}$ = 2.2 µm/1.08 µm, $(W/L)_{N1}$ = 0.22 µm/1.08 µm, $(W/L)_{N2}$ = 0.88 µm/1.08 µm. The sizes of the inverter's transistors are: $(W/L)_P$ = 7.7 µm/1.08 µm, $(W/L)_N$ = 2.2 µm/1.08 µm. The ST layout area is 21.56 µm x 51.80 µm whereas the inverter layout area is 10.78 µm x 23.61 µm. The area penalty of about 4x presented by the ST if compared to the conventional inverter is compensated by the better performance shown.



(a) (b)

Figure 44 – (a) Schmitt trigger layout; (b) inverter layout.

Figure 45 shows the VTCs of the measured ST and the inverter, for supply voltages between 50 mV and 150 mV. At a supply voltage of 150 mV, the ST presents hysteresis, while for the other supply voltages it does not. For V_{DD} = 100 mV the gain of the ST is much higher than that measured for the standard inverter.

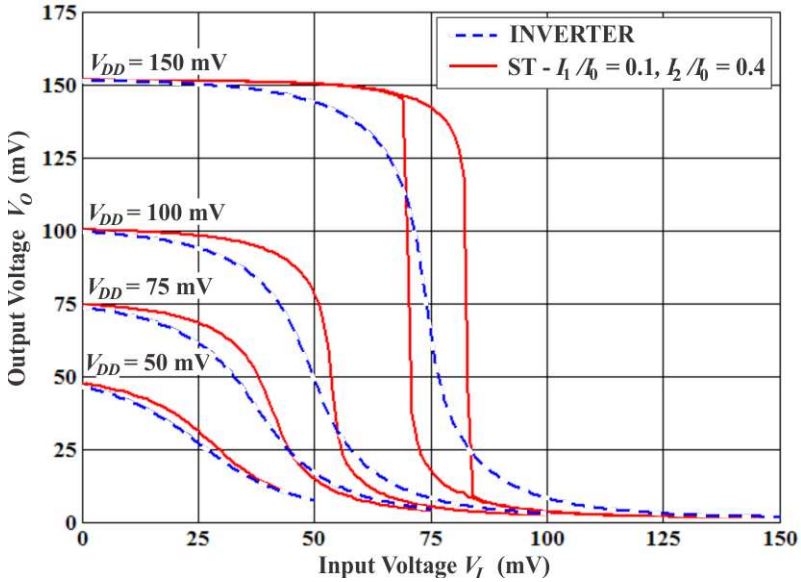


Figure 45 – Measured VTC comparison of the ST and the inverter for V_{DD} = 50 mV, 75 mV, 100 mV, and 150 mV.

The minimum supply voltage that results a gain equal –1 V/V is shown in Fig. 46 for chip sample number 5, and was measured as 44 mV for the inverter and 42 mV for the ST. Measurements in all 30 available chip samples reveals that in all cases the minimum supply voltage that results in a voltage gain equal –1 V/V is lower in the case of the ST than in the case of the inverter, as summarized in Fig. 47. The minimum supply voltage of the ST ranges between 40 mV and 43 mV, and between 44 mV and 45 mV for the inverter. Although the difference is only a few millivolts, it is systematic and always lower for the ST than it is for the inverter. Sample number 18 has the minimum supply voltage closest to the minimum theoretical supply voltage of 31.5 mV. The higher measured supply voltage can be readily explained because the ST was optimized for 40 mV and because the MOSFETs are not ideal, with a slope factor higher than unity.

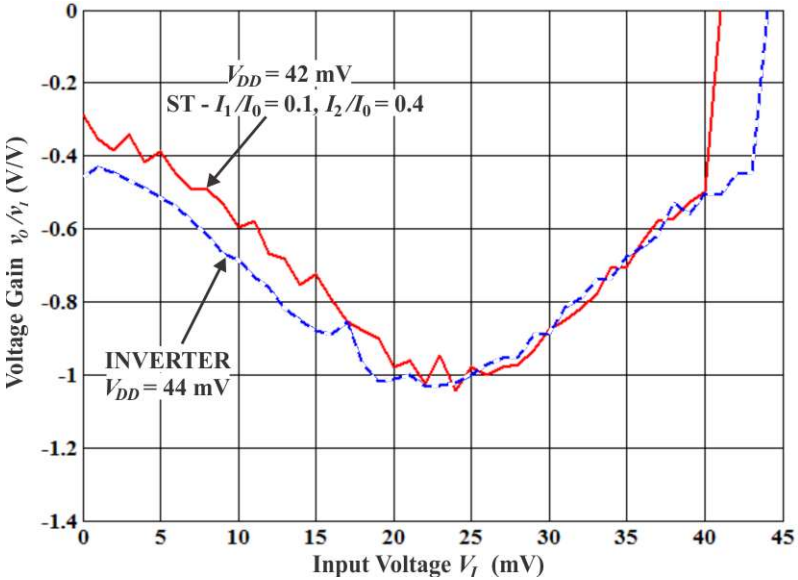


Figure 46 – Measured voltage gain transfer, for minimum supply voltage for the ST and the inverter in chip sample number 5.

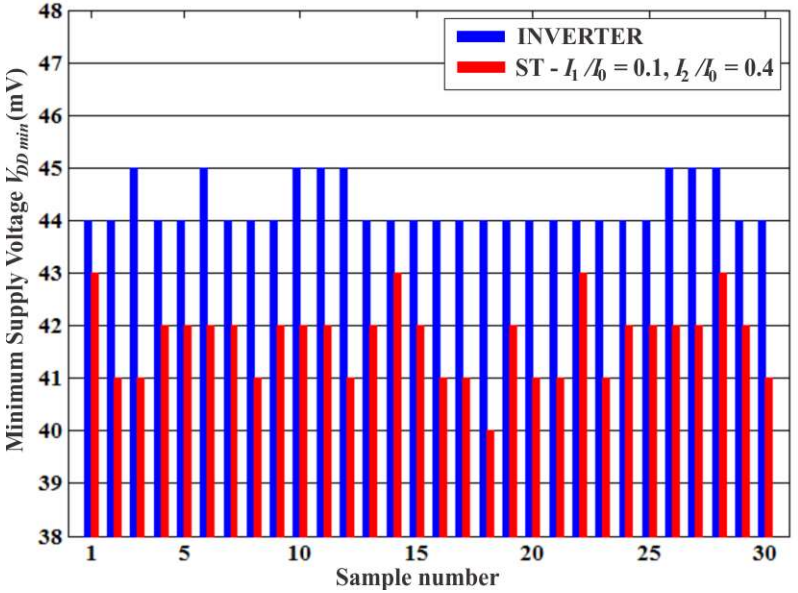


Figure 47 – Measured minimum supply voltage of both the ST and the inverter on 30 samples.

4.1.2 Comparison of the voltage gain of the Schmitt trigger and the standard inverter – Analytical, simulation and experimental results

Another comparison between the gain of the ST and that of the standard inverter is shown in Fig. 48, obtained from eq. (16) and eq. (38), respectively, for n = 1. The curves are obtained using the exponential characteristic of the MOS transistor with balanced PMOS and NMOS networks, for both the ST and the standard inverter. It can be observed that, for supply voltages ranging from 60 mV to 80 mV, the ST can achieve gains considerably higher than those of the conventional inverter. With a supply voltage of 80 mV, for instance, the ST gain (for $I_1/I_0 = I_2/I_0 = 1$) is 4.9 times greater than that of the standard inverter. The ST for which $I_1/I_0 = 10$ is the only case that shows lower absolute gain if compared to the standard inverter, between 30 mV and 73 mV of supply voltage. This can be readily explained due to the fact that the series transistor ratio is very high ($I_1/I_0 >> 0$) and degrades the gain. The asymptotic trend of the ST voltage gain tending to infinite indicates the appearance of hysteresis. When this happens, the ST is no longer useful as an amplifier. The slope factor, n, equals unity in the curves of Fig. 48. In the real case, $n > 1$; accordingly, the voltage gain decreases and the hysteresis appears for higher supply voltages.

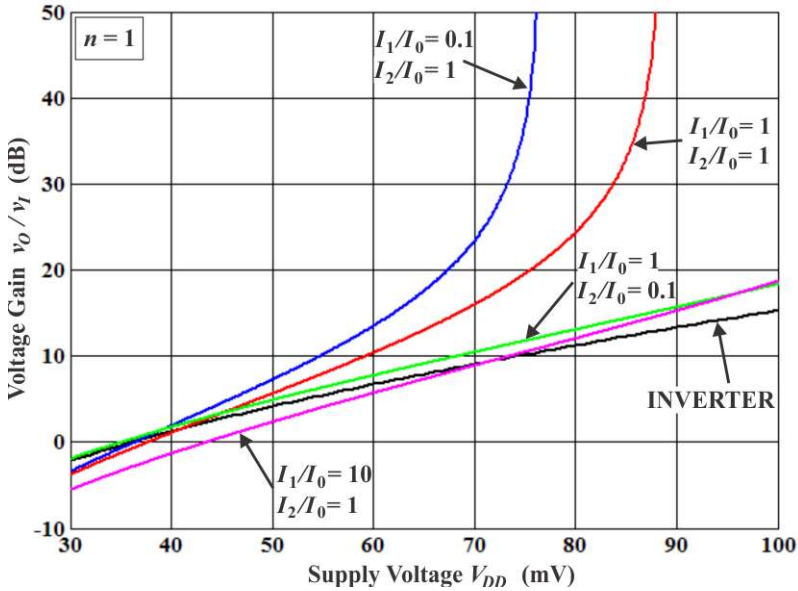


Figure 48 – Comparison of the gains of the standard inverter and the Schmitt trigger, from analytical expressions, with different transistor strength ratios.

To validate the comparison of the gains of the Schmitt trigger and the conventional inverter, we ran some simulations, assuming that the NMOS and PMOS networks have the same current strength. We also designed and fabricated another chip with an inverter and some Schmitt triggers in a 180 nm technology. In both the simulation and the fabricated design, the length of the transistors was fixed at 6 times the minimum transistor length allowed by the technology (L_{min} = 180 nm), for the reasons already explained.

Figure 49 shows the simulated VTCs of two STs, with different I_2/I_0 ratios and I_1/I_0 = 1 in both cases, and an inverter for V_{DD} = 75 mV and V_{DD} = 100 mV. As can be observed, the voltage gain with V_{DD} = 100 mV is much higher for the STs than for the inverter. The ST and the inverter dimensions are given in Table IV.

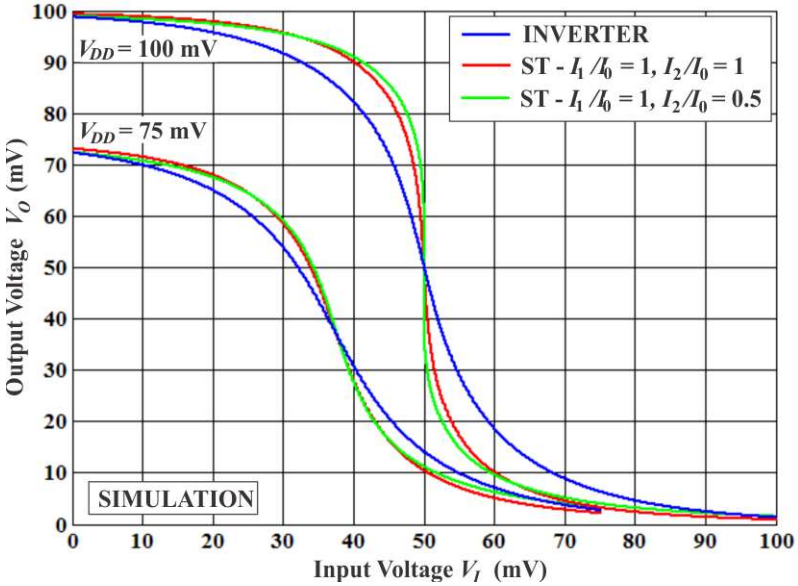


Figure 49 – Simulated VTCs of the ST and the inverter for V_{DD} = 75 mV and V_{DD} = 100 mV in a 180 nm technology.

TABLE IV – Schmitt trigger and inverter transistor aspect ratios.

Inverter	$\left(\frac{W}{L}\right)_P = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_N = \frac{1.08\mu m}{1.08\mu m}$
ST $I_1/I_0 = 1$ $I_2/I_0 = 1$	$\left(\frac{W}{L}\right)_{P0} = \left(\frac{W}{L}\right)_{P1} = \left(\frac{W}{L}\right)_{P2} = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N0} = \left(\frac{W}{L}\right)_{N1} = \left(\frac{W}{L}\right)_{N2} = \frac{1.08\mu m}{1.08\mu m}$
ST $I_1/I_0 = 1$ $I_2/I_0 = 0.5$	$\left(\frac{W}{L}\right)_{P0} = \left(\frac{W}{L}\right)_{P1} = 2\times\frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{P2} = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N0} = \left(\frac{W}{L}\right)_{N1} = 2\times\frac{1.08\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N2} = \frac{1.08\mu m}{1.08\mu m}$

Figure 50 shows plots of the maximum voltage gain versus the supply voltage, obtained from simulations, for the same STs and the inverter of Fig. 49. The gain of the STs is considerably higher than that of the inverter for supply voltages approaching 100 mV. However, the gain of the ST simulated with $I_1/I_0 = I_2/I_0 = 1$ is lower than that of the inverter for V_{DD} lower than 50 mV. This can be explained because the series ratio of the ST, I_1/I_0, is considerably higher than the optimum.

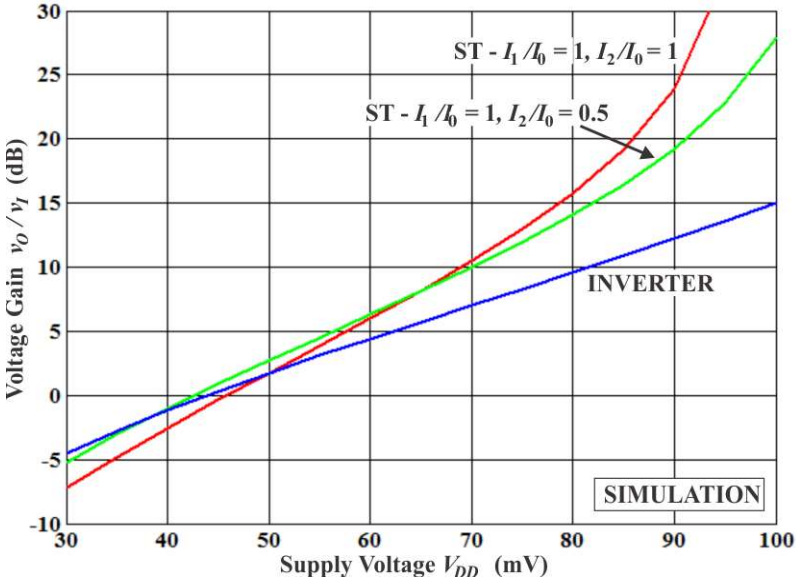


Figure 50 – Simulated voltage gains obtained for the inverter and STs with I_2/I_0 = 0.5 and I_2/I_0 = 1, and I_1/I_0 = 1.

A set of test circuits, shown in Fig. 51, containing several Schmitt triggers with different relative transistor strengths (I_1/I_0 = 0.4, 1 and I_2/I_0 = 0.5, 1, and 3) was designed and fabricated in a 180 nm technology. The results for the STs with I_1/I_0 = 0.4 are not reported here, since they are very similar to those of the STs with I_1/I_0 = 1. The micrograph and layout of the chip are shown in Appendix F, Fig. 74 and Fig. 75, respectively.

The measured VTCs of 3 ST circuits are shown in Fig. 52, for supply voltages of 50 mV, 75 mV, and 100 mV. As expected for supply voltages of 100 mV or less, none of the curves exhibit hysteresis. For V_{DD} = 50 mV, the maximum absolute voltage gain is higher than unity only in the case of the ST with I_2/I_0 = 0.5. For V_{DD} = 100 mV, the maximum absolute gain for the ST with I_2/I_0 = 0.5 is around –10.3 V/V (or 20.2 dB), whereas for the other two the gain is greater than –10 V/V (20 dB). For the sake of comparison, the maximum voltage gain of a symmetrical standard inverter, for which n = 1 and V_{DD} = 100 mV, is around –5.8 V/V (15.2 dB). On the other hand, when n = 1.3, the maximum gain of a perfectly symmetrical inverter, with V_{DD} = 100 mV, is around –4.5 V/V (13 dB).

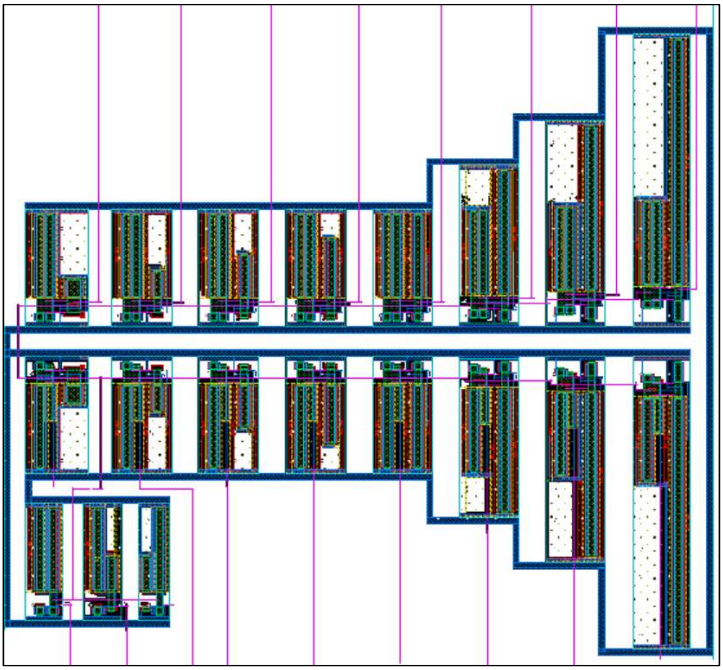


Figure 51 – Layout of the fabricated Schmitt triggers and inverter.

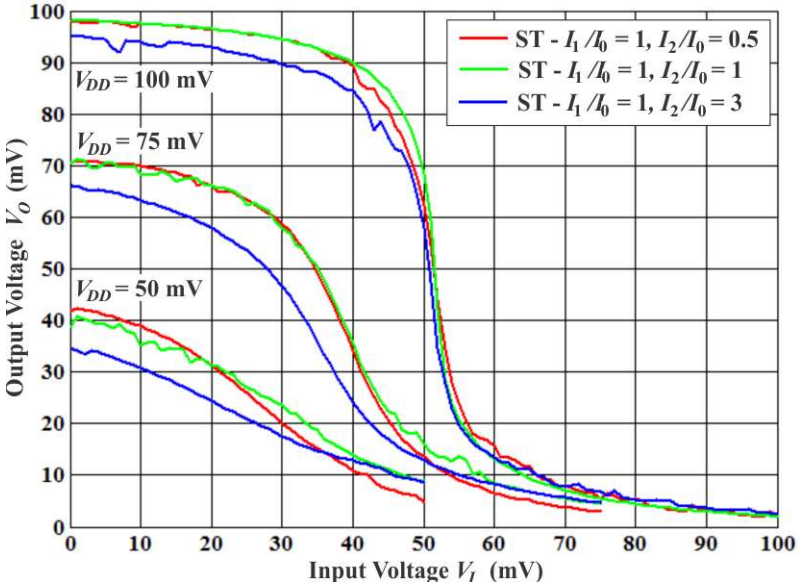


Figure 52 – Measured VTCs of the ST with $I_1/I_0 = 1$ and $I_2/I_0 = 0.5$, 1, and 3, for $V_{DD} = 50$ mV, 75mV, and 100 mV.

A comparison between simulated and measured voltage gains for a ST and values for a simulated inverter is shown in Fig. 53 for supply voltages ranging from 30 mV to 100 mV. The ST was designed with $I_1/I_0 = I_2/I_0 = 1$. The simulation and the measurement results for the ST are well matched and show that, for supply voltages higher than around 53 mV, the absolute voltage gains are higher than those of the simulated inverter.

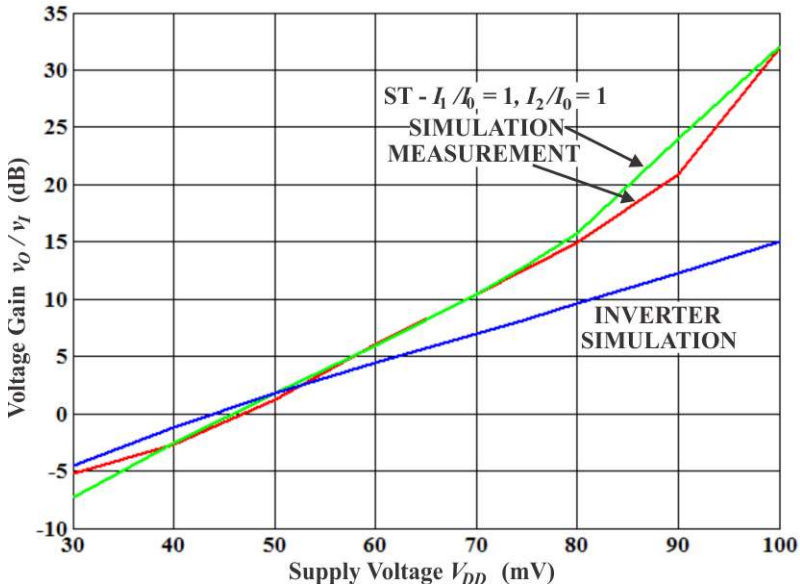


Figure 53 – Comparison between the voltage gain of a simulated inverter, and both simulated and measured values for a ST with $I_1/I_0 = I_2/I_0 = 1$.

4.1.3 Comparison of the maximum absolute gain of the optimized Schmitt trigger and the standard inverter – Analytical results

Another comparison of the gain of the ST optimized for every supply voltage (I_1/I_0 and I_2/I_0 are given by eq. (33) and eq. (37), respectively), a ST optimized for a supply voltage of 50 mV ($I_1/I_0 = 0$ and $I_2/I_0 = 0.58$), and of a conventional inverter is shown in Fig. 54. For example, at 50 mV the inverter has a gain of –1.6 V/V whereas the optimized ST has a gain of –2.7 V/V. At 70 mV the difference between the gains of the inverter and the optimized ST is even larger; –2.8 V/V for the inverter in contrast with –19.1 V/V for the ST. Also, note that the optimized ST reaches a gain of –1 V/V for a supply voltage of 31.5 mV (open circle ○), whereas the conventional inverter reaches a gain of –1 V/V only at a supply voltage of 36 mV (closed circle ●), as already explained. At the same time, both the gain and the minimum supply voltage for a gain higher than –1 V/V (crossed circle ⊗) of the ST optimized for $V_{DD} = 50$ mV are very close to those of the ST optimized for every supply voltage.

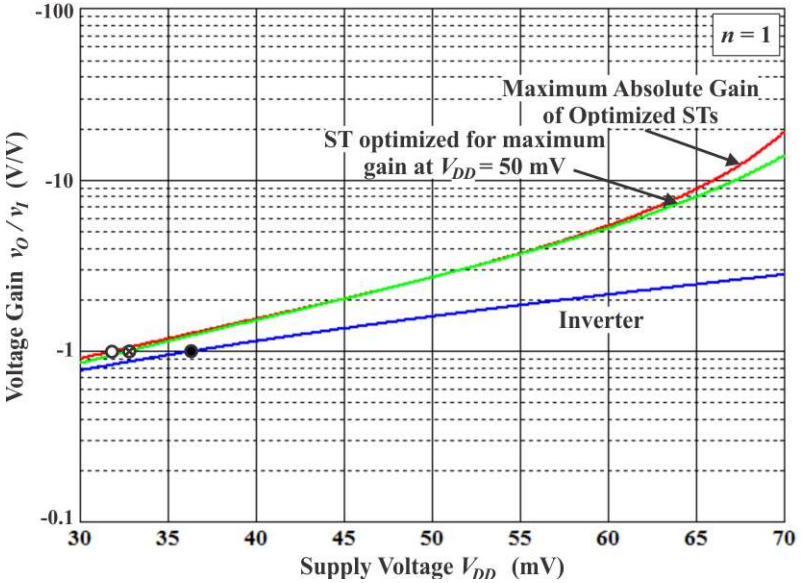


Figure 54 – Comparison of the maximum absolute gains of the Schmitt trigger optimized for maximum gain at any supply voltage, the Schmitt trigger optimized for 50 mV, and the conventional inverter.

At the same time, if the ST operates at a different supply voltage for which it was optimized, it still provides higher gains than the gain of the inverter, as summarized in Table V. Bold values show that the ST provides the highest gain if it is supplied by a voltage equal to the one it was optimized for.

TABLE V – Comparison between the inverter and the optimized Schmitt trigger gain for different supply voltages (n = 1).

V_{DD} (mV)	Inverter Gain (V/V)	Schmitt trigger Gain (V/V) Optimized for V_{DD} (mV)				
		30	40	50	60	70
30	–0.78	**–0.9**	–0.9	–0.8	–0.8	–0.7
40	–1.16	–1.5	**–1.6**	–1.5	–1.4	–1.3
50	–1.62	–2.5	–2.6	**–2.7**	–2.6	–2.5
60	–2.17	–4.2	–4.8	–5.3	**–5.5**	–5.3
70	–2.84	–7.6	–10.4	–14.0	–17.5	**–19.1**

4.1.4 Comparison between the Schmitt trigger and conventional inverter under technological and process parameters variations – Analytical and simulation results

The ST has a beneficial characteristic when operating with ultralow supply voltages: it is less susceptible to variations in technological parameters than the conventional inverter [45]-[48]. This is due to the fact that, in contrast to the standard inverter, the pull-up network (PUN) of the ST is composed of both P-channel (P_0 and P_1) and N-channel (N_2) transistors (see Fig. 8). Thus, if the strength of the PMOS transistors is higher than that of the NMOS transistor, this difference is partially compensated in the pull-up circuit. The same idea is applied to the pull-down network (PDN).

Based on the analytical expressions (9)-(11), a comparison between the VTCs (with worst case envelopes) of the standard inverter and the ST inverter is shown in Fig. 55 (a)-(b), for V_{DD} = 70 mV (without hysteresis) and V_{DD} = 150 mV (with hysteresis), and ±30 mV variation in the threshold voltage of the NMOS and PMOS transistors, with $I_1/I_0 = I_2/I_0 = 1$. TT stands for typical threshold voltage, SF stands for slow (higher threshold voltage) NMOS and fast (lower threshold voltage) PMOS transistors, and FS stands for fast NMOS and slow PMOS transistors. As can be observed in the VTCs, when V_{DD} = 70 mV, the ST is appropriate for logic circuit even considering process variation, which is not the case for the conventional inverter. When V_{DD} = 150 mV, both circuits can be used as logic inverters. However, the ST is less prone to process variations and has higher static noise margin, as Section 4.1.5 shows. Figure 56 (a)-(b) presents the same results from simulations. The sizes of the simulated Schmitt triggers and inverter are given in Table IV.

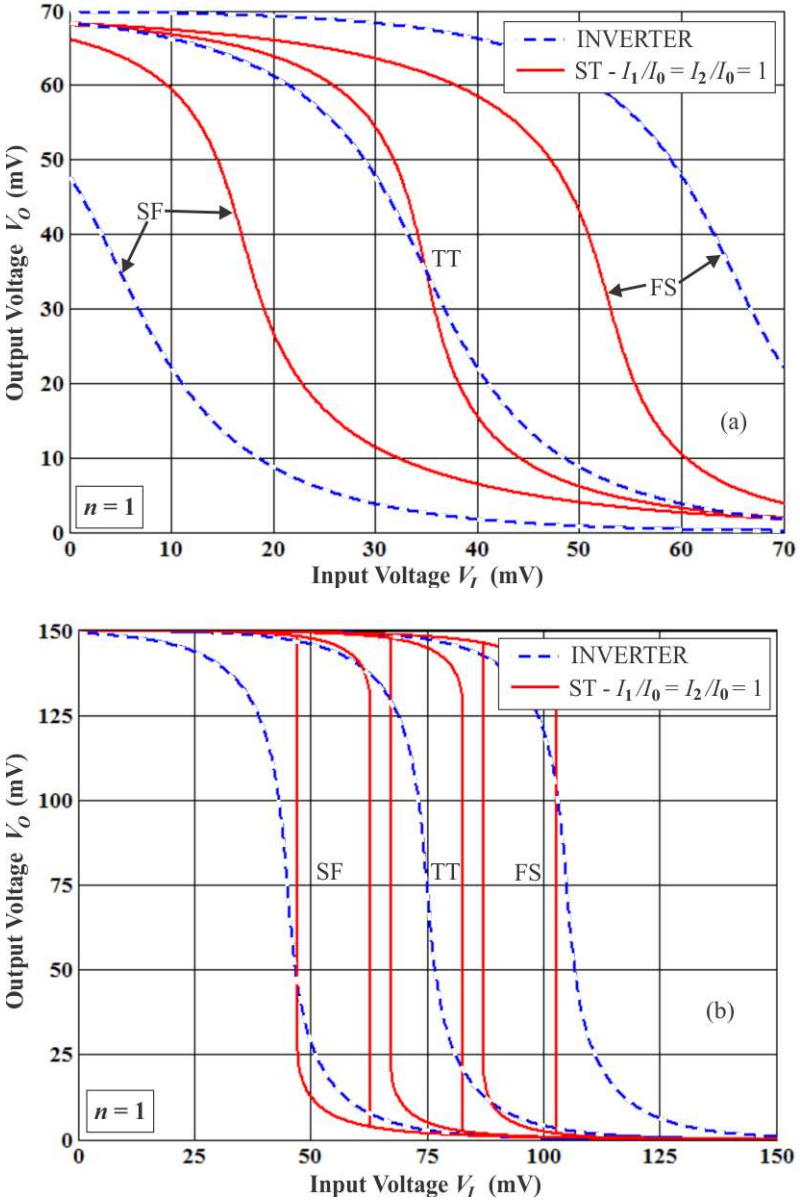


Figure 55 – Comparison of the VTCs of the standard inverter and the ST with $I_1/I_0 = I_2/I_0 = 1$, from analytical expressions, under a ±30 mV variation in the threshold voltage for: (a) $V_{DD} = 70$ mV; (b) $V_{DD} = 150$ mV.

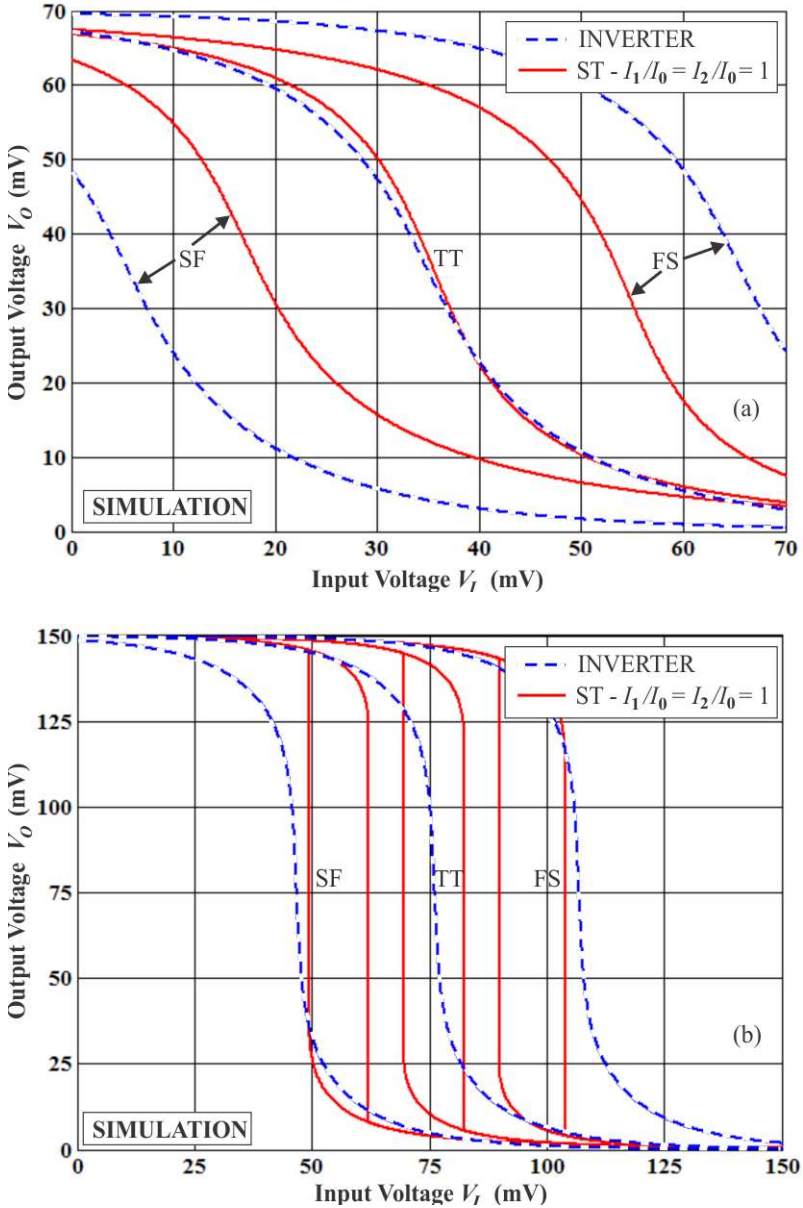


Figure 56 – Comparison of the VTCs of the standard inverter and the ST with $I_1/I_0 = I_2/I_0 = 1$, from simulation, for SF, TT, and FS corners for: (a) V_{DD} = 70 mV; (b) V_{DD} = 150 mV.

4.1.5 Comparison between the static noise margin of the Schmitt trigger and the conventional inverter

The amount of interference or noise that can be added to the input signal of a logic gate until it changes state is measured by the static noise margin, SNM. The SNM of a logic gate can be determined by the butterfly plot and is measured as the horizontal distance between the VTC and the inverted VTC (VTC^{-1}) where the gain is –1 V/V. In practice, SNM is measured as the side of the largest square that fits the VTC and the VTC^{-1}. In every butterfly plot two SNM can be measured: to keep logic level '0' and to keep logic level '1'.

Figure 57 shows a comparison of the butterfly plots of the Schmitt trigger and a standard inverter, obtained from the analytical expressions, for V_{DD} = 75 mV and n = 1.2. In this example, the ST was designed with I_1/I_0 = 0.1 and I_2/I_0 = 0.5. The higher gain of the ST obviously results in a higher SNM in both states '0' and '1', which are equal when the ST is symmetric. The ST SNM is 18.27 mV and the inverter SNM is 11.46 mV, which corresponds to a reduction of 37 %, as compared to the SNM of the ST.

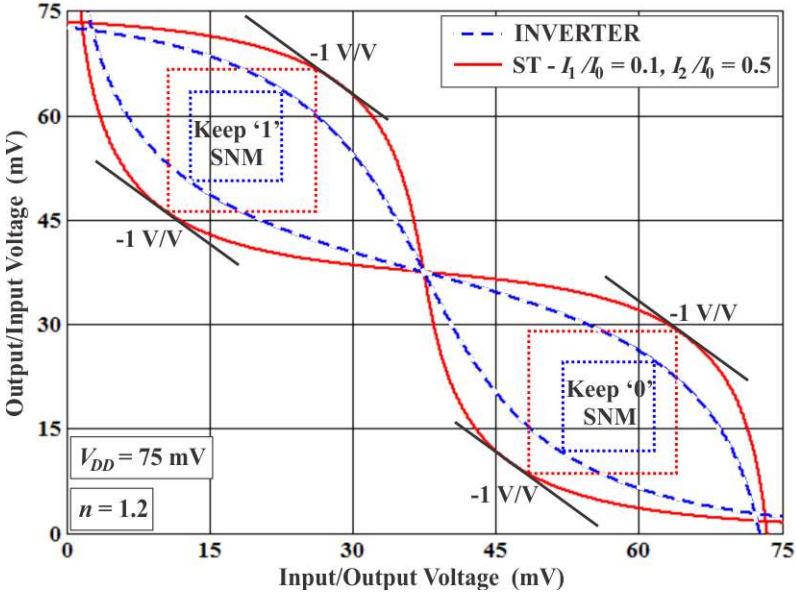


Figure 57 – Butterfly plots for the "Keep '1' SNM" and "Keep '0' SNM" states of the Schmitt trigger (I_1/I_0 = 0.1, I_2/I_0 = 0.5) and the conventional inverter for V_{DD} = 75 mV, n = 1.2.

Figures 58 and 59 show the butterfly plots of the “keep ‘1’” and “keep ‘0’” states, respectively, of the same ST and inverter of Fig. 57, for V_{DD} = 200 mV. In this case the ST presents hysteresis. As can be observed in the figures, the hysteresis in the ST increases significantly the value of the SNM. The symmetric ST with hysteresis can have a SNM higher than $V_{DD}/2$ depending on the feedback strength, whereas the conventional inverter will always present a SNM lower than $V_{DD}/2$. The ST SNM is 100.8 mV and the inverter SNM is 72.5 mV, representing a reduction of 28 %.

The higher static noise margin presented by the ST when compared to the conventional inverter is one of the main advantages of using the ST as a voltage comparator. Note that, due to PVT variations, the VTC and, consequently, the SNM can be highly degraded. However, since the ST has lower dependence on technological parameters variations if compared to the standard inverter, it will still present a better SNM under this circumstance.

The cases of very high feedback ratios, which severely degrade the VTC, will not be considered here because they have no practical use, as far as we know.

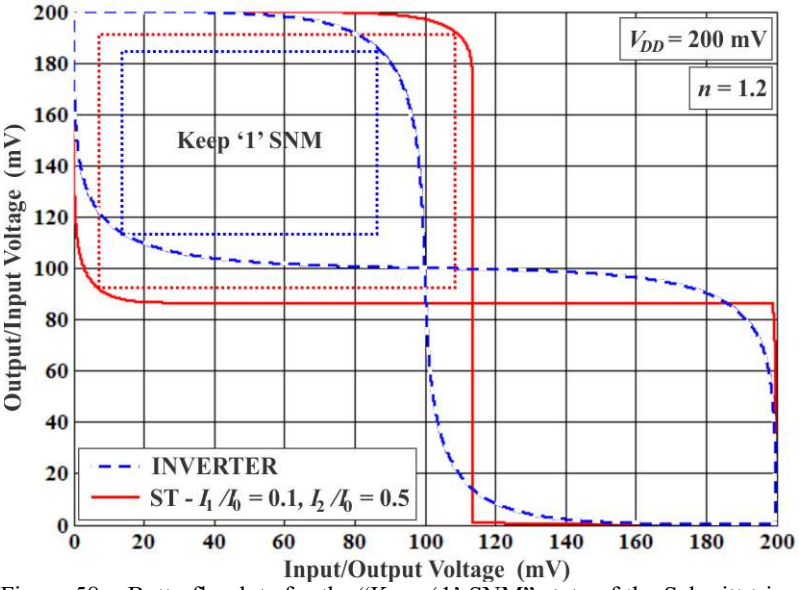


Figure 58 – Butterfly plots for the “Keep ‘1’ SNM” state of the Schmitt trigger (I_1/I_0 = 0.1, I_2/I_0 = 0.5) and the conventional inverter for V_{DD} = 200 mV, n = 1.2.

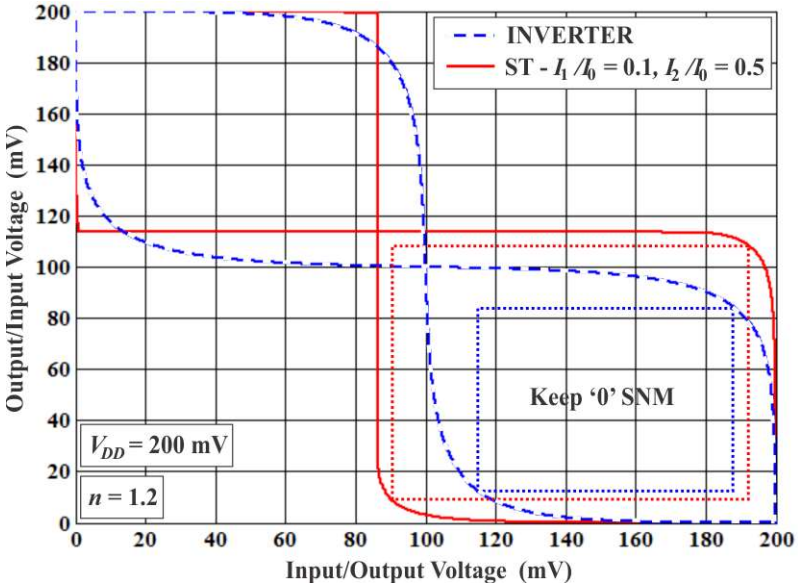


Figure 59 – Butterfly plots for the "Keep '0' SNM" state of the Schmitt trigger (I_1/I_0 = 0.1, I_2/I_0 = 0.5) and the conventional inverter for V_{DD} = 200 mV, n = 1.2.

4.1.6 Dynamic analysis of the Schmitt trigger – Transient response

The sharp transition shown in the VTC of the ST with hysteresis, for example in Fig. 11, is inherently a dynamic phenomenon [25],[26]. As soon as the input voltage crosses the hysteresis limit the output current starts to flow and charges the output node, just to the value of V_O at which the output current becomes zero again.

To illustrate the dynamics of the ST with $I_1/I_0 = I_2/I_0 = 1$, having as the load an identical ST, Fig. 60 shows the simulated transient response to an input step voltage. For V_{DD} = 150 mV, the hysteresis low and high limits are 69.5 mV and 82.3 mV, respectively, and these are very close to the measured limits of 70 mV and 79 mV, respectively, as shown in Fig. 35. The step input in Fig. 60 (a) changes from 70 mV to 69 mV while the output node is initially charged to 20 mV. A step input of –1 mV is sufficient to force a transition in the output voltage from 20 mV to approximately V_{DD}. Initially, the current that charges the output capacitor is low, since the drive input voltage is only 69 mV and very close to one of the metastable points. However, it increases to an absolute maximum value of I_{OUT} = –35 pA (absolute maximum measured I_{OUT} = –26 pA as shown in Fig. 34 for V_I = 69 mV). The

resulting rise time is approximately 3 ms. The same analysis can be carried out for a falling transition of the output with input voltages from 81.8 mV to 82.8 mV.

When the step changes from 150 mV to 0 mV, the drive current is high and the rise time lowers to approximately 400 µs, as can be noted in Fig. 60 (b).

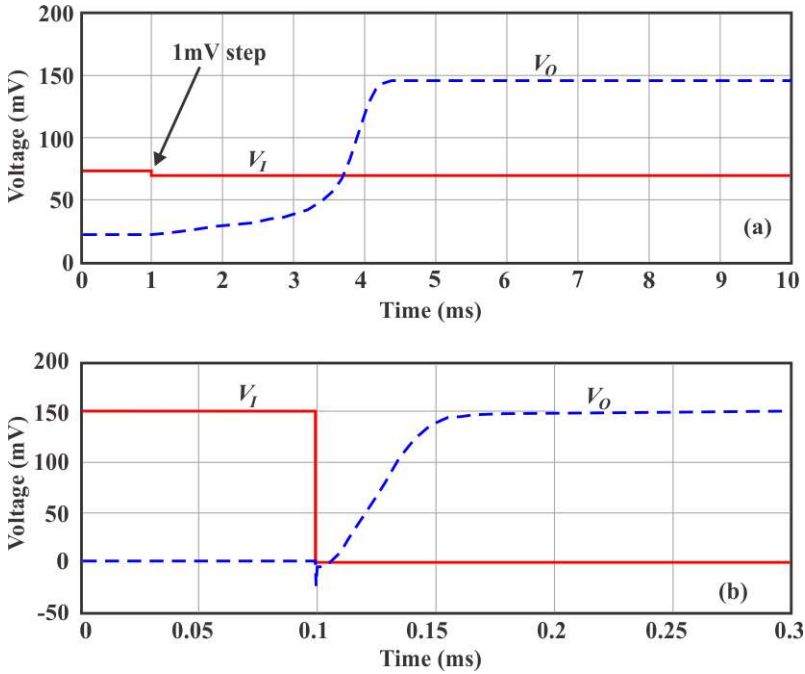


Figure 60 – Simulated transient time of the ST with $I_1/I_0 = I_2/I_0 = 1$, for V_{DD} = 150 mV, for: (a) 1 mV input step; (b) 150 mV input step.

For a step input between GND and V_{DD}, the rise (T_{LH}) and the fall times (T_{HL}) of the output voltage can be solved from

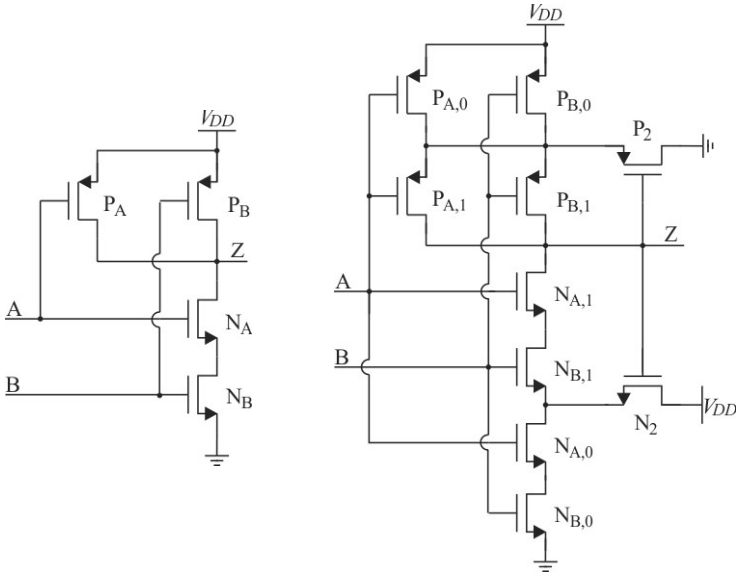
$$-I_{OUT} = C_O \cdot \frac{dV_O}{dt}. \tag{42}$$

The lengthy expression for $T_{HL(LH)}$, resulted from (42), is given in Appendix G.

4.2 LOGIC FAMILIES WITH THE SCHMITT TRIGGER

As shown previously, the Schmitt trigger inverter has many advantages if compared to the conventional inverter for the implementation of low-voltage digital circuits. To expand these advantages to other more complex circuits such as NAND and NOR gates, the presence of an internal node within the NMOS and PMOS blocks is of great importance. The solution for the Schmitt trigger NAND (ST-NAND) and NOR (ST-NOR) gates is to substitute the series NMOS and PMOS transistors with the corresponding gate function, as was done in reference [39].

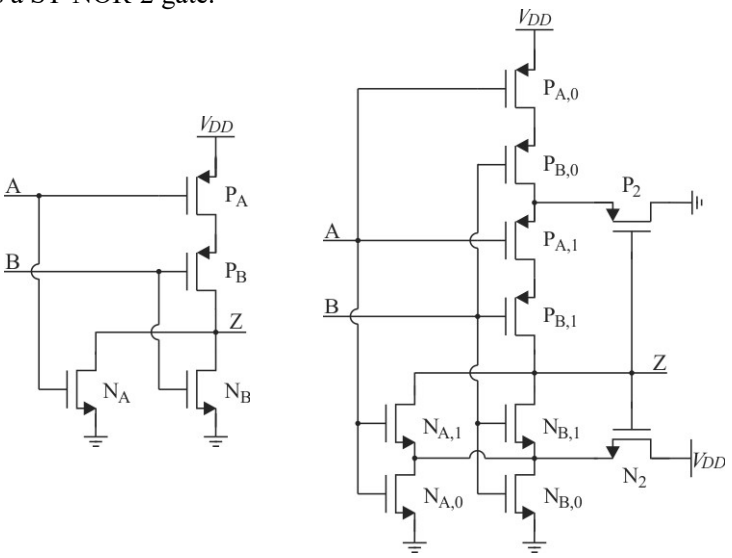
The ST-NAND-2 gate, with two inputs, say A and B, derived from the conventional NAND-2 gate, in Fig. 61 (a), is shown in Fig. 61 (b). Note that each transistor of the conventional NAND-2 gate is replaced by two transistors in the case of the ST-NAND-2 gate. For example, P_A transistor from the NAND-2 gate is replaced by $P_{A,0}$ and $P_{A,1}$ in the ST-NAND-2 gate, and so on. However, only one transistor is responsible for the feedback in the PUN and another one in the PDN.



(a) (b)

Figure 61 – (a) Conventional NAND-2 gate; (b) ST-NAND-2 gate.

Figure 62 (a) shows a conventional NOR-2 gate, while Fig. 62 (b) shows a ST-NOR-2 gate.



(a) (b)

Figure 62 – (a) Conventional NOR-2 gate; (b) ST-NOR-2 gate.

The output of the ST-NAND-2 gate changes states in one of the following events. In the first case, one of the inputs, *e.g.*, V_A, changes whereas the other input is held constant at (or close to) V_{DD}. In the second case, both inputs vary simultaneously, i.e., $V_A \equiv V_B$. In this case, the logic gate is equivalent to an ST inverter with series and parallel association of transistors as will be explained in the next paragraph.

Considering a ST-NAND-2 gate derived from a ST inverter with $I_1/I_0 = I_2/I_0 = 1$ (the p-channel transistors have the same strength, and the n-channel transistors have the same strength), the equivalent circuits when only one input varies or when both inputs vary together are shown in Fig. 63 (a) and (b), respectively. Note that the circuit of Fig. 63 (a) is equivalent to a symmetric ST, while that of Fig. 63 (b) is not. Thus, equations (9)-(11) cannot be used; equations (5), (6) and (8) must be used instead. From Fig. 63 (a), the equivalent transistors strengths are $I_{N0} = I_{P0} = 1$, $I_{N1} = I_{P1} = 1$, $I_{N2} = I_{P2} = 1$, while from Fig. 63 (b), the equivalent transistors strengths are $I_{P0} = I_{P1} = 2$, $I_{P2} = 1$, $I_{N0} = I_{N1} = 0.5$, $I_{N2} = 1$. The VTCs of the ST-NAND-2 when only one input varies and when both inputs vary together are shown in Fig. 64 for $V_{DD} = 150$ mV (with hysteresis), and $V_{DD} = 75$ mV (without hysteresis).

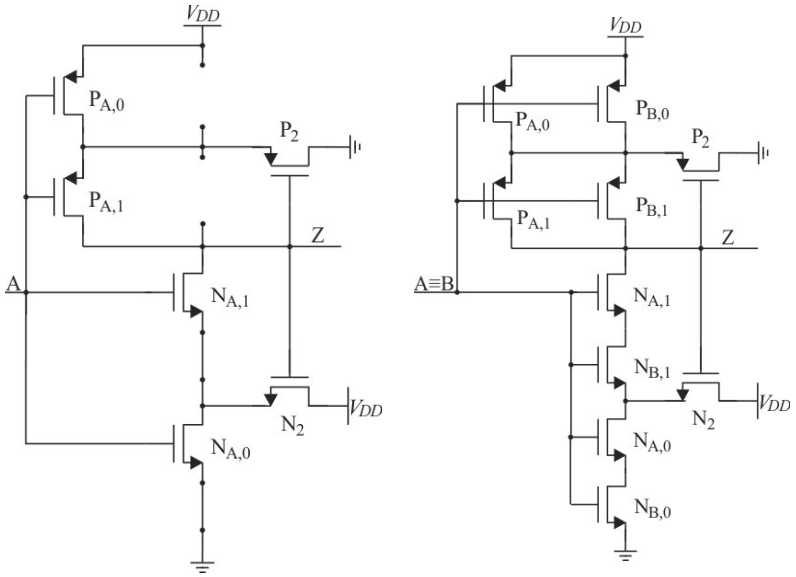


Figure 63 – ST-NAND-2 equivalent circuits when (a) only one input varies; (b) both inputs vary together.

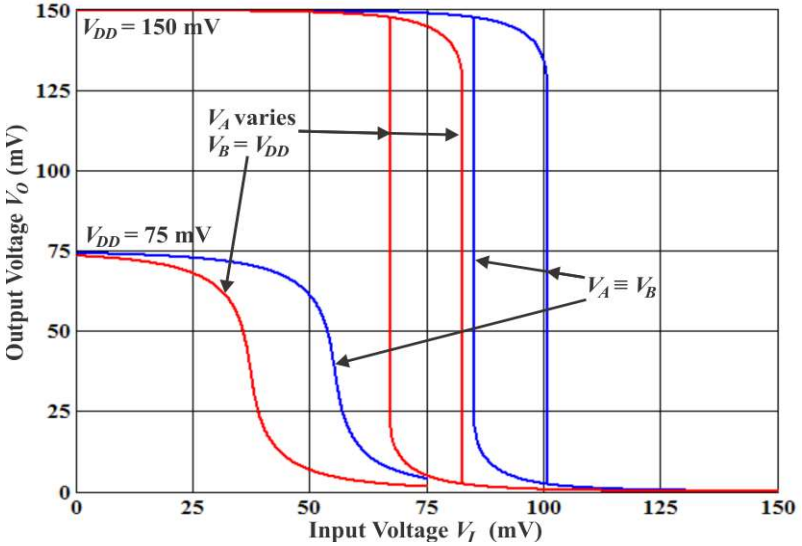


Figure 64 – ST-NAND-2 VTC when only one input varies and when both inputs vary together, from analytical expressions, for V_{DD} = 75 mV and 150 mV, and n = 1.

Note from Fig. 64 that when only one input varies, the VTC is perfectly centered at $V_{DD}/2$. However, when both inputs vary together, $V_A \equiv V_B$, the VTC is shifted to the right (NOR gates shift to the left) [33],[76]-[77], *i.e.*, the VTC varies according to the input pattern. The VTC will be shifted away from $V_{DD}/2$ according to the number of inputs; thus, for ULV operation logic gates with more than 2 inputs are highly undesirable [39]. Figure 65 shows the VTC of a 3-input ST-NAND gate for illustration. This situation is even worse under PVT variations (see Section 4.1.4 for comparison). Although the strong limitation of a logic library with gates with only one or two inputs, it is clearly advantageous for V_{DD} minimization. On the other hand, it may increase the total number of logic gates necessary for the design of a complete system, resulting in increased area and leakage currents. So, its usefulness is application dependent [39].

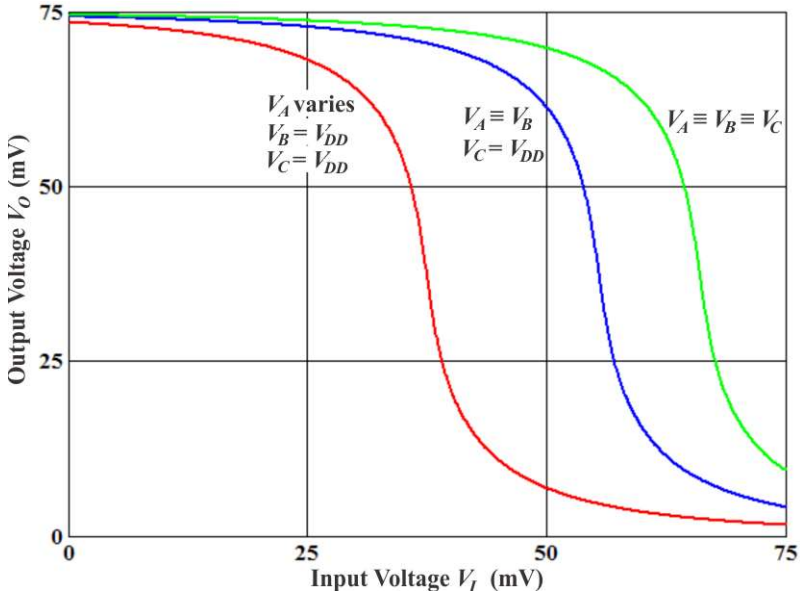


Figure 65 – ST-NAND-3 VTC when only one input varies, and when two and three inputs vary together, from analytical expressions, for V_{DD} = 75 mV, n = 1.

The total number of transistors in a ST gate is $4m+2$, where m is the number of inputs [70]. This is one of the main drawbacks of Schmitt trigger-based logic gates. While a 2-input NAND gate has only 4 transistors, the ST-NAND gate with the same number of inputs has 10 transistors. Even worse, a 3-input NAND gate has 6 transistors, while a

3-input ST-NAND gate has 14 transistors. Considering that a Schmitt trigger-based logic gate is derived from the Schmitt trigger inverter, with $I_1/I_0 \approx 0$ (or $I_1 << I_0$, $I_2 >> I_1$), the area occupied by the ST gate tends to be much bigger than that of a conventional gate.

4.3 RING OSCILLATOR WITH THE SCHMITT TRIGGER

In order to compare the frequency response of the ST with that of the inverter, two ST-based (one with $I_1/I_0 = I_2/I_0 = 1$ and another with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$), Fig. 66 (a), and one inverter-based, Fig. 66 (b), 3-stage ring oscillators (ROs) were simulated. C_O represents the node capacitance. The Schmitt triggers and inverter dimensions are shown in Table VI (note that unit transistors were used in parallel). As expected, the operating frequency of the ST-based RO at a fixed supply voltage is lower than that of the inverter-based RO, because the ratio of the current drive capability to the node capacitance is smaller for the ST than for the standard inverter. The output node of the ST-based RO must charge and discharge the input capacitance of the next stage, which is composed of four transistors (P_0, P_1, N_0 and N_1 in Fig. 9), and its own capacitance, which is composed of two transistors (P_2 and N_2 in Fig. 9). Yet, the drive capability of the ST is lower than that of the inverter, since the ST has two series transistors to charge (P_0 and P_1) and discharge (N_0 and N_1) the output node.

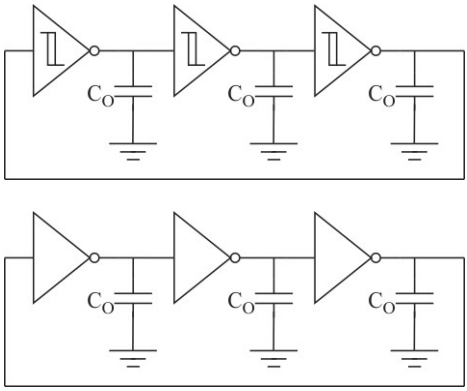


Figure 66 – 3-stage ring oscillators: (a) ST-based; (b) inverter-based.

TABLE VI – Schmitt trigger and inverter transistor aspect ratios of the 3-stage ring oscillators.

Inverter	$\left(\frac{W}{L}\right)_P = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_N = \frac{1.08\mu m}{1.08\mu m}$
ST $I_1/I_0 = 1$ $I_2/I_0 = 1$	$\left(\frac{W}{L}\right)_{P0} = \left(\frac{W}{L}\right)_{P1} = \left(\frac{W}{L}\right)_{P2} = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N0} = \left(\frac{W}{L}\right)_{N1} = \left(\frac{W}{L}\right)_{N2} = \frac{1.08\mu m}{1.08\mu m}$
ST $I_1/I_0 = 0.1$ $I_2/I_0 = 1$	$\left(\frac{W}{L}\right)_{P0} = \left(\frac{W}{L}\right)_{P2} = 10\times\frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{P1} = \frac{14\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N0} = \left(\frac{W}{L}\right)_{N2} = 10\times\frac{1.08\mu m}{1.08\mu m}$ $\left(\frac{W}{L}\right)_{N1} = \frac{1.08\mu m}{1.08\mu m}$

Figure 67 shows the output voltage waveform of each ring oscillator for V_{DD} = 70 mV. Note that, due to the reduced supply voltage, the output voltage swing is also reduced. The output voltage swing of the circuits are 43.36 mVpp in the case of the inverter-based RO, 51.61 mVpp in the case of the ST-based RO with $I_1/I_0 = I_2/I_0 = 1$ and 54.34 mVpp in the case of the ST-based RO with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$.

Figure 68 shows a comparison between the oscillation frequencies of the ST and the inverter-based ring oscillators as a function of the supply voltage. Below 70 mV of supply voltage, both the ST with $I_1/I_0 = I_2/I_0 = 1$ and the inverter-based ROs do not oscillate due to the low voltage gain. However, the RO composed of the ST with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$ oscillates at a supply voltage as low as 57 mV, even though the frequency is extremely low (113 Hz). We have limited the abscissa in Fig. 67 to V_{DD} = 150 mV, because for higher supply voltages the STs present hysteresis. In Fig. 68, it can be seen that the oscillation frequency of the inverter-based RO is around 5.5 times higher than that of the ST-based RO with $I_1/I_0 = I_2/I_0 = 1$, and 19.6 times higher if compared to the ST-based RO with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$.

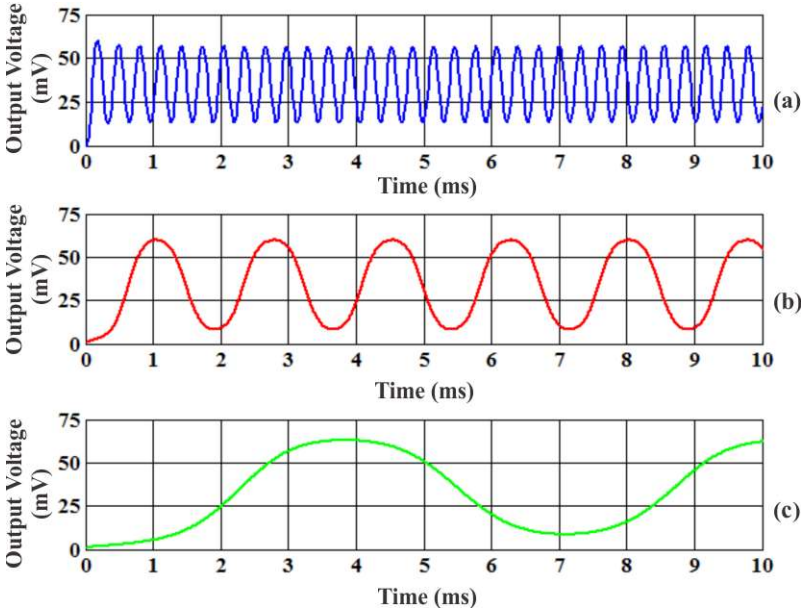


Figure 67 – Output voltage of the 3-stage ring oscillators, with V_{DD} = 70 mV: (a) inverter-based; (b) ST-based I_1/I_0=I_2/I_0 =1; (c) ST-based I_1/I_0 = 0.1, I_2/I_0 = 1.

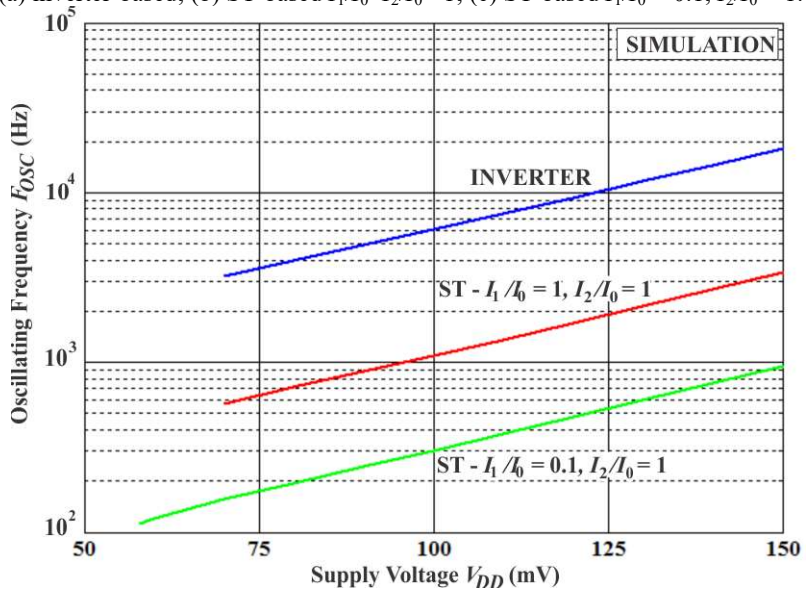


Figure 68 – Comparison between the oscillation frequencies of the simulated STs and inverter based 3-stage ring oscillators.

5 CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

In this thesis, the operation of the CMOS Schmitt trigger has been fully analyzed in weak inversion.

If compared to the conventional CMOS inverter, the ST has many advantages for applications targeting ultralow voltage. The first one is that the presence of hysteresis results in a simple circuit that can be used as a dual-threshold comparator with good efficiency to noise present in the input signal. At the same time, its power consumption is considerably lower than OP-AMP-based comparators, since it is a much simpler circuit.

The second advantage of the ST is that its voltage gain is much higher than that of the standard inverter when no hysteresis is present. Optimal transistors ratios result in considerable higher voltage gains if compared to the standard inverter. However, the drawback is that the area occupied by the ST tends to be much greater than that of the standard inverter. As a consequence, the operating frequency is lower for the same supply voltage. At considerable high supply voltage and when hysteresis is desired, the size of the transistors tends to be lower. So, the occupied area of the ST tends to be similar to that of the conventional inverter. At the same time, the operating frequency of the ST tends to be closer to that of the conventional inverter, although still lower due to the higher number of transistors in the ST.

In both cases when hysteresis is present or not, the static noise margin of the Schmitt trigger is higher than that of the conventional inverter. When hysteresis is present, and depending on the feedback ratio, which determines the hysteresis width, the SNM can be even higher than $V_{DD}/2$, which is not the case for the inverter. This result is of paramount importance because in ultralow voltage operation the noise present in the circuits tends to disturb its operation.

Additionally, a very important fact is that the ST is less prone to PVT variations. Even in the presence of PVT variations the VTC of the ST is well defined and it can work as an inverter circuit even for very low supply voltages.

Finally, the optimized ST is theoretically capable of operating at a supply voltage that is slightly lower than that of the standard inverter, which was regarded as the *fundamental limit*. The optimized ST is theoretically capable of operating at a supply voltage as low as 31.5 mV, while the standard inverter works at 36 mV of minimum supply voltage.

This remarkable result is very important because it sets a new limit for the lower bound of the supply voltage of ultralow-voltage circuits and reopens the quest for new ultralow voltage circuits and topologies.

5.2 FUTURE WORK

For future work we suggest:

- **Apply body-bias compensation to the Schmitt trigger inverter.** The usefulness of body bias compensation techniques has been proved in many different applications, mainly with standard CMOS logic. This thesis dealt with the analysis of the Schmitt trigger and showed that is presents lower dependence of PVT variations. Although good results have been achieved, applying both forward and reverse body bias techniques to the ST may increase its operating frequency, may reduce even more the dependence on PVT variations and may operate closer to the minimum supply voltage.

- **Development of a Schmitt trigger based logic family.** Although some results regarding the NAND and NOR gates based on the ST have been presented here, these gates still need further simulations and verification with real world measurements. With that, a complete logic family composed of the ST inverter, NAND and NOR gates, a latch and a flip-flop can be proposed for operation with supply voltages in the range of 50-100 mV.

- **Study of the Schmitt trigger-based SRAM**. The proposed SRAM based on the Schmitt trigger in [37] and [38] works appropriately at a supply voltage as low as 150 mV. However, the lack of feedback in the PMOS network of the ST may affect its operation; the authors state that the PMOS degeneration is good, but it actually decreases the gain of the ST and, consequently, the SNM. So, we propose the study of the SRAM based on the 6T Schmitt trigger inverter. From the experience acquired in the current work we think that a SRAM

composed of a well designed Schmitt trigger is capable of operating at supply voltages as low as 50-60 mV, with no post-silicon improvements such as charge injection for threshold voltage compensation or body biasing techniques.

- **Development of an ultralow voltage microprocessor.** To fully verify the effectiveness of the Schmitt trigger logic family and SRAM, we suggest the development of a simple microprocessor intended for sensor applications supplied by an energy harvesting source. The microprocessor can be similar to the Phoenix processor showed in [15], operating with a supply voltage as low as possible, with only a few instructions.

APPENDIX A – SCHMITT TRIGGER VOLTAGE TRANSFER CHARACTERISTIC

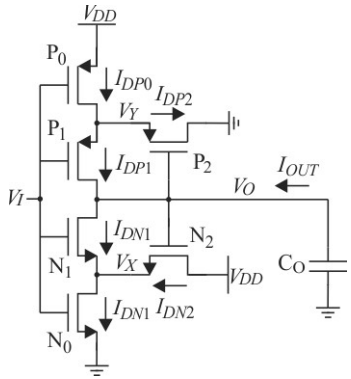


Figure 69 – Classical 6-transistor Schmitt trigger currents and voltages.

The classical 6-transistor Schmitt trigger from Fig. 9 is reproduced in Fig. 69 for the sake of clarity.

The DC equation for node V_X is determined from KCL:

$$I_{DN0} = I_{DN1} + I_{DN2}\,. \tag{A1}$$

Calculating the currents I_{DN0}, I_{DN1}, and I_{DN2} from (1) results in

$$I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}\cdot\left(1-e^{-\frac{V_X}{\phi_t}}\right) = I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}\cdot\left(e^{-\frac{V_X}{\phi_t}}-e^{-\frac{V_O}{\phi_t}}\right)+ \\ + I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}}\cdot\left(e^{-\frac{V_X}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}\right). \tag{A2}$$

$$I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}} - I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}-\frac{V_X}{\phi_t}} = I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}-\frac{V_X}{\phi_t}} - I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}-\frac{V_O}{\phi_t}} + \\ + I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}-\frac{V_X}{\phi_t}} - I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}-\frac{V_{DD}}{\phi_t}} \tag{A3}$$

$$I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}-\frac{V_O}{\phi_t}}+I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}=$$
$$=e^{-\frac{V_X}{\phi_t}}\cdot\left(I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}}\right) \quad \text{(A4)}$$

$$e^{-\frac{V_X}{\phi_t}}=\frac{I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}-\frac{V_O}{\phi_t}}+I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}}{I_{N0}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}+I_{N2}\cdot e^{\frac{V_O}{n_N\cdot\phi_t}}} \quad \text{(A5)}$$

Finally, rearranging (A5) for V_X, results in

$$e^{\frac{V_X}{\phi_t}}=\frac{I_{N0}+I_{N1}+I_{N2}\cdot e^{\frac{V_O-V_I}{n_N\cdot\phi_t}}}{I_{N0}+I_{N1}\cdot e^{-\frac{V_O}{\phi_t}}+I_{N2}\cdot e^{\frac{V_O-V_I}{n_N\cdot\phi_t}}\cdot e^{-\frac{V_{DD}}{\phi_t}}}. \quad \text{(A6)}$$

Similarly, the KCL for node V_Y is

$$I_{DP0}=I_{DP1}+I_{DP2} \quad \text{(A7)}$$

Calculating the currents I_{DP0}, I_{DP1}, and I_{DP2} from (1) results in

$$I_{P0}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}}\cdot\left(1-e^{-\frac{V_{DD}-V_Y}{\phi_t}}\right)=I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}}\cdot\left(e^{-\frac{V_{DD}-V_Y}{\phi_t}}-e^{-\frac{V_{DD}-V_O}{\phi_t}}\right)+$$
$$+I_{P2}\cdot e^{\frac{V_{DD}-V_O}{n_P\cdot\phi_t}}\cdot\left(e^{-\frac{V_{DD}-V_Y}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}\right) \quad \text{(A8)}$$

$$I_{P0}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}}-I_{P0}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}+\frac{V_I-V_{DD}}{\phi_t}}=I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}+\frac{V_Y-V_{DD}}{\phi_t}}-$$
$$-I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}+\frac{V_O-V_{DD}}{\phi_t}}+I_{P2}\cdot e^{\frac{V_{DD}-V_O}{n_P\cdot\phi_t}+\frac{V_Y-V_{DD}}{\phi_t}}-I_{P2}\cdot e^{\frac{V_{DD}-V_O}{n_P\cdot\phi_t}-\frac{V_{DD}}{\phi_t}} \quad \text{(A9)}$$

$$I_{P0}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}}+I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}+\frac{V_O-V_{DD}}{\phi_t}}+I_{P2}\cdot e^{\frac{V_{DD}-V_O}{n_P\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}=$$
$$=e^{\frac{V_Y}{\phi_t}}\cdot\left(I_{P0}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}+I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}+I_{P2}\cdot e^{\frac{V_{DD}-V_O}{n_P\cdot\phi_t}-\frac{V_{DD}}{\phi_t}}\right) \quad \text{(A10)}$$

Finally, multiplying both sides of (A10) by $e^{\frac{V_I-V_{DD}}{n_P\cdot\phi_t}+\frac{V_{DD}}{\phi_t}}$ and rearranging for V_Y, results in

$$e^{\frac{V_Y}{\phi_t}}=\frac{I_{P0}\cdot e^{\frac{V_{DD}}{\phi_t}}+I_{P1}\cdot e^{\frac{V_O}{\phi_t}}+I_{P2}\cdot e^{\frac{V_I-V_O}{n_P\cdot\phi_t}}}{I_{P0}+I_{P1}+I_{P2}\cdot e^{\frac{V_I-V_O}{n_P\cdot\phi_t}}} \quad \text{(A11)}$$

At the same time, the KCL for node V_O, with unloaded ST (I_{OUT} =0), is

$$I_{DN1}=I_{DP1}. \quad \text{(A12)}$$

Substituting the values of I_{DN1} and I_{DP1} from (1) into (A12), results in

$$I_{N1}\cdot e^{\frac{V_I}{n_N\cdot\phi_t}}\cdot\left(e^{-\frac{V_X}{\phi_t}}-e^{-\frac{V_O}{\phi_t}}\right)=I_{P1}\cdot e^{\frac{V_{DD}-V_I}{n_P\cdot\phi_t}}\cdot\left(e^{-\frac{V_{DD}-V_Y}{\phi_t}}-e^{-\frac{V_{DD}-V_O}{\phi_t}}\right). \quad \text{(A13)}$$

Rearranging (A13), results in

$$e^{\frac{V_I-n_N\cdot V_X}{n_N\cdot\phi_t}}-e^{\frac{V_I-n_N\cdot V_O}{n_N\cdot\phi_t}}=\frac{I_{P1}}{I_{N1}}\cdot e^{\frac{V_{DD}\cdot(1-n_P)}{n_P\cdot\phi_t}}\cdot\left(e^{\frac{-V_I+n_P\cdot V_Y}{n_P\cdot\phi_t}}-e^{\frac{-V_I+n_P\cdot V_O}{n_P\cdot\phi_t}}\right). \quad \text{(A14)}$$

APPENDIX B – THE VOLTAGE TRANSFER CHARACTERISTIC AS A 4TH DEGREE EQUATION

Equations (9) and (10) can be substituted into equation (11) to find the output voltage V_O in terms of the input voltage V_I, with V_{DD}, I_0, I_1, and I_2 as parameters. The result is an equation of the fourth degree in terms of e^{V_O/ϕ_t} and e^{V_I/ϕ_t}, as shown below:

$$e^{4\frac{V_O}{\phi_t}} \cdot c_4 + e^{3\frac{V_O}{\phi_t}} \cdot c_3 + e^{2\frac{V_O}{\phi_t}} \cdot c_2 + e^{\frac{V_O}{\phi_t}} \cdot c_1 + c_0 = 0 \tag{B1}$$

$$c_4 = -I_2 \cdot e^{-\frac{V_I}{\phi_t}}$$

$$c_3 = I_2 \cdot \left(e^{\frac{V_{DD}-V_I}{\phi_t}} - e^{\frac{V_I-V_{DD}}{\phi_t}} \right) - I_1 - I_0 - \frac{I_2^2}{I_0} - \frac{I_1 \cdot I_2}{I_0} \cdot e^{\frac{V_I-V_{DD}}{\phi_t}}$$

$$c_2 = (I_0 + I_1) \cdot e^{\frac{V_{DD}}{\phi_t}} + \frac{I_2^2}{I_0} - \frac{I_2}{I_0} \cdot (I_0 + I_1) \cdot e^{\frac{V_I}{\phi_t}} - (I_0 + I_1) \cdot e^{2\frac{V_I}{\phi_t}} -$$
$$- \frac{I_2^2}{I_0} \cdot e^{\frac{2V_I-V_{DD}}{\phi_t}} + \frac{I_2}{I_0} \cdot (I_0 + I_1) \cdot e^{\frac{V_I}{\phi_t}}$$

$$c_1 = \frac{I_2}{I_0} \cdot (I_0 + I_1) \cdot e^{\frac{V_I}{\phi_t}} - \frac{I_1}{I_0} \cdot (I_0 + I_1) \cdot e^{2\frac{V_I}{\phi_t}} - I_2 \cdot e^{3\frac{V_I}{\phi_t}} +$$
$$+ \frac{(I_0 + I_1)^2}{I_0} \cdot e^{2\frac{V_I}{\phi_t}} + \frac{I_2^2}{I_0} \cdot e^{2\frac{V_I}{\phi_t}}$$

$$c_0 = -\frac{I_2 \cdot (I_0 + 2 \cdot I_1)}{I_0} \cdot e^{3\frac{V_I}{\phi_t}} \tag{B2}$$

Coefficients c_4, c_3, c_2, c_1, and c_0 in (B2) depend solely on V_{DD}, I_0, I_1, and I_2. Equation (B1) can be solved using Ferrari´s method for quartic functions. If the input voltage is outside the hysteresis limits,

three solutions are always negative in terms of e^{V_O/ϕ_t}, which results in complex values of V_O, without physical meaning; there is only one valid stable operating point for V_O. However, when the input voltage is between the hysteresis voltage limits, the equation results in three valid solutions, one of which represents a metastable operating point. The other two solutions are stable operating points. For example, in Fig. 11 the circles represent stable points, for some input voltages. As the ST is symmetrical, $V_I=V_O=V_{DD}/2$ is always a solution of equation (B1), either stable (for V_{DD} = 60 mV) or metastable (for V_{DD} = 150 mV, not shown in Fig. 11) operating point.

For example, calculating the solutions of equation (B1), with $I_0 = I_1 = I_2 = 1$ nA, for V_{DD} = 150 mV, we have:

a) For V_I = 60 mV (outside the hysteresis voltage limits):
   V_{O1} = 0.096 + 0.026j – has no physical meaning
   V_{O2} = 0.072 + 0.082j – has no physical meaning
   V_{O3} = 0.148 – is a stable solution
   V_{O4} = 0.096 – 0.026j – has no physical meaning

b) For V_I = 67.24 mV (at the hysteresis voltage limit):
   V_{O1} = 0.023 – is a stable solution
   V_{O2} = 0.074 + 0.081j – has no physical meaning
   V_{O3} = 0.147 – is a stable solution
   V_{O4} = 0.023 – is a metastable solution

c) For V_I = 75 mV (between hysteresis voltage limits):
   V_{O1} = 0.005 – is a stable solution
   V_{O2} = 0.075 + 0.081j – has no physical meaning
   V_{O3} = 0.144 – is a stable solution
   V_{O4} = 0.075 – is a metastable solution

d) For V_I = 85 mV (outside the hysteresis voltage limits):
   V_{O1} = 0.002 – is a stable solution
   V_{O2} = 0.075 + 0.081j – has no physical meaning
   V_{O3} = 0.131 + 0.015j – has no physical meaning
   V_{O4} = 0.131 – 0.015j – has no physical meaning

For V_{DD} = 60 mV, with $I_0 = I_1 = I_2$ = 1 nA, we have:

a) For V_I = 20 mV:
V_{O1} = – 0.001 + 0.049j – has no physical meaning
V_{O2} = 0.032 + 0.082j – has no physical meaning
V_{O3} = 0.050 – is a stable solution
V_{O4} = 0.001 – 0.049j – has no physical meaning

b) For V_I = 30 mV:
V_{O1} = 0.029 + 0.047j – has no physical meaning
V_{O2} = 0.029 – 0.047j – has no physical meaning
V_{O3} = 0.030 – is a stable solution
V_{O4} = 0.029 + 0.081j – is a metastable solution

c) For V_I = 40 mV:
V_{O1} = 0.061 + 0.049j – has no physical meaning
V_{O2} = 0.060 – 0.049j – has no physical meaning
V_{O3} = 0.010 – is a stable solution
V_{O4} = 0.027 + 0.082j – has no physical meaning

APPENDIX C – DERIVATION OF THE OUTPUT STABLE POINTS OF THE SCHMITT TRIGGER-BASED LATCH

Considering a latch composed of two symmetrical STs, with $n = n_N = n_P$, and the butterfly plot of the ST from Fig. 13, V_I and V_O can be written as

$$V_I = V_{Low} = \frac{V_{DD}}{2} - \varepsilon \;\rightarrow\; V_O = V_{High} = \frac{V_{DD}}{2} + \varepsilon\,, \tag{C1}$$

or

$$V_I = V_{High} = \frac{V_{DD}}{2} + \varepsilon \;\rightarrow\; V_O = V_{Low} = \frac{V_{DD}}{2} - \varepsilon\,. \tag{C2}$$

Applying (C1) into (5) and (6), respectively, results

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{2\varepsilon}{n}}}{I_0 + I_1 \cdot e^{-\frac{V_{DD}}{2\phi_t} - \varepsilon} + I_2 \cdot e^{\frac{2\varepsilon}{n}} \cdot e^{-\frac{V_{DD}}{\phi_t}}}, \tag{C3}$$

and

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_{DD}}{2\phi_t} + \varepsilon} + I_2 \cdot e^{-\frac{2\varepsilon}{n}}}{I_0 + I_1 + I_2 \cdot e^{-\frac{2\varepsilon}{n}}}. \tag{C4}$$

Substituting (C3) and (C4) into (8) results

$$\begin{aligned} & e^{\frac{V_{DD}}{n\cdot\phi_t} - \frac{2\varepsilon}{n}} \cdot \left(\frac{I_0 + I_1 \cdot e^{-\frac{V_{DD}}{2\phi_t} - \varepsilon} + I_2 \cdot e^{\frac{2\varepsilon}{n}} \cdot e^{-\frac{V_{DD}}{\phi_t}}}{I_0 + I_1 + I_2 \cdot e^{\frac{2\varepsilon}{n}}} - e^{-\frac{V_{DD}}{2n\cdot\phi_t} - \varepsilon} \right) = \\ & = e^{\frac{V_{DD}}{\phi_t}\left(\frac{1}{n} - 1\right)} \cdot \left(\frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_{DD}}{2\phi_t} + \varepsilon} + I_2 \cdot e^{-\frac{2\varepsilon}{n}}}{I_0 + I_1 + I_2 \cdot e^{-\frac{2\varepsilon}{n}}} - e^{\frac{V_{DD}}{2n\cdot\phi_t} + \varepsilon} \right) \end{aligned} \tag{C5}$$

$$e^{\frac{V_{DD}}{n\cdot\phi_t}-\frac{2\varepsilon}{n}}\left[\left(I_0+I_1\cdot e^{-\frac{V_{DD}}{2\phi_t}-\varepsilon}+I_2\cdot e^{\frac{2\varepsilon}{n}}\cdot e^{-\frac{V_{DD}}{\phi_t}}\right)\left(I_0+I_1+I_2\cdot e^{-\frac{2\varepsilon}{n}}\right)\right]-$$
$$-e^{\frac{V_{DD}}{n\cdot\phi_t}-\frac{2\varepsilon}{n}}\cdot e^{-\frac{V_{DD}}{2n\cdot\phi_t}-\varepsilon}\cdot\left(I_0+I_1+I_2\cdot e^{\frac{2\varepsilon}{n}}\right)\cdot\left(I_0+I_1+I_2\cdot e^{-\frac{2\varepsilon}{n}}\right)=$$
$$=\left(I_0\cdot e^{\frac{V_{DD}}{\phi_t}}+I_1\cdot e^{\frac{V_{DD}}{2\phi_t}+\varepsilon}+I_2\cdot e^{-\frac{2\varepsilon}{n}}\right)\cdot\left(I_0+I_1+I_2\cdot e^{\frac{2\varepsilon}{n}}\right)-$$
$$-e^{\frac{V_{DD}}{2n\cdot\phi_t}+\varepsilon}\cdot\left(I_0+I_1+I_2\cdot e^{\frac{2\varepsilon}{n}}\right)\cdot\left(I_0+I_1+I_2\cdot e^{-\frac{2\varepsilon}{n}}\right) \tag{C6}$$

Expanding and rearranging (C6), results in:

$$\left[e^{-\varepsilon\cdot\left(1+\frac{3}{n}\right)}-e^{\varepsilon\cdot\left(1+\frac{3}{n}\right)}\right]\cdot d_4+\left[e^{-\frac{3\varepsilon}{\mathrm{n}}}-e^{\frac{3\varepsilon}{n}}\right]\cdot d_3+$$
$$+\left[e^{-\varepsilon\cdot\left(1+\frac{1}{n}\right)}-e^{\varepsilon\cdot\left(1+\frac{1}{n}\right)}\right]\cdot d_2+\left[e^{-\frac{\varepsilon}{\mathrm{n}}}-e^{\frac{\varepsilon}{n}}\right]\cdot d_1+ \tag{C7}$$
$$+\left[e^{-\varepsilon\cdot\left(-1+\frac{1}{n}\right)}-e^{\varepsilon\cdot\left(-1+\frac{1}{n}\right)}\right]\cdot d_0=0$$

where

$$
\begin{aligned}
d_4 &= -I_0 \cdot I_2 \cdot e^{\frac{V_{DD}}{2\phi_t}} \\
d_3 &= I_0 \cdot I_2 \cdot e^{\frac{V_{DD}}{\phi_t}} \\
d_2 &= -\left[I_0 \cdot \left(I_0 + I_{1\cdot}\right) + I_2^2\right] \cdot e^{\frac{V_{DD}}{2\phi_t}} \\
d_1 &= I_0 \cdot \left(I_0 + I_1\right) \cdot e^{\frac{V_{DD}}{\phi_t}} - I_2 \cdot \left(I_0 + I_1\right) + I_2^2 \\
d_0 &= I_2 \cdot \left(I_0 + I_1\right) \cdot e^{\frac{V_{DD}}{2\phi_t}}
\end{aligned}
\tag{C8}
$$

Note that the output voltage swing of the latch is given by $2\mathcal{E}$.

APPENDIX D – TRANSCONDUCTANCES OF THE SCHMITT TRIGGER

D.1 WEAK INVERSION

Considering a symmetrical Schmitt trigger ($I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$), and $n_N = n_P = n$, in weak inversion (WI) of operation, the transconductances of the small-signal model of Fig. 27, can be written [71] as

$$g_{ms(d)} = \frac{2 \cdot I_{F(R)}}{\phi_t \cdot \left(\sqrt{1 + i_{F(R)}} + 1\right)} \approx \frac{I_{SQ} \cdot S \cdot i_{F(R)}}{\phi_t} = \frac{2e \cdot I_{SQ} \cdot S \cdot e^{\frac{V_P - V_{S(D)}}{\phi_t}}}{\phi_t}, \tag{D1}$$

$$g_m = \frac{g_{ms} - g_{md}}{n} \approx \frac{g_{ms}}{n} \cdot \left(1 - e^{-\frac{V_{DS}}{\phi_t}}\right), \tag{D2}$$

where $I_{F(R)}$ is the transistor forward (reverse) current strength, comprised of technological and geometrical parameters, $i_{f(r)}$ is the forward (reverse) inversion level, S is the transistor aspect ratio (W/L), I_{SQ} is the specific current and V_P is the pinch-off voltage. The pinch-off voltage can be approximated by [71]

$$V_P = \frac{V_{GB} - |V_{TN0}|}{n} \tag{D3}$$

The transconductances of the MOSFETs of the ST small signal model in Fig. 27 are given in Table VII, considering the case when $V_I = V_O = V_{DD}/2$.

TABLE VII – Transconductances of the ST in WI for $V_O = V_I = V_{DD}/2$.

	g_{ms}	g_{md}	g_m
N_0 or P_0	$\frac{I_0}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}$	$\frac{I_0}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_0}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(1-e^{-\frac{V_{X0}}{\phi_t}}\right)$
N_1 or P_1	$\frac{I_1}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_1}{\phi_t}\cdot e^{\frac{V_{DD}}{2\phi_t}\left(\frac{1}{n}-1\right)}$	$\frac{I_1}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)$
N_2 or P_2	$\frac{I_2}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_2}{\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{DD}}{\phi_t}}$	$\frac{I_2}{n\phi_t}\cdot e^{\frac{V_{DD}}{2n\phi_t}}\cdot\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}\right)$

Let $V_{X0} = V_X$ ($V_I = V_O = V_{DD}/2$). From (5), V_{X0} is given by

$$e^{\frac{V_{X0}}{\phi_t}} = \frac{I_0 + I_1 + I_2}{I_0 + I_1\cdot e^{-\frac{V_{DD}}{2\phi_t}} + I_2\cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{D4}$$

D.2 STRONG INVERSION

Considering a symmetrical Schmitt trigger, in strong inversion (SI) of operation, the transconductances of the mosfets of the ST small signal model of Fig. 27, can be written as [71]

$$g_{ms(d)} = \frac{2\cdot I_{F(R)}}{\phi_t\cdot\left(\sqrt{1+i_{F(R)}}+1\right)} \approx \frac{2I_{SQ}\cdot S\cdot\sqrt{i_{F(R)}}}{\phi_t} = \frac{2I_{SQ}\cdot S\cdot\left(V_P - V_{S(D)}\right)}{\phi_t^2}, \tag{D5}$$

$$g_{ms(d)} \approx \frac{2\cdot I_{SQ}\cdot S}{\phi_t^2}\left(V_{GB} - |V_{T0}| - V_{SB(DB)}\right). \tag{D6}$$

The transconductances of the MOSFETs of the ST small signal model in Fig. 27 are given in Table VIII, considering the case when $V_I = V_O = V_{DD}/2$.

TABLE VIII – Transconductances of the ST in SI for $V_O = V_I = V_{DD}/2$.

	g_{ms}	g_{md}	g_m
N_0 or P_0	$\frac{2I_{S0}}{\phi_t^2}\left(\frac{V_{DD}}{2}-V_{T0}\right)$	$\frac{2I_{S0}}{\phi_t^2}\left(\frac{V_{DD}}{2}-V_{T0}-V_{X0}\right)$	$\frac{2I_{S0}}{n\phi_t^2}V_{X0}$
N_1 or P_1	$\frac{2I_{S1}}{\phi_t^2}\left(\frac{V_{DD}}{2}-V_{T0}-V_{X0}\right)$	$\frac{2I_{S1}}{\phi_t^2}\left(-V_{T0}\right)$	$\frac{2I_{S1}}{n\phi_t^2}\left(\frac{V_{DD}}{2}-V_{X0}\right)$
N_2 or P_2	$\frac{2I_{S2}}{\phi_t^2}\left(\frac{V_{DD}}{2}-V_{T0}-V_{X0}\right)$	$\frac{2I_{S2}}{\phi_t^2}\left(\frac{V_{DD}}{2}-V_{T0}-V_{DD}\right)$	$\frac{2I_{S2}}{n\phi_t^2}\left(V_{DD}-V_{X0}\right)$

In strong inversion, the drain current of a NMOS (PMOS) MOSFET in saturation is given by [71]

$$I_{DN(P)} = I_{SN(P)} \cdot \left(\frac{V_{GB(BG)} - \left|V_{T0}\right| - n_{N(P)} \cdot V_{SB(BS)}}{n_{N(P)} \cdot \phi_t} \right)^2 . \qquad \text{(D7)}$$

Assuming the N_1 and N_2 in saturation, V_{X0} is given by

$$V_{X0} = \frac{V_{DD} - 2 \cdot \left|V_{T0}\right|}{2n} \cdot \left(1 - \sqrt{\frac{I_{S0}}{I_{S0} + I_{S1} + I_{S2}}} \right) . \qquad \text{(D8)}$$

Note that the current strength of the MOSFET in strong inversion and the current strength in weak inversion are related by the following expression

$$I_{SN(P)} = \frac{I_{N(P)} \cdot e^{\frac{\left|V_{T0}\right|}{\phi_t} - 1}}{2} . \qquad \text{(D9)}$$

APPENDIX E – HYSTERESIS WIDTH IN MODERATE AND STRONG INVERSION REGIMES

E.1 STRONG INVERSION

In strong inversion it follows [71] that

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = 1+\frac{I_0}{I_2}\cdot\frac{Q'_{IS}}{Q'_{IX}} = 1+\frac{I_0}{I_2}\cdot\frac{V_P}{V_P-V_{X0}} \tag{E1}$$

and $I_{DN0} = I_{DN1} + I_{DN2}$ is written as

$$I_0\cdot\left\{V_P^2-\left(V_P-V_{X0}\right)^2\right\} = I_1\cdot\left(V_P-V_{X0}\right)^2 + I_2\cdot\left(V_P-V_{X0}\right)^2. \tag{E2}$$

Thus,

$$\frac{V_P}{V_P-V_{X0}} = \sqrt{1+\frac{I_1}{I_0}+\frac{I_2}{I_0}}\,. \tag{E3}$$

Finally, from (E1) and (E3)

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = 1+\frac{I_0}{I_2}\cdot\sqrt{1+\frac{I_1}{I_0}+\frac{I_2}{I_0}}\,. \tag{E4}$$

Applying (E4) into (28), and accepting that $\Delta V \approx 0$, results

$$V_L = \frac{V_{DD}}{1+\frac{I_0}{I_2}\cdot\sqrt{1+\frac{I_1}{I_0}+\frac{I_2}{I_0}}}\,. \tag{E5}$$

E.2 MODERATE INVERSION

The hysteresis width in moderate inversion cannot be written as a closed form equation since there is no simple expression for the drain current in this regime of inversion. So, the hysteresis width in moderate inversion can be calculated by the linear interpolation of the hysteresis width in weak inversion, eq. (32), and in strong inversion, eq. (E5).

APPENDIX F – DESIGNED CHIPS

F.1 DESIGNED CHIP #1

Technology: IBM 180 nm
Chip Description: A set of Schmitt triggers optimized for a supply voltage of 40 mV, with different p-channel and n-channel strengths, in order to pre-compensate for process variations (slow-fast, midway between slow-fast and typical, typical, midway between fast-slow, and fast-slow corners). It also includes a set of inverters that also pre-compensate process variations.

The designed chip #1 micrograph is shown in Fig. 70, while the chip layout is shown in Fig. 71.

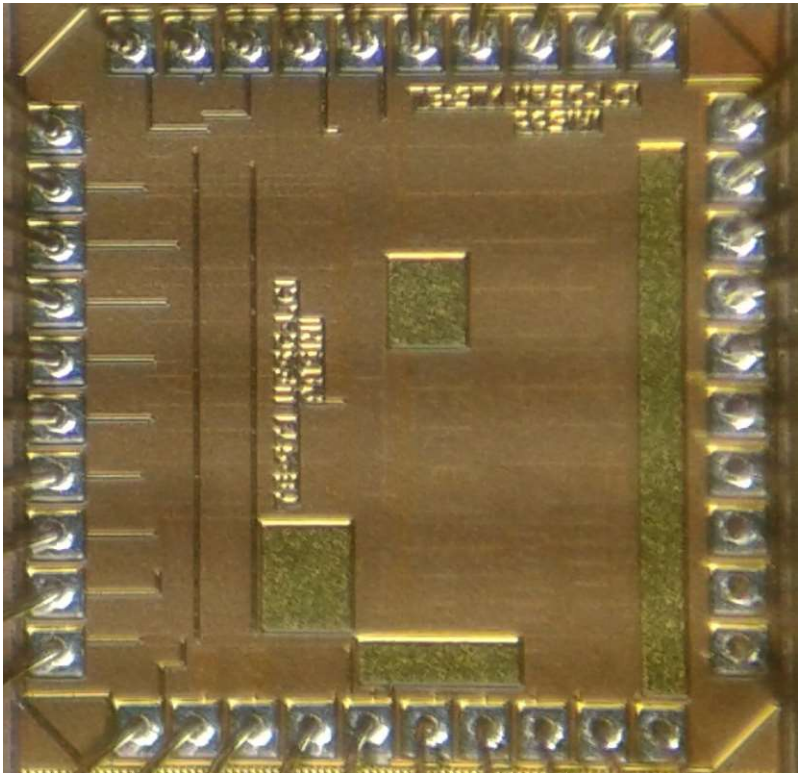


Figure 70 – Micrograph of the designed chip 1.

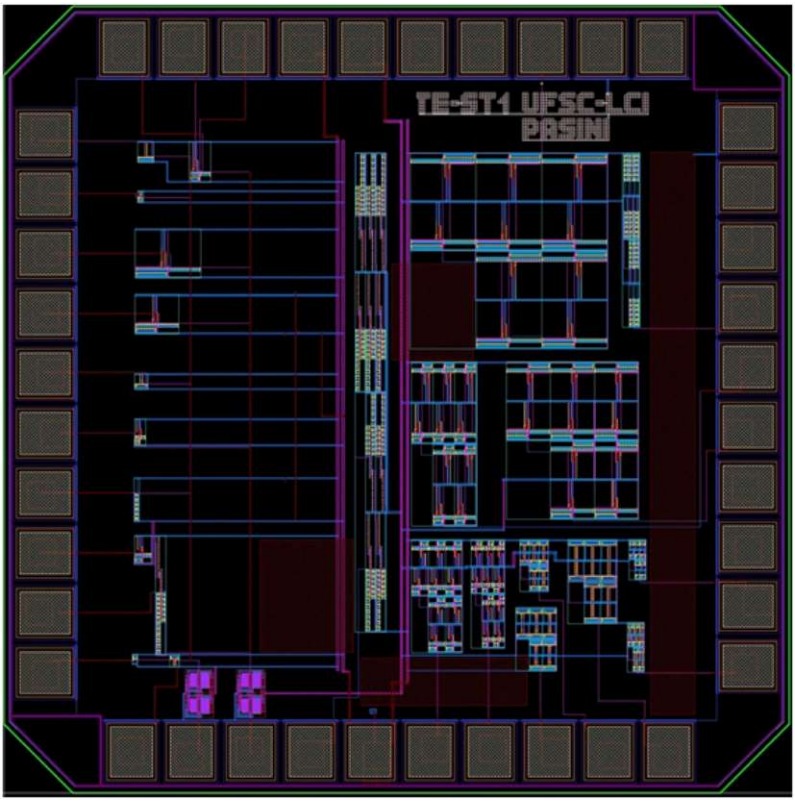


Figure 71 – Layout of the designed chip 1.

F.2 DESIGNED CHIP #2

Technology: IBM 180 nm
Chip Description: A set of Schmitt triggers designed with different feedback ratios, in order to measure hysteresis widths for different supply voltages.

The designed chip #2 micrograph is shown in Fig. 72, while the chip layout is shown in Fig. 73.

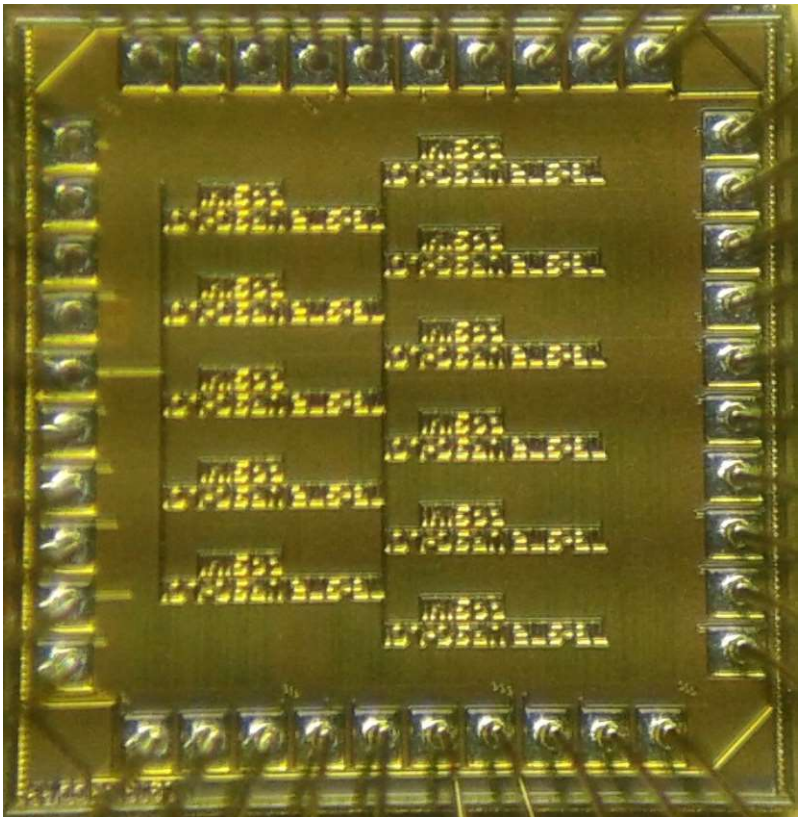


Figure 72 – Micrograph of the designed chip 2.

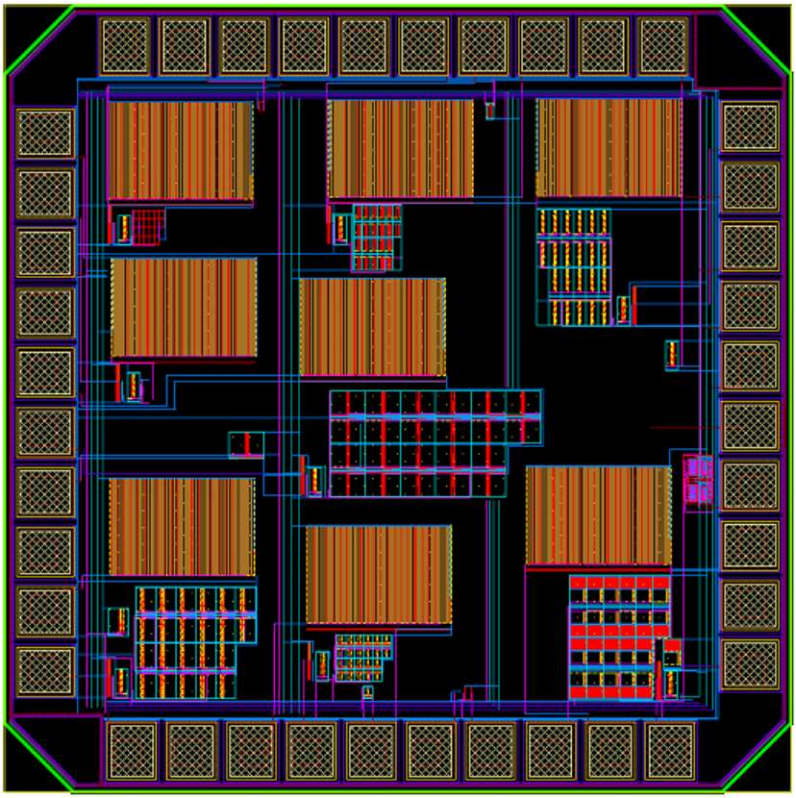


Figure 73 – Layout of the designed chip 2.

F.3 DESIGNED CHIP #3

Technology: IBM 180 nm
Chip Description: A set of Schmitt triggers designed with different feedback and series ratios and conventional inverters, in order to measure the voltage gain for different supply voltages.

The designed chip #3 micrograph is shown in Fig. 74, while the chip layout is shown in Fig. 75. Details about the layout of the designed circuits are shown in Fig. 76.

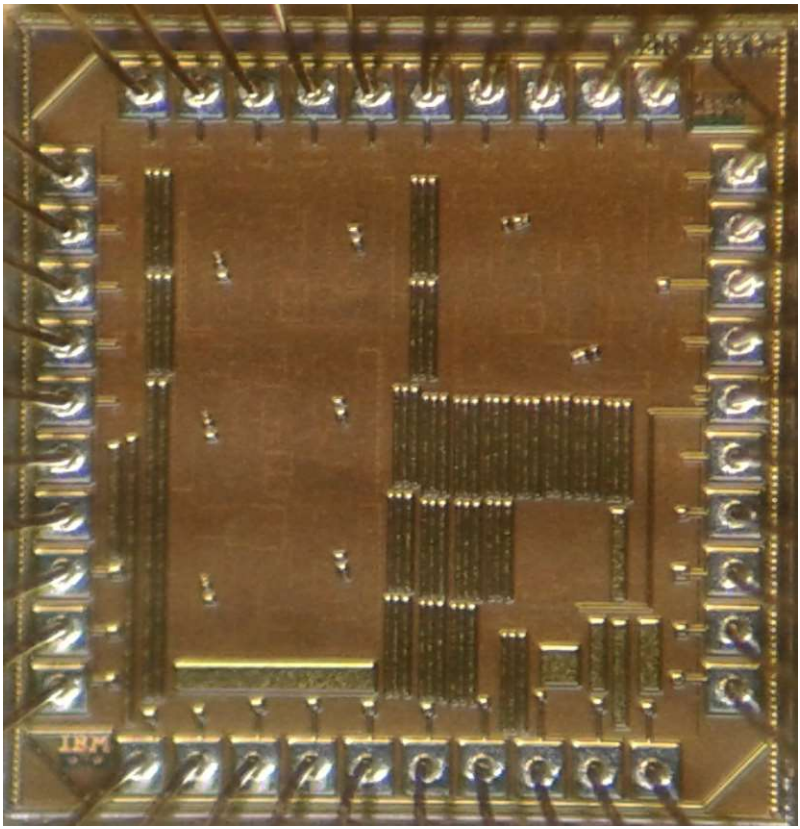


Figure 74 – Micrograph of the designed chip 3.

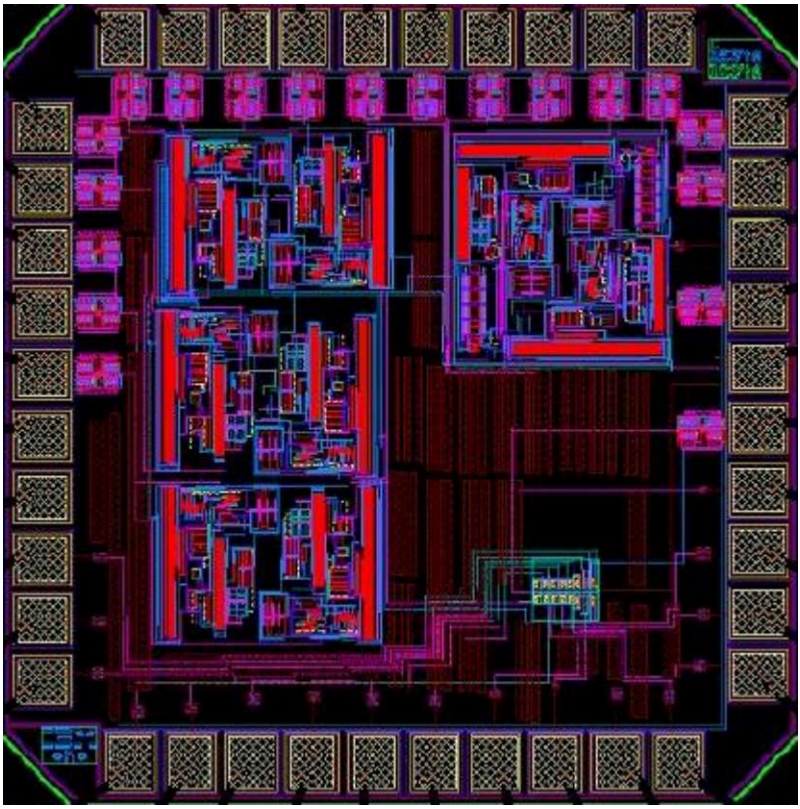


Figure 75 – Layout of the designed chip 3.

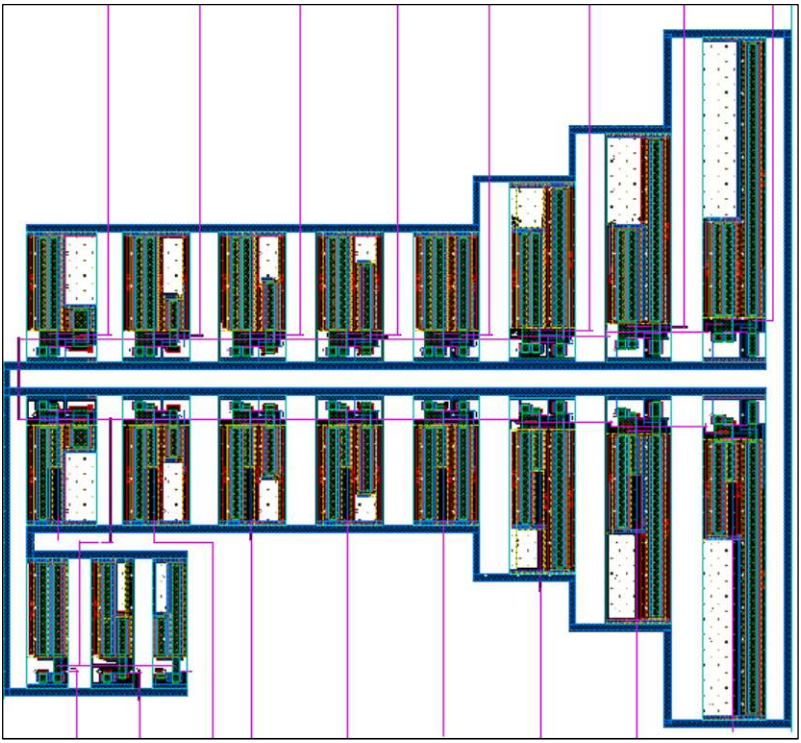


Figure 76 – Layout of the designed Schmitt triggers inside chip 3.

APPENDIX G – SCHMITT TRIGGER RISE AND FALL TIMES

In a positive input transition, the output capacitor will discharge from V_{DD} down to GND when $V_I = V_{DD}$. Only leakage current flows in the p- network ($I_{DP1} << I_{DN1}$), so, $I_{OUT} \approx I_{DN1}$. The discharging circuit is shown in Fig. 77 (a). The same analysis can be done for a negative input transition; the charging circuit is shown in Fig. 77 (b). In these circuits, the capacitance of nodes X and Y are considered irrelevant for the calculation of the transient.

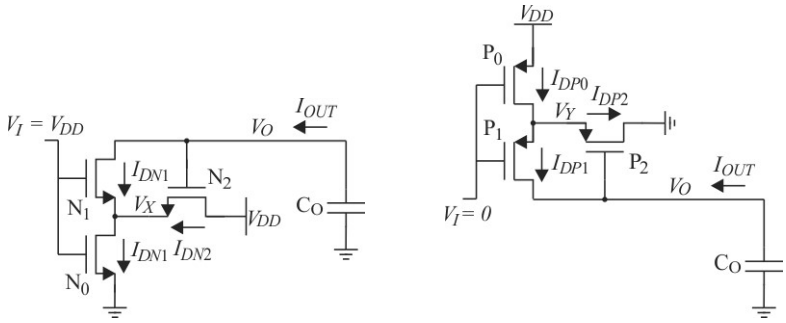


Figure 77 – Schmitt trigger (a) discharge circuit; (b) charge circuit.

The rise time, T_{LH}, can be calculated from equation (47) as

$$dt = -\int \frac{C_O}{I_{OUT}} dV_O \tag{G1}$$

Approximating $I_{OUT} \approx I_{DN1}$:

$$dt = -\int \frac{C_O}{I_{DN1}} dV_O \tag{G2}$$

Substituting the value of the drain current of transistor N_1 from (1), with $n = 1$, into (G2):

$$dt = -\frac{C_O}{I_1 \cdot e^{\frac{V_{DD}}{\phi_t}}} \int \frac{1}{e^{-\frac{V_X}{\phi_t}} - e^{-\frac{V_O}{\phi_t}}} dV_O \tag{G3}$$

Finally, substituting the value of $e^{\frac{V_X}{\phi_t}}$ from (9) and evaluating the rise (fall) time between 10% (90%) and 90% (10%) of the supply voltage, (G3) results in the lengthy equation (G4). Note that $T_{HL} = T_{LH}$ for the case of the symmetrical Schmitt trigger.

$$T_{HL(LH)} = \frac{C_O}{I_1 \cdot \sqrt{2 \cdot I_0 \cdot I_2 \cdot \left(e^{\frac{3V_{DD}}{\phi_t}} - 2 \cdot e^{\frac{2V_{DD}}{\phi_t}} \right) - I_2^2 \cdot e^{\frac{2V_{DD}}{\phi_t}} - I_0^2 \cdot e^{\frac{4V_{DD}}{\phi_t}}}} \cdot$$

$$\left\{ \frac{1}{2} \cdot \ln \left[\frac{I_2 \cdot \left(1 - e^{0.1\frac{V_{DD}}{\phi_t}} \right) + I_0 \cdot \left(e^{1.1\frac{V_{DD}}{\phi_t}} - e^{0.2\frac{V_{DD}}{\phi_t}} \right)}{I_2 \cdot \left(1 - e^{0.9\frac{V_{DD}}{\phi_t}} \right) + I_0 \cdot \left(e^{1.9\frac{V_{DD}}{\phi_t}} - e^{1.8\frac{V_{DD}}{\phi_t}} \right)} \right] + 0.8 \cdot \frac{V_{DD}}{\phi_t} + \right.$$

$$+ \left(2 \cdot I_0 + 2 \cdot I_1 + I_2 - I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} \right) \cdot$$

$$\left[\arctan \left(\frac{I_2 \cdot e^{\frac{V_{DD}}{\phi_t}} - I_0 \cdot \left(e^{2\frac{V_{DD}}{\phi_t}} - 2 \cdot e^{1.1\frac{V_{DD}}{\phi_t}} \right)}{\sqrt{\left(I_2 \cdot e^{\frac{V_{DD}}{\phi_t}} - I_0 \cdot e^{2\frac{V_{DD}}{\phi_t}} \right)^2 + 4 \cdot I_0 \cdot I_2 \cdot e^{2\frac{V_{DD}}{\phi_t}}}} \right) - \right.$$

$$\left. \left. - \arctan \left(\frac{I_2 \cdot e^{\frac{V_{DD}}{\phi_t}} - I_0 \cdot \left(e^{2\frac{V_{DD}}{\phi_t}} - 2 \cdot e^{1.9\frac{V_{DD}}{\phi_t}} \right)}{\sqrt{\left(I_2 \cdot e^{\frac{V_{DD}}{\phi_t}} - I_0 \cdot e^{2\frac{V_{DD}}{\phi_t}} \right)^2 + 4 \cdot I_0 \cdot I_2 \cdot e^{2\frac{V_{DD}}{\phi_t}}}} \right) \right] \right\}$$

(G4)

APPENDIX H – PUBLICATIONS

Following is the list of publications regarding this thesis:

[1] L. A. P. Melek, M. C. Schneider, C. Galup-Montoro, “Optimized design of the CMOS Schmitt trigger for ultra-low-voltage operation”, Iberchip 2014, Santiago, Chile, February 2014.

[2] L. A. P. Melek, M. C. Schneider, C. Galup-Montoro, “Ultra-low voltage CMOS logic circuits”, Invited paper at the Argentine School of Micro-Nanoelectronics, Technology and Applications – EAMTA 2014, Mendoza, Argentina, July 2014, pp. 1-7, available in IEEE XPLORE.

[3] L. A. P. Melek, A. L. da Silva Jr., M. C. Schneider, C. Galup-Montoro, “Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation”, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 869-878, April 2017.

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